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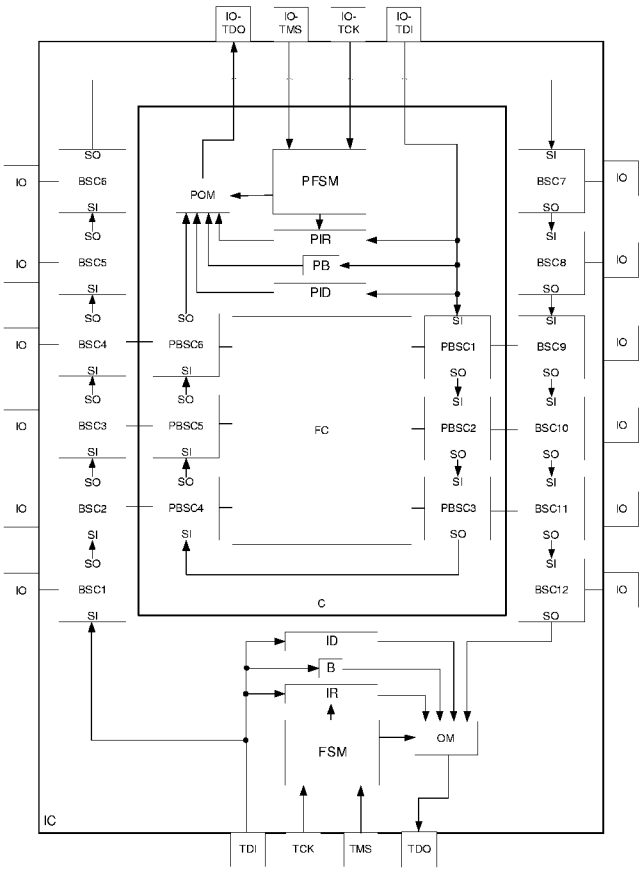
(54) Title: A JTAG TESTING ARRANGEMENT FOR AN INTEGRATED CIRCUIT



(57) Abstract: The invention relates to an integrated circuit (IC) comprising a core function block (FC) and a first chain of boundary-scan cells (BSC1-BSC12) implemented around it, and a state machine (FSM) controlling the same. The integrated circuit also comprises a second chain of boundary-scan cells (PBSC1-PBSC6) implemented between the core function block (FC) of the integrated circuit and said first chain of boundary-scan cells (BSC1-BSC12), or as a part of the core function block (FC) of the circuit, at least partly in parallel with said first chain of boundary-scan cells; a test interface (IO-TDO, IO-TMS, IO-TCK, IO-TDI; TAP) adapted to said second chain of boundary-scan cells; and a second state machine (PFSM) arranged to control said second chain of boundary-scan cells.

WO 2007/042622 A1

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A JTAG TESTING ARRANGEMENT FOR AN INTEGRATED CIRCUIT

Field of the invention

The invention relates to JTAG testing and particularly to the JTAG testing of integrated circuits.

Background of the invention

A universal standard IEEE 1149.1, also known as JTAG (Joint Test Action Group) according to the consortium that established the standard, has been developed for testing various circuit boards and components connected to them, as well as integrated circuits. The JTAG is a boundary-scan method in which an input signal is fed into a boundary pin of the circuit board, and an output signal is measured from another boundary pin. Consequently, the basic idea of JTAG is to transfer predetermined serial data sequences through integrated circuit (IC) components in a circuit board or in a part thereof and to sample the output data. As the relative topology and logical functions of the components of the circuit board to be tested are known in advance, it is also possible to determine an expected output. Test equipment may be used to compare the output data of a Device Under Test DUT with the expected output, and if these match, the device under test DUT operates correctly. However, if the output data does not match with the expected data, the circuit under test may be open, an external signal may be connected to it, or a component in the circuit may be defective. In such a case, the defect can typically be determined by running various test data sequences through the device under test and by analyzing the obtained output using software included in the test equipment.

The JTAG standard defines for both the test equipment comprising a JTAG controller and the device under test DUT an identical interface Test Access Port TAP, with a fixed synchronous line therebetween, comprising at least five conductors for five compulsory signals: a Test

Clock signal TCK, a Test Mode Select signal TMS, Test Data Input TDI, Test Data Output TDO, and a GrouND reference signal GND, as well as an optional test ReSeT signal TRST. The applicant's patent EP 1189070 B1 describes a solution to avoid the use of a fixed synchronous line between the test equipment and the device under test, substantially diversifying the potential uses of JTAG testing. The solution described in the patent is based on the use of transceivers both in the test equipment and in the device under test DUT, the transceivers arranging the signals arriving from the interface TAP to be transmitted via an asynchronous transmission path in such a way that the received signals can again be synchronized into the mode required by the interface TAP. Such a solution makes it possible to use a wireless asynchronous transmission path for the transmission of test data, enabling, for example, the testing of circuit boards and the analysis of defects using the test equipment by remote control without a fixed connection to the device under test. In a corresponding manner, the solution makes it possible to test, for example, circuit boards even at a long distance from each other by remote control, for example, across the Internet.

The solution described in patent EP 1189070 B1 works well in situations in which the device under test comprises different types of circuit boards having several components to be boundary-scanned. However, if the device under test is a single integrated circuit having built-in JTAG functionality with its own TAP interface and internal Finite State Machine FSM, the described transceiver cannot be used for testing the core logic element or the external connections of the integrated circuit. Such an integrated circuit has no possibility of controlling, by means of the described transceiver, such structures according to the JTAG standard that can only be controlled by using signals relating to the external TAP interface of the integrated circuit, because these conductor pins used for signalling are not controllable by the transceiver when the circuit is in the JTAG test mode. This is due to the fact that when the circuit is controlled by the TAP interface in the JTAG test mode, the external conductor pins of the circuit can be controlled

by inputting test data in the boundary-scan cells from the conductor TDI, and in a corresponding manner, by reading test data received from the conductor TDO. Thus, the signalling between the IO conductor pins and the core logic element of the circuit is isolated, wherein the integrated circuit itself cannot be subjected to JTAG testing by means of the asynchronous transceiver; in other words, the integrated circuit cannot perform a Built-In Self-Test (BIST) under the control of the asynchronous transceiver. Such a problem occurs, for example, in most Field Programmable Gate Array (FPGA) circuits.

Summary of the invention

Now, an improved integrated circuit structure has been invented to overcome the above-mentioned problems. As an implementation of the invention, we present an integrated circuit having the characteristics set forth in the independent claim. The dependent claims disclose advantageous embodiments of the invention.

The invention is based on the idea of providing an integrated circuit comprising a core function block and a first chain of boundary-scan cells implemented around the core function block, and a state machine controlling the chain. The integrated circuit further comprises a second chain of boundary-scan cells implemented between the core function block of the integrated circuit and said first chain of boundary-scan cells, or as a part of the core function block of the circuit, at least partly in parallel with said first chain of boundary-scan cells; a separate test interface adapted for said second chain of boundary-scan cells; and a second state machine arranged to control said second chain of boundary-scan cells.

In one embodiment, the integrated circuit is a programmable circuit, such as a Field Programmable Gate Array FPGA or a Programmable Logic Device PLD.

In another embodiment, said second chain of boundary-scan cells is different in length, preferably shorter than said first chain of boundary-scan cells.

In another embodiment, the integrated circuit also comprises a transceiver arranged to convert the test data to be transmitted to said test interface to a form suitable for the asynchronous transmission path and, correspondingly, to convert the test data to be received from the asynchronous transmission path to a synchronous form required by said interface.

The arrangement according to the invention provides significant advantages. It is an advantage of the invention that the boundary-scan testing of the integrated circuit can be performed in such a way that the TAP signalling relating to this boundary-scan testing can be implemented completely within the integrated circuit by using, instead of the external TAP interface of the circuit, for example the signals TMS, TCK, TDI and TDO of the JTAG standard provided in the integrated circuit after or at its manufacturing stage or later by the user. Another advantage of the invention is that the test chain to be formed of boundary-scan cells and the other boundary-scan functions can be freely defined by the user, which enables, for example, faster testing, thanks to the shorter test chain, as well as redefinition of the test chain. Yet another advantage is that the transceiver described in the patent EP 1189070 B1 can be included as a part of the second chain of boundary-scan cells, whereby the JTAG testing of the integrated circuit, defined by the user, can be performed by remote testing by means of said transceiver.

Brief description of the drawings

The invention will now be described in more detail in connection with preferred embodiments with reference to the appended drawings, in which:

Fig. 1 is a block chart illustrating an integrated circuit of prior art, comprising a built-in boundary-scan logic according to the standard IEEE 1149.1;

Fig. 2 is a block chart illustrating an integrated circuit comprising a test architecture according to one embodiment;

Fig. 3 is a block chart illustrating an integrated circuit comprising a transceiver solution attached to the testing arrangement according to one embodiment;

Fig. 4 is a block chart illustrating an electronic connection of a boundary-scan cell according to one embodiment.

Description of the embodiments

Figure 1 shows a reduced model of a typical integrated circuit IC with in-built boundary-scan logic of prior art according to the IEEE 1149.1 standard. The integrated circuit IC may be a Field Programmable Gate Array FPGA programmable by the user, or, more generally, a Programmable Logic Device PLD. The integrated circuit may also be an Application Specific Integrated Circuit ASIC.

The circuit IC comprises external conductor pins TDI, TMS, TCK, and TDO according to the JTAG standard IEEE 1149.1. The interface formed by these conductor pins is generally called a Test Access Port TAP. Optionally, the TAP interface of the circuit may also comprise a Test ReSeT pin TRST. The internal boundary-scan logic of the circuit is controlled by a Finite State Machine FSM controlled by an external JTAG controller by using TMS and TCK signals. The input test data TDI is entered in registers according to the JTAG standard, and the output data is conveyed from one of these registers under the control of the state machine FSM through a multiplexer OM into an external conductor pin TDO. The integrated circuit IC comprises a Bypass Register B consisting of a shift register of boundary-scan cells, and an

Instruction Register IR that is used in combination with the state machine FSM and the TDI information to provide the desired boundary-scan function. Furthermore, the integrated circuit IC comprises a boundary-scan register consisting of boundary-scan cells which may form boundary-scan cell groups BSC1–BSC12. One boundary-scan cell group BSCn, as shown in Fig. 1, may consist of one or more actual boundary-scan cells. Furthermore, the integrated circuit IC may optionally comprise a circuit identification data register ID that comprises a type code typically identified for this integrated circuit. The boundary-scan cells are controlled by means of a state machine FSM by external excitation from the external conductors TDI, TMS and TCK of the circuit. The data read from the external IO conductor pins of the circuit into the boundary-scan cells can be led to the output TDO.

In the normal mode of the circuit, the core logic element C of the circuit is logically connected to the external conductor pins IO, bypassing the boundary-scan cell chain according to the JTAG standard and the test option provided by the cells included in it. Thus, the boundary-scan cells are permeable to the parallel-form signals connected to them between the IO conductor pins and the core logic element C without alterations. When, in turn, the circuit is controlled in the JTAG test mode by means of the TAP interface, the external conductor pins IO of the circuit can be controlled by entering test data from the conductor TDI in the boundary-scan cells BSC, and in a corresponding manner by reading the test data obtained from the IO conductor pins, outside the circuit by means of the conductor TDO. Thus, the signalling between the IO conductor pins and the core logic element C of the circuit is isolated.

This will be problematic, for example, in a situation in which the downlink transceiver of EP 1189070 B1 should be implemented inside the core logic element C of a single FPGA circuit. Thus, it would be impossible to use the boundary-scan cell chain of the circuit built in the infrastructure of the circuit, because the FSM logic that controls the boundary-scan cell chain is not accessible to this downlink transceiver

to be implemented. Typically, the TAP interface of the integrated circuit can only be controlled by means of the external boundary pins of the circuit. When the FPGA is in the JTAG test mode, all the circuits connected to the logic that can be defined by its user are controlled by the state machine FSM.

In the following, a test architecture according to one embodiment of the invention will be described with reference to Fig. 2. The integrated circuit IC comprises a boundary-scan cell array similar to that of an integrated circuit of prior art, shown in Fig. 1: Built-in external signal conductors TDI, TCK, TMS and TDO of the TAP interface according to the IEEE 1149.1 standard, for controlling the state machine FSM which, in turn, controls the registers IR, B and ID according to the standard as well as a boundary-scan register consisting of boundary-scan cells or boundary-scan cell groups BSC1–BSC12. Such a design is typical, for example, in the infrastructure of an unprogrammed or reconfigurable FPGA circuit. Furthermore, the integrated circuit IC comprises a basic function block FC implemented on the circuit by the user and operating in the normal mode, corresponding to the core logic element C of Fig. 1. This functional implementation FC that can be defined by the user can be implemented, for example, in the VHDL (VHSIC Hardware Description Language), Verilog or SystemC languages.

However, a substantial difference to the test architecture of prior art shown in Fig. 1 is that the embodiment of Fig. 2 comprises a second functional configuration according to the IEEE 1149.1 standard. This second JTAG test architecture is preferably implemented around the basic function core FC, as a part of element C in the integrated circuit IC. Said second JTAG test architecture also comprises a TAP interface (IO-TDI, IO-TCK, IO-TMS, IO-TDO) for controlling the state machine PFSM, and the registers according to the standard; an optional identification register PID, a bypass register PB, an instruction register PIR, and a boundary-scan register consisting of boundary-scan cells PBSC implemented by the user by programming. In Fig. 2, the second boundary-scan register (boundary-scan cell chain) implemented

around the basic function core FC is implemented preferably shorter than the original boundary-scan register belonging to the infrastructure of the circuit, consisting of boundary-scan cells BSCn.

By means of this second JTAG test architecture, the test architecture according to the IEEE 1149.1 can be preferably implemented by entering predetermined test data via either internal or external TDI signalling into registers controlled by a state machine PFSM, and by conveying test data output TDO via a multiplexer POM either into an external TDO conductor or into an internal interface of the integrated circuit.

Thus, the integrated circuit according to the presented embodiment can be set in two discrete boundary-scan test modes. The first test mode implemented by the inbuilt structures of the circuit is activated by using the boundary pins TMS and TCK of the external TAP interface of the circuit, and the test data is transmitted by using the external boundary pins TDI and TDO. In this test mode, typically all the other IO conductor pins than those belonging to the TAP interface of the circuit are isolated from the logic C and FC defined by the user. When the circuit is in the normal mode, the inbuilt JTAG test mode is not activated, the state machine FSM is in a reset state, and the boundary-scan cells BSCn are permeable to signalling for the IO conductor pins as defined by the user, without alterations. Thus, the second JTAG test architecture in the C block, defined by the user, can be activated either within or outside the circuit by IO-TMS and IO-TCK signalling belonging to the TAP interface, and the test data can be transmitted in a corresponding manner by using either external or internal IO-TDI and IO-TDO signalling facilities.

The integrated circuit according to the above-described embodiment, which may be, for example, an FPGA circuit, can be advantageously supplemented with a downlink transceiver described in patent EP 1189070 B1, for example, by connecting the TAP interface included in the downlink transceiver to the second JTAG test architecture shown in

Fig. 2. When the user wants to perform boundary-scan testing for such an FPGA integrated circuit by using a communication interface that is asynchronous with respect to the test clock signal TCK, the built-up JTAG logic of the FPGA circuit is kept inactive, and only the boundary-scan functions defined by the user in this FPGA circuit are activated.

Figure 3 shows an embodiment in which the integrated circuit structure of Fig. 2 is supplemented with the downlink transceiver DL described in patent EP 1189070 B1 by implementing the transceiver DL in the block C that can be configured by the user. The transceiver DL receives TDI-TMS data from the asynchronous transmission path by means of the normal IO boundary pin IO-RX of the circuit. In a corresponding manner, the transceiver DL transmits TDO data to the asynchronous transmission path by means of the IO-TX boundary pin of the circuit. The transceiver DL generates the signals TDI, TMS and TCK of the TAP interface internally on the basis of data received from the transmission path RX, and receives the TDO signal from the last cell in the boundary-scan cell chain defined by the user via the multiplexer POM, and the transceiver DL transmits the TDO signal further to the transmission path TX. In this embodiment, the JTAG testing defined by the user can be performed without signals transmitted via the external TAP interface of the circuit. Advantageously, the JTAG testing controlled by means of the transceiver DL and defined by the user can also be implemented in integrated circuits of other than the ASIC type.

The internal boundary-scan logic (second JTAG test architecture) implemented by the normal logic resources in the programmable circuit, such as an FPGA circuit, can be reconfigured, and thus its length and other properties can be optimized for different purposes. For example, there may be several test sequences intended for internal boundary scanning tailored for different purposes, and these may be adopted or bypassed, if necessary.

According to one embodiment, the JTAG testing can be controlled and reconfigured by means of auxiliary functions according to the IEEE

1149.1 standard, which may be controlled, for example, by auxiliary instructions defined by the user. One or more auxiliary instructions may be used to enter different JTAG test chains in the bypass or normal mode, wherein the same implementation can be advantageously used to provide both an optimum test coverage and a JTAG test chain of a minimum length. The shortness of the JTAG test chain is advantageous, for example, in the programming of Flash memory circuits, in which the length of the boundary-scan cell chain has a linear effect on the programming time. The use of several chains may also be advantageous in situations in which one or more processing units are implemented as an either component-based or software-based macrostructure within the circuit. Thus, it is advantageously possible to control merely the processing unit, for example in connection with software development by using ICE equipment (In-Circuit Emulator) at the same time when the other logics of the integrated circuit function normally and are connected via IO conductor pins to the outside of the circuit according to the normal mode. This may be necessary, for example, when a DRAM-type memory requiring active refreshing is connected to the control of the circuit under test. Thus, if a DRAM controller is provided within a programmable circuit, it can be instructed to refresh the memory even though the state of the processor is simultaneously monitored by means of the JTAG connection.

The above description has dealt with ways of defining the auxiliary JTAG test logic and its implementation in the integrated circuit by using a Hardware Description Language (HDL), such as VHDL. In addition to this, the JTAG standard requires that said logical operation of the second boundary-scan function must be described in the Boundary-Scan Description Language (BSDL) so that the JTAG test equipment and the software controlling it can control the JTAG test logics by appropriate signalling. Because the BSDL is a subset of the VHDL language, the description of the physical functions of the circuit in the VHDL language and the description of the logical boundary-scan function in the BSDL language offer obvious synergy benefits. It is certainly obvious for a person skilled in the art that the structure and the physical functions of

the circuit can also be described in any other way that is characteristic of said circuit type.

The second JTAG test chain defined by the user (in other words, the boundary-scan register) may differ from the original JTAG test chain of the circuit in respect of its length and other properties. If the IO conductor pin of the integrated circuit, for example FPGA circuit, can be configured both as an input, an output and a three-state mode, possibly three different boundary-scan cells may be connected to this IO conductor pin. Thus, one cell may control a buffer connected to the IO conductor pin, which enables, for example, that this IO conductor pin can be switched to a three-state mode (HiZ), if desired. Another cell controls the state of the IO conductor pin when the circuit has been switched to the JTAG test mode, and a third cell can be used to read the state of the IO conductor pin so that this state can be entered from the boundary-scan shift register into the TDO conductor. If such an IO conductor pin is used only by the functional logic part FC in the second JTAG test chain as either an output or a three-state IO conductor pin, it is possible to make the boundary-scan cell group PBSC connected to this IO conductor pin of the second JTAG test chain a two-cell array which will thus save the necessary logic resources and speed up testing due to the shortened boundary-scan register structure. Also, the other functions can be made either more or less extensive than those contained in the original JTAG test functionality of the circuit.

In many cases, the boundary-scan function is used for the programming of memories, such as Flash-type memories, externally connected to the circuit. Thus, for memory programming at a maximum rate, the chain formed by the boundary-scan cells connected to these IO conductor pins should be as short as possible. Typically, for example in FPGA circuits, this boundary-scan cell chain comprises several hundreds or even thousands of cells, whereas the number of IO conductor pins required for the programming of the Flash memory circuit is typically in the order of some tens at a maximum. Thus, for each signalling required for the programming sequence of the Flash circuit, new data

must be circulated via several hundreds of extra cells, which causes an undue long delay. Consequently, one advantage of the solution according to the invention is that the user can select a boundary-scan cell chain of a suitable length for each application. Thus, for example, in the programming of the Flash memory circuit, this chain can be defined to consist of only those boundary-scan cells whose IO conductor pins are connected to said Flash memory circuit. As a result, the required programming time can be radically reduced, as the data to be programmed does not need to be transmitted via boundary-scan cells not connected to the Flash circuit.

In a corresponding manner, the integrated circuit and the boundary-scan function comprised by it can be used as a part of testing of circuit connections, wherein the user can select the chain to comprise only those boundary-scan cells required for testing, whose IO boundary pins are used for the testing of said circuit connections. Said configurable or programmable integrated circuits connected to the integrated circuit, such as Flash memory circuits, or circuit connections connected to said integrated circuit and to be tested may naturally be either internal circuits within said integrated circuit, or external circuits.

In the solution according to the invention, one functional logic element is added between the functional block FC and the external IO conductor pin, for example a port or a multiplexer, to control the signal to the IO conductor pin either directly from the functional block or from a new boundary-scan cell defined by the user. This addition of one logical port will naturally cause a short delay in the signal chain. In Fig. 4, the block C to be defined by the user is provided with a boundary-scan cell PBSC defined by user in, for example, the VDHL language. The signal PI coupled from the block C is led via a multiplexer MUX controlled by a Mode signal in the PBSC block into a cell BSC in the built-in HC element, from whose output the signal PO is coupled to the IO conductor pin. This multiplexer causes a short signal delay as a difference to a situation of the signal entering the cell BSC directly from the functional block C. Typically, the delay formed by such a multiplexer or other cor-

responding functional logic means in, for example, PLD circuits, such as FPGA circuits, is very short (typically less than 1 ns), and it can be ignored in the design of the desired function of the circuit. In the case of a circuit comprising very fast external signalling, this short delay can be taken into account in the design when the timings of the circuit are trimmed by using, for example, restrictions on the synthesis tools and other information about delays.

It should be noted that the structure of the boundary-scan cells shown in Fig. 4 is given as an example. The IEEE 1149.1 standard does not define this structure in detail, and practical solutions may thus differ from that shown. In the figures illustrating the invention and in their descriptions, logical structural descriptions have been used, whose physical implementation may differ from that presented, within the limits defined by the IEEE 1149.1 standard.

It will be obvious for a person skilled in the art that the basic idea of the invention can be implemented in a variety of ways. Thus, the invention and its embodiments are not limited to the above-described examples but they may vary within the scope of the claims.

Claims:

1. An integrated circuit (IC) comprising a core function block (FC) and a first chain of boundary-scan cells (BSC1–BSC12) implemented around it, and a state machine (FSM) controlling the same, **characterized** in that the integrated circuit also comprises

a second chain of boundary-scan cells (PBSC1–PBSC6) implemented between the core function block (FC) of the integrated circuit and said first chain of boundary-scan cells (BSC1–BSC12), or as a part of the core function block (FC) of the circuit, at least partly in parallel with said first chain of boundary-scan cells,

a test interface (IO-TDO, IO-TMS, IO-TCK, IO-TDI; TAP) adapted to said second chain of boundary-scan cells, and

a second state machine (PFSM) arranged to control said second chain of boundary-scan cells.

2. The integrated circuit according to claim 1, **characterized** in that

the integrated circuit (IC) is a circuit that is at least partly programmable by the user, such as an FPGA or a PLD.

3. The integrated circuit according to claim 1 or 2, **characterized** in that

said second chain of boundary-scan cells (PBSC1–PBSC6) is different in length, preferably shorter, and in structure from said first chain of boundary-scan cells (BSC1–BSC12).

4. The integrated circuit according to any of the preceding claims, **characterized** in that the integrated circuit also comprises

a transceiver (DL) arranged to convert test data to be transmitted to said test interface (TAP) into a form suitable for the asynchronous transmission path and, correspondingly, to convert the test data to be received from the asynchronous transmission path into a synchronous form required by said interface.

5. The integrated circuit according to any of the preceding claims, **characterized** in that the integrated circuit also comprises

at least one boundary-scan register consisting of one or more of said chains of boundary-scan cells.

6. The integrated circuit according to any of the preceding claims, **characterized** in that the integrated circuit also comprises

at least one function operable by means of an auxiliary command according to the JTAG standard, arranged to control the JTAG testing of said integrated circuit according to auxiliary commands defined by the user.

7. The integrated circuit according to any of the preceding claims, **characterized** in that

said integrated circuit is adapted to be used for configuring or programming integrated circuits connected to the same, wherein said second chain of boundary-scan cells is adapted to comprise only those boundary-scan cells needed for configuration or programming, whose IO boundary pins are connected to said integrated circuits.

8. The integrated circuit according to any of the preceding claims, **characterized** in that

said integrated circuit is adapted to be used as a part of testing of circuit connections, wherein said second chain of boundary-scan cells is adapted to comprise only those boundary-scan cells required for testing, whose IO boundary pins are used for the testing of said circuit connections.

9. The integrated circuit according to claim 7 or 8, **characterized** in that

said configurable or programmable integrated circuits connected to said integrated circuit, or the circuit connections connected to said integrated circuit and to be tested are inside or outside said integrated circuit.

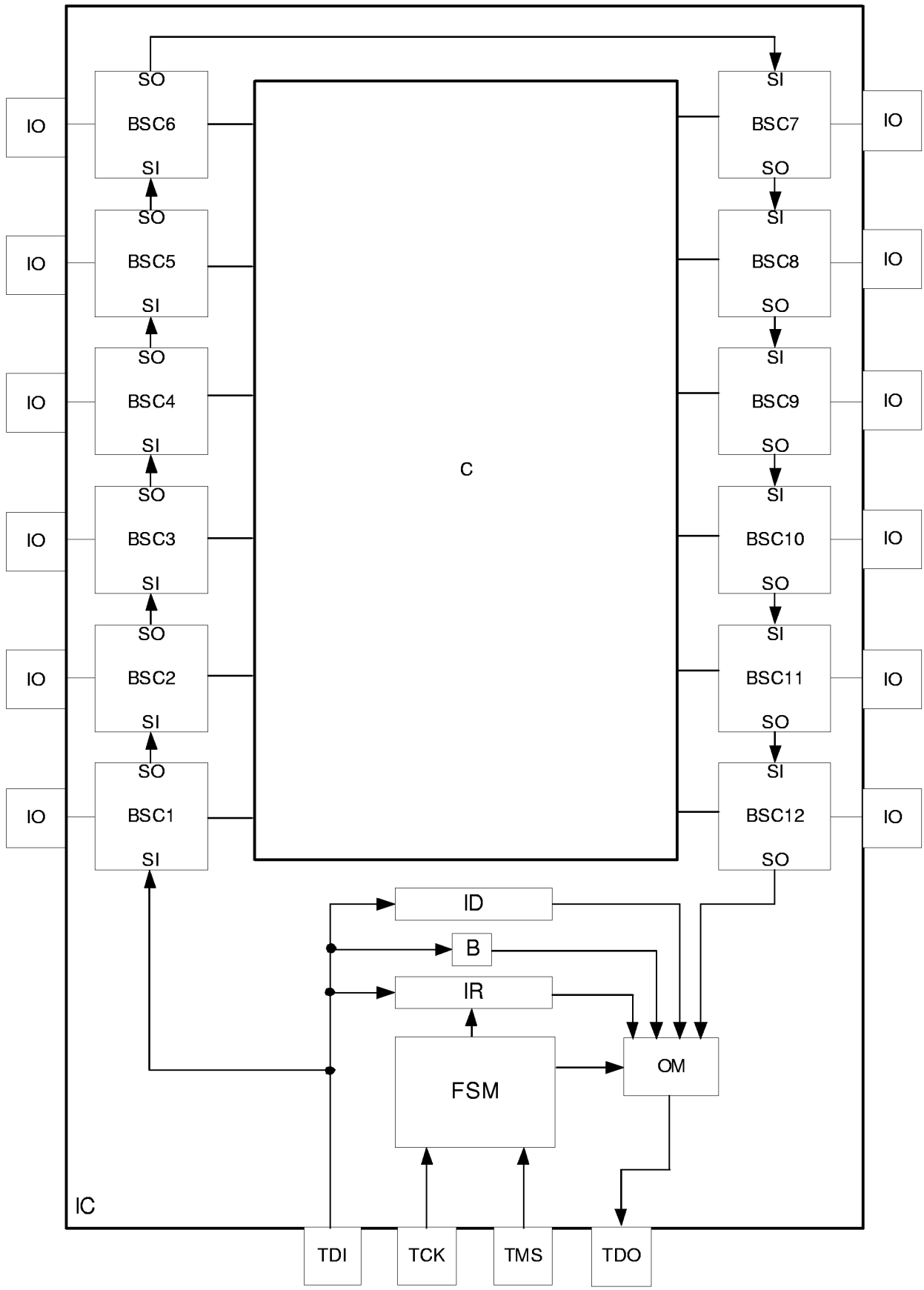
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Fig. 1

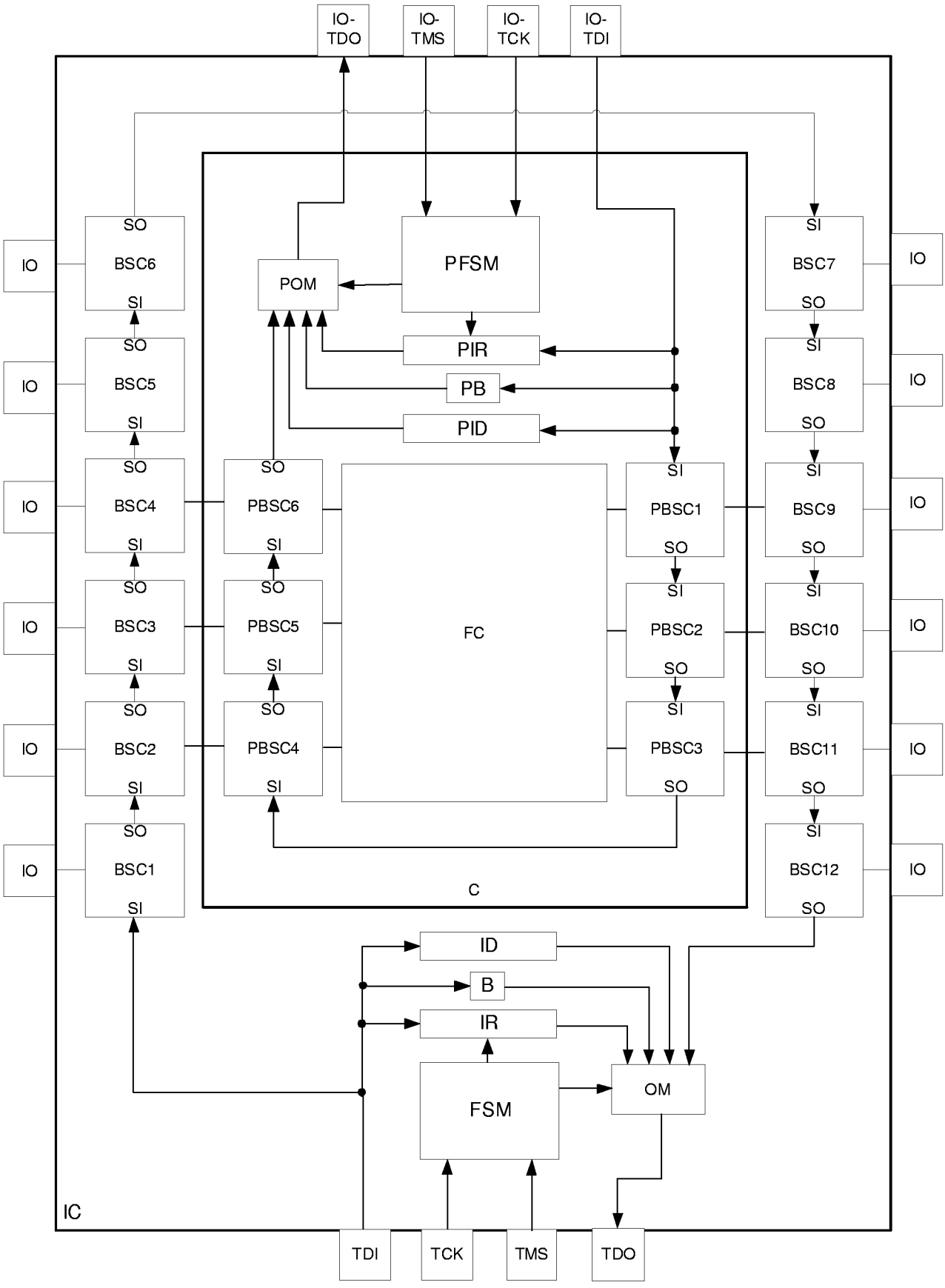
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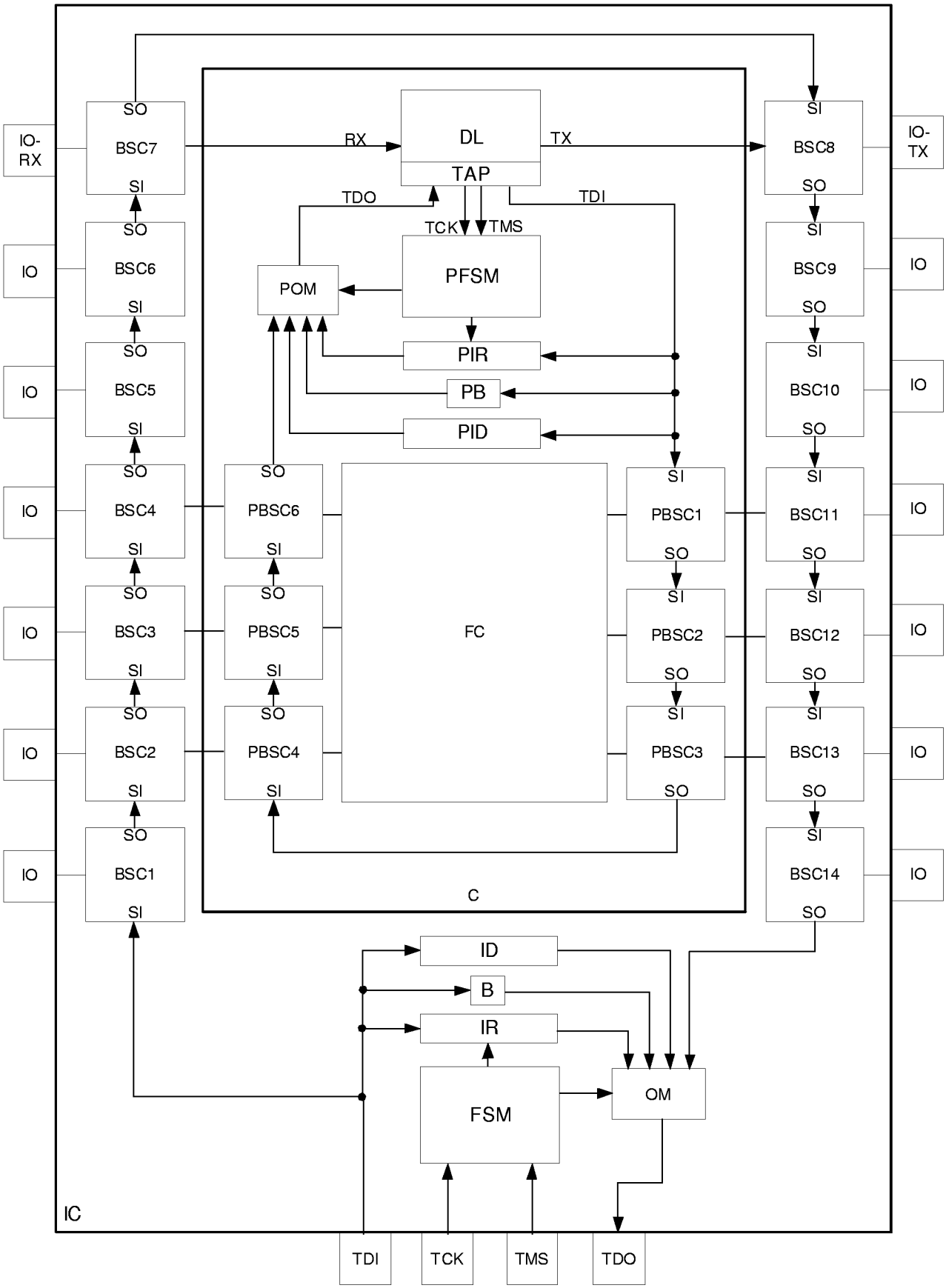
Fig. 2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PBSC4
PBSC3
BSC13
BSC1
BSC14
C
ID
B
IR
FSM
OM
IC
TDI
TCK
TMS
TDO

Fig. 3

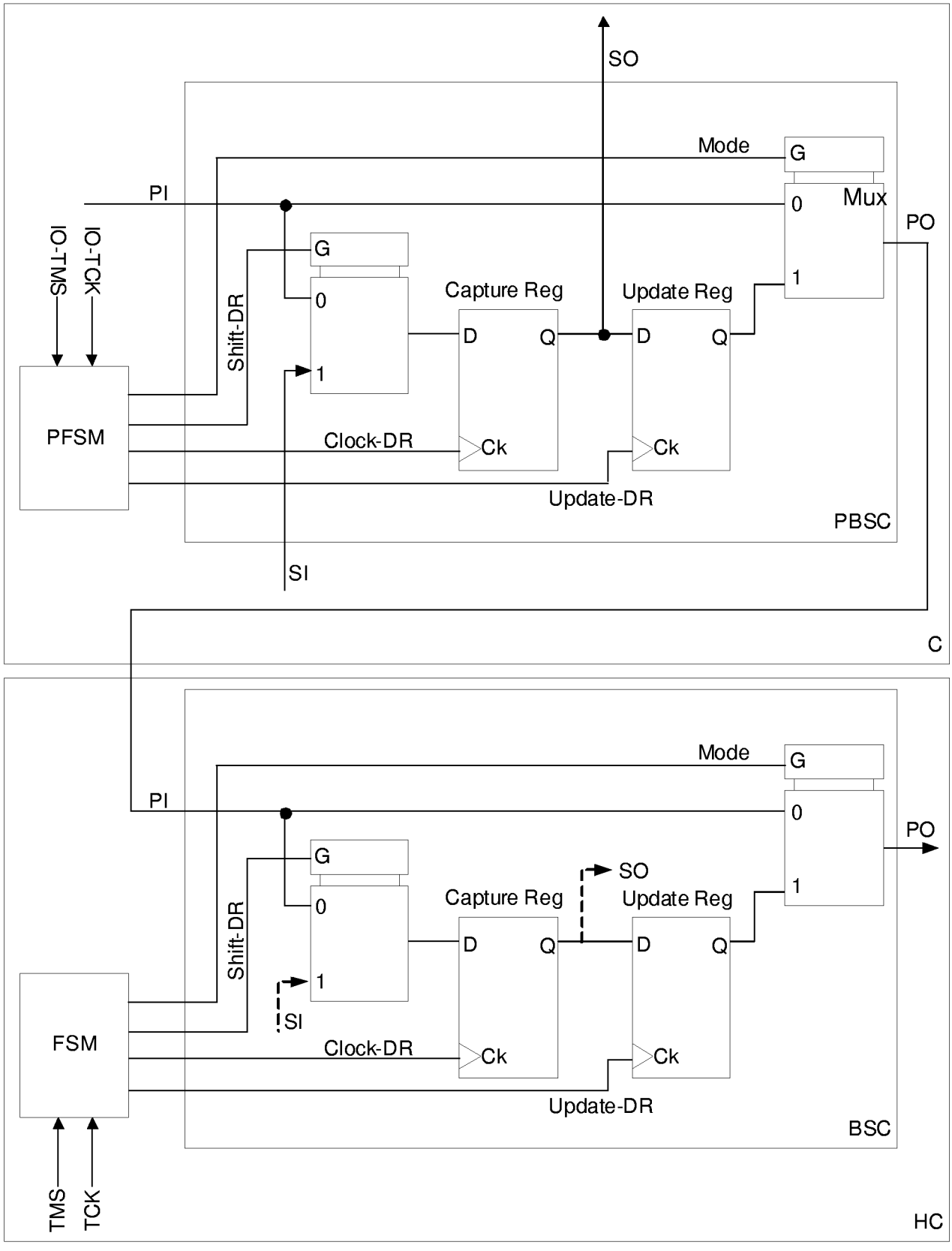
SO
Mode
G
PI
0
Mux
PO
IO-TMS
IO-TCK
G
Shift-DR
0
Capture Reg
Update Reg
D
Q
D
Q
1
1
PFSM
Clock-DR
Ck
Ck
Update-DR
PBSC
SI
C
Mode
G
PI
0
PO
G
SO
Shift-DR
0
Capture Reg
Update Reg
1
D
Q
D
Q
1
SI
FSM
Clock-DR
Ck
Ck
Update-DR
BSC
TMS
TCK
HC

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI2006/050438

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC8: G01R31

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

FI, SE, NO, DK

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI, IEEEXplore

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002040458 A1 (DERVISOGLU, B. et al.) 04 April 2002 (04.04.2002) Fig. 2 and 6; paragraphs [0051],[0052] and [0090]	1, 3, 5, 6
Y	Fig. 2 and 6; paragraphs [0051],[0052] and [0090]	4
Y	EP 1486909 A2 (ST MICROELECTRONICS INC) 15 December 2004 (15.12.2004), Fig. 1; paragraphs [0024] and [0032]-[0035]	4
A	US 6191603 B1 (MURADALI, F. et al.) 20 February 2001 (20.02.2001), whole document	

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 January 2007 (08.01.2007)	29 January 2007 (29.01.2007)

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/FI2006/050438

Patent document cited in search report	Publication date	Patent family members(s)	Publication date
US 2002040458 A1	04/04/2002	US 2005066295 A1	24/03/2005
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EP 1486909 A2	15/12/2004	JP 2005004765 A	06/01/2005
		US 2004222305 A1	11/11/2004
US 6191603 B1	20/02/2001	None	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI2006/050438

CLASSIFICATION OF SUBJECT MATTER

Int.Cl.
G01R 31/3185 (2006.01)
G01R 31/319 (2006.01)