CIRCUIT OF MEASURING LEAKAGE CURRENT IN A SEMICONDUCTOR INTEGRATED CIRCUIT

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ABSTRACT
An integrated circuit includes an operational circuit and a test circuit for measuring a leakage current associated with all or part of the operational circuit. The leakage current measurement circuit may include a mirror circuit configured to mirror leakage current to a current-to-voltage converter and an analog-to-digital converter configured to convert the analog voltage representative of the leakage current developed by the current-to-voltage converter to a digital value.
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CIRCUIT OF MEASURING LEAKAGE CURRENT IN A SEMICONDUCTOR INTEGRATED CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATION


BACKGROUND

[0002] 1. Field

[0003] Embodiments of the inventive concept relate to a semiconductor integrated circuit, and, particularly, to a circuit of measuring a leakage current flowing through transistors or functional blocks included in the semiconductor integrated circuit.

[0004] 2. Description of Related Art

[0005] Leakage current of a transistor maybe measured in order to ensure proper performance of a semiconductor integrated circuit. In a system-on-chip (SoC) integrated circuit, leakage current flowing through a transistor in a specific location in the SoC may be measured to ensure that the SoC will operate with sufficient speed without consuming excessive power.

[0006] Conventionally, leakage current flowing through transistors in a test chip, rather than that flowing through a real product (that is, an operational chip), has been measured. As a result, conventional measurements of leakage current flowing through transistors or functional blocks may not accurately reflect the leakage current flowing through operational chips (operation, that is, in opposition to test chips).

SUMMARY

[0007] In various embodiments of inventive concepts a circuit for measuring a leakage current in a semiconductor integrated circuit includes an operational amplifier configured to receive a reference voltage at a non-inverted input terminal and a feedback voltage at an inverted input terminal connected to a feedback node, and to amplify a difference between the reference voltage and the feedback voltage, a first PMOS transistor having a gate to which an output voltage of the operational amplifier is applied, a source connected to a first supply voltage, and a drain connected to the feedback node, a first switch connected between the feedback node and a circuit block to be tested, a second PMOS transistor having a gate connected to the gate of the first PMOS transistor, and a source connected to the first supply voltage, a resistor connected between a drain of the second PMOS transistor and a ground voltage and an analog-to-digital (A/D) converter configured to perform an A/D conversion on a first voltage signal measured from the resistor to generate output data.

[0008] In various embodiments of inventive concepts a circuit for measuring a leakage current includes a reference voltage configured to have a voltage level lower than the first supply voltage.

[0009] In various embodiments of inventive concepts a circuit for measuring a leakage current includes a second switch connected between the circuit block to be tested and the ground voltage.

[0010] In various embodiments of inventive concepts a circuit for measuring a leakage current includes a circuit block to be tested that includes a first NMOS transistor.

[0011] In various embodiments of inventive concepts a circuit for measuring a leakage current includes a second switch connected between the source of the first NMOS transistor and the ground voltage, a third switch having a first terminal connected to a first terminal of the first switch, a second terminal connected to the ground voltage, and a third terminal connected to a gate of the first NMOS transistor, and a fourth switch having a first terminal connected to a first terminal of the first switch, a second terminal connected to the ground voltage, and a third terminal connected to a drain of the first NMOS transistor.

[0012] In various embodiments of inventive concepts a circuit for measuring a leakage current includes a circuit block to be tested includes a third PMOS transistor.

[0013] In various embodiments of inventive concepts a circuit for measuring a leakage current includes a second switch connected between the drain of the third PMOS transistor and the ground voltage, a third switch having a first terminal connected to a first terminal of the first switch, a second terminal connected to a second supply voltage, and a third terminal connected to a gate of the third PMOS transistor, a fourth switch having a first terminal connected to the first terminal of the first switch, a second terminal connected to the second supply voltage, and a third terminal connected to a source of the third PMOS transistor, and a fifth switch having a first terminal connected to the first terminal of the first switch, a second terminal connected to the second supply voltage, and a third terminal connected to the bulk of the third PMOS transistor.

[0014] In various embodiments of inventive concepts a circuit for measuring a leakage current includes a first NMOS transistor and a third PMOS transistor.

[0015] In various embodiments of inventive concepts a circuit for measuring a leakage current includes a second switch connected between the source of the first NMOS transistor and the ground voltage, a third switch having a first terminal connected to a first terminal of the first switch, a second terminal connected to the ground voltage, and a third terminal connected to the gate of the first NMOS transistor, a fourth switch having a first terminal connected to the first terminal of the first switch, a second terminal connected to the ground voltage, and a third terminal connected to the bulk of the third PMOS transistor.

[0016] In various embodiments of inventive concepts a circuit for measuring a leakage current includes a gate-on current (Ig-on) of an NMOS transistor is measured with the gate of the first NMOS transistor electrically connected to the feedback node;
and the source and drain of the first NMOS transistor electrically connected to the ground voltage.

[0017] In various embodiments of inventive concepts a circuit for measuring a leakage current a drain-off current (I_d_off) of an NMOS transistor is measured with the gate and source of the first NMOS transistor electrically connected to the ground voltage, and the drain of the first NMOS transistor electrically connected to the feedback node.

[0018] In various embodiments of inventive concepts a circuit for measuring a leakage current a gate-off current (I_g_off) of a PMOS transistor is measured with the gate of the third PMOS transistor electrically connected to the feedback node, the source and bulk of the third PMOS transistor electrically connected to the second supply voltage, and the drain of the third PMOS transistor electrically connected to the ground voltage.

[0019] In various embodiments of inventive concepts a circuit for measuring a leakage current a source-off current (I_s_off) of a PMOS transistor is measured with the gate and bulk of the third PMOS transistor electrically connected to the second supply voltage, the source of the third PMOS transistor electrically connected to the feedback node, and the drain of the third PMOS transistor electrically connected to the ground voltage.

[0020] In various embodiments of inventive concepts a circuit for measuring a leakage current a bulk-off current (I_b_off) of a PMOS transistor is measured with the gate and source of the third PMOS transistor electrically connected to the second supply voltage, the bulk of the third PMOS transistor electrically connected to the feedback node, and the drain of the third PMOS transistor electrically connected to the ground voltage.

[0021] In various embodiments of inventive concepts a semiconductor integrated circuit includes a circuit block to be tested and a circuit for measuring leakage current from the test block, wherein the circuit for measuring includes an operational amplifier configured to receive a reference voltage at a non-inverted input terminal and a feedback voltage at an inverted input terminal connected to a feedback node, and amplify a difference between the reference voltage and the feedback voltage, a first PMOS transistor having a gate to which an output voltage of the operational amplifier is applied, a source connected to a first supply voltage, and a drain connected to the feedback node, a first switch connected between the feedback node and the circuit block to be tested, a second PMOS transistor having a gate connected to the gate of the first PMOS transistor, and a source connected to the first supply voltage, a resistor connected between a drain of the second PMOS transistor and a ground voltage, and an A/D converter configured to perform an A/D conversion on a first voltage signal measured from the resistor to generate output data.

[0022] In various embodiments of inventive concepts a semiconductor integrated circuit includes an operational circuit for which leakage current is to be tested and a leakage current measurement circuit configured to test leakage current of the operational circuit, including a mirror circuit to mirror leakage current to a current-to-voltage converter and an analog-to-digital converter configured to convert the analog voltage representative of the leakage current developed by the current-to-voltage converter to a digital value.

[0023] In various embodiments of inventive concepts a semiconductor integrated circuit includes a mirror circuit that includes transistors of different sizes to yield an output current that is a multiple of the leakage current, the multiplying factor being the ratio of sizes of mirror circuit transistors.

[0024] In various embodiments of inventive concepts a semiconductor integrated circuit includes a current-to-voltage converter that is a resistor.

[0025] In various embodiments of inventive concepts a semiconductor integrated circuit leakage current measurement circuit is switchably connected to the operational circuit for which leakage current is to be tested.

[0026] In various embodiments of inventive concepts a semiconductor integrated circuit the multiple of a current mirror is chosen to correlate the input range of the analog-to-digital-converter to the output of the current to voltage converter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The foregoing and other features and advantages of inventive concepts will be apparent from the more particular description of embodiments of the inventive concepts, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the inventive concepts. In the drawings:

[0028] FIG. 1 is a circuit diagram illustrating a semiconductor integrated circuit that includes a circuit for measuring a leakage current according to an embodiment of the inventive concept;

[0029] FIG. 2 is a circuit diagram illustrating a semiconductor integrated circuit that includes a circuit for measuring a leakage current according to another embodiment of the inventive concept;

[0030] FIG. 3 is a circuit diagram illustrating a semiconductor integrated circuit that includes a circuit for measuring a leakage current according to still another embodiment of the inventive concept;

[0031] FIG. 4 is a circuit diagram illustrating a semiconductor integrated circuit that includes a circuit for measuring a leakage current according to yet another embodiment of the inventive concept;

[0032] FIG. 5 is a table illustrating voltages applied to transistors included in an integrated circuit according to modes of measuring a leakage current;

[0033] FIG. 6 is a circuit diagram illustrating a semiconductor integrated circuit that includes a circuit for measuring a leakage current according to yet another embodiment of the inventive concept;

[0034] FIG. 7 is a circuit diagram illustrating a semiconductor integrated circuit that includes a circuit for measuring a leakage current according to yet another embodiment of the inventive concept;

[0035] FIG. 8 is a circuit diagram illustrating a semiconductor integrated circuit that includes a circuit for measuring a leakage current according to yet another embodiment of the inventive concept; and

[0036] FIG. 9 is a circuit diagram illustrating a semiconductor integrated circuit that includes a circuit for measuring a leakage current according to yet another embodiment of the inventive concept.

DESCRIPTION

[0037] Various exemplary embodiments will be described more fully hereinafter with reference to the accompanying
drawings, in which exemplary embodiments are shown. Exemplary embodiments may, however, be embodied in many different forms and should not be construed as limited to exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure will be thorough, and will convey the scope of exemplary embodiments to those skilled in the art. In the drawings, the sizes and relative sizes of layers and regions may be exaggerated for clarity.

[0038] It will be understood that when an element or layer is referred to as being “on,” “connected to” or “coupled to” another element or layer, it can be directly on, connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being “directly on,” “directly connected to” or “directly coupled to” another element or layer, there are no intervening elements or layers present. Like numerals refer to like elements throughout. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items. The term “or” is used in an inclusive sense unless otherwise indicated.

[0039] It will be understood that, although the terms first, second, third, for example, may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. In this manner, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of exemplary embodiments.

[0040] Spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatial relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as “below” or “beneath” other elements or features would then be oriented “above” the other elements or features. In this manner, the express term “below” can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0041] The terminology used herein is for the purpose of describing particular exemplary embodiments only and is not intended to be limiting of exemplary embodiments. As used herein, the singular forms “a,” “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises” and/or “comprising,” when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0042] Exemplary embodiments are described herein with reference to illustrations that are schematic illustrations of idealized exemplary embodiments (and intermediate structures). As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. In this manner, exemplary embodiments should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, an implanted region illustrated as a rectangle will, typically, have rounded or curved features and/or a gradient of implant concentration at its edges rather than a binary change from implanted to non-implanted region. Likewise, a buried region formed by implantation may result in some implantation in the region between the buried region and the surface through which the implantation takes place. In this manner, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to limit the scope of exemplary embodiments.

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which exemplary embodiments belong. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein. When it is possible to implement any embodiment in any other way, a function or an operation specified in a specific block may be performed differently from a flow specified in a flowchart. For example, two consecutive blocks may actually perform the function or the operation simultaneously, and the two blocks may perform the function or the operation conversely according to a related operation or function.

[0043] Inventive concepts will now be described more fully with reference to the accompanying drawings, in which embodiments of inventive concepts are shown.

[0044] In exemplary embodiments in accordance with principles of inventive concepts, a semiconductor device may incorporate one or more leakage testing circuits to measure the leakage current of devices, circuits, or functional blocks that are a part of the same device that the testing circuit is a part of. By employing “on-board” leakage current test circuits (that is, leakage current test circuits that are a part of the operational device, rather than a separate device devoted to testing) a system and method in accordance with principles of inventive concepts may improve testing results and reduce requirements for output pads, for example. In exemplary embodiments a leakage current testing circuit may include an amplifier that may be connected through switches to a circuit to be tested and an analog-to-digital converter configured to measure the circuit’s leakage current. Switches may be operated by a self-test circuit or by processor integral to the integrated circuit, for example, to measure various currents. A plurality of such leakage current test circuits may be incorporated in a semiconductor device in accordance with principles of inventive concepts, each dedicated to one or more circuits to be tested. In various configurations test circuits may be configured to test NAND, NOR, or INVERTER circuits, for example. Semiconductor devices in accordance with principles of inventive concepts may be implemented in system-on-chip (SoC) circuits, for example. A leakage current measurement circuit in accordance with principles of inventive concepts may include a mirror circuit configured to mirror leakage current to a current-to-voltage converter (which may be a resistor), and an analog-to-digital converter configured to convert the analog voltage representative of the
leakage current developed by the current-to-voltage converter to a digital value. A leakage current measurement circuit in accordance with principles of inventive concepts may be switchably configured to test leakage current during a test mode or to be disconnected from the circuit during an operational mode. The mode in which the leakage current measurement test circuit operates may be controlled by a self-test circuit or processor, for example, that also resides in the operational integrated circuit.

[0045] FIG. 1 is a circuit diagram illustrating a semiconductor integrated circuit 100 that includes an exemplary embodiment of a circuit for measuring leakage current in accordance with principles of inventive concepts. Semiconductor integrated circuit 100 may include a block to be tested 150 and a circuit 110 for measuring the leakage current of the block to be tested 150.

[0046] The circuit 110 for measuring a leakage current may include an operational amplifier OP1, a first PMOS transistor MP1, a first switch 113, a second PMOS transistor MP2, a resistor R1 and an analog-to-digital (A/D) converter 111.

[0047] In exemplary embodiments operational amplifier OP1 receives a reference voltage VREF1 at a non-inverted input terminal and a feedback voltage VFB at an inverted input terminal connected to a feedback node NFB, and amplifies a difference between the reference voltage VREF1 and the feedback voltage VFB. The first PMOS transistor MP1 has a gate to which an output voltage of the operational amplifier OP1 is applied, a source connected to a first supply voltage VDDH and a drain connected to the feedback node NFB. The first switch 113 is connected between the feedback node NFB and the block to be tested 150. The second PMOS transistor MP2 has a gate connected to the gate of the first PMOS transistor MP1, and a source connected to the first supply voltage VDDH. The resistor R1 is connected between a drain of the second PMOS transistor MP2 and a ground voltage GND. The A/D converter 111 performs an A/D conversion on a first voltage signal measured from the resistor R1 to generate output data DOUT. This digital representation of the measured leakage current may be employed by a semiconductor chip in accordance with principles of inventive concepts as a measure of the chip’s, or segment of the chip’s, operational efficiency, for example.

[0048] In exemplary embodiments circuit 110 for measuring leakage current includes a second switch 112 connected between the block to be tested 150 and the ground voltage GND.

[0049] The reference voltage VREF1 may have a voltage level lower than the first supply voltage VDDH. The first supply voltage VDDH may have a voltage level higher than a second supply voltage VDD supplied to the block to be tested 150. In exemplary embodiments, the reference voltage VREF1 may have a voltage level of the second supply voltage VDD. Additionally, the voltage of the feedback node NFB, that is a feedback voltage VFB, may have nearly the same voltage level of the reference voltage VREF1.

[0050] The leakage current ILK flowing through the block to be tested 150 flows through the first PMOS transistor MP1, and then flows through the second PMOS transistor MP2 connected to the first PMOS transistor MP1 in a current-mirror form and the resistor R1. That is, because transistors MP1 and MP2 are arranged as a current mirror, the leakage current ILK flowing through transistor MP1 is reflected in transistor MP2. When the size (W/L) of the second PMOS transistor MP2 is A times larger than the first PMOS transistor MP1, a current corresponding to A times of ILK may flow through the second PMOS transistor MP2. That is, leakage current ILK may be multiplied by the size ratio(487,876),(596,915) of the first transistor to the second transistor. The A/D converter 111 performs an A/D conversion on the first voltage signal measured from the resistor R1 to generate output data DOUT, a digital representation of leakage current ILK. In this manner, the circuit 110 for measuring a leakage current may measure a leakage current flowing through transistors or functional blocks included in each of semiconductor integrated circuits of a real product (that is, an operational integrated circuit), without requiring separate pads that may be required for testing were a conventional approach to testing, one requiring external test circuits, employed.

[0051] FIG. 2 is a circuit diagram illustrating an exemplary embodiment of a semiconductor integrated circuit 200 that includes a circuit for measuring a leakage in accordance with principles of inventive concepts. Semiconductor integrated circuit 200 may include a block to be tested 250 and a circuit 210 for measuring a leakage current from the block to be tested 250. The block to be tested 250 may include a first NMOS transistor MN1.

[0052] The circuit 210 for measuring leakage current may include an operational amplifier OP1, a first PMOS transistor MP1, a first switch 113, a second PMOS transistor MP2, a resistor R1, an A/D converter 111, a second switch 112, a third switch 114 and a fourth switch 115.

[0053] In exemplary embodiments second switch 112 is connected between a source of the first NMOS transistor MN1 and the ground voltage GND. The third switch 114 has a first terminal connected to a first terminal of the first switch 113, a second terminal connected to the ground voltage GND, and a third terminal connected to a gate of the first NMOS transistor MN1. The fourth switch 115 has a first terminal connected to a first terminal of the first switch 113, a second terminal connected to the ground voltage GND, and a third terminal connected to a drain of the first NMOS transistor MN1.

[0054] In exemplary embodiments, switches 112 through 115 may be operated so that, when gate-on current (Ig_on) of an NMOS transistor is measured, the gate of the first NMOS transistor may be electrically connected to the feedback node NFB, and the source and drain of the first NMOS transistor MN1 may be electrically connected to the ground voltage GND and when drain-off current (Id_off) of an NMOS transistor is measured, the gate and source of the first NMOS transistor MN1 may be electrically connected to the ground voltage GND, and the drain of the first NMOS transistor MN1 may be electrically connected to the feedback node NFB. Operation of current mirror MP1/MP2, operational amplifier OP1, and A/D converter 111 has been described in detail in the discussion related to FIG. 1 and that description will not be repeated here.

[0055] FIG. 3 is a circuit diagram illustrating an exemplary embodiment of a semiconductor integrated circuit 300 that includes a circuit for measuring a leakage current in accordance with principles of inventive concepts. Semiconductor integrated circuit 300 may include a block to be tested 350 and a circuit 310 for measuring a leakage current associated with the block to be tested 350. The block to be tested 350 may include a third PMOS transistor MP3.

[0056] The circuit 310 for measuring a leakage current may include an operational amplifier OP1, a first PMOS transistor MP1, a first switch 113, a second PMOS transistor MP2, a
resistor R1, an A/D converter 111, a second switch 120, a third switch 117, a fourth switch 118 and a fifth switch 119.

[0057] In exemplary embodiments, switch 120 is connected between a drain of the third PMOS transistor MP3 and the ground voltage GND. Third switch 117 has a first terminal connected to a first terminal of the first switch 113, a second terminal connected to a second terminal and a third terminal connected to a gate of the third PMOS transistor MP3. The fourth switch 118 has a first terminal connected to the first terminal of the first switch 113, a second terminal connected to the second supply voltage VDD, and a third terminal connected to a source of the third PMOS transistor MP3. The fifth switch 119 has a first terminal connected to the second terminal of the first switch 113, a second terminal connected to the second supply voltage VDD, and a third terminal connected to a bulk of the third PMOS transistor MP3.

[0058] In exemplary embodiments switches 113, 117, 118, 119, and 120 may be operated so that, when a gate-off current (Ig_off) of a PMOS transistor is measured, the gate of the third PMOS transistor MP3 may be electrically connected to the feedback node NFB, the source and bulk of the third PMOS transistor MP3 may be electrically connected to the second supply voltage VDD, and the drain of the third PMOS transistor MP3 may be electrically connected to the ground voltage GND. Additionally, when a source-off current (Is_off) of a PMOS transistor is measured, the gate and bulk of the third PMOS transistor MP3 may be electrically connected to the second supply voltage VDD, the source of the third PMOS transistor MP3 may be electrically connected to the feedback node NFB, and the drain of the third PMOS transistor MP3 may be electrically connected to the ground voltage GND. Also, when a bulk-off current (Ig_off) of a PMOS transistor is measured, the gate and source of the third PMOS transistor MP3 may be electrically connected to the second supply voltage VDD, the bulk of the third PMOS transistor MP3 may be electrically connected to the feedback node NFB, and the drain of the third PMOS transistor MP3 may be electrically connected to the ground voltage GND. Operation of current mirror MP1/MP2, operational amplifier OP1, and A/D converter 111 has been described in detail in the discussion related to FIG. 1 and that description will not be repeated here.

[0059] FIG. 4 is a circuit diagram illustrating an exemplary embodiment of a semiconductor integrated circuit 400 that includes a circuit for measuring a leakage current in accordance with principles of inventive concepts. Semiconductor integrated circuit 400 may include a block to be tested 450 and a circuit 410 for measuring leakage current associated with the block to be tested 450. The block to be tested 450 may include a second NMOS transistor MN2 and a fourth PMOS transistor MP4.

[0060] The circuit 410 for measuring a leakage current may include an operational amplifier OP1, a first PMOS transistor MP1, a first switch 113, a second PMOS transistor MP2, a resistor R1, an A/D converter 111, a second switch 112, a third switch 114, a fourth switch 115, a fifth switch 120, a sixth switch 117, a seventh switch 118 and an eighth switch 119.

[0061] The second switch 112 is connected between a source of the second NMOS transistor MN2 and the ground voltage GND. The third switch 114 has a first terminal connected to a first terminal of the first switch 113, a second terminal connected to the ground voltage GND, and a third terminal connected to a gate of the second NMOS transistor MN2. The fourth switch 115 has a first terminal connected to the first terminal of the first switch 113, a second terminal connected to the ground voltage GND, and a third terminal connected to a drain of the second NMOS transistor MN2. The fifth switch 120 is connected between a drain of the fourth PMOS transistor MP4 and the ground voltage GND. The sixth switch 117 has a first terminal connected to the first terminal of the first switch 113, a second terminal connected to a second supply voltage VDD, and a third terminal connected to a gate of the fourth PMOS transistor MP4. The seventh switch 118 has the first terminal connected to the first terminal of the first switch 113, a second terminal connected to the second supply voltage VDD, and a third terminal connected to a source of the third PMOS transistor. The eighth switch 119 has the first terminal connected to the first terminal of the first switch 113, a second terminal connected to the second supply voltage VDD, and a third terminal connected to a bulk of the fourth PMOS transistor MP4.

[0062] In exemplary embodiments switches 112, 114, 115, 117, 118, and 120 may be operated so that, when a gate-on current (Ig_on) of an NMOS transistor is measured, the gate of the second NMOS transistor MN2 may be electrically connected to the feedback node NFB, and the source and drain of the second NMOS transistor MN2 may be electrically connected to the ground voltage GND. When a drain-off current (Ig_off) of an NMOS transistor is measured, the gate and source of the second NMOS transistor MN2 may be electrically connected to the ground voltage GND, and the drain of the second NMOS transistor MN2 may be electrically connected to the feedback node NFB. Additionally, when a gate-off current (Ig_off) of a PMOS transistor is measured, the gate of the fourth PMOS transistor MP4 may be electrically connected to the feedback node NFB, the source and bulk of the fourth PMOS transistor MP4 may be electrically connected to the second supply voltage VDD, and the drain of the fourth PMOS transistor MP4 may be electrically connected to the ground voltage GND. When a source-off current (Ig_off) of a PMOS transistor is measured, the gate and bulk of the fourth PMOS transistor MP4 may be electrically connected to the second supply voltage VDD, the source of the fourth PMOS transistor MP4 may be electrically connected to the feedback node NFB, and the drain of the fourth PMOS transistor MP4 may be electrically connected to the ground voltage GND. Also, when a bulk-off current (Ig_off) of a PMOS transistor is measured, the gate and source of the fourth PMOS transistor MP4 may be electrically connected to the second supply voltage VDD, the bulk of the fourth PMOS transistor MP4 may be electrically connected to the feedback node NFB, and the drain of the fourth PMOS transistor MP4 may be electrically connected to the ground voltage GND. Operation of current mirror MP1/MP2, operational amplifier OP1, and A/D converter 111 has been described in detail in the discussion related to FIG. 1 and that description will not be repeated here.

[0063] FIG. 5 is a table illustrating voltages applied to transistors included in an integrated circuit according to modes of measuring a leakage current in accordance with principles of inventive concepts. As indicated in the table, in the mode in which a gate-on current Ig_on of an NMOS transistor is measured, the feedback voltage VFB may be applied to the gate of the NMOS transistor, and the source and drain of the NMOS transistor may be electrically connected to the ground voltage GND. In the mode in which a drain-off
current $I_{d\_off}$ of an NMOS transistor is measured, the gate and source of the NMOS transistor may be electrically connected to the ground voltage GND, and the feedback voltage VFB may be applied to the drain of the NMOS transistor.

In the mode in which a gate-off current $I_{g\_off}$ of a PMOS transistor is measured, the feedback voltage VFB may be applied to the gate of the PMOS transistor, the second supply voltage VDD may be applied to the source and bulk of the PMOS transistor, and the drain of the PMOS transistor may be electrically connected to the ground voltage GND. In the mode in which a source-off current $I_{s\_off}$ of a PMOS transistor is measured, the second supply voltage VDD may be applied to the gate and bulk of the PMOS transistor, the feedback voltage VFB may be applied to the source of the PMOS transistor, and the drain of the fourth PMOS transistor MP4 may be electrically connected to the ground voltage GND. In the mode in which a bulk-off current $I_{b\_off}$ of a PMOS transistor is measured, the second supply voltage VDD may be applied to the gate and source of the fourth PMOS transistor MP4, the feedback voltage VFB may be applied to the bulk of the PMOS transistor, and the drain of the PMOS transistor may be electrically connected to the ground voltage GND.

FIG. 6 is a circuit diagram illustrating an exemplary embodiment of a semiconductor integrated circuit 500 that includes a circuit for measuring a leakage current in accordance with principles of inventive concepts. Semiconductor integrated circuit 500 may include a block to be tested 550 and a circuit 110 for measuring a leakage current from the block to be tested 550. The circuit 110 for measuring a leakage current in FIG. 6 may have the same configuration as the circuit 110 for measuring a leakage current shown in FIG. 1. The block to be tested 550 may include an inverter that includes a PMOS transistor MP1 and an NMOS transistor MN11. The circuit 110 for measuring a leakage current in FIG. 6 may measure a leakage current flowing through the block to be tested 550 that includes the inverter. Operation of current mirror MP1/MIP2, operational amplifier OP1, and A/D converter 111 has been described in detail in the discussion related to FIG. 1 and that description will not be repeated here.

FIG. 7 is a circuit diagram illustrating an exemplary embodiment of a semiconductor integrated circuit 600 that includes a circuit for measuring a leakage current in accordance with principles of inventive concepts. Semiconductor integrated circuit 600 may include a block to be tested 650 and a circuit 110 for measuring a leakage current from the block to be tested 650. The circuit 110 for measuring a leakage current from the block to be tested 650 may include a NAND gate. The circuit 110 for measuring a leakage current in FIG. 7 may measure a leakage current flowing through the block to be tested 650 that includes the NAND gate. Operation of current mirror MP1/MIP2, operational amplifier OP1, and A/D converter 111 has been described in detail in the discussion related to FIG. 1 and that description will not be repeated here.

FIG. 8 is a circuit diagram illustrating an exemplary embodiment of a semiconductor integrated circuit 700 that includes a circuit for measuring a leakage current in accordance with principles of inventive concepts. Semiconductor integrated circuit 700 may include a block to be tested 750 and a circuit 110 for measuring a leakage current from the block to be tested 750. The circuit 110 for measuring a leakage current in FIG. 8 may have the same configuration as the circuit 110 for measuring a leakage current shown in FIG. 1. The block to be tested 750 may include a NOR gate. The circuit 110 for measuring a leakage current in FIG. 8 may measure a leakage current flowing through the block to be tested 750 that includes the NOR gate. Operation of current mirror MP1/MIP2, operational amplifier OP1, and A/D converter 111 has been described in detail in the discussion related to FIG. 1 and that description will not be repeated here.

FIG. 9 is a circuit diagram illustrating an exemplary embodiment of a semiconductor integrated circuit 800 that includes a circuit for measuring a leakage current in accordance with principles of inventive concepts. Semiconductor integrated circuit 800 may include a plurality of leakage current measuring circuits 802 and 804 and a plurality of functional blocks 810 to 860.

The semiconductor integrated circuit 800 shown in FIG. 9 may measure leakage current flowing through functional blocks 810 to 860 using leakage current measuring circuits 802 and 804 included in the semiconductor integrated circuit 800. Each of the leakage current measuring circuits 802 and 804 may be configured as any of the circuits 110, 210, 310 or 410 for measuring a leakage current according to exemplary embodiments in accordance with principles of inventive concepts and may measure leakage currents flowing through the functional blocks 810 to 860.

A circuit for measuring leakage current from a semiconductor integrated circuit according to embodiments of inventive concepts is able to precisely measure leakage current flowing through transistors or functional blocks included in a semiconductor integrated circuit of a real product (that is, an operational chip, not a test chip). Because the testing takes place “on board” the chip, no additional pads are required for testing. Exemplary embodiments of inventive concepts may be applied to a semiconductor integrated circuit, and particularly, to a system-on-chip (SoC).

The foregoing is illustrative of embodiments and is not to be construed as limiting thereof. Although a few embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in embodiments without materially departing from the novel teachings and advantages. Accordingly, all such modifications are intended to be included within the scope of inventive concepts as defined in the claims. The foregoing is illustrative of various embodiments and is not to be construed as limited to the specific embodiments disclosed, and that modifications to the disclosed embodiments, as well as other embodiments, are intended to be included within the scope of the appended claims.

What is claimed is:

1. A circuit for measuring a leakage current in a semiconductor integrated circuit, comprising:
   - an operational amplifier configured to receive a reference voltage at a non-inverted input terminal and a feedback voltage at an inverted input terminal connected to a feedback node, and to amplify a difference between the reference voltage and the feedback voltage;
   - a first PMOS transistor having a gate to which an output voltage of the operational amplifier is applied, a source connected to a first supply voltage, and a drain connected to the feedback node;
a first switch connected between the feedback node and a circuit block to be tested;
a second PMOS transistor having a gate connected to the gate of the first PMOS transistor, and a source connected to the first supply voltage;
a resistor connected between a drain of the second PMOS transistor and a ground voltage; and
an analog-to-digital (A/D) converter configured to perform an A/D conversion on a first voltage signal measured from the resistor to generate output data.

2. The circuit of claim 1, wherein the reference voltage is configured to have a voltage level lower than the first supply voltage.

3. The circuit of claim 1, further comprising:
a second switch connected between the circuit block to be tested and the ground voltage.

4. The circuit of claim 1, wherein the circuit block to be tested includes a first NMOS transistor.

5. The circuit of claim 4, further comprising:
a second switch connected between a source of the first NMOS transistor and the ground voltage;
a third switch having a first terminal connected to a first terminal of the first switch, a second terminal connected to the ground voltage, and a third terminal connected to a gate of the first NMOS transistor; and
a fourth switch having a first terminal connected to a first terminal of the first switch, a second terminal connected to the ground voltage, and a third terminal connected to a drain of the first NMOS transistor.

6. The circuit of claim 1, wherein the circuit block to be tested includes a third PMOS transistor.

7. The circuit of claim 6, further comprising:
a second switch connected between a drain of the third PMOS transistor and the ground voltage;
a third switch having a first terminal connected to a first terminal of the first switch, a second terminal connected to a second supply voltage, and a third terminal connected to a gate of the third PMOS transistor;
a fourth switch having a first terminal connected to the first terminal of the first switch, a second terminal connected to the ground voltage, and a third terminal connected to a source of the third PMOS transistor; and
a fifth switch having a first terminal connected to a first terminal of the first switch, a second terminal connected to the second supply voltage, and a third terminal connected to a bulk of the third PMOS transistor.

8. The circuit of claim 1, wherein the circuit block to be tested includes a first NMOS transistor and a third PMOS transistor.

9. The circuit of claim 8, further comprising:
a second switch connected between a source of the first NMOS transistor and the ground voltage;
a third switch having a first terminal connected to a first terminal of the first switch, a second terminal connected to the ground voltage, and a third terminal connected to a gate of the first NMOS transistor;
a fourth switch having a first terminal connected to the first terminal of the first switch, a second terminal connected to the ground voltage, and a third terminal connected to a drain of the first NMOS transistor; and
a fifth switch connected between a drain of the third PMOS transistor and the ground voltage;
a sixth switch having a first terminal connected to the first terminal of the first switch, a second terminal connected to a second supply voltage, and a third terminal connected to a gate of the third PMOS transistor;
a seventh switch having the first terminal connected to the first terminal of the first switch, a second terminal connected to the second supply voltage, and a third terminal connected to a source of the third PMOS transistor; and
an eighth switch having a first terminal connected to the first terminal of the first switch, a second terminal connected to the second supply voltage, and a third terminal connected to a bulk of the third PMOS transistor.

10. The circuit of claim 9, wherein a gate-on current (I_{on}) of an NMOS transistor is measured with the gate of the first NMOS transistor electrically connected to the feedback node, and the source and drain of the first NMOS transistor electrically connected to the ground voltage.

11. The circuit of claim 9, wherein a drain-off current (I_{off}) of an NMOS transistor is measured with the gate and source of the first NMOS transistor electrically connected to the ground voltage, and the drain of the first NMOS transistor electrically connected to the feedback node.

12. The circuit of claim 9, wherein a gate-off current (I_{g-off}) of a PMOS transistor is measured with the gate of the third PMOS transistor electrically connected to the feedback node, the source and bulk of the third PMOS transistor electrically connected to the second supply voltage, and the drain of the third PMOS transistor electrically connected to the ground voltage.

13. The circuit of claim 9, wherein a source-off current (I_{s-off}) of a PMOS transistor is measured with the gate and bulk of the third PMOS transistor electrically connected to the second supply voltage, the source of the third PMOS transistor electrically connected to the feedback node, and the drain of the third PMOS transistor electrically connected to the ground voltage.

14. The circuit of claim 9, wherein a bulk-off current (I_{b-off}) of a PMOS transistor is measured with the gate and source of the third PMOS transistor electrically connected to the second supply voltage, the bulk of the third PMOS transistor electrically connected to the feedback node, and the drain of the third PMOS transistor electrically connected to the ground voltage.

15. A semiconductor integrated circuit, comprising:
a circuit block to be tested; and
a circuit for measuring leakage current from the test block, wherein the circuit for measuring comprises:
an operational amplifier configured to receive a reference voltage at a non-inverted input terminal and a feedback voltage at an inverted input terminal connected to a feedback node, and amplify a difference between the reference voltage and the feedback voltage;
a first PMOS transistor having a gate to which an output voltage of the operational amplifier is applied, a source connected to a first supply voltage, and a drain connected to the feedback node;
a first switch connected between the feedback node and the circuit block to be tested;
a second PMOS transistor having a gate connected to the gate of the first PMOS transistor, and a source connected to the first supply voltage;
a resistor connected between a drain of the second PMOS transistor and a ground voltage; and
an A/D converter configured to performing an A/D conversion on a first voltage signal measured from the resistor to generate output data.
16. A semiconductor device, comprising:
an operational circuit for which leakage current is to be
tested; and
a leakage current measurement circuit configured to test
leakage current of the operational circuit, including a
mirror circuit to mirror leakage current to a current-to-
voltage converter and an analog-to-digital converter
configured to convert the analog voltage representative
of the leakage current developed by the current-to-volt-
age converter to a digital value.

17. The semiconductor device of claim 16, wherein the
mirror circuit includes transistors of different sizes to yield an
output current that is a multiple of the leakage current, the
multiplying factor being the ratio of sizes of mirror circuit
transistors.

18. The semiconductor device of claim 16, wherein the
current-to-voltage converter is a resistor.

19. The semiconductor device of claim 16, wherein the
leakage current measurement circuit is switchably connected
to the operational circuit for which leakage current is to be
tested.

20. The semiconductor device of claim 17, wherein the
multiple is chosen to correlate the input range of the analog-
to-digital-converter to the output of the current to voltage
converter.