

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
25 August 2011 (25.08.2011)

(10) International Publication Number
WO 2011/103214 A1

- (51) International Patent Classification:
H01L 21/00 (2006.01)
- (21) International Application Number:
PCT/US2011/025127
- (22) International Filing Date:
16 February 2011 (16.02.2011)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
61/305,121 16 February 2010 (16.02.2010) US
13/028,380 16 February 2011 (16.02.2011) US
- (71) Applicant (for all designated States except US): **CY-
PRESS SEMICONDUCTOR CORPORATION**
[US/US]; 198 Champion Court, San Jose, California
95134 (US).
- (72) Inventor; and
(75) Inventor/Applicant (for US only): **OLSON, Tim**
[US/US]; 198 Champion Court, San Jose, California
95134 (US).
- (81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP,
KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD,
ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI,
NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD,
SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG,
ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,

[Continued on next page]

(54) Title: INTEGRATED SHIELDING FOR WAFER PLATING

(57) Abstract: A semiconductor substrate carrier for use during wet chemical processing may comprise a conductive flange to couple the carrier with processing equipment, a frame coupled with the conductive flange, where the frame is configured to hold a semiconductor substrate, and an integrated shield coupled with the frame. The integrated shield is configured to alter an electric field near at least a portion of a surface of the semiconductor substrate during the wet chemical processing.

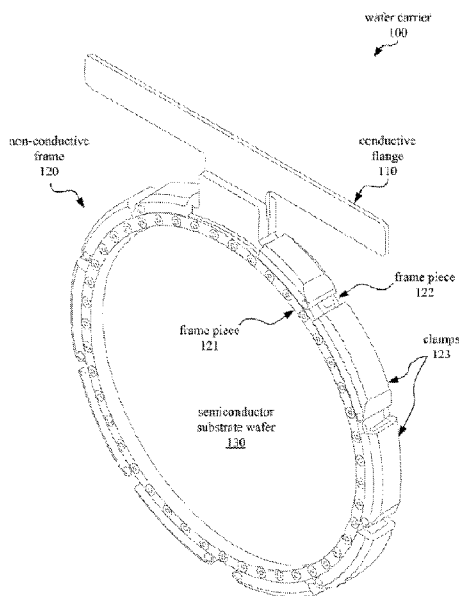


FIGURE 1



WO 2011/103214 A1

LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, **Published:**
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, — *with international search report (Art. 21(3))*
GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

INTEGRATED SHIELDING FOR WAFER PLATING

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 61/305,121, filed on February 16, 2010.

TECHNICAL FIELD

[0002] This disclosure relates to the field of semiconductor device manufacturing and, in particular, to an integrated shield for use in wet chemical processing of a substrate.

BACKGROUND

[0003] Integrated circuits are formed through a process known as semiconductor device fabrication. The semiconductor device may be formed on a thin slice, or wafer, of semiconductor material, such as silicon crystal. The wafer serves as a substrate for microelectronic devices built on the wafer. During fabrication of these integrated circuits, the silicon wafer is put through a sequence of wet chemical processing steps. One wet chemical processing step in the sequence is electrochemical deposition, commonly known as electroplating.

[0004] In the electroplating process, electrical current is used to deposit

metal ions from a solution onto a wafer, forming a film or patterned structure of metal on the wafer. Certain semiconductor packaging technologies, such as Wafer Level Chip Scale Packaging and Flip Chip, involve multiple electroplating steps. Many electroplating processes make use of semiconductor fabrication plant (fab) equipment. The fab equipment is designed to plate a single wafer at a time causing the electroplating process to be slow. The fab equipment is also typically very expensive. In addition, downtime is common due to high maintenance requirements and plating chemistries are expensive due to the small quantities used. These factors result in a high cost per wafer to perform electroplating.

[0005] Plating equipment used in other industries, including batch and continuous processing systems used in traditional semiconductor packaging are considerably less expensive and more efficient than the fab equipment. This plating equipment may include that used for printed circuit boards or leadframe plating lines. Such plating equipment provides typical throughputs which are approximately ten times greater than that of fab equipment at a cost that is typically half that of the fab equipment.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present disclosure is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0007] **Figure 1** illustrates an embodiment of a semiconductor substrate carrier.

[0008] **Figure 2A** illustrates an embodiment of a semiconductor substrate carrier having an integrated shield with holes.

[0009] **Figure 2B** illustrates a cross section of a semiconductor substrate carrier having an integrated shield, according to an embodiment.

[0010] **Figure 2C** illustrates an embodiment of a semiconductor substrate carrier having an integrated shield with holes.

[0011] **Figure 3** illustrates an embodiment of a semiconductor substrate carrier with an integrated shield having a central cutout.

[0012] **Figure 4** illustrates an embodiment of a semiconductor substrate carrier with an integrated shield having slot shaped cutouts.

[0013] **Figure 5** illustrates an embodiment of a semiconductor substrate carrier with an integrated shield having a star shaped cutout.

[0014] **Figure 6** is a flow diagram illustrating a process for using a semiconductor substrate with an integrated shield, according to an embodiment.

DETAILED DESCRIPTION

[0015] The following description sets forth numerous specific details such as examples of specific systems, components, methods, and so forth, in order to provide a good understanding of several embodiments of the present invention. It will be apparent to one skilled in the art, however, that at least some embodiments of the present invention may be practiced without these specific details. In other instances, well-known components or methods are not described in detail or are presented in a simple block diagram format in order to avoid unnecessarily obscuring the present invention. Thus, the specific details set forth are merely exemplary. Particular implementations may vary from these exemplary details and still be contemplated to be within the spirit and scope of the present invention.

[0016] Described herein is a method and apparatus for a semiconductor substrate carrier having an integrated shield. Such a carrier may hold a semiconductor substrate wafer during electroplating or other wet chemical processing of the substrate using low cost, printed circuit board or leadframe style plating equipment.

[0017] A carrier with integrated shielding may allow a significant cost reduction for one of the most expensive process steps in creating a wafer-level

chip scale package (WLCSP) or wafer bump, which is the electroplating process.

In one embodiment, the semiconductor substrate carrier may be used to electroplate 200 mm and 300 mm semiconductor wafers on low cost, in-line plating equipment such as those used to plate leadframe packages. In one embodiment, the integrated shielding may be used to control uniformity of the thickness of the plating across the substrate.

[0018] The current industry standard for electroplating semiconductor substrate wafers to create a WLCSP or bump structure involves use of a single wafer, fab style machine such as a SemiTool Raider platform. These machines typically run at 10 to 20 wafers per hour and may cost approximately 4 million dollars. In one embodiment, a semiconductor substrate carrier with integrated shielding may enable the use of well proven, low cost leadframe strip plating or similar equipment to create the WLCSP and bump structures. Plating semiconductor substrate wafers using these inline strip type machines will enable a throughput on the order of 100 to 200 wafers per hour, while the cost of the machine may be much lower, at approximately 2 million dollars.

[0019] In one embodiment, an integrated circuit (IC) or discrete semiconductor wafer may be automatically placed into a semiconductor substrate carrier with integrated shielding. The carrier may be loaded onto a belt, transfer arm(s), flight bar(s) or other transport mechanisms of the

electroplating equipment. The transport mechanism(s) may move the semiconductor substrate through various chemicals to accomplish the electroplating or other wet chemical process. Once the process is complete, the wafer may be automatically removed from the carrier.

[0020] In one embodiment, the carrier may be single sided such that the carrier holds a single wafer. Alternatively, the carrier may be dual sided and may hold two wafers. A dual sided carrier may be used to approximately double the throughput of an in-line plating system.

[0021] Depending on the embodiment, the substrate held in the carrier may be any of a number of different substrate types. For example, the substrate may be a crystalline substrate, such as a semiconductor wafer, a composite material such as a laminate substrate or molded structure, a flex circuit or polymer based structure, a metallic substrate, or other type of substrate. As an example, further description herein will be in terms of a wafer and the carrier may be referred to as a wafer carrier, however, this description shall not be construed as limiting in any way.

[0022] **Figure 1** is a diagram illustrating a wafer carrier 100, which is one embodiment of a semiconductor substrate carrier. The wafer carrier 100 includes a conductive flange 110 which couples the wafer carrier 100 to a machine transport mechanism within a plating machine (not shown). In one embodiment,

the processing equipment may include an in-line plating machine. The in-line plating machine may be similar to equipment used in leadframe strip plating lines. Leadframe strip plating lines are well established in the packaging industry and may generally suspend and traverse conductive copper leadframes on a metal belt through a sequence of steps in the plating process. In another embodiment, the wafer carrier may be used with rack style plating equipment such as that used in electroplating of printed circuit boards. In other embodiments, some other transport mechanism may be used.

[0023] Conductive flange 110 emulates a leadframe and may be used to create a temporary mechanical and electrical connection to a conductive metal transfer belt of the plating equipment. In one embodiment, the conductive flange 110 attaches to the transport mechanism of the plating equipment and allows the wafer carrier 100 to be advanced through the plating machine. Electrical contact may be established between the plating machine and the conductive flange enabling a plating electrical circuit to be selectively established when the carrier and semiconductor substrate 130 is suspended by the machine transport mechanism in a wet chemical bath during processing. In one embodiment, the wafer carrier may maintain low resistance electrical contact between the conductive flange and the outer 2.5 mm edge of the semiconductor substrate wafer 130 for carrying high plating currents.

[0024] In one embodiment conductive flange 110 may be formed from stainless steel, although in other embodiments, conductive flange 110 may be formed from another conductive material such as, for example, copper, another metal, or a non-metal conductive material. In one embodiment, the neck of a conductive flange, which is a portion of the conductive flange connected with the frame 120, may be shorter or longer than the neck of conductive flange 110, as illustrated in Figure 1. In one embodiment, the length of the neck may be adjustable.

[0025] In one embodiment, conductive flange 110 is thin enough to afford it some degree of flexibility. In certain in-line plating machines, the belt may be curved around drums as the belt changes direction. The conductive flange 110, when attached to the belt, may be sufficiently flexible to also curve around the drums. In one embodiment, conductive flange 110 may be flexible enough to bend in an arc having a radius of approximately 24 inches.

[0026] Wafer carrier 100 also includes non-conductive frame 120 that prevents plating of anything except an outer surface of the semiconductor wafer 130. For example, the non-conductive frame may prevent plating of contacts, wafer sides, the wafer back, or elements of the carrier itself. Nonconductive frame 120 is coupled to conductive flange 110 so that non-conductive frame 120 is able to be suspended from the machine transport mechanism of the plating

machine. In one embodiment, non-conductive frame 120 is formed from a ring of nonconductive material, such as for example chlorinated polyvinyl chloride (CPVC). In other embodiments, other non-conductive materials may be used. Non-conductive frame 120 may be formed into a ring of non-conductive material having an inside diameter slightly smaller than the diameter of the wafer 130 to be electroplated. For example, nonconductive frame 120 may be sized appropriately to hold a 200 millimeter (mm) or a 300 mm silicon wafer. In other embodiments, non-conductive frame 120 may be sized to hold a wafer having some other size.

[0027] In one embodiment, non-conductive frame 120 may be formed from two separate frame pieces 121 and 122. Frame pieces 121 and 122 may be identical or substantially identical having one or more built-in clamps 123 to hold the pieces 121 and 122 together. In one embodiment, the frame pieces 121 and 122 clamp together to create a sealed assembly that prevents process chemicals from attacking or plating electrical contacts, as well as sides and back of wafer 130. In one embodiment, a vacuum test system may be used to ensure adequate sealing for each wafer loaded into the carrier.

[0028] In one embodiment, each frame piece is identical and includes half of the total number of clamps. In other embodiments, the clamps 123 may all be included on one frame piece or arranged between the two frame pieces in some

other proportion. In one embodiment, each frame piece 121 and 122 holds a wafer such as wafer 130 and the frame pieces 121 and 122 are secured together with the wafers being oriented parallel to one another and held together by clamps 123 to form non-conductive frame 120. The frame pieces 121 and 122 may be oriented so that the wafers are back-to-back, with the front side of each wafer facing out. Optionally, a spacer or spacers may be placed in between the two wafers within the frame assembly to provide a compliant layer. In one embodiment, the frame can hold two semiconductor substrates or one substrate and one dummy structure to handle uneven batch sizes.

[0029] In one embodiment, the frame pieces 121 and 122 may be secured together using magnets instead of clamps. For example, one or both of frames 121 and 122 may include a series of magnets spaced around the perimeter for attaching the frame 121 or 122 to another frame piece. In one embodiment, the magnets may be recessed into one or both of the frame pieces 121 and 122.

[0030] **Figure 2A** illustrates an embodiment of a wafer carrier 200 having an integrated shield 210. In one embodiment, the integrated shielding 210 affects the electrical field within the plating process enabling deposition of a uniform thickness across the area of the wafer 130. In an alternative embodiment, the integrated shielding 210 may also be used to restrict or control the flow of liquid

during wet chemical processing of the wafer 130. In one embodiment, the shield 210 may be made from plastic or some other non-conductive material.

[0031] In one embodiment, the shield 210 is attached to the non-conductive frame 120. For example, shield 210 may be attached to frame piece 121 of the frame 120 using one or more fasteners such as screws 220 or some type of snap or sliding fit fasteners. In one embodiment, the screws 220 are arranged along the perimeter of the shield 210. In one embodiment where two semiconductor wafers such as wafer 130 may be held within the carrier 200, fasteners such as screws 220 may be used in similar fashion to attach a second shield (not shown) to frame piece 122.

[0032] In one embodiment, one or more retaining guides may be attached to one of the frame pieces 121 or 122 to form a slot into which shield 210 may be inserted and held in place parallel to a wafer 130.

[0033] In one embodiment, the shield 210 has one or more holes 230 or cutout sections such as cutout section 240 designed to control the electrical field or the flow of plating fluid or other liquid chemical near the surface of the wafer 130 during wet chemical processing. In one embodiment, the area corresponding to the cutout section 240 and the holes 230 decreases nearer to the edges of the shield 210 such that the flow of ions or plating fluid or other chemical is more restricted near the edges of the wafer 130. For example, the holes 230 nearer to

the center of the integrated shield 210 may be larger in diameter than the holes 230 that are nearer to the edge of the shield 210. Alternatively, the holes 230 may be similar in size, and the density of the holes 230 may increase nearer to the center of the shield 210.

[0034] In one embodiment, the progressively increasing restriction of ion flow or the flow of plating fluid towards the edges of the wafer 130 counteracts the tendency of thicker plating to be deposited near the edges of the wafer 130 during the plating process. Thus, the shield 210 allows for more uniform plating over the surface of the wafer 130. In one embodiment, the pattern of holes 230 and the size or shape of cutout section 240 may be changed to control the uniformity of the plating for other applications.

[0035] **Figure 2B** illustrates a cross section of the wafer carrier 200. Carrier 200 is holding two semiconductor substrate wafers 130 and 131 and has an integrated shield 210 and 211 for each of the wafers 130 and 131, respectively. Shield 210 is attached to the frame piece 121 of non-conductive frame 120 by screws including screw 221, while shield 211 is attached to the other frame piece 122 of non-conductive frame 120 by screws including screw 222.

[0036] **Figure 2B** illustrates the back-to-back orientation of the wafers 130 and 131 in the carrier 200, in an embodiment of a carrier 200 capable of holding two

wafers. In one embodiment, the outer surfaces wafers 130 and 131 are spaced apart from the shields 210 and 211.

[0037] **Figure 2C** illustrates an embodiment of a wafer carrier 200 having an integrated shield 212 which may be attached to wafer carrier 200 via nonconductive frame 120 in a similar fashion as shield 210. Integrated shield 212 is designed to fully cover a semiconductor wafer held by wafer carrier 200, with the exception of a number of holes 231 distributed across the surface of the shield 212. In one embodiment, the holes 231 are larger near the center of the shield 212 and smaller near the edge of shield 212. For example, the holes 231 may be approximately 1/4 inch in diameter near the center and may be approximately 1/16 inches in diameter near the edges. In one embodiment, the sizes of the holes 231 may become progressively larger from the center to the edge of the shield 212.

[0038] **Figure 3** illustrates an embodiment of a wafer carrier 300 having a shield 310 with a single large cutout section 340. The shield 310 restricts the flow of ions in solution or of liquid chemical, such as plating fluid, near the edges of the wafer 130 by blocking the fluid with the solid material of the shield 310. In one embodiment, the shield 310 may be made from plastic or some other non-conductive material.

[0039] **Figure 4** illustrates an embodiment of a wafer carrier 400 having a shield 410 with a cutout section 440 and several slot-shaped holes 430. In one embodiment, the slots 430 are arranged around a perimeter of the shield 410. The shield 410 can thus restrict the flow of ions in solution or of liquid chemical, such as plating fluid, near the edges of the wafer 130, while the cutout section 440 allows for less restricted flow of the liquid chemical near the center of the wafer 130. In one embodiment, the shield 410 may be made from plastic or some other non-conductive material.

[0040] **Figure 5** illustrates an embodiment of a wafer carrier 500 having an integrated shield 510 with a star-shaped cutout section 540. The area of the cutout section 540 includes several outwardly radiating points that taper as they approach the edges of the shield 510. Thus, the shield 510 has more solid material to restrict the flow of ions in solution or of liquid chemical, such as plating fluid, near the edges of the wafer 130. In one embodiment, the shield 510 may be made from plastic or some other non-conductive material.

[0041] The wafer carrier with integrated shield could also be used on more conventional rack type plating lines in either single or dual configurations. It would also be possible to extend the concept to 4, 8 or perhaps more wafers depending upon the size of the wafers and practical limitations. In one embodiment, the wafer carrier with integrated shield may be used to hold 200 &

300 mm semiconductor wafers. Alternatively, a wafer carrier with integrated shield could also be used for other size semiconductor wafers such as 4 inch, 5 inch, 150mm or perhaps someday, 450mm. The wafer carrier could also be used for plating solar wafers.

[0042] In addition to the electrochemical deposition, the wafer carrier described herein may be used during other wet chemical processing steps. These processing steps may include for example, plating pattern resist strip, etching of the seed layer metal, or other processes. During electroplating, a template formed from a plating pattern resist, such as a photoresist, is applied to the surface of the wafer, covering a portion of the surface. The uncovered portion of the wafer surface is electroplated. In a subsequent processing step, the plating pattern resist is removed during plating pattern resist strip. A seed layer metal on the wafer, which may be formed from titanium-tungsten and copper, is removed through an etching process. Etchants are applied to the wafer to remove the exposed seed layer metal. In one embodiment, the wafer carrier may hold the wafers during these and other processes.

[0043] **Figure 6** is a flow diagram illustrating a process 600 for shielding a semiconductor wafer during a plating process or other wet chemical process. In one embodiment, the shielding process 600 may be performed by a wafer carrier such one of wafer carriers 200, 300, 400, or 500, as illustrated in Figures 2A-5.

[0044] The process 600 begins at block 602. At block 602, the semiconductor substrate wafer is automatically placed in a wafer carrier prior to wet chemical processing. In one embodiment, the wet chemical processing may be an electroplating process.

[0045] From block 602, the process 600 continues at block 604. At block 602, the wafer carrier is used to hold the semiconductor substrate wafer between a first frame piece and a second frame piece of the wafer carrier. For example, the wafer 130 may be held between frame pieces 121 and 122 of non-conductive frame 120, as illustrated in Figures 2A and 2B. In one embodiment, the wafer carrier may hold two wafers 130 and 131 between the frame pieces 121 and 122. The frame pieces 121 and 122 may be held together by clamps 123 to form a non-conductive frame 120 holding the wafers 130 and 131.

[0046] From block 604, the process 600 continues at block 606. At block 606, the carrier is coupled with wet chemical processing equipment. For example, a wafer carrier 200 may have a conductive flange 110 that may be attached to a belt which is driven by the processing equipment. In one embodiment, the conductive flange 110 emulates a leadframe in a leadframe plating machine, such that an electrical connection may be established between the plating equipment and the wafer 130 through the conductive flange 110. The plating machine may

thus apply the appropriate potentials to the wafer during the wet chemical processing.

[0047] From block 606, the process 600 continues at block 608. At block 608, the processing equipment moves the wafer carrier through plating fluid or some other liquid chemical during the wet chemical process. For example, the belt to which the wafer carrier 200 is attached may be used to convey the wafer carrier 200, along with the wafer 130, through a liquid chemical, such as plating fluid.

[0048] From block 608, the process 600 continues at block 610. At block 610, the carrier maintains a position of a shield relative to the semiconductor substrate wafer by coupling the shield to a frame piece. For example, with reference to Figure 2A, the shield 210 may be fastened to the frame piece 121 of the non-conductive frame 120 by screws 220. The screws 220 hold the shield 210 so that it remains in a fixed position relative to the wafer 130 for the duration of the plating process or other wet chemical process. In one embodiment, the shield 210 may already be attached to the frame piece when the wafer 130 is placed in the carrier 200 at block 602.

[0049] From block 610, the process 600 continues at block 612. At block 612, the shield alters the electric field to restrict the flow of ions and may physically restrict the flow of plating fluid or another liquid chemical near specific portions of the semiconductor substrate. In one embodiment, the flow of ions or fluid is

progressively more restricted towards the edges of the wafer, and is less restricted near the center of the wafer. For example, the shield 210 may have holes 230 and a cutout section 240 such that the area corresponding to the holes 230 or the cutout section 240 is greater near the center of the shield 210. The shield 210 may thus allow greater flow of ions or fluid through the large cutout section 240 near the center of the wafer 130, and more restricted flow of ions or fluid through the smaller holes 230 near the edges of the wafer 130. The flow of ions and liquid chemical, such as plating fluid, is thus controlled during the electroplating processor other wet chemical process. In one embodiment, use of the shield 210 results in a more uniform plating thickness across the surface of the wafer 130.

[0050] From block 612, the process 600 continues at block 614. At block 614, the semiconductor substrate wafer is automatically removed from the carrier. For example, after the plating or other wet chemical process is completed for a wafer 130, the wafer 130 may be automatically removed from the wafer carrier 200.

[0051] In one embodiment, the operations represented by blocks 602-614 of process 600 may be performed during wet chemical processing to control the flow of a liquid chemical near the surface of the semiconductor substrate. In one embodiment, the process 600 may be used to ensure an even deposit of plating material over the surface of the semiconductor substrate.

[0052] Embodiments of the present invention, described herein, include various operations. These operations may be performed by hardware components, software, firmware, or a combination thereof. Although the operations of the methods herein are shown and described in a particular order, the order of the operations of each method may be altered so that certain operations may be performed in an inverse order or so that certain operation may be performed, at least in part, concurrently with other operations. In another embodiment, instructions or sub-operations of distinct operations may be in an intermittent and/or alternating manner. As used herein, the term "coupled to" may mean coupled directly or indirectly through one or more intervening components.

[0053] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A semiconductor substrate carrier, comprising:
 - a conductive flange configured to couple the carrier with processing equipment;
 - a frame coupled with the conductive flange, wherein the frame is configured to hold a semiconductor substrate; and
 - an integrated shield coupled with the frame, wherein the integrated shield is configured to alter an electric field near at least a portion of a surface of the semiconductor substrate during wet chemical processing.
2. The semiconductor substrate carrier of claim 1, wherein the integrated shield is further configured to restrict flow of a fluid near at least a portion of the surface of the semiconductor substrate.
3. The semiconductor substrate carrier of claim 1, wherein the integrated shield further comprises at least one coupling device configured to attach the integrated shield to the carrier.

4. The semiconductor substrate carrier of claim 3, wherein the at least one coupling device comprises at least one screw.
5. The semiconductor substrate carrier of claim 3, wherein the at least one coupling device is configured to attach the integrated shield to the frame.
6. The semiconductor substrate carrier of claim 1, wherein the frame is further configured to hold a second semiconductor substrate.
7. The semiconductor substrate carrier of claim 6, further comprising a second integrated shield configured to alter the electric field near at least a portion of a surface of the second semiconductor substrate during the wet chemical processing.
8. The semiconductor substrate carrier of claim 1, wherein the integrated shield is configured to alter the electric field near an edge of the semiconductor substrate.
9. The semiconductor substrate carrier of claim 1, wherein the integrated shield comprises a surface having one or more holes.

10. The semiconductor substrate carrier of claim 9, wherein a density of the one or more holes is greater nearer to a center of the semiconductor substrate.
11. The semiconductor substrate carrier of claim 1, wherein the integrated shield comprises a surface having a cutout section.
12. The semiconductor substrate carrier of claim 11, wherein the area of the cutout section is greater nearer a center of the semiconductor substrate.
13. The semiconductor substrate carrier of claim 1, wherein the integrated shield comprises a nonconductive material.
14. The semiconductor substrate carrier of claim 1, wherein the frame is made from a nonconductive material.
15. The semiconductor substrate carrier of claim 1, wherein the frame comprises:
 - a first frame piece; and
 - a second frame piece coupled with the first frame piece, wherein the frame is configured to hold the semiconductor wafer between the first frame piece and the second frame piece.

16. The semiconductor substrate carrier of claim 15, further comprising one or more magnets configured to attach the first frame piece to the second frame piece.
17. A method, comprising:
holding a semiconductor substrate in a carrier;
coupling the carrier to wet chemical processing equipment; and
during wet chemical processing,
maintaining a position of a shield relative to the semiconductor substrate, and
altering an electric field near at least a portion of the semiconductor substrate using the shield.
18. The method of claim 16, further comprising restricting flow of fluid near the semiconductor substrate using the shield.
19. The method of claim 18, wherein the fluid comprises plating fluid.
20. The method of claim 16, further comprising moving the semiconductor substrate through process fluids.

21. The method of claim 16, wherein altering the electric field comprises altering the electric field near an edge of the semiconductor substrate.
22. The method of claim 16, wherein holding the semiconductor substrate in the carrier comprises holding the semiconductor substrate between a first frame piece and a second frame piece.
23. The method of claim 22, further comprising attaching the first frame piece to the second frame piece using one or more magnets.
24. The method of claim 22, wherein maintaining the position of the shield relative to the semiconductor substrate comprises coupling the shield to the first frame piece or the second frame piece.
25. An apparatus, comprising:
- means for holding a semiconductor substrate;
 - means for coupling the means for holding with wet chemical processing equipment;
 - means for altering an electric field near a surface of the semiconductor substrate during wet chemical processing; and

means for maintaining a position of the means for altering the electric field relative to the semiconductor substrate.

26. The apparatus of claim 25, wherein the means for maintaining the position further comprises means for attaching the means for restricting with the means for holding the semiconductor substrate.

27. The apparatus of claim 25, wherein the means for restricting flow of the fluid comprises means for restricting flow of the fluid near a surface of a second semiconductor substrate.

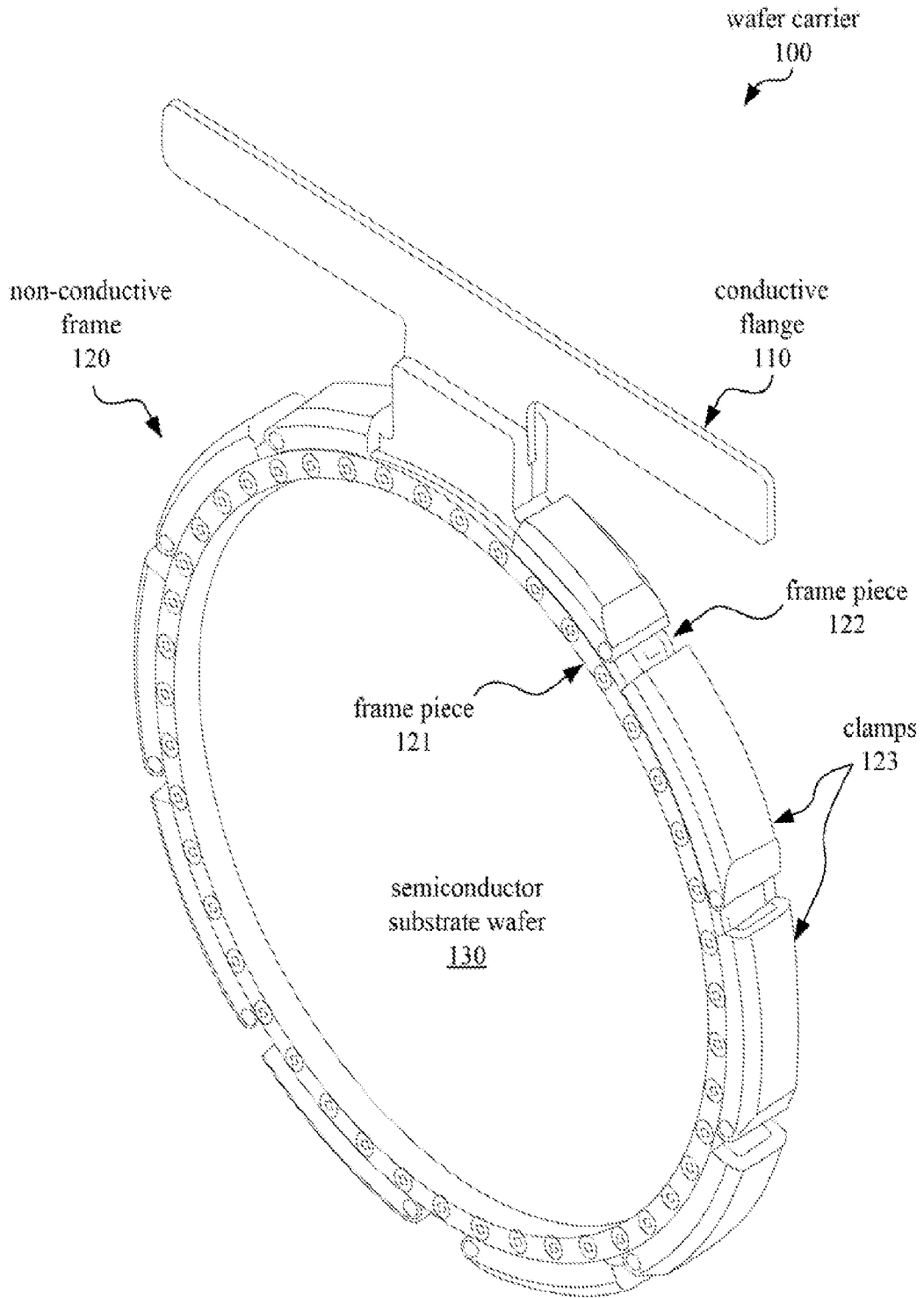


FIGURE 1

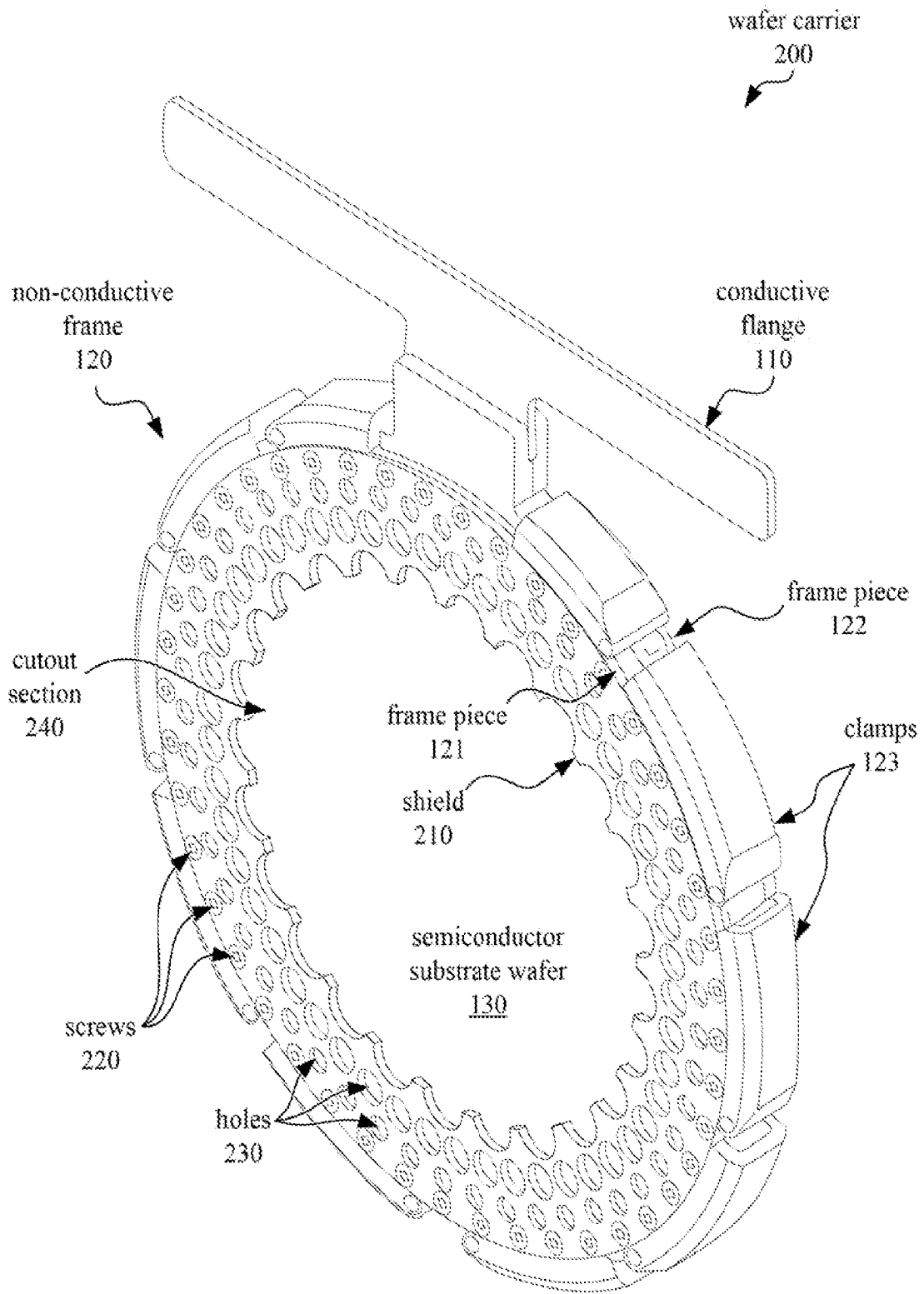


FIGURE 2A

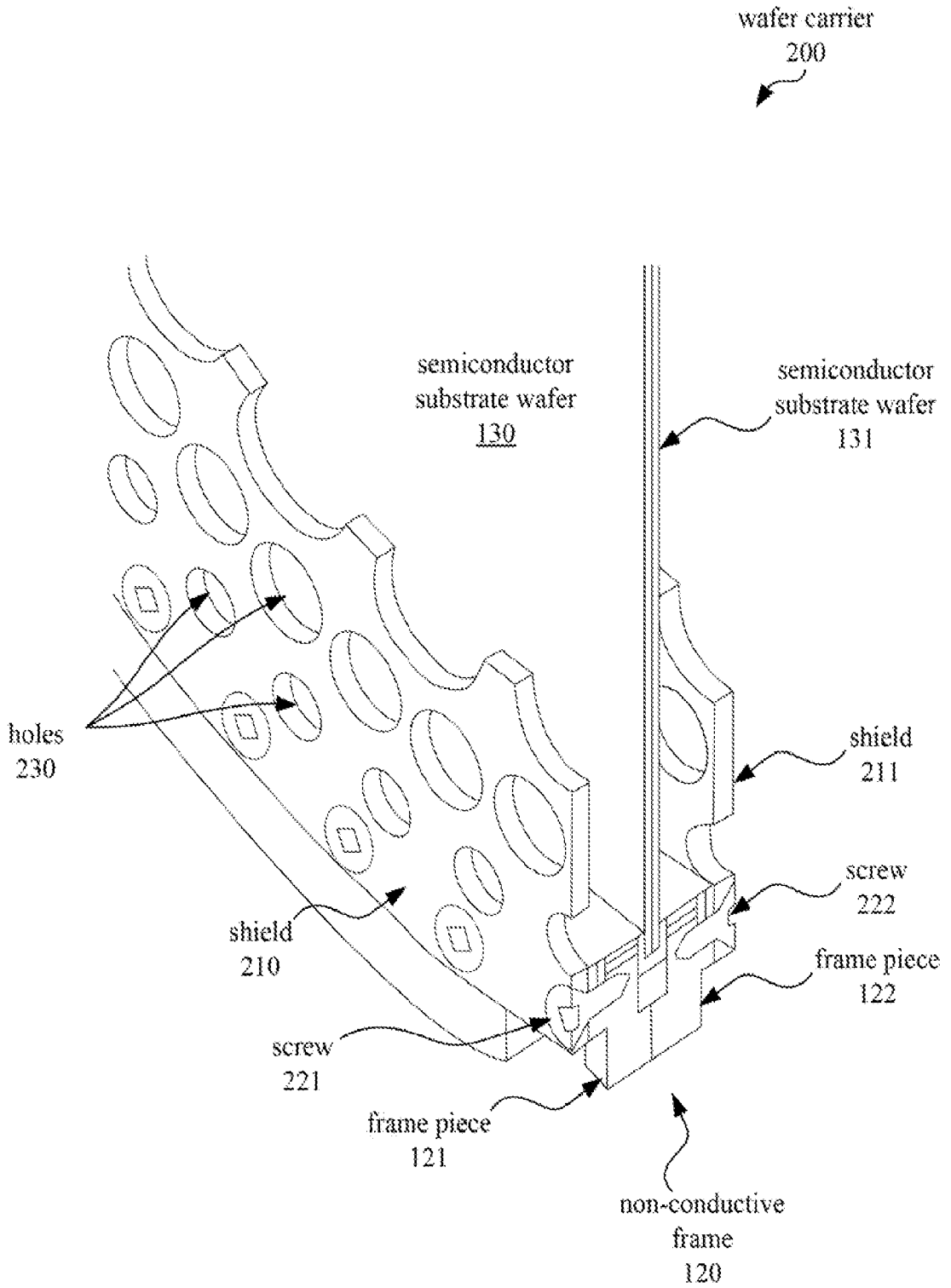


FIGURE 2B

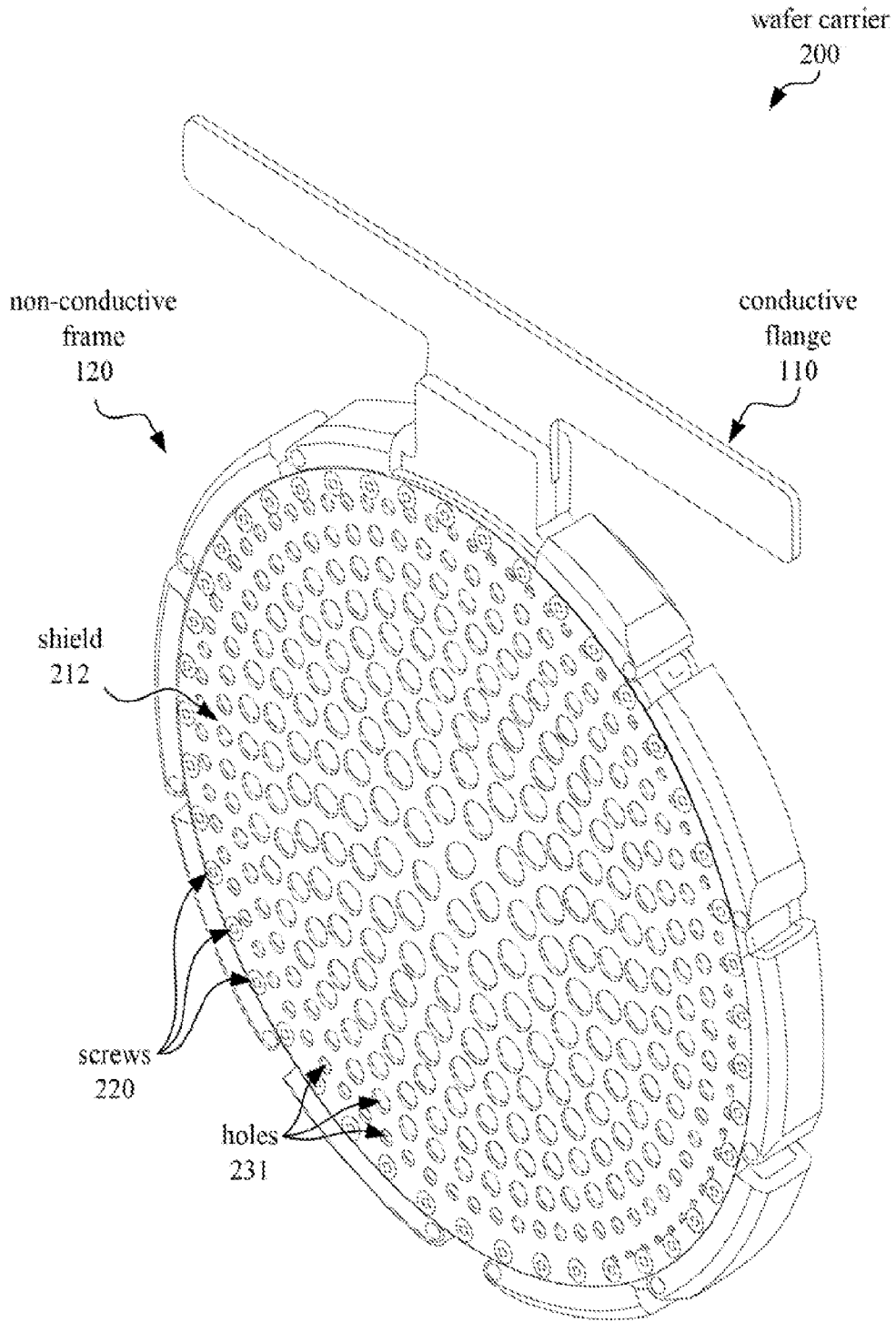


FIGURE 2C

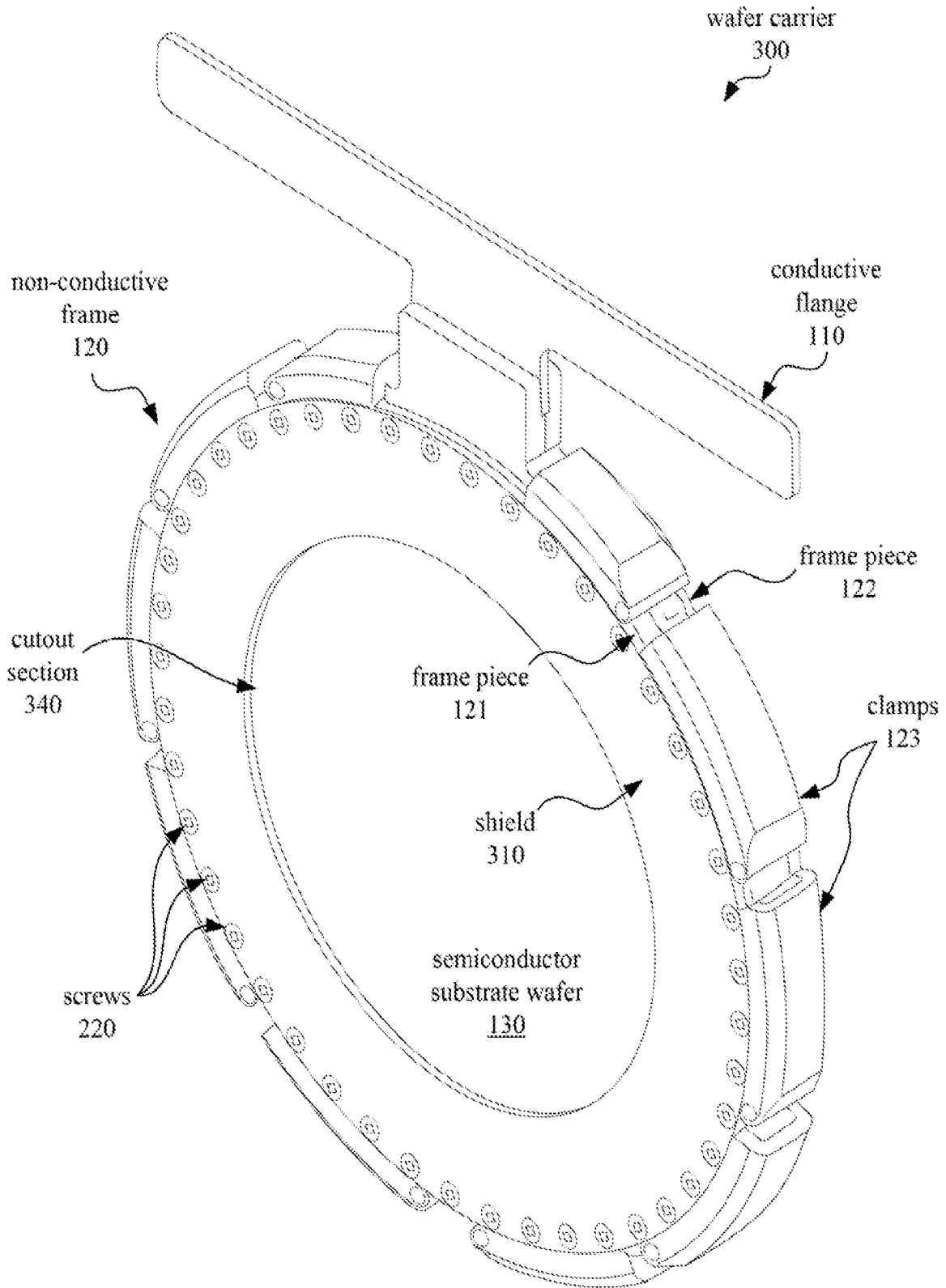


FIGURE 3

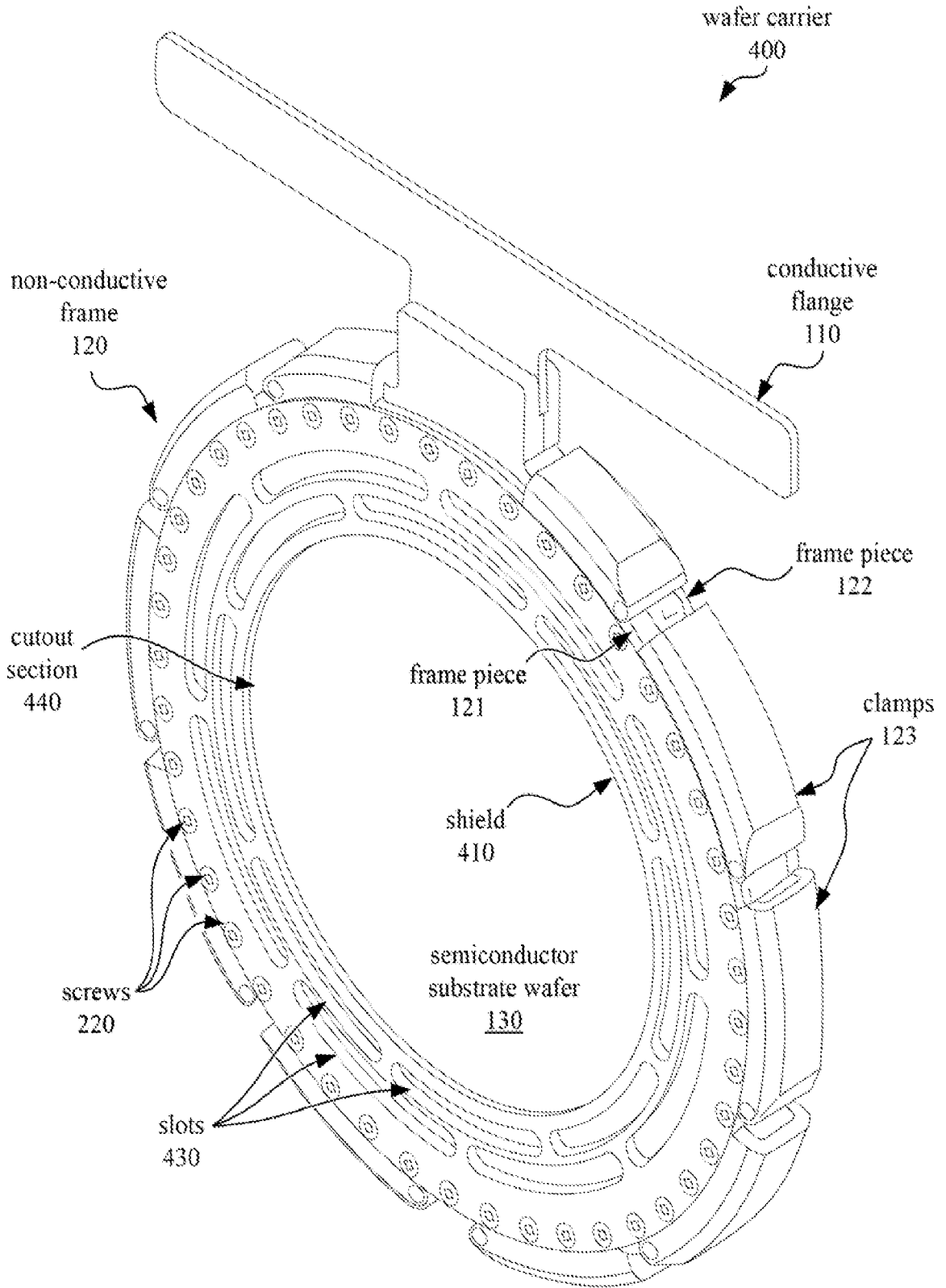


FIGURE 4

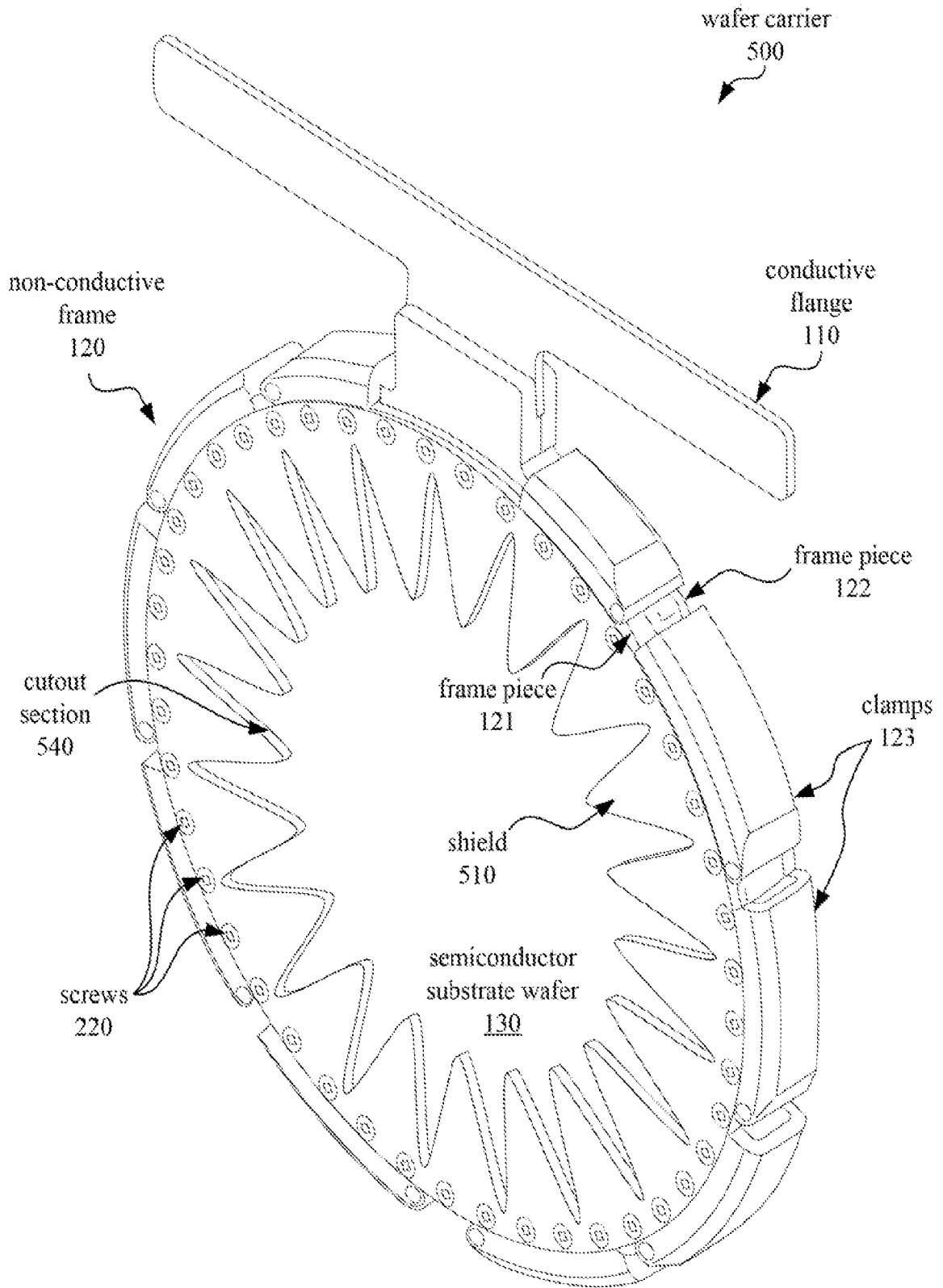


FIGURE 5

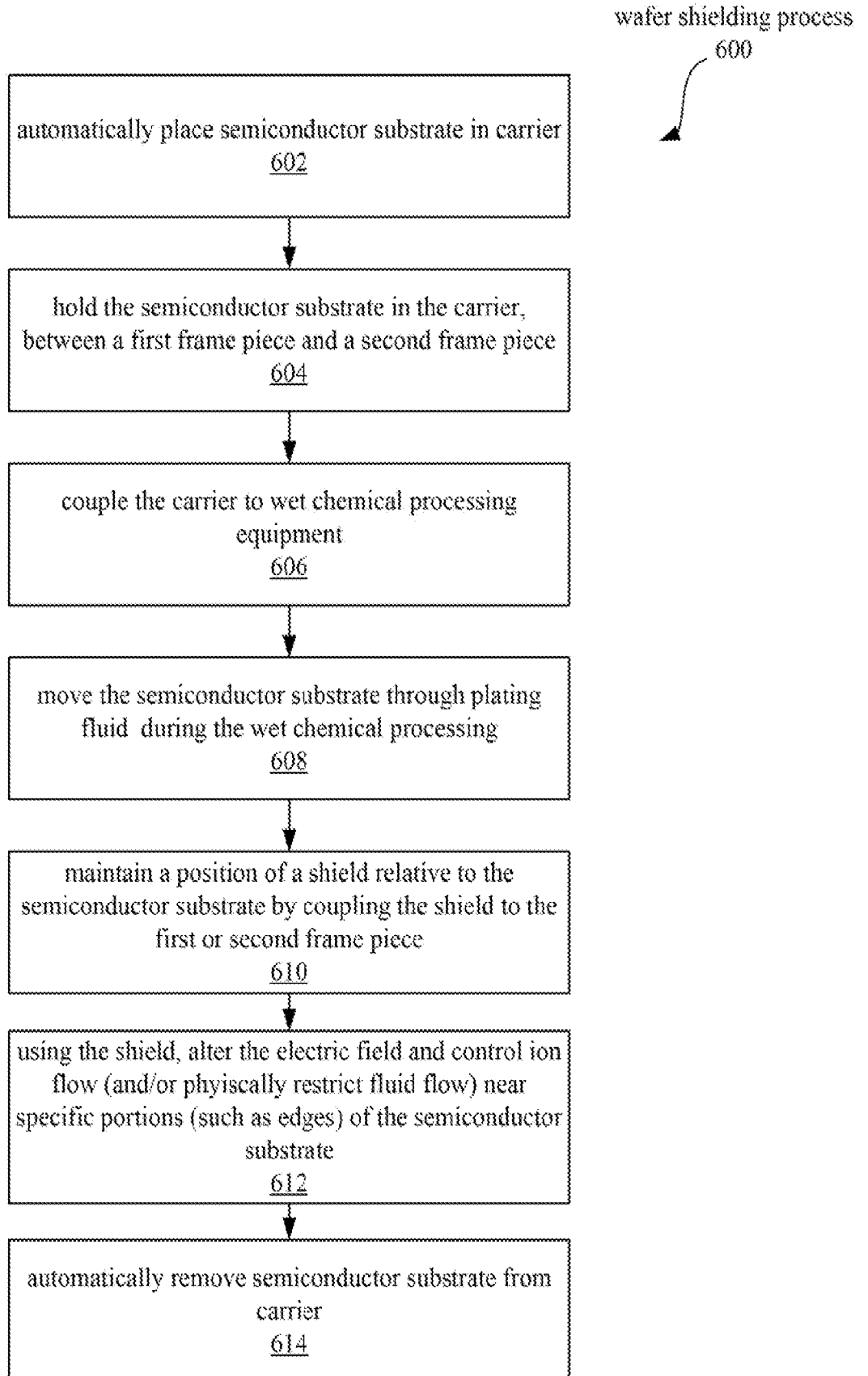


FIGURE 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 11/25127

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 21/00 (2011.01)

USPC - 414/217; 414/936

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) -- H01L 21/00 (2011.01)

USPC -- 414/217; 414/936

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

IPC(8) -- C25D5; H01L 21/00; H01L; H05K3 (2011.01)

USPC -- 204/242; 205/157; 414/217, 936; 438/745, 758

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWest (PGPB,USPT,USOC,EPAB,JPAB); DialogWeb (File 348 European Patents Fulltext; File 349 WIPO/PCT Patents Fulltext; File 652 US Patents Fulltext (1971-1975); File 654 US Patents Fulltext (1976-present); USPTO; Espacenet; Google Patents; Google Scholar; Google -- please see extra sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|-----------|---|-----------------------|
| Y | US 2005/0061665 A1 (Pavani et al.) 24 March 2005 (24.03.2005) Fig 1; Fig 1A; Fig 2; Fig 3; Fig 7; Fig 14; para [0002]; [0025]; [0026]; [0027]; [0033]; [0046] | 1-27 |
| Y | US 2006/0113185 A1 (Kuriyama et al.) 01 June 2006 (01.06.2006) Fig 4; Fig 6; Fig 28; para [0009]; [0010]; [0015]; [0101]; [0122]; [0123] | 1-27 |
| Y | US 2008/0152922 A1 (Cheng et al.) 26 June 2008 (26.06.2008) Fig 4; Fig 5; para [0034] | 16,18,19,20-24 |
| Y | US 2004/0175504 A1 (Hasselblatt et al.) 09 September 2004 (09.09.2004) Figs 4-6; para [0062]; [0063]; [0064] | 24-27 |
| Y | US 2005/0051437 A1 (Kurashina et al.) 10 March 2005 (10.03.2005) Figs 14; Fig 15; para [0002]; [0016]; [0017]; [0043]; [0179] | 2,10-12,18,19,26,27 |
| Y | US 2005/0092600 A1 (Yoshioka et al.) 05 May 2005 (05.05.2005) Figs 2, 3, 4, 5, 9 and 10; para [0042] | 2,10-12,18,19,26,27 |
| A | WO 2009/085337 A2 (Dugas et al.) 09 July 2009 (09.07.2009) Fig 3 | 1-27 |
| E, A | WO 2010/054677 A1 (Fredenberg et al.) 20 May 2010 (20.05.2010) Fig 12A-B; Fig 13A-B | 1-27 |

 Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

05 MAY 2011 (05.05.2011)

Date of mailing of the international search report

17 MAY 2011

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents

P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-3201

Authorized officer:

Lee W. Young

PCT Helpdesk: 571-272-4300

PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 11/25127

Search Terms Used:

(BATH OR WET) NEAR20 (PLATING OR ELECTROPLAT\$ OR ELECTRO-PLAT\$ OR ELECTRODEPOSIT\$ OR ELECTRO-DEPOSIT\$)

(HANDLE OR HANDLER OR FIXTURE OR CARRIER OR HOLDER)

CLAMP\$

((CONTROL\$ OR MODULAT\$ OR VARY OR VARYING OR ALTER\$ OR AFFECT\$ OR CHANG\$ OR INFLUENC\$) NEAR10 (FLOW)) NEAR10 ((EDGE OR SURFACE) NEAR10 (WAFER OR SUBSTRATE))

(CONTROL\$ OR MODULAT\$ OR VARY OR VARYING OR ALTER\$ OR AFFECT\$ OR CHANG\$ OR INFLUENC\$) NEAR10 (FIELD OR POTENTIAL)

FLANGE OR FLANGED

(FLOW OR FIELD OR POTENTIAL) NEAR10 ((EDGE OR SURFACE) NEAR10 (WAFER OR SUBSTRATE))

MATING OR MATCHING

THICKNESS NEAR20 (((ELECTRIC OR ELECTRICAL) NEAR10 (FIELD OR POTENTIAL)) NEAR10 ((EDGE OR SURFACE) NEAR10 (WAFER OR SUBSTRATE)))

(WAFER OR SUBSTRATE).TI,AB. AND (PLATING OR ELECTROPLATING).TI,AB. AND (HANDLE OR HANDLER OR FIXTURE OR CARRIER OR HOLDER)

(MAGNET?)(20N)(CLAMP? OR CLIP OR CLIPPING OR FASTEN?)(20N)(SUBSTRATE OR WAFER)(20N)(CARRIER OR HOLDER)