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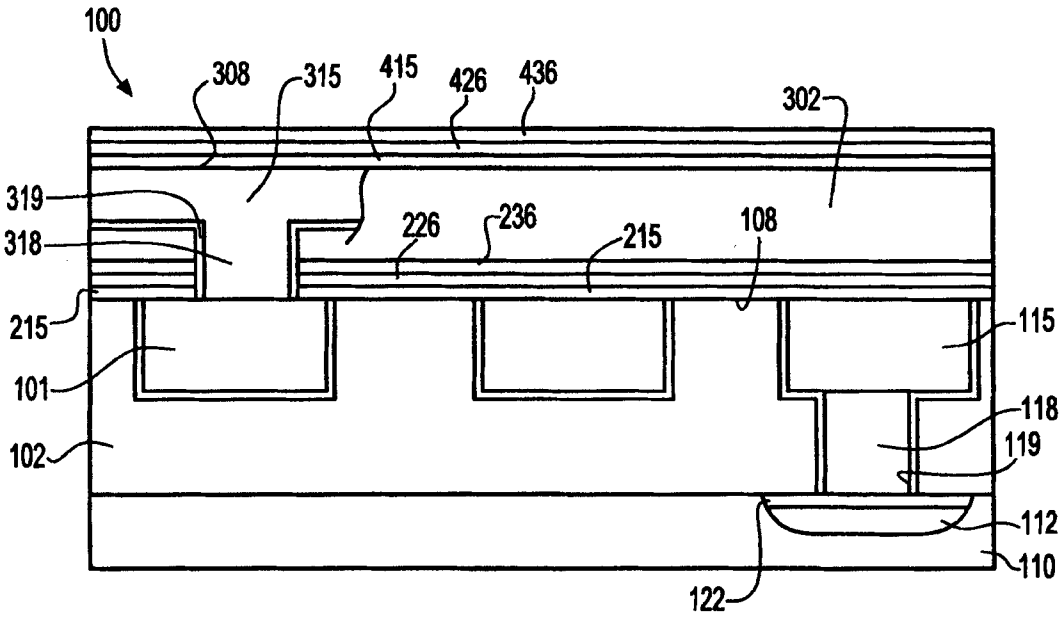

(57) Abstract: An interconnect structure and method of making the same are provided. The interconnect structure includes a dielectric layer having a patterned opening, a metal feature disposed in the patterned opening, and a dielectric cap overlying the metal feature. The dielectric cap has an internal tensile stress, the stress helping to avoid electromigration from occurring in a direction away from the metal line, especially when the metal line has tensile stress.

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METAL INTERCONNECT STRUCTURE FOR A MICROELECTRONIC ELEMENT

BACKGROUND OF THE INVENTION

The present invention relates to microelectronics including microelectronic wiring elements and semiconductor integrated circuits having metal interconnect structures.

Electromigration is a problem which can seriously affect the long-term reliability of microelectronic elements. The problem can be particularly serious in copper interconnects which are provided as "back end of line" ("BEOL") structures of semiconductor integrated circuits ("ICs" or "chips"). Electromigration tends to occur at ends of horizontally oriented metal lines and locations where vertically oriented vias are joined to such metal lines, mainly because the metal lines are subject to different kinds of stresses at such locations.

Failure mechanisms include the formation of a void in the copper line and mass transport of copper which occurs along the interface of a layer of dielectric material used as a cap layer overlying the copper line. A common cause of such failure includes the positive divergence of metal ions moving downstream under force of the flow of electrons ("electron wind"). As deposited, copper lines include vacancies which are microscopic gaps between deposited particles. Over time and with application of heat and/or current, vacancies are prone to move and accumulate together to form voids having substantial size. As a result, voids tend to form in metal interconnects at locations upstream in the predominant path of electrons.

SUMMARY OF THE INVENTION

According to one aspect of the invention, an interconnect structure and method of making the interconnect structure are provided. The interconnect structure includes a dielectric layer having a patterned opening, a metal feature disposed in the patterned opening, and a dielectric cap overlying the metal feature. The dielectric cap has an internal tensile stress, such stress helping to avoid electromigration of the metal in a direction leading away from the metal line, especially when the metal line has an internal tensile stress.

In an embodiment of the invention, the dielectric cap is formed by depositing multiple layers of a thin dielectric material, each layer being under about 50 angstroms in thickness. Each dielectric layer is plasma treated prior to depositing each succeeding dielectric layer such that the dielectric cap has an internal tensile stress.

According to one embodiment of the invention, the metal feature includes at least one metal selected from the group consisting of aluminum, copper, tungsten, silver, gold, and nickel.

The metal feature preferably includes a diffusion barrier layer lining the walls and bottom of the patterned opening and a filling of copper overlying the diffusion barrier layer within the opening.

In a preferred embodiment, an upper surface of the dielectric layer defines a major surface, the patterned opening is a first patterned opening oriented in a direction parallel to the major surface and the metal feature is a first metal feature. The dielectric layer further includes a second patterned opening which is aligned with the first patterned opening and oriented in a direction transverse to the major surface. The interconnect structure may further include a second metal feature disposed in the second patterned opening, the second metal feature being conductivity connected to the first metal feature.

The dielectric cap layer may include one or more dielectric materials or combinations of dielectric materials selected from the group consisting of silicon dioxide (Sio_ux), Si_3N_4, and $SiC_xN_yH_z$, where x, y and z are variable percentages.

In one embodiment, a plurality of the dielectric cap layers are formed successively in a stacked arrangement, each of the dielectric cap layers having internal tensile stress.

The plurality of dielectric cap layers may include at least three dielectric cap layers, each of the dielectric cap layers having a thickness between about 5 angstroms and 50 angstroms.

A dielectric underlayer may be provided which underlies the plurality of dielectric cap layers but overlies the metal feature, the dielectric underlayer having a thickness substantially greater than 50 angstroms.

A diffusion barrier layer may be aligned with the metal feature and contacts the metal feature, and the dielectric cap layer overlies the diffusion barrier layer. The diffusion barrier layer preferably has a thickness between about 10 angstroms and about 500 angstroms.

An integrated circuit is provided according to another aspect of the invention. The integrated circuit includes an interconnect structure which has a dielectric layer having a patterned opening and a metal feature disposed in the patterned opening. A dielectric cap is provided over the metal feature, the dielectric cap having an internal tensile stress.

According to another aspect of the invention, a method is provided for forming an interconnect structure. According to such method, an opening is patterned in a dielectric layer. A metal feature is formed in the patterned opening. A dielectric cap is formed over the metal feature, the dielectric cap having an internal tensile stress.

According to one embodiment a metal barrier layer may be deposited in contact with an upper surface of the metal feature prior to forming the dielectric cap. According to a particular aspect of the invention, the metal barrier layer includes an alloy of cobalt. In a particular embodiment, the metal barrier layer has a thickness of between about 10 angstroms and about 500 angstroms.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be described, by way of example only, and with reference to the following drawings in which:

FIG. 1 is a sectional view of a structure of a semiconductor chip in a stage of fabrication in accordance with an embodiment of the invention.

FIG. 2 is a sectional view of a structure of a semiconductor chip in a stage of fabrication subsequent to that of FIG. 1, in accordance with an embodiment of the invention.

FIG. 3 is a sectional view of a structure of a semiconductor chip in a stage of fabrication subsequent to that of FIG. 2, in accordance with an embodiment of the invention.

FIG. 4 is a sectional view of a structure of a semiconductor chip in accordance with an embodiment of the invention.

FIG. 5 is a sectional view of a structure of a semiconductor chip in accordance with another embodiment of the invention.

FIG. 6 is a sectional view of a structure of a semiconductor chip in accordance with yet another embodiment of the invention.

DETAILED DESCRIPTION

In accordance with the embodiments of the invention herein, one goal is reducing unwanted transport of copper in an outward direction from the metal lines of a chip. Another goal is avoiding or reducing the incidence of voids at an interface between a via and a metal line.

FIG. 1 is a sectional view of a portion of a microelectronic element or chip in which a plurality of metal interconnects are provided by metal fillings 101 formed in patterned openings 105 in accordance with an embodiment of the invention. FIG. 1 illustrates a stage in fabrication in which an interlevel dielectric layer or "ILD" 102 has been formed. The ILD typically overlies an active semiconductor layer 110 of a semiconductor chip 100, the active semiconductor layer including one or more active devices and conductive interconnects (not shown) formed by so-called "front end of line" processing, such conductive interconnects providing a basis for connection to the metal fillings 101. Within the ILD, a plurality of patterned openings 105 are provided, typically in form of line patterns which extend horizontally in a direction of a major surface 108 which is defined by the upper surface of the dielectric layer 102, or which extend in a direction parallel to such surface. Within each patterned opening, a diffusion barrier material 103 is deposited to line the walls and bottom of each opening, after which a metal 101 is deposited to fill the remaining space within each opening. These steps are followed typically by a planarization process, such as a chemical mechanical polishing ("CMP") process, which removes any excess metal that contacts the upper surface 108 of the ILD 102 outside of the patterned openings 105.

The metal 101 that fills each opening in the dielectric layer 102 is preferably a metal, for example, a noble metal, that is not prone to destructive corrosion and has good conductive properties. However, a few

metals and alloys of metals stand out as being especially suited for forming conductive interconnect lines in the BEOL fabrication of integrated circuits or chips. Such metals include aluminum, copper, tungsten, silver, gold, aluminum-copper and nickel. In a particular embodiment, the metal 101 which fills the patterned opening 105 in the dielectric layer 102 consists essentially of copper. When the metal filling 101 includes copper or other metal prone to diffusing through dielectric materials, i.e., when the metal has a "high coefficient of diffusion", the layer 101 is preferably formed over a layer of metal or compound of a metal which functions as a diffusion barrier. The diffusion barrier prevents the copper from diffusing from the metal filling 101 into the ILD 102 adjacent to the walls and bottom of the metal line. The barrier layer is preferably formed by sputtering, using chemical vapor deposition ("CVD"), or atomic layer deposition ("ALD") to deposit a metal or compound of metal which does not interact with the copper, such that the barrier layer does not affect the conductive properties of the copper or interact with the dielectric material of the ILD 102 to affect its dielectric properties. Such barrier layers are well-known and need not be discussed further.

Next, referring to FIG. 2, the exposed major surface 108 of the ILD 102 and the metal filled line patterns 101 are subjected to plasma treatment, preferably using a combination of ammonia and nitrogen species (NH_3 and N_2) or, alternatively, hydrogen (H_2).

After plasma treatment, this is followed by the deposition of a dielectric cap layer 215. The first dielectric cap layer 215 can include any dielectric material or combination of dielectric materials which is capable of maintaining a stress relative to the metal filled line patterns. Preferably, the first dielectric cap layer consists essentially of one or more dielectric materials or combinations of dielectric materials selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), and or other dielectric compound of silicon such as $SiC_xN_yH_z$, where x, y and z are variable percentages. The plasma treatment and dielectric cap deposition are preferably performed *in situ*, i.e., in the same process chamber or in the same tool having one or more connected chamber. In that way, it is performed without having to manually remove the substrate from the chamber to deposit the dielectric cap after plasma treating the surface of the ILD. In one embodiment, a first dielectric cap layer 215 is deposited to cover the upper surface 108 of the ILD 102 to a thickness of less than about 50 angstroms. After deposition, the exposed upper surface 225 of the first dielectric cap

layer 215 is subjected to a second plasma treatment. The second plasma treatment has an effect of imparting a tensile stress to the first dielectric cap layer 215.

Thereafter, referring to FIG. 3, a second dielectric cap layer 226 is deposited to cover the upper surface 225 of the first dielectric cap layer. Like the first dielectric cap layer 215, the second dielectric cap layer 226 preferably is formed to a thickness of less than about 50 angstroms. Like the first dielectric cap layer 215, the second dielectric cap layer can include any dielectric material or combination of dielectric materials which is capable of maintaining a stress. Preferably, the second dielectric cap layer consists essentially of one or more dielectric materials or combinations of materials selected from the group consisting of silicon dioxide, silicon nitride and a compound of silicon, carbon, nitrogen and hydrogen in the form of $SiC_xN_yH_z$ where x, y and z are variable percentages. Preferably, the second dielectric cap layer consists essentially of the same dielectric material as the first dielectric cap layer. Like the first dielectric cap layer, the upper surface 230 of the second dielectric cap layer 226 also undergoes plasma treatment after deposition to control the tensile stress of the deposited second dielectric cap layer, preferably using the same species that are used during the plasma treatment of the first dielectric cap layer. For example, the plasma treatment can include a mixture of ammonia and nitrogen, or alternatively, hydrogen as the reactive species. As in the case of the first dielectric cap layer, these deposition and plasma treatment processes are preferably performed *in situ*.

Following deposition and plasma treatment of the second dielectric cap layer 226, a third dielectric cap layer 236 is deposited to cover the upper surface 230 of the second dielectric cap layer. Like the first and second dielectric cap layers 215 and 226, the third dielectric cap layer 236 is formed to a thickness of less than about 50 angstroms. Like the first and second dielectric cap layers 215, 226, the third dielectric cap layer can include any dielectric material or combination of dielectric materials which is capable of maintaining a stress. Preferably, the third dielectric cap layer consists essentially of one or more dielectric materials or combinations of dielectric materials selected from the group consisting of silicon dioxide, silicon nitride and a compound of silicon, carbon, nitrogen and hydrogen in the form of $SiC_xN_yH_z$. Again, preferably, the third dielectric cap layer 236 consists essentially of the same dielectric material as the first and second dielectric cap layers. As in the plasma treatments performed to the first and second dielectric cap

layers, the upper surface 240 of the third dielectric cap layer 236 also undergoes plasma treatment after deposition to control or produce a tensile stress in the third dielectric cap layer, preferably using the same species that are used during the plasma treatment of the first and second dielectric cap layers. For example, the plasma treatment can include a mixture of ammonia and nitrogen, or alternatively, hydrogen as the reactive species. As in the case of the first and second dielectric cap layers, these deposition and plasma treatment processes are preferably performed *in situ*.

The goal of successively depositing the dielectric cap layers and the plasma treatments is to achieve a dielectric cap which has an internal tensile stress. The internally tensile stressed dielectric cap will exert a compressive stress at the surface of the metal fill material 101 which it contacts. As a result, the metal fill, e.g., copper fill, is less likely to exert a tensile stress on the metal features it contacts, which could then result in the problems described above in the background. Note that the number of dielectric cap layers that are used and other parameters associated with their fabrication are not of primary importance. Rather, the magnitude and stability of the internal tensile stress of the dielectric cap are of greater importance. Therefore, if a single layer of the dielectric cap material is deposited to have the required internal tensile stress of the desired magnitude and properties, then a single such dielectric cap layer suffices. On the other hand, if more than three such dielectric cap layers are needed to achieve these properties, then more than three such dielectric cap layers need to be deposited and plasma treated in accordance with the method described above.

FIG. 4 is a sectional view illustrating a preferred embodiment of an active semiconductor chip 100 which includes a metal interconnect fabricated in accordance with the above-described method. In such embodiment, a metal line 115 is oriented in a horizontal direction, i.e., in a direction into and out of the page in FIG. 4, such direction also being parallel to the upper surface 108 of the ILD 102. A vertically oriented conductive via 118 conductively contacts a layer of metal silicide 122 overlying an active area 112 of an active semiconductor layer 110 to provide conductive communication between the active area 112 and the metal line 115. The ILD 102 electrical isolates the via 118 and the metal line 115 from other features of the semiconductor chip 100. In one embodiment, the conductive via 118 is filled with a metal such as tungsten or the same metal, e.g., copper, which is used to fill the metal line 115.

As the case with the metal lines, when the via 118 is filled with a metal such as copper which has a high coefficient of diffusion, the walls of the via 118 are preferably lined with a barrier material 119. Alternatively, the conductive via 118 can be filled with doped polysilicon or compound of silicon, e.g., a conductive or metal silicide, or the via 118 can be filled with a combination of doped polysilicon and conductive compound of silicon. In such case, the barrier layer 119 may or may not be present, as it is not necessary to prevent such silicon-containing conductive fill from diffusing from the via into the ILD.

FIG. 4 further illustrates the structure of a second level metal line 315 which is disposed in a second interlayer dielectric level ("ILD2") 302 overlying the metal interconnects formed in the first interlayer dielectric level (ILD 102), and overlying the dielectric cap provided in form of three dielectric cap layers 415, 426 and 436. In an exemplary arrangement, the metal interconnect line 315 is oriented in a horizontal direction parallel to the upper surface 108 of the first ILD 102, the metal interconnect line 315 being transverse to the direction of metal line 115. The second level metal line 315, like the first metal line 115, is disposed in a patterned opening of a dielectric layer, ILD2 (302). The dielectric cap layers 415, 426 and 436 are successively deposited and plasma-treated to overlie the second level metal line in order to apply a compressive stress at the interfacial upper surface 308 of the second metal line 315. The second level metal line 315 is preferably conductively connected by a conductive via 318 to the metal filling 101 of a metal line provided in the first ILD 102.

The conductive via 318 is preferably provided by etching a vertically oriented opening in ILD2 302 and the existing dielectric cap layers 215, 226 and 236. Thereafter, a diffusion barrier layer 319 is preferably deposited to line the walls of the via 318 and the walls and bottom of the horizontally oriented opening above the via. A layer of metal is then deposited to fill the remaining opening, followed by a CMP process to form the metal line, in a manner similar to that described above for forming the metal lines within the first ILD 102. Subsequently, as further shown in FIG. 4, a series of dielectric cap layers are deposited and plasma-treated, each in succession, until a dielectric cap having the desired internal stress property and stability results. The dielectric cap layers can include any dielectric material or combination of dielectric materials which is capable of maintaining a stress. However, preferably, the dielectric cap layers consist essentially of one or more dielectric materials or combinations of dielectric materials selected from

the group consisting of silicon dioxide, silicon nitride and a compound of silicon, carbon, nitrogen and hydrogen in the form of $SiC_xN_yH_z$, where x, y and z are variable percentages.

FIG. 5 illustrates a variation of the above-described embodiment. In such variation, a thicker dielectric cap layer 310 is first deposited to cover the ILD 102 and metal line patterns 101 therein, prior to successively depositing and plasma-treating the series of individual relatively thin dielectric cap layers 215, 226 and 236. In this embodiment, the thicker dielectric layer has a thickness preferably between about 50 angstroms and about 500 angstroms. This layer 310 can include any dielectric material or combination of dielectric materials which is capable of maintaining a stress. The layer 310 preferably consists essentially of one or more dielectric materials or combination of dielectric materials selected from the group consisting of silicon dioxide, silicon nitride or a compound of silicon, carbon, nitrogen and hydrogen according to the formula $SiC_xN_yH_z$, where x, y and z are variable percentages. Preferably, the dielectric layer 310 consists essentially of the same material at that from which the overlying dielectric cap layers 215, 226, and 236 are formed. In a preferred embodiment, the thicker dielectric layer 310 is formed by depositing one or more dielectric materials selected from the group consisting of silicon dioxide, silicon nitride or a compound of silicon, carbon, nitrogen and hydrogen according to the formula $SiC_xN_yH_z$, where x, y and z are variable percentages, followed by plasma treatment in a manner as described above.

In another embodiment illustrated in the sectional view of FIG. 6, a metal capping layer 410 is selectively deposited to cover each of the metal lines 101, prior to formation of the tensile-stressed dielectric cap layers 215, 226 and 236. Such metal capping layer preferably functions as a diffusion barrier helping to prevent a metal within metal line 101 such as copper, which has a high diffusion coefficient, from diffusing into the dielectric cap layers or the ILD 102. Such metal capping layer preferably consists essentially of a metal compound which is compatible with copper and which can be selectively deposited, e.g., plated onto the metal lines 101, such as by electroplating or electro-less plating. In an exemplary embodiment, the metal capping layer 410 consists essentially of one or more compounds selected from the group consisting of CoWP, CoSnP, CoP, CoB, CoSnB, and CoWB. Preferably, the metal capping layer has a thickness between about 10 angstroms and 500 angstroms. Preferably, the metal capping layer is selectively deposited onto the metal lines after

excess metal from prior processing to form the metal lines has been removed, as through a CMP process.

While the invention has been described in accordance with certain preferred embodiments thereof, those skilled in the art will understand the many modifications and enhancements which can be made thereto without departing from the true scope of the invention, which is limited only by the claims appended below.

CLAIMS

1. An interconnect structure, comprising:
a dielectric layer having a patterned opening;
a metal feature disposed in said patterned opening; and
a dielectric cap overlying said metal feature, said dielectric cap having an internal tensile stress.

2. The interconnect structure as claimed in claim 1, wherein said metal feature includes at least one metal selected from the group consisting of aluminum, copper, tungsten, silver, gold, and nickel.

3. The interconnect structure as claimed in claim 1, wherein said metal feature includes a diffusion barrier layer lining walls and bottom of said patterned opening and a filling of copper overlying said diffusion barrier layer within said opening.

4. The interconnect structure as claimed in claim 1, wherein an upper surface of said dielectric layer defines a major surface, said patterned opening is a first patterned opening oriented in a direction parallel to said major surface, said metal feature is a first metal feature, and said dielectric layer further comprises a second patterned opening aligned with said first patterned opening and oriented in a direction transverse to said major surface, said interconnect structure further comprising a second metal feature disposed in said second patterned opening, said second metal feature being conductively connected to said first metal feature.

5. The interconnect structure as claimed in claim 1, wherein said dielectric cap includes at least one material selected from the group consisting of silicon dioxide (SiO_2), Si_3N_4, and $SiC_xN_yH_z$, where x, y and z are variable percentages.

6. The interconnect structure as claimed in claim 1, wherein said dielectric cap includes a plurality of dielectric cap layers formed successively in a stacked arrangement, each said dielectric cap layer having internal tensile stress.

7. The interconnect structure as claimed in claim 6, wherein said plurality of dielectric cap layers includes at least three said dielectric cap layers, each said dielectric cap layer having a thickness between about 5 angstroms and 50 angstroms.

8. The interconnect structure as claimed in claim 7, further comprising a dielectric underlayer overlying said metal feature and underlying said plurality of dielectric cap layers, said dielectric underlayer having a thickness substantially greater than 50 angstroms.

9. The interconnect structure as claimed in claim 1, further comprising a diffusion barrier layer aligned to said metal feature and contacting said metal feature, wherein said dielectric cap overlies said diffusion barrier layer.

10. The interconnect structure as claimed in claim 9, wherein said diffusion barrier layer has a thickness between about 10 angstroms and about 500 angstroms.

11. The interconnect structure as claimed in claim 1, further comprising a metal diffusion barrier layer in contact with an upper surface of said metal feature, said metal diffusion barrier including an alloy of cobalt.

12. An integrated circuit, comprising an interconnect structure as claimed in any of claims 1 to 11.

13. A method of forming an interconnect structure, comprising:
patterning an opening in a dielectric layer;
forming a metal feature in said patterned opening; and
forming a dielectric cap over said metal feature, said dielectric cap having an internal tensile stress.

14. The method as claimed in claim 13, wherein said dielectric cap is formed by depositing a layer including a dielectric material and plasma treating said deposited layer.

15. The method as claimed in claim 14, wherein said metal feature includes at least one metal selected from the group consisting of aluminum, copper, tungsten, silver, gold, and nickel.

16. The method as claimed in claim 14, wherein said step of forming said metal feature includes depositing a diffusion barrier layer lining walls and a bottom of said patterned opening to form a lined opening and filling said lined opening with copper.

17. The method as claimed in claim 16, wherein an upper surface of said dielectric layer defines a major surface, said patterned opening is a

first patterned opening oriented in a first direction parallel to said major surface and said metal feature is a first metal feature, said method further comprising patterning a second opening aligned with said first patterned opening, said second opening oriented in a second direction transverse to said first direction, and said step of forming said metal feature includes forming a second metal feature in said second patterned opening, said second metal feature conductively connected to said first metal feature.

18. The method as claimed in claim 14, wherein said step of forming said dielectric cap includes depositing each of a plurality of dielectric cap layers and plasma treating each said dielectric cap layer prior to depositing each succeeding dielectric cap layer such that each said dielectric cap layer has an internal tensile stress.

19. The method as claimed in claim 18, further comprising forming a dielectric underlayer over said metal feature prior to forming said plurality of dielectric cap layers.

20. The method as claimed in claim 14, further comprising selectively depositing a metal barrier layer in contact with an upper surface of said metal feature prior to forming said dielectric cap.

AMENDED CLAIMS
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1. An interconnect structure for a microelectronic element, comprising:
a dielectric layer having a patterned opening;
a metal feature disposed in said patterned opening; and
a dielectric cap, comprising a plurality of dielectric cap layers, overlying said metal feature, said dielectric cap having an internal tensile stress.

2. The interconnect structure as claimed in claim 1, wherein said metal feature includes at least one metal selected from the group consisting of aluminum, copper, tungsten, silver, gold, and nickel.

3. The interconnect structure as claimed in claim 1, wherein said metal feature includes a diffusion barrier layer lining walls and bottom of said patterned opening and a filling of copper overlying said diffusion barrier layer within said opening.

4. The interconnect structure as claimed in claim 1, wherein an upper surface of said dielectric layer defines a major surface, said patterned opening is a first patterned opening oriented in a direction parallel to said major surface, said metal feature is a first metal feature, and said dielectric layer further comprises a second patterned opening aligned with said first patterned opening and oriented in a direction transverse to said major surface, said interconnect structure further comprising a second metal feature disposed in said second patterned opening, said second metal feature being conductively connected to said first metal feature.

5. The interconnect structure as claimed in claim 1, wherein said dielectric cap includes at least one material selected from the group consisting of silicon dioxide (SiO_2), Si_3N_4, and $SiC_xN_yH_z$, where x, y and z are variable percentages.

6. The interconnect structure as claimed in claim 1, wherein said plurality of dielectric cap layers includes at least three said dielectric cap layers, each said dielectric cap layer having a thickness between about 5 angstroms and 50 angstroms.

7. The interconnect structure as claimed in claim 6, further comprising a dielectric underlayer overlying said metal feature and underlying said

plurality of dielectric cap layers, said dielectric underlayer having a thickness substantially greater than 50 angstroms.

8. The interconnect structure as claimed in claim 1, further comprising a diffusion barrier layer aligned to said metal feature and contacting said metal feature, wherein said dielectric cap overlies said diffusion barrier layer.

9. The interconnect structure as claimed in claim 8, wherein said diffusion barrier layer has a thickness between about 10 angstroms and about 500 angstroms.

10. The interconnect structure as claimed in claim 1, further comprising a metal diffusion barrier layer in contact with an upper surface of said metal feature, said metal diffusion barrier including an alloy of cobalt.

11. An integrated circuit, comprising an interconnect structure as claimed in any of claims 1 to 10.

12. A method of forming an interconnect structure of a microelectronic element, comprising:

patterning an opening in a dielectric layer;

forming a metal feature in said patterned opening; and

forming a dielectric cap over said metal feature, said dielectric cap having an internal tensile stress;

wherein said step of forming said dielectric cap includes depositing each of a plurality of dielectric cap layers and plasma treating each said dielectric cap layer prior to depositing each succeeding dielectric cap layer such that each said dielectric cap layer has an internal tensile stress.

13. The method as claimed in claim 12, wherein said metal feature includes at least one metal selected from the group consisting of aluminum, copper, tungsten, silver, gold, and nickel.

14. The method as claimed in claim 12, wherein said step of forming said metal feature includes depositing a diffusion barrier layer lining walls and a bottom of said patterned opening to form a lined opening and filling said lined opening with copper.

15. The method as claimed in claim 14, wherein an upper surface of said dielectric layer defines a major surface, said patterned opening is a

first patterned opening oriented in a first direction parallel to said major surface and said metal feature is a first metal feature, said method further comprising patterning a second opening aligned with said first patterned opening, said second opening oriented in a second direction transverse to said first direction, and said step of forming said metal feature includes forming a second metal feature in said second patterned opening, said second metal feature conductively connected to said first metal feature.

16. The method as claimed in claim 12, further comprising forming a dielectric underlayer over said metal feature prior to forming said plurality of dielectric cap layers.

17. The method as claimed in claim 12, further comprising selectively depositing a metal barrier layer in contact with an upper surface of said metal feature prior to forming said dielectric cap.

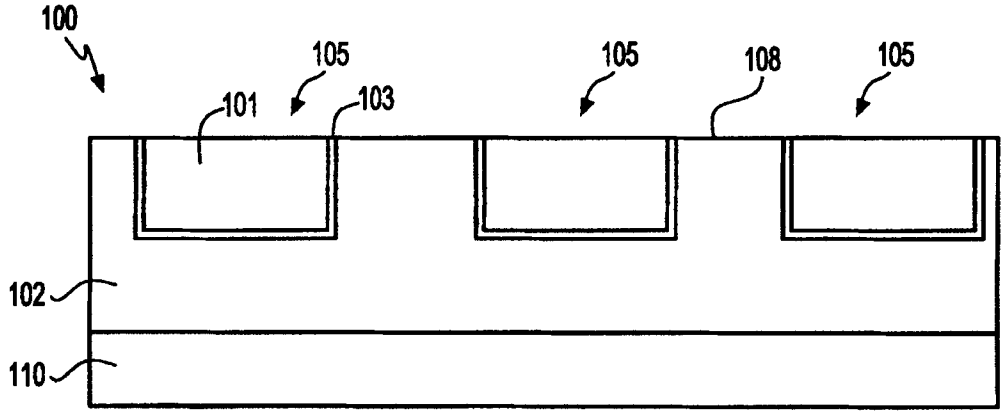

FIG. 1

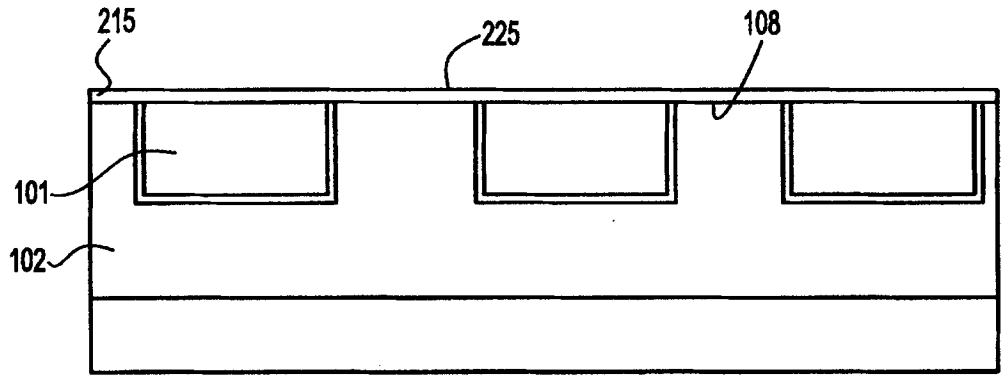

FIG. 2

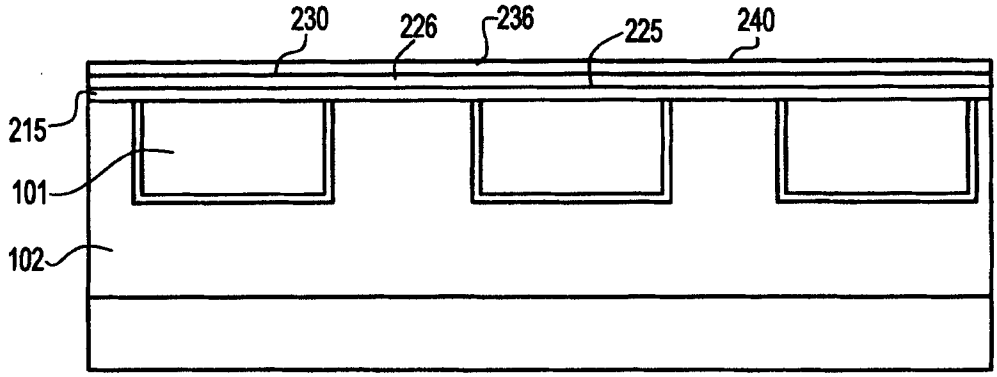
230
226
236
225
240
215
101
102

FIG. 3

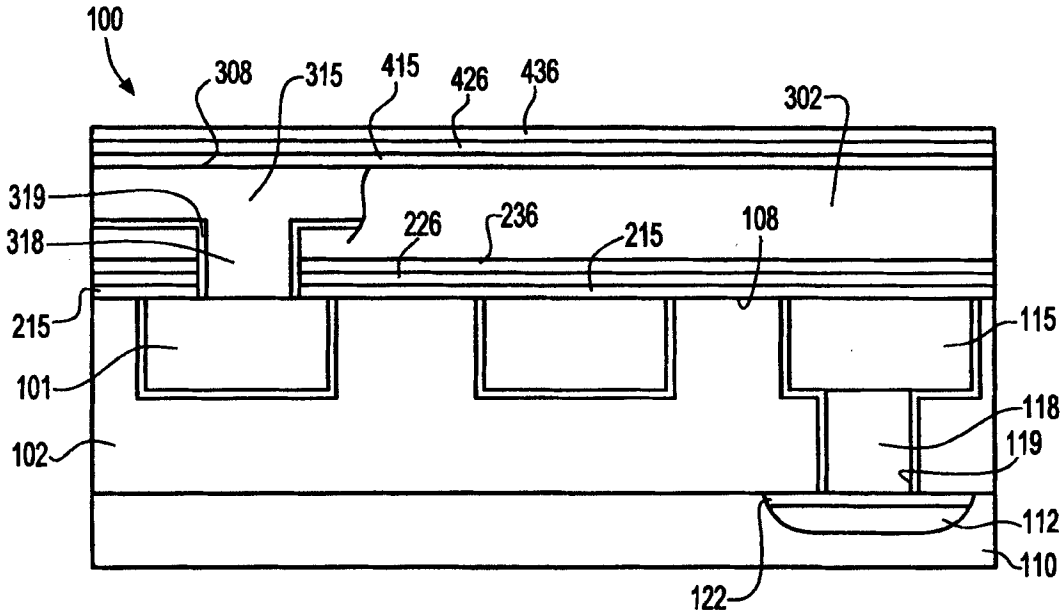
100
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FIG. 4

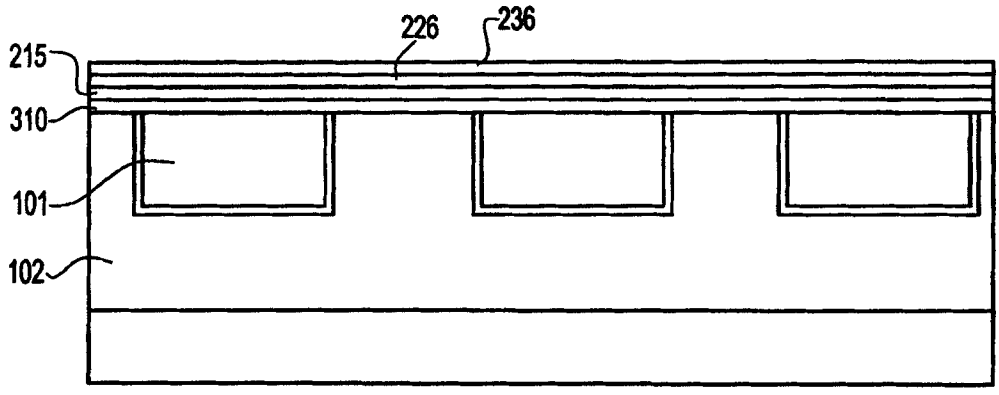

FIG. 5

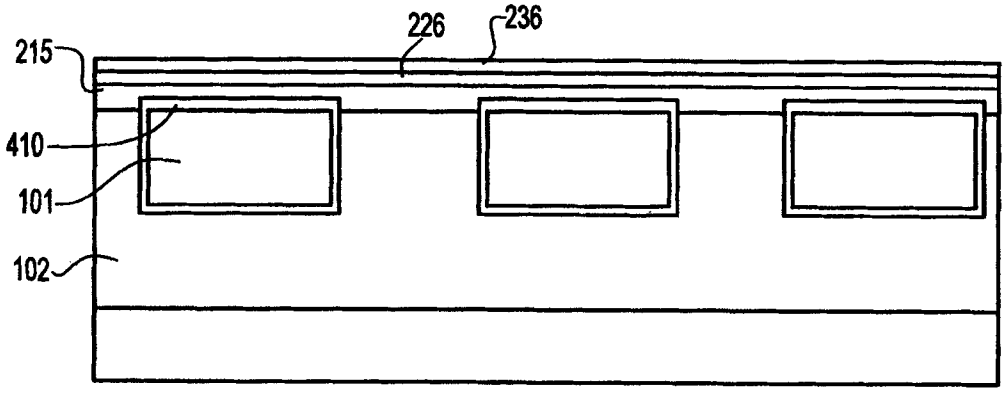

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/066077

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/532 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ISHIKAWA K ET AL: "Impact of Cu barrier dielectrics upon stress-induced voiding of dual-damascene copper interconnects" INTERCONNECT TECHNOLOGY CONFERENCE, 2005. PROCEEDINGS OF THE IEEE 2005 INTERNATIONAL BURLINGAME, CA, USA 6-8 JUNE 2005, PISCATAWAY, NJ, USA,IEEE, US, 6 June 2005 (2005-06-06), pages 39-41, XP010829452 ISBN: 0-7803-8752-X the whole document	1-4,12, 13
X	US 2005/042889 A1 (LEE ALBERT [US] ET AL LEE ALBERT [US] ET AL) 24 February 2005 (2005-02-24)	1-6, 12-18
Y	paragraphs [0030] - [0051], [0102] - [0124]; figures 1,2H	9-11,20
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 January 2007	22/01/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Edmeades, Michael

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/066077

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6 617 690 B1 (GATES STEPHEN M [US] ET AL) 9 September 2003 (2003-09-09) column 4, line 32 - column 10, line 48; figure 3	1-4,6-8, 12,13 9-11,20
Y	WO 01/08213 A (IBM [US]) 1 February 2001 (2001-02-01) page 2, paragraph 3 - page 4, paragraph 2 page 7, line 3, paragraph 3 - page 9, paragraph 2; figure 3E	9-11,20
A	US 2003/134499 A1 (CHEN TZE-CHIANG [US] ET AL) 17 July 2003 (2003-07-17) paragraphs [0030] - [0033]; figure 2	1-20
P,A	BALSEANU M ET AL: "STRESS-MODULATION OF PECVD SILICON NITRIDE" MEETING ABSTRACTS, ELECTROCHEMICAL SOCIETY, PENNINGTON, NJ, US, vol. MA 2005-2, 2005, page 1042, XP001248329 ISSN: 1091-8213 the whole document	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2006/066077

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