Jan. 19, 1965 R. C. CLARK 3,166,735

CODE SELECTORS FOR SELECTIVE CALLING SYSTEMS

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FIG. 1.

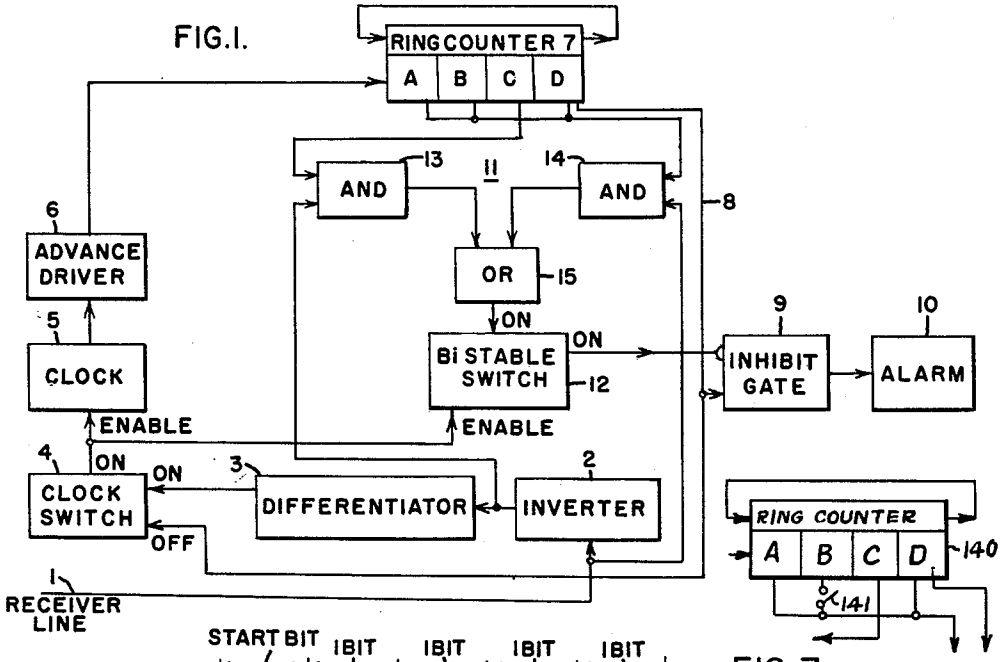


FIG. 3.

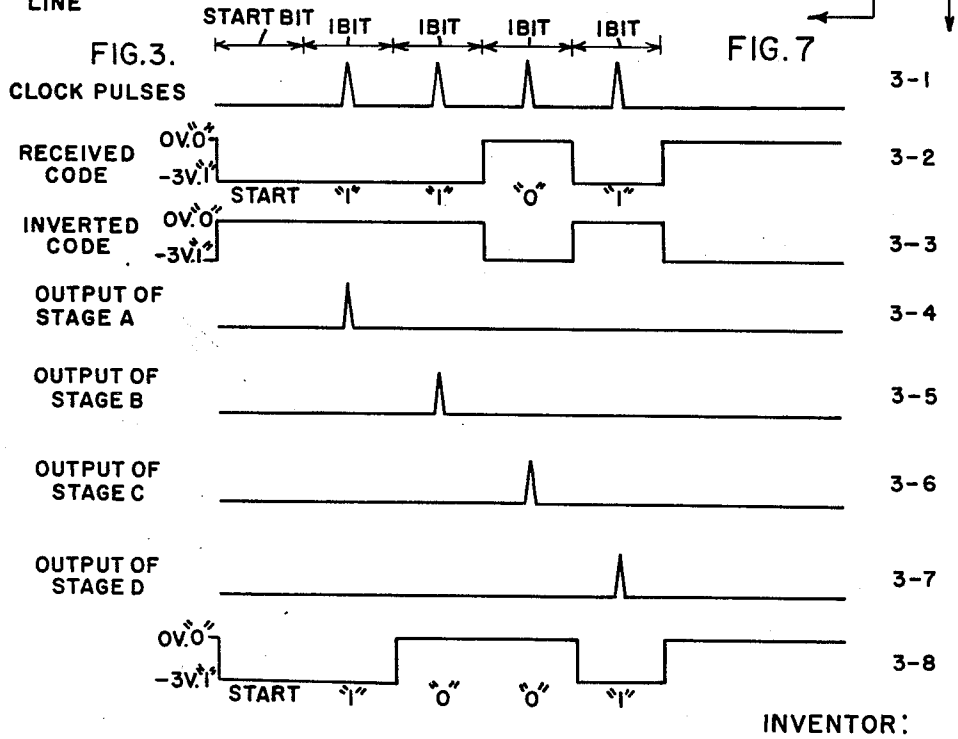


FIG. 7

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CODE SELECTORS FOR SELECTIVE CALLING SYSTEMS

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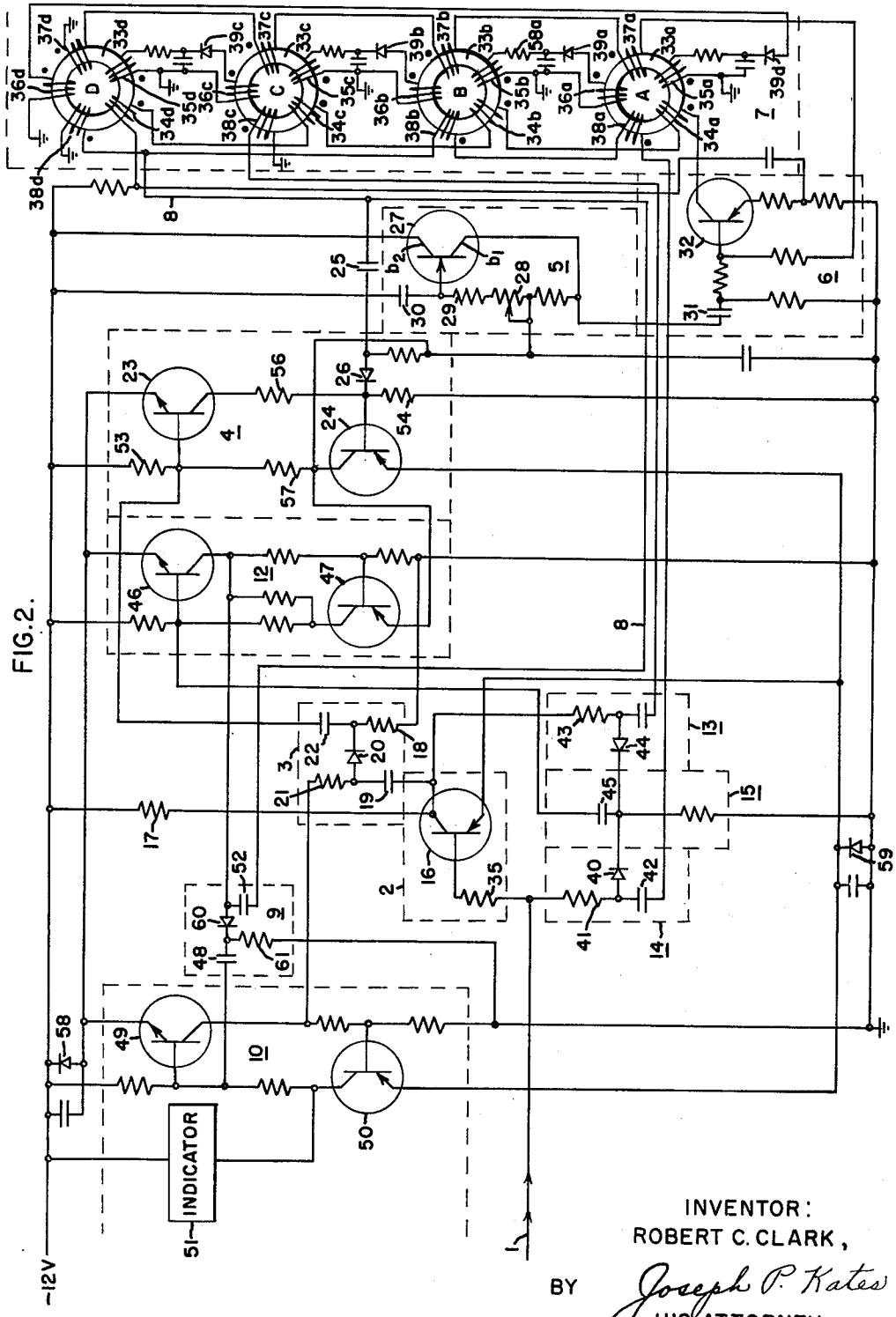


FIG. 2.

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FIG.4.

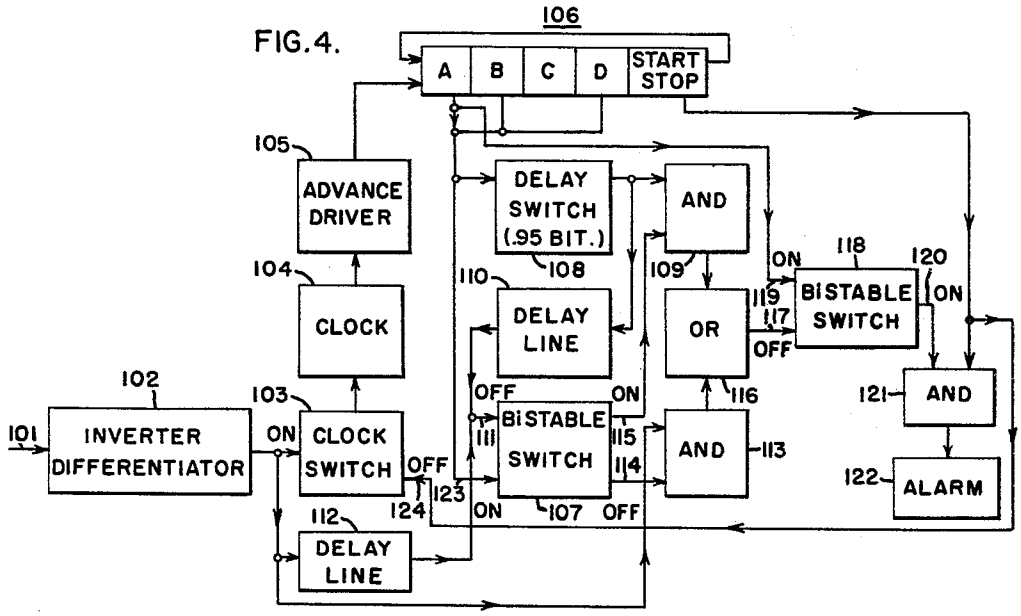


FIG.5.

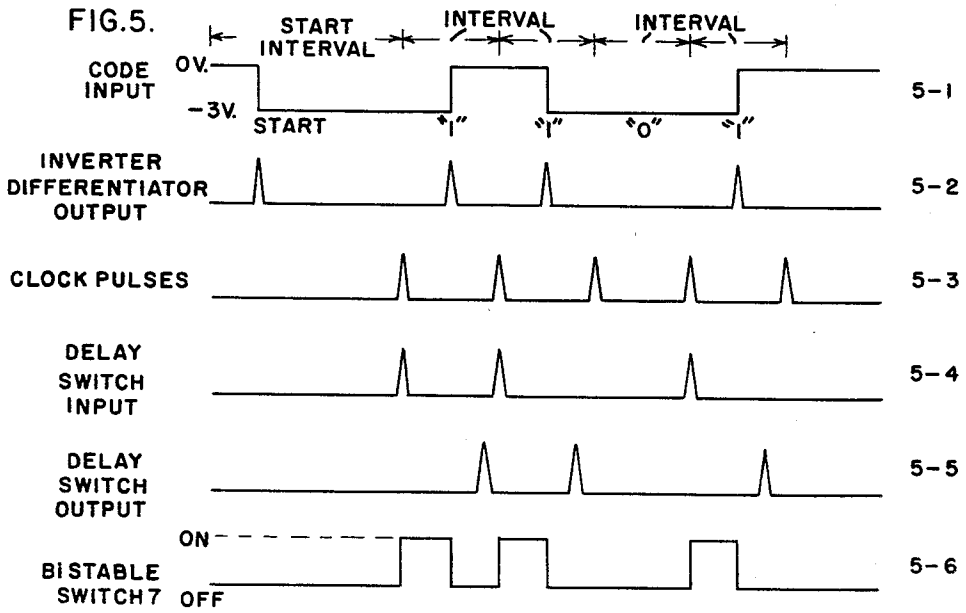
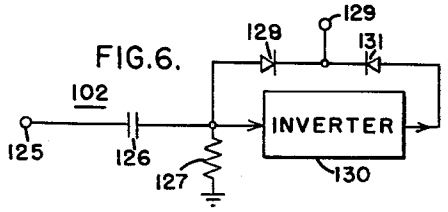


FIG.6.



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CODE SELECTORS FOR SELECTIVE CALLING SYSTEMS

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8 Claims. (Cl. 340—164)

This invention relates to communication systems, and more particularly, is concerned with code selectors for selective calling systems.

Various systems have heretofore been proposed in the prior art for paging doctors or other persons who move from place to place and who otherwise could not be contacted. Such a system must have a receiver which is small enough to fit into the pocket of the person who is to be called. This receiver must have a selector capable of actuating an alarm in response to only the transmitted code designated for that particular receiver. Additionally, the selector must perform its decoding functions reliably and without error.

Prior art selective calling systems have used selectors in which a vibrating reed actuates an alarm in response to the reception of a particular radio frequency. These selectors have the disadvantage of requiring the use of a separate frequency in the already over-crowded radio frequency spectrum to page each selector. This disadvantage has been overcome in this invention by making each selector responsive to a binary code made up of the presence or absence of a single radio frequency.

Prior art selectors which have attempted to make use of a binary code to page the selector have been so complex as to make their use prohibitive. These selectors have attempted to store the received code in a shift register or a binary counting chain until the received, stored code can be compared with the code which the selector is designed to recognize. This invention avoids much of the complexity necessary in a selector which stores a complete received code by sampling the code as it is received to determine any errors between the received code and the code which the selector is designed to recognize. A single error in the received code is stored to prevent actuation of an alarm which indicates that the selector has been paged.

It is accordingly an object of this invention to provide an improved selector for a selective calling communication system by means of which one of a plurality of receivers can be paged.

Another object of this invention is the provision of an improved code selector for actuating an alarm in response to only one of a plurality of received codes.

Another object of this invention is the provision of a code selector having a size small enough to conveniently fit into the pocket of the person who carries the receiver.

Another object of this invention is the provision of a code selector which will perform its function reliably and accurately.

Another object of this invention is the provision of a code selector which utilizes a code requiring only a single radio frequency.

Still another object of this invention is the provision of a code selector of simplified construction.

These and other objects of the invention which will become apparent as the description proceeds are achieved in one form of my invention by providing a completely transistorized code selector which decodes information which is transmitted in the form of binary code groups. The code identifying a particular receiver consists of a number of binary bits.

Binary codes, each identifying a particular receiver, are received by all receivers. The first bit of each code is a start bit which enables a clock circuit in the selector

to drive a ring counter through one complete cycle. This ring counter has a number of stages, each of which corresponds to one bit of the received code. As the ring counter is driven through its cycle, gating circuitry compares the output of each stage of the ring counter with the corresponding bit of the received code. If there is a coincidence between the binary code which the selector is designed to recognize and the incoming binary code, an alarm is actuated at the end of the ring counter cycle. However, if the gating circuitry detects a difference between any bit of the received code and the corresponding bit of the code which the selector is designed to recognize, the gating circuitry will store the error to inhibit the actuation of the alarm at the end of the ring counter cycle.

The received code may be decoded in the selector by a technique commonly known as amplitude sampling or by another technique known as transition sampling. Both of these techniques will be described in this application.

For a better understanding of the invention, reference should be made to the accompanying drawings wherein:

FIG. 1 is a block diagram of the selector of the subject invention.

FIG. 2 is a schematic drawing of the block diagram of FIG. 1.

FIG. 3 (1 through 8) shows waveform diagrams depicting the operation of the selector of FIG. 1.

FIG. 4 is a block diagram of a modification of the selector of the subject invention.

FIG. 5 (1 through 6) shows waveform diagrams depicting the operation of the selector of FIG. 4.

FIG. 6 is a schematic drawing of the inverter-differentiator shown in block form in FIG. 4.

FIG. 7 is a fragmentary illustration of a code selector incorporating a conference code modification.

FIGS. 1 and 2 show a selector which decodes the received code by the amplitude sampling technique. The outputs of the ring counter stages are successively compared with the corresponding received bit or with the corresponding inverted received bit of the code to determine whether the received code is the same as the code which the selector is adapted to recognize. Two AND circuits are used to compare the outputs of the ring counter stages with the received or inverted bits.

Referring particularly to FIG. 1, there is shown a receiver line 1 upon which the incoming binary code is impressed. The binary code is made up of a number of binary bits, each bit consisting of one of two given input conditions which are referred to herein as the "1" and "0" states. In the subject embodiment, the "1" state is a —3 v. condition while the "0" state is a 0 v. condition. The first bit of the code is a binary "1" which is inverted in the inverter 2 and differentiated in the differentiator 3. The differentiated "1" turns on the clock switch 4. The clock switch enables a clock 5. The clock, together with the advance driver 6 produce pulses having the same time spacing as the spacing between the bits of binary information in the incoming binary code. These clock pulses drive a ring counter 7. The ring counter, of a type well-known in the art, has in the form shown, four magnetic core binary storage elements A, B, C and D. A binary "1" is stored in the first stage, A, before the binary code is received. This binary "1" is driven to succeeding stages of the ring counter by the clock pulses.

When the binary "1," which is driven to succeeding stages by the clock pulses is driven from stage D, a pulse is transferred by the trip line 8 through the inhibit gate 9, to the alarm 10. Actuation of the alarm indicates that the proper binary code has been received by the selector.

Gating circuitry 11 is provided to detect the presence

of a code other than the code which the selector has been designed to recognize, and to inhibit the actuation of the alarm through the bi-stable switch 12 and the inhibit gate 9. The gating circuitry shown has been arranged to recognize the binary code 1101. This gating circuitry consists of an AND circuit 14 connected to stages A, B and D, and another AND circuit 13 connected to stage C. The incoming code from receiver line 1 is also connected to AND circuit 13 through the inverter 2. The incoming code on receiver line 1 is directly connected to the AND circuit 14. The outputs of both AND circuits 13 and 14 are connected to the OR circuit 15. The output of OR circuit 15 is connected to turn on the bi-stable switch 12.

Before attempting a comprehensive description of the operation of the selector of FIG. 1, the operation of each of the circuits shown in block form in FIG. 1 will be described with reference to the schematic drawing, FIG. 2.

The inverter 2 is formed of a transistor 16 and associated components. The receiver line 1 is connected to the base of transistor 16 through a resistor 35 and the collector of the transistor 16 is connected to −12 v. through a resistor 17. When the receiver line 1 is at 0 volts, the transistor 16 is non-conducting and the output of the inverter, which is connected to the collector of the transistor 16, will be at −12 v. because of the −12 v. potential connected to the collector. When the receiver line 1 is at −3 v. condition, corresponding to a binary "1," the transistor will conduct and the output of the inverter will be at the 0 v. level. Thus, the inverter 2 will invert each received bit to produce a corresponding inverted bit at the output.

The output of the inverter is differentiated in the differentiator 3, which consists of a resistor 18 and a capacitor 19. A diode 20, tied to the alarm 10 through the resistor 21 merely serves as an AND gate to prevent passage of a pulse from the inverter 2 through the differentiator 3, when the alarm 10 has been actuated.

The output of the differentiator is fed through a capacitor 22 to the clock switch 4 and more specifically to the base of a transistor 23 which, together with a transistor 24 and associated circuitry, forms the clock switch 4. The collector of transistor 23 is connected to the base of transistor 24 through a resistor 56 and the collector of transistor 24 is connected to the base of transistor 23 through a resistor 57. The base electrodes of transistors 23 and 24 are connected to −12 v. and 0 v. respectively through biasing resistors 53 and 54. The emitters of transistors 23 and 24 are connected to −12 v. and 0 v. respectively through the diodes 58 and 59. The transistors 23 and 24 are normally non-conducting. A positive pulse on the line from the differentiator to the base of transistor 23 will switch transistors 23 and 24 from the non-conducting, or OFF, state to the conducting, or ON, state. The positive pulse on the base of transistor 23 allows transistor 23 to conduct, thus lowering the collector voltage toward the −12 v. which is connected to the emitter. The negative voltage on the collector, which is connected to the base of transistor 24, causes this transistor to conduct. When conducting, the collector voltage of the transistor 24 will rise toward the 0 v. level of the emitter. This positive going voltage on the collector of transistor 24, which is connected back to the base of transistor 23, will turn transistor 23 on more fully thus locking both transistors 23 and 24 in the ON condition. The transistors will remain ON until a positive pulse is transferred from the trip line 8 through a capacitor 25 and a diode 26 to the base of transistor 24. A positive pulse at the base of transistor 24 will turn this transistor OFF. The coupling between the collector of transistor 24 and the base of transistor 23 will turn transistor 23 OFF also. The biasing resistors 53 and 54 will hold transistors 23 and 24 in the OFF condition until a positive pulse at the base of transistor 23 turns both transistors ON again.

The output of the clock switch 4, taken from the collector of transistor 24, is connected to the clock 5 through resistors 28 and 29. The clock 5 comprises a double base diode 27 and associated circuitry. The collector of transistor 24 is connected through resistors 28 and 29 to the emitter of the transistor 27. A charging capacitor 30 is connected between the emitter of transistor 27 and −12 v. The base b_2 of the transistor 27 is connected directly to −12 v. When enabled by the clock switch 4, the clock 5 will oscillate to produce periodic negative clock pulses. When the clock switch 4 is in the OFF condition, the −12 v. on the collector of transistor 24, which is connected to the emitter of transistor 27, prevents the clock from oscillating. However, when the clock switch is turned ON, the collector of transistor 24 will be switched to 0 v. The capacitor 30 will charge toward 0 v. until the potential at the emitter of transistor 27 reaches a point at which transistor 27 will conduct. When transistor 27 conducts, the capacitor 30 will be discharged and a negative pulse will appear at the base b_1. After discharge of the capacitor 30, the transistor 27 will again be cut OFF until the capacitor 30 again becomes charged to the potential at which transistor 27 will conduct.

Each time the transistor 27 conducts, a negative clock pulse appears at the base b_1 of transistor 27. This negative pulse is coupled through a capacitor 31 to the advance driver 6. This driver consists of the transistor 32, together with associated circuitry. The negative pulses at the base of the transistor 32 will allow the transistor 32 to conduct. Each time the transistor 32 conducts, a positive pulse will be fed from the collector of the transistor 32 to a magnetic core ring counter 7.

The ring counter 7 is of a type well-known in the prior art. This ring counter consists of four bi-stable storage elements A, B, C and D. The storage element A consists of the core 33*a* having wound thereon on advance winding 34*a*, a shift winding 35*a*, a drive winding 36*a*, a regenerative winding 37*a* and an output winding 38*a*. The storage elements B, C and D have corresponding components. The same numerals are employed for the components of these storage elements, the subscripts *b*, *c* and *d*, respectively, being added.

The advance windings 34*a*, 34*b*, 34*c* and 34*d* are connected in series with one end being connected to −12 v. and the other end being connected to the advance driver 6. The regenerative windings 37*a*, 37*b*, 37*c* and 37*d* are connected in series with one end being connected to 0 v. and the other end being connected to provide regenerative feedback to the advance driver 6. One end of the drive winding 36*a* is connected through a diode 39*a* and a resistor 58*a* to one end of the shift winding 35*b*. Similarly, the drive winding of each stage is connected to the shift winding of the next successive stage. The drive winding 36*d* is connected to the shift winding 35*a* of storage element A to complete the ring as is common in ring counters of this type.

The operation of the ring counter can be described briefly as follows. Clock pulses from the advance driver 6 are applied to the series connected advance windings to drive the cores toward the "0" position. Before the recurrent clock pulses are applied to the advance windings, the first magnetic core 33*a* has been set in the "1" position. The first clock pulse will tend to drive this core back to the "0" position and at the same time a positive pulse will be induced in the drive winding 36*a*. This positive pulse will be transferred by the diode 39*a* and the resistor 58*a* to the shift winding 35*b* of the magnetic core 33*b* with a polarity such that the magnetic core 33*b* will be driven to the "1" position. Similarly, the next clock pulse through the advance windings will drive the magnetic core 33*b* back to the "0" position while at the same time shifting the "1" to the third magnetic core 33*c*. Each clock pulse will transfer the binary "1" to the next succeeding magnetic storage element. When the binary "1" has reached the last storage element D, the next clock

pulse will transfer the binary "1" to the first magnetic storage element A. This transfer is effected in the same manner as the transfer of the binary "1" to successive storage elements previously described. The same clock pulse that transfers the "1" from stage D to stage A will shift stage D back to the "0" state and cause a positive pulse to be transferred from the output winding 38*d* on core 33*d* over the trip line 8 through a capacitor 52, to inhibit gate 9. The pulse from output winding 38*d* will also be coupled through the capacitor 25 and the diode 26 to the clock switch 4 so as to turn the clock switch 4 OFF. The ring counter 7 will then have a "1" in stage A, the clock 5 will be turned OFF, and the counter will be in a state to receive the next group of clock pulses. The ring counter has been driven through one complete cycle.

If the selector has been designed to recognize the code 1101, the output windings 38*a*, 38*b* and 38*d* are connected in series with one end being connected to 0 v. and the other end being connected to AND circuit 14. The output winding 38*c* has one end connected to 0 v. while the other end is connected to the AND circuit 13. The arrangement of the connections of the output windings of the ring counter stages to the AND circuits 13 and 14 determines the particular code which the selector is designed to recognize.

These connections of the output windings cause a positive pulse to be transferred from the output windings 38*a*, 38*b* or 38*d* to AND circuit 14 whenever any one of the stages A, B or D is shifted from the "1" to the "0" state. Similarly, a positive pulse will be transferred to AND circuit 13 whenever stage C is shifted from the "1" to the "0" state.

The AND circuit 14 consists of a diode 40, a resistor 41 and a capacitor 42. Positive pulses from the series-connected output windings of stages A, B and D are coupled to the anode of the diode 40 through the capacitor 42. These positive pulses will be coupled through the diode 40 only when the other input to the AND circuit, the input from the receiver line through the resistor 41 is at 0 v., the "0" state of the receiver line. Similarly, the AND circuit 13 consists of a resistor 43 and a diode 44. Positive pulses from the output winding of stage C will be coupled through the AND circuit 13 only when the input from the inverter 2 through resistor 43 is at 0 v. The outputs of AND circuits 13 and 14, taken from the cathodes of diodes 40 and 44, are connected together to form the OR circuit 15.

The output of the OR circuit 15 is connected through the capacitor 45 to the bi-stable switch 12. More specifically, the pulse is coupled to the base of a transistor 46 which, together with a transistor 47, forms the bi-stable switch 12. This bi-stable switch 12 is normally OFF and will be turned ON by a pulse from the OR circuit 15.

However, the bi-stable switch 12 can be turned ON only when the clock switch 4 is in the ON position. In order to insure that the transistor 47 can conduct only when the clock switch 4 is in the ON position, the collector of the transistor 24 is connected directly to the emitter of transistor 47. The transistor 47 can conduct only when the collector of transistor 24 is at 0 v. This occurs when transistor 24 is in the conducting or ON state. When clock switch 4 is ON, a positive pulse from either AND circuit 13 or AND circuit 14 through capacitor 45 to the base of transistor 46 will turn the bi-stable switch 12 ON. The operation of bi-stable switch 12 in switching between the ON and the OFF states is similar to the operation of clock switch 4 previously described. Once bi-stable switch 12 has been turned ON, it will remain ON until clock switch 4 is turned OFF, thus returning the emitter of transistor 47 to −12 v. and shutting OFF both transistors 46 and 47.

The inhibit gate 9 consists of a diode 60, a resistor 61 and a capacitor 48. Trip line 8 is connected to the inhibit gate 9 and more specifically to the anode of diode 60 through the capacitor 52. The bi-stable switch 12 is connected directly to the anode of diode 60. A positive pulse from the trip line 8 of the ring counter will pass through the diode 60 only when the bi-stable switch 12 is in the OFF condition. If bi-stable switch 12 has been turned ON during the operation of the ring counter, the pulse will not pass through diode 60 to the alarm 10.

The alarm 10 includes a switch consisting of transistors 49 and 50, and associated circuitry. The operation of this switch is similar to the operation of the clock switch which has been already described. A positive pulse from inhibit gate 9 to the base of transistor 49 will turn the switch ON. Both transistors 49 and 50 will conduct and any suitable indicator 51 which is connected between the collector of transistor 50 and −12 v. will be actuated.

The operation of the selector of FIGS. 1 and 2 in recognizing the particular code 1101 can now be described in detail. This can best be done by referring to the waveform diagrams in FIG. 3. FIG. 3–1 shows the clock pulses which are fed into the advance windings of the ring counter. FIG. 3–2 shows the incoming code on the receiver line 1 and FIG. 3–3 shows the inverted receiver line output from the inverter 2. The first bit of the code shown in FIG. 3–2 is the start bit which enables the clock to drive the ring counter. The remainder of the bits shown in FIG. 3–2 represents the binary code 1101 which the selector of the subject embodiment has been designed to recognize.

The first transition from "0" to "1" on the receiver line will turn ON the clock switch 4. The first clock pulse will occur 1.5 bits after the first transition and thereafter clock pulses will occur midway between the transition from one bit to another on the receiver line. The clock circuit previously described in detail can be designed so that the first clock pulse occurs the desired 1.5 bits after the reception of the start bit. The first clock pulse will shift the first stage A of the ring counter from the "1" position back to the "0" position. This clock pulse will induce a positive pulse output on the output winding 38*a* of core A, as shown in FIG. 3–4. This positive pulse will be transferred to the AND circuit 14. The pulse cannot pass through the AND circuit since the other input to AND circuit 14, the receiver line input, is in the "1" or −3 v. position, as shown in FIG. 3–2. This AND circuit 14 will pass a pulse only when the pulse occurs at the same time that the receiver line input is in the "0" position. The same first clock pulse has driven the second stage of the ring counter B to the "1" position.

The second clock pulse will drive the second stage, B, to the "0" position and at the same time induce a positive output pulse on the output winding of stage B, as shown in FIG. 3–5. This output pulse likewise will be transferred to the AND circuit 14. The output pulse, shown in FIG. 3–5, will not pass through the AND circuit 14 because the receiver line input to the AND circuit 14 is still in the "1" position as shown in FIG. 3–2. This "1" position of the receiver line is the second bit, "1," in the incoming code. The next clock pulse will drive the third stage C from the "1" to the "0" position, inducing an output pulse on the output winding of stage C. This output pulse, shown in FIG. 3–6, is transferred to the input of the AND circuit 13. This pulse will not pass through the AND circuit 13 since the other input to the AND circuit 13, the inverted receiver line input, as shown in FIG. 3–3, is in the "1" position. This "1" position of the inverted receiver line corresponds to the third bit, "0" in the received code 1101.

Similarly, the fourth clock pulse will drive the stage D from the "1" position to the "0" position inducing an output pulse on the output winding of stage D. This pulse, shown in FIG. 3–7, will not pass through the AND circuit 14 since the receiver line input, FIG. 3–2, is in the "1" position corresponding to the fourth bit, "1," in the incoming code. Since no pulses have passed the AND circuits 13 and 14, the bi-stable switch 12 has not been turned ON.

If this bi-stable switch 12 had been turned ON, the inhibit gate 9 would not pass a pulse. Since this gate 9 is not inhibited wthen the "1" is shifted from the last stage D, the positive pulse appearing on the output winding will pass through this gate to actuate the alarm 10. Actuation of this alarm indicates that the code selector has received the proper binary code input on the receiver line.

A short illustration will indicate the operation of the code selector when a binary code input is received which is one other than the code which the selector is designed to recognize. FIG. 3–8 shows a binary code 1001. This differs from the code which the selector is adapted to recognize in only one bit; the second bit of the code shown in FIG. 3–8 is a "0" instead of a "1" as in the desired code. The first clock pulse will produce a positive output pulse on the output winding of stage A, shown in FIG. 3–4, which will not pass the AND circuit 14 because the receiver line input, FIG. 3–8, is in the "1" position. However, the second clock pulse will cause an output on the output winding of stage B, shown in FIG. 3–5, which will pass the AND circuit 14. The receiver line input of FIG. 3–8 is in the "0" position since the second bit differs from the code which the selector is adapted to recognize. Since the receiver line input in the "0" position and the positive pulse from stage B are applied to the AND circuit 14 smultaneously, the pulse will pass the AND circuit 14 and turn the bi-stable switch 12 ON. The bi-stable switch 12 will inhibit the gate 9 so that when the last stage D is driven from the "1" to the "0" stage, the resultant pulse will not pass through the gate 9 to actuate the alarm 10. In a similar manner, whenever one of the binary bits on the incoming receiver line differs from the desired code 1101, a pulse will pass through either the AND circuit 13 or the AND circuit 14 to turn the bi-stable switch 12 ON and inhibit any actuation of the alarm 10.

Note that in both illustrations the same pulse which is produced at the output of stage D and is fed to the inhibit gate 10 is also connected to the clock switch 4. This pulse will turn the clock switch 4 OFF so that no further clock pulses are fed to the ring counter. The clock pulse which drives stage D from the "1" to the "0" stage, also transfers the binary "1" to the stage A. The ring counter has been driven through one complete cycle and the selector is in a condition to receive the next received code.

FIG. 4 shows a selector which utilizes a system of recognizing a single code by means of transition sampling rather than the amplitude sampling system previously described. The code differs from the code used in the previous system in that a transition between the two input conditions in a desired interval represents a binary "1" and no change in the input condition represents a binary "0." The code 1101 is shown in FIG. 5–1. The first transition shown in FIG. 5–1 is the start transition which enables the clock to drive the ring counter through its cycle. The first transition in the code 1101 occurs two intervals after the start transition and thereafter a transition in a particular interval represents a binary "1" and an absence of a transition represents a binary "0."

The selector of FIG. 4 is designed to test for the presence of a transition in an undesired interval and the absence of a transition in a desired interval. It stores a single error as in the previous example to prevent an alarm at the end of the code.

The incoming binary code on a receiver line 101, shown in FIG. 5–1, is differentiated in an inverter-differentiator 102 so that only transitions in the code are fed to the selector. The inverter-differentiator 102 differs from an ordinary differentiator in that it will produce a positive output pulse whenever there is a positive or a negative going transition in the input. FIG. 6 shows the inverter-differentiator 102 in detail. The input code, shown in FIG. 5–1, is differentiated by a capacitor 126 and a resistor 127. Positive transitions pass through a diode 128 to an output 129. Negative transitions are inverted in an inverter 130 and pass through a diode 131 to the output 129. There will be a positive output pulse at 129, shown in FIG. 5–2, whether there has been a positive or a negative transition in the code.

Since the other circuit elements shown in block form in FIG. 4 have been described in detail in conjunction with the previous embodiment, no further attempt will be made to explain the details of the circuits.

Referring back to FIG. 4, the start transition in the received code turns on a clock switch 103 which enables the clock 104 and an advance driver 105 to feed clock pulses to the ring counter 106. The ring counter 106 is of the same type as the ring counter described in the previous example except that an extra stage has been added. This start-stop stage is required to actuate the alarm after the last transition interval.

If the selector is adapted to recognize the code 1101, the outputs of stages A, B and D of the ring counter are connected in series to the ON input of a bi-stable switch 107. The outputs of stages A, B and D are also connected to a .95 bit delay switch 108. This delay switch can be of any well-known type which will delay the incoming pulse for .95 bit.

The output of delay switch 108 is connected to one input of an AND circuit 109 and to a delay line 110. The output of the delay line 110 is connected to the OFF input 111 of the bi-stable switch 107.

The output of the inverter-differentiator 102 is fed to a delay line 112 and to one input of an AND circuit 113. The output of the delay line 112 is connected to the OFF input 111 of the bi-stable switch 107. The OFF output 114 of the bi-stable switch 107 is connected to the other input to the AND circuit 113. The ON output 115 of the bi-stable switch 107 is connected to the other input to the AND circuit 109.

The outputs of AND circuit 109 and 113 are the inputs to OR circuit 116. The output of OR circuit 116 is connected to the OFF input 117 of a second bi-stable switch 118.

The output of stage A of the ring counter is connected to the bi-stable switch 118 so that bi-stable switch 118 will be turned ON only when a "1" is shifted from stage A of the ring counter into stage B. When this occurs, an output will be transferred from stage A to the ON input 119 of the bi-stable switch 118. The ON output 120 of bi-stable switch 118 is connected to one input of an AND circuit 121. The other input to AND circuit 121 is the output from the start stop stage of the ring counter. Energization of both inputs to the circuit 121 will cause an output from AND circuit 121 which will actuate an alarm 122 to indicate that the proper code has been received.

Operation of the selector of FIG. 4 is as follows. Before the code is received, a "1" is in stage A of the ring counter. The clock 104 and bi-stable switches 107 and 118 are OFF. The start transition in the received code turns on the clock switch 103 and enables the clock 104 and advance driver 105 to feed clock pulses shown in FIG. 5–3, to the ring counter 106. The "1" is shifted by the first clock pulse from stage A to stage B. When the "1" is shifted into stage B, an output pulse will appear on the series connected output windings as shown by the first pulse in FIG. 5–4. This output pulse will turn on the bi-stable switch 118 through the input 119. Bi-stable switch 118 will remain on unless a transition in the received code occurs during an interval in which there should be no transition or if there is no transition in the received code during an interval in which there should be a transition.

The time intervals during which a transition must occur are determined by connections from the ring counter stages A, B and D to the ON circuit 123 of the bi-stable switch 107 and to delay switch 108. When the first clock pulse moves the "1" into stage B, bi-stable switch 107 is turned ON by the first pulse shown in FIG. 5–4. The condition of bi-stable switch 107 is shown in

FIG. 5–6. Approximately .95 bit later the delay switch **108** pulses the AND circuit **109**. FIG. 5–5 shows the output of delay switch **108**. The delay switch **108** may have a delay of between .5 bit and 1.0 bit so that the output of the delay switch occurs between the next transition and the next clock pulse. If a transition has come in during this interval, bi-stable switch **107** has been turned OFF through the input **111**; hence the AND circuit **109** will produce no output because there is no ON input to the AND circuit **109** from bi-stable switch **107**. On the other hand, if the transition did not occur to turn OFF bi-stable switch **107**, the pulse from delay switch **108** will pass through the AND circuit **109** and will turn the bi-stable switch **118** OFF. If bi-stable switch **118** is turned OFF, actuation of the alarm at the end of the ring counter cycle is inhibited.

The output from delay switch **108** is further delayed slightly by the delay line **110** to reset bi-stable switch **107** OFF so that the sensing for the desired transition is confined to the specific clock interval in which it should occur.

Sensing a transition in an undesired interval is accomplished as follows. Bi-stable switch **107** will remain OFF during an interval in which the "1" has been shifted from one of the stages in the ring counter which is not connected to the ON input **123**. If switch **107** is OFF, prior to the occurrence of any transition, that transition will pass through the AND circuit **113** to turn OFF bi-stable switch **118**. Again, if bi-stable switch **118** has been turned OFF, the actuation of the alarm at the end of the ring counter cycle will be inhibited.

Although a transition always turns OFF bi-stable switch **107**, the transition is delayed by the delay line **112** so that its operation on that switch is delayed to permit AND circuit **113** operation prior to bi-stable switch **107** turnoff.

As the binary "1" passes from the start-stop stage of the ring counter, a pulse on the output winding stops the clock through the OFF input **124** to the clock switch **103**. This pulse is also connected to one input to the AND circuit **121**. If bi-stable switch **118** has not been turned OFF, the pulse will pass through AND circuit **121** to actuate the alarm **122**. However, if bi-stable switch **118** has been turned OFF, by the presence or absence of a transition as described above, the alarm will not be actuated.

The number of different codes which the selectors of the subject invention can distinguish is limited only by the number of stages in the ring counter. Each stage which is added to the ring counter allows an additional bit to be added to the code which the selector is adapted to recognize.

Reference to the following chart will show the binary codes which are possible with a four-bit selector as shown in FIGS. 1 or 4.

Table I

0000	1000
0001	1001
0010	1010
0011	1011
0100	1100
0101	1101
0110	1110
0111	1111

The addition of each bit to the code will double the number of possible codes which can be distinguished.

The selectors of this application can be easily adapted for conference calling of two or more selectors with one code. The adaptation of the selector of FIG. 1 so that it will actuate an alarm in response to a conference call code as well as the specific code which the selector is adapted to recognize can best be explained with reference to Table I above showing the binary codes which are possible with a four bit selector. The selector of FIG. 1, which is adapted to recognize the code 1101, can be adapted to actuate the alarm on the reception of a conference call code, for example 1001, by making a very simple change in the gating circuitry. The other selectors which are adapted to recognize the codes 0001, 1011 and 1000 can also be adapted to recognize the conference code 1001 in addition to the code which they are particularly adapted to recognize. The selector of FIG. 1 can be adapted to recognize this conference code as shown in FIG. 7 by simply omitting the connection from the output of storage element B to the AND circuit **14** as, for example, by opening a suitable switch. By omitting this connection, the alarm of FIG. 1 will be actuated when either the code 1101 which the selector is adapted to recognize or the conference code 1001 is received as shown in FIG. 7, a ring counter **140** similar to ring counter **7** of FIG. 1 has a plurality of stages A, B, C, and D. The outputs from stages A and D are connected to an AND GATE, not shown, corresponding to AND GATE **14** of FIG. 1, and the output from stage C is connected to an AND GATE, not shown, corresponding to AND GATE **13** of FIG. 1. The output from stage B of the counter is not connected to either of the AND GATES as by opening switch **141** or by completely omitting this lead. Thus, if the second bit is either zero (0) or a one (1), there is no output pulse from either of the AND GATES, and the bistable switch is not actuated to inhibit actuation of the alarm. Thus, it can be seen that ring counter **140** will respond to the binary code 1001 or 1101. The outputs of these AND GATES are connected to an OR GATE, also not shown, corresponding to OR GATE **15** of FIG. 1. This OR GATE produces an output pulse in response to a pulse from either AND GATE which output pulse actuates a bistable switch, not shown, to inhibit an alarm gate to prevent the output pulse from stage D of ring counter **140** from actuating the alarm. The selector which is adapted to recognize the code 0001 can also be adapted to recognize the conference code by omitting the connection from the output of the A stage to the gating circuits. Similarly, the selector adapted to recognize the code 1011 can be made to recognize the conference code by omitting the connection between the C stage and the gating circuitry and the selector adapted to recognize the code 1000 can be made to recognize the conference code by omitting the connection between the D stage and the gating circuitry. In the four bit selector shown, four selectors can be made responsive to a conference code as well as to a particular code. The number of selectors which can be made responsive to a conference code, depends upon the number of bits in the binary code used. When fourteen bit selectors are used, for example, up to fourteen selectors can be made responsive to a conference code as well as to a particular code.

Another advantage of the code selectors of this invention is the ease with which they may be adapted to error correcting. An error correcting system is desirable to insure that the selector is actuated in response to a desired code even though one of the bits of the code is in error due to faulty transmission. If the selectors are designed so that two errors must occur in the received code before actuation of the alarm is inhibited, the probability of a selector failing to actuate an alarm in response to a particular code is greatly diminished.

The amplitude sampling selector of FIG. 1 may be changed so that actuation of the alarm is inhibited only when there are two errors in the received code by inserting another bi-stable switch between bi-stable switch **12** and inhibit gate **9**. This additional bi-stable switch woulld be enabled by bi-stable switch **12** being turned ON and would be turned ON by the output of OR gate **15**. Thus, the alarm would be inhibited only after two or more errors in the received code. The number of codes which can be used out of the total number of pos-

sible codes is somewhat limited when an error correcting system such as the one described above is used. The selection of the codes which are to be used to obtain the highest degree of reliability is discussed in detail in The Design of Switching Circuits, by W. Keister, A. E. Ritchie and S. H. Washburn, chapter 12, section 12.4 of this book is particularly pertinent.

The selectors described above have been quite successful when used with a selective calling system. A 14-bit selector was constructed using transistors and printed circuitry. The selector performed successfully. A fourteen bit selector such as this is capable of recognizing one of 16,384 codes which are possible when using a fourteen bit code.

The novel features believed descriptive of the invention are defined particularly in the appended claims.

What I claim as new and desire to secure by Letters Patent of the United States is:

1. A code selector of the type used in the receiver of a selective calling system in which an alarm is actuated at a particular receiver only when a particular binary code is received and recognized by the selector comprising a receiver line upon which is impressed a received binary code consisting of a number of binary bits, a ring counter having a number of stages, each stage corresponding to one bit of the received code, means including a source of clock pulses for driving said ring counter through one complete cycle in response to the first binary bit which is received, an inverter for inverting each received bit to produce a corresponding inverted bit, means for comparing the output of each stage of the ring counter with the corresponding received bit on the receiver line if that bit in the code which selector is designed to recognize is a "1," means for comparing the output of each stage of the ring counter with the corresponding inverted bit from the inverter if that bit in the code which the selector is adapted to recognize is a "0," an alarm, said alarm being actuated upon completion of the ring counter cycle only when each bit of the received code is the same as the corresponding bit of the code which the selector is designed to recognize.

2. A code selector of the type used in the receiver of a selective calling system in which an alarm is actuated at a particular receiver only when a particular binary code is received and recognized by the selector comprising a receiver line upon which is impressed a received binary code consisting of a number of binary bits, a ring counter having a number of stages, each stage corresponding to one bit of the received code, means including a source of clock pulses for driving said ring counter through one complete cycle in response to the first binary bit which is received, an inverter for inverting each received bit to produce a corresponding inverted bit, the outputs of the ring counter stages corresponding to the binary "1" bits in the code which the selector is adapted to recognize being connected in series, said outputs being connected to a first AND circuit, said inverter being connected to said AND circuit so as to couple said inverted bits to said AND circuit, said AND circuit producing an output only when one of the stages whose output is connected to said AND circuit is shifted from the "1" to the "0" state at the same time the corresponding inverted bit is in the "0" state, the outputs of the ring counter stages corresponding to the binary "0" bits in the code which the selector is adapted to recognize being connected in series, said outputs being connected to a second AND circuit, said receiver line being connected to said second AND circuit so as to couple said received bits to said second AND circuit, said second AND circuit producing an output only when one of the stages whose output is connected to said second AND circuit is shifted from the "1" to the "0" state at the same time the corresponding received bit is in the "0" state, the outputs of said AND circuits being connected to an OR circuit, a bi-stable switch, said bi-stable switch being connected to the output of said OR circuit and being turned ON by a pulse output from said OR circuit, an alarm, the output of said bi-stable switch being connected to said alarm, said alarm being actuated upon completion of the ring counter cycle only when bi-stable switch is in the OFF condition.

3. A code selector of the type used in the receiver of a selective calling system in which an alarm is actuated at a particular receiver only when a particular binary code is received and recognized by the selector comprising a receiver line upon which is impressed a received binary code consisting of a number of binary bits, a clock circuit, said clock circuit producing periodic clock pulses, a ring counter, said ring counter having a number of stages, each stage corresponding to one bit in the received binary code, said clock pulses being connected to the first of said stages, said first stage being in the binary "1" condition before the occurrence of the first of said clock pulses, each of said clock pulses transferring the binary "1" to the next succeeding stage, an inverter for inverting each received bit to produce a corresponding inverted bit, means for comparing the output of each stage of the ring counter with the corresponding received bit if that bit in the code which selector is adapted to recognize is a "1," means for comparing the output of each stage of the ring counter with the corresponding inverted bit if that bit in the code which the selector is adapted to recognize is a "0," an alarm, said alarm being connected to the last stage of the ring counter, said alarm being actuated upon completion of the ring counter cycle only when each bit of the received code is the same as the corresponding bit of the code which the selector is adapted to recognize.

4. A code selector of the type used in the receiver of a selective calling system in which an alarm is actuated at a particular receiver only when a particular binary code is received and recognized by the selector comprising a receiver line upon which is impressed a received binary code consisting of a number of binary bits, a clock circuit, said clock circuit producing periodic clock pulses, a ring counter, said ring counter consisting of a number of stages, each stage corresponding to one bit in the received binary code, said clock pulses being connected to the first of said stages, said first stage being in the binary "1" condition before the occurrence of the first of said clock pulses, each of said clock pulses transferring the binary "1" to the next succeeding stage, an inverter for inverting each received bit to produce a corresponding inverted bit, the outputs of the ring counter stages corresponding to the binary "0" bits in the code which the selector is adapted to recognize being connected in series, said outputs being connected to an AND circuit, said inverter being connected to said AND circuit so as to couple said inverted bits to said AND circuit, said AND circuit producing an output only when one of the stages whose output is connected to said AND circuit is shifted from the "1" to the "0" state at the same time the corresponding inverted bit is in the "0" state, the outputs of the ring counter stages corresponding to the binary "1" bits in the code which the selector is adapted to recognize being connected in series, said outputs being connected to a second AND circuit, said receiver line being connected to said second AND circuit, so as to couple said received bits to said second AND circuit, said second AND circuit producing an output only when one of the stages whose output is connected to said second AND circuit is shifted from the "1" to the "0" state at the same time the corresponding received bit is in the "0" state, the outputs of said AND circuits being connected to an OR circuit, a bi-stable switch, said bi-stable switch being connected to the output of said OR circuit so as to turn said bi-stable switch ON when a pulse is transmitted to said switch from said OR circuit, an alarm, the output of said bi-stable switch being connected to said alarm, said alarm being actuated

upon completion of the ring counter cycle only when said bi-stable switch is in the OFF condition.

5. A code selector of the type used in the receiver of a selective calling system in which an alarm is actuated at a particular receiver only when a particular binary code is received and recognized by the selector comprising a receiver line upon which is impressed a received binary code consisting of a number of binary bits, a ring counter having a number of stages, each stage corresponding to one bit of the received code, each of said stages including a core of a magnetic material, means including a transistorized source of clock pulses for driving said ring counter through one complete cycle in response to the first transition of the received code, means including a transistor, for inverting each received bit to produce a corresponding inverted bit, the outputs of the ring counter stages corresponding to the binary "1" bits in the code which the selector is adapted to recognize being connected in series, said outputs being connected to a first AND circuit, the output of said inverter being connected to said AND circuit, said AND circuit producing an output only when one of the stages whose output is connected to said AND circuit is shifted from the "1" to the "0" state at the same time the corresponding inverted bit is in the "0" condition, the outputs of the ring counter stages corresponding to the binary "0" bits in the code which the selector is adapted to recognize being connected in series, said outputs being connected to a second AND circuit, said receiver line being connected to said second AND circuit, said second AND circuit producing an output only when one of the stages whose output is connected to said second AND circuit is shifted from the "1" to the "0" state at the same time the corresponding received bit is in the "0" condition, the outputs of said AND circuits being connected to an OR circuit, a bi-stable switch, said bi-stable switch comprising two transistors connected to be switched between two states, both of said transistors being conducting in one of said states and both of said transistors being non-conducting in the other of said states, said bi-stable switch being connected to the output of said OR circuit and being turned ON by a pulse output from said OR circuit, an alarm, said alarm being actuated upon completion of the ring counter cycle only when said bi-stable switch is in the OFF condition.

6. A code selector of the type used in the receiver of a selective calling system in which an alarm is actuated at a particular receiver only when a particular binary code is received and recognized by the selector comprising a receiver line upon which is impressed a received binary code consisting of a number of binary bits, a ring counter having a number of stages, each stage corresponding to one bit of the received code, means including a source of clock pulses for driving said ring counter through one complete cycle in response to the first received binary bit, gating circuitry, the outputs of said ring counter stages being connected to said gating circuitry, said receiver line being connected to said gating circuitry, so as to couple said received binary code to said gating circuitry, an alarm, said alarm being connected to said gating circuitry, said gating circuitry being responsive to the received binary code and the condition of said ring counter stages to change the condition of said gating circuitry whenever an individual received code bit differs from the corresponding bit preset into said ring counter thereby disabling said alarm circuit so as to actuate an alarm only when the received binary code is the code which the selector is designed to recognize, said gating circuitry being connected so as to be non-responsive to the condition of a selected stage of said ring counter so that the selector will actuate the alarm in response to a received conference code in addition to the code which the selector is adapted to recognize.

7. A code selector of the type used in the receiver of a selective calling system in which an alarm is actuated at a particular receiver only when a particular binary code is received and recognized by the selector comprising a receiver line upon which is impressed a received binary code consisting of a number of binary bits, a ring counter having a number of stages, each stage corresponding to one bit of the received code, means including a source of clock pulses for driving said ring counter through one complete cycle in response to the first binary bit which is received, an inverter for inverting each received bit to produce a corresponding inverted bit, means for comparing the output of each stage of the ring counter with the corresponding received bit on the receiver line if that bit in the code which selector is designed to recognize is a "1," means for comparing the output of each stage of the ring counter with the corresponding inverted bit from the inverter if that bit in the code which the selector is designed to recognize is a "0," an alarm, said alarm being actuated upon completion of the ring counter cycle only when each bit of the received code is the same as the corresponding bit of the code which the selector is designed to recognize, the output from a selected stage of the ring counter not being connected to be compared with the received code so that the selector will actuate the alarm in response to a received conference code in addition to the code which the selector is designed to recognize.

8. A code selector of the type used in the receiver of a selective calling system in which an alarm is actuated at a particular receiver only when a particular binary code is received and recognized by the selector comprising a receiver line upon which is impressed a received binary code consisting of a number of binary bits, a ring counter having a number of stages, each stage corresponding to one bit of the received code, means including a source of clock pulses for driving said ring counter through one complete cycle in response to the first transition of the received code, an inverter for inverting each received bit to produce a corresponding inverted bit, the outputs of the ring counter stages corresponding to the binary "1" bits in the code which the selector is adapted to recognize being connected in series, said outputs being connected to a first AND circuit, said inverter being connected to said AND circuit so as to couple said inverted bits to said AND circuit, said AND circuit producing an output only when one of the stages whose output is connected to said AND circuit is shifted from the "1" to the "0" state at the same time the corresponding inverted bit is in the "0" condition, the outputs of the ring counter stages corresponding to the binary "0" bits in the code which the selector is adapted to recognize being connected in series, said outputs being connected to a second AND circuit, said receiver line being connected to said second AND circuit so as to couple said received bits to said second AND circuit, said second AND circuit producing an output only when one of the stages whose output is connected to said second AND circuit is shifted from the "1" to the "0" state at the same time the corresponding received bit is in the "0" condition, the outputs of said AND circuits being connected to an OR circuit, a bi-stable switch, said bi-stable switch being turned ON by a pulse output from said OR circuit, an alarm, said alarm being actuated upon completion of the ring counter cycle only when said bi-stable switch is in the OFF condition, the connection between the output winding of a selected stage of said ring counter and a selected one of said AND circuits being omitted so that the selector will actuate the alarm in response to a received conference code in addition to the code which the selector is designed to recognize.

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