United States Patent [19]

Freeman

[11] **3,716,725**

[45] **Feb. 13, 1973**

[54] RING COUNTER

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[22] Filed: **Jan. 4, 1971**

[21] Appl. No.: **103,675**

Related U.S. Application Data

[62] Division of Ser. No. 699,149, Jan. 19, 1968, Pat. No. 3,553,334.

[52] **U.S. Cl.**.....**307/223,** 328/43

[51] **Int. Cl.**.....**H03k 23/08**

[58] **Field of Search** 307/223; 328/43, 45, 46

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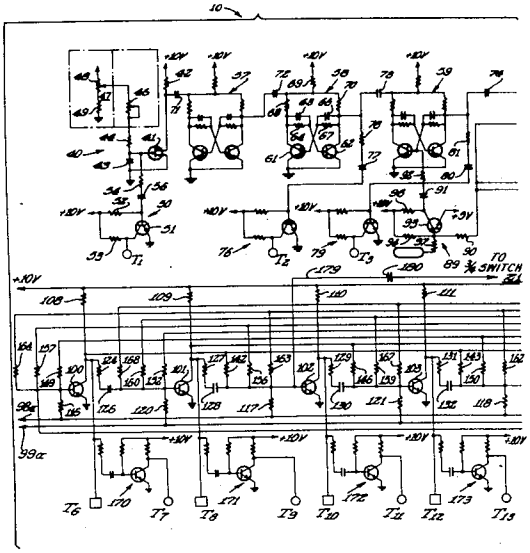
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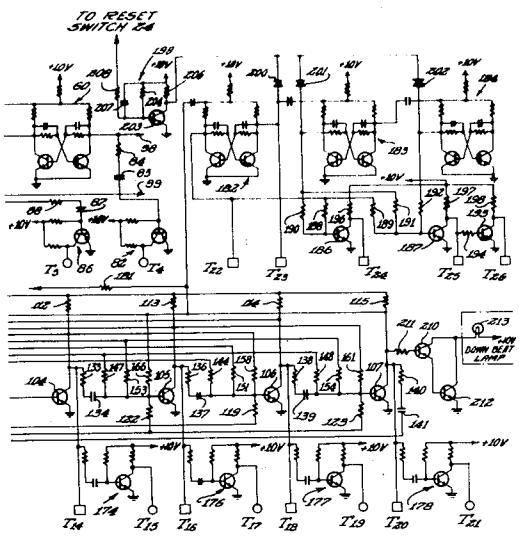
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[57] **ABSTRACT**

An electronic ring counter driven by a source of pulses and having controls to bypass some of the stages of the ring counter, each stage employing a single transistor.

3 Claims, 3 Drawing Figures





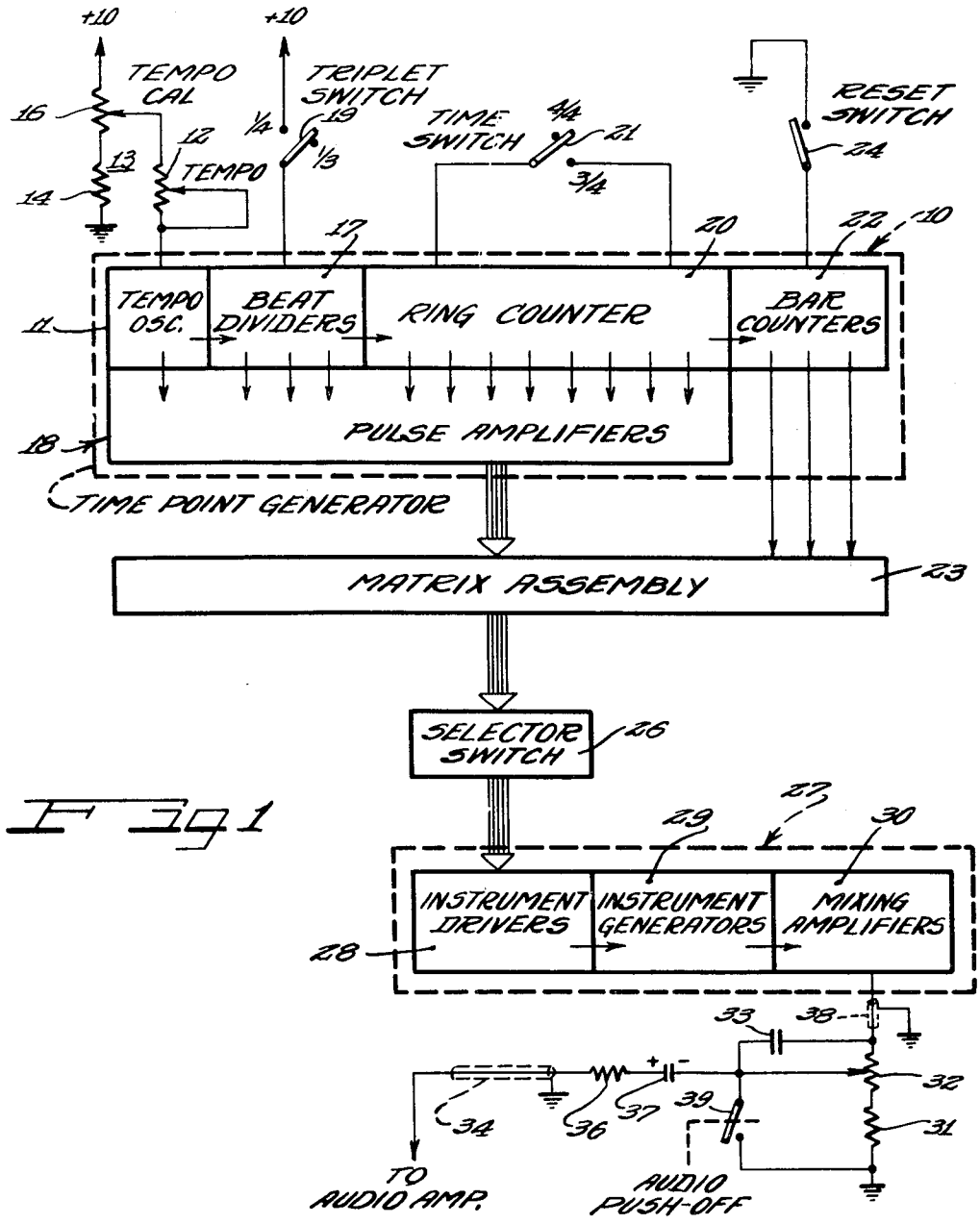


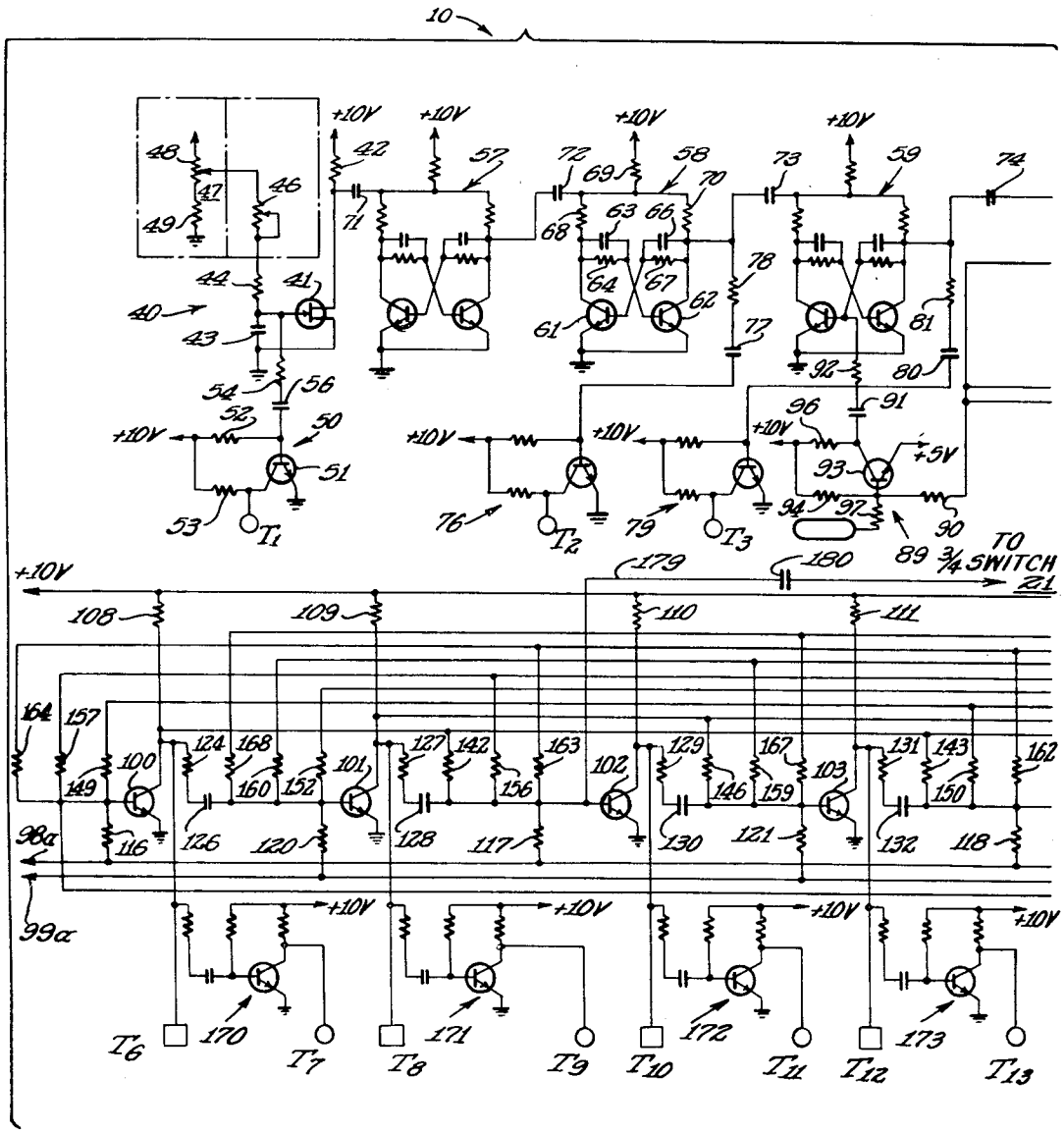
Fig 1

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Fig. 2a



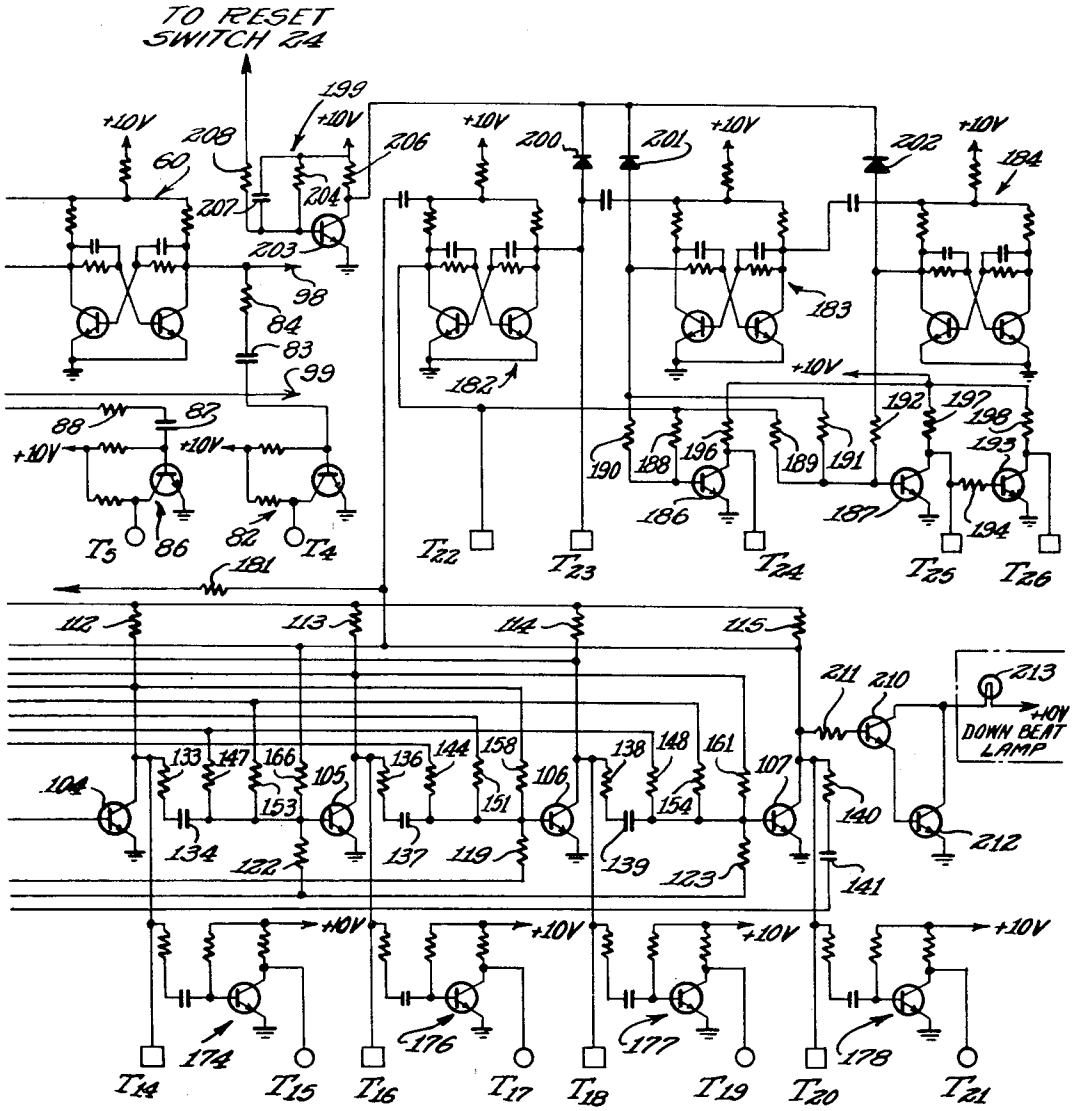
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Fig. 2b



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RING COUNTER

This application is a division of my copending application for U. S. Pat., Ser. No. 699,149, filed Jan. 19, 1968, now U. S. Pat. No. 3,553,334.

This invention is directed to a ring counter, such as for use in an electronic rhythm producing sound device for automatically generating sounds in rhythmic patterns for use alone or in accompaniment with other musical instruments.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing generally the circuit arrangement of a rhythm sound producing device embodying a ring counter constructed in accordance with principles of this invention; and

FIG. 2 is divided into two segments designated FIGS. 2*a* and 2*b* and shows a detailed schematic diagram of the circuit arrangement of the time-point generator including the ring counter of FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a diagram of a musical rhythm sound producing device embodying a ring counter constructed according to this invention. The device includes a time-point generator **10** (utilizing a ring counter **20**) which produces a plurality of sequential spaced apart pulses which may correspond to the sequential spacing of a line or bar of written music. The time-point generator **10** includes a tempo oscillator **11** the frequency of which is selectively variable by a potentiometer **12**. The potentiometer **12** is connected to a voltage divider network **13** comprising a resistor **14** and a potentiometer **16**. The potentiometer **16** is used to calibrate the voltage applied to the tempo oscillator, thereby calibrating the range of frequency of oscillation.

The output of the tempo oscillator **11** is delivered to a beat divider network **17** and to one of a plurality of pulse amplifiers designated generally at **18**. A switch **19** is connected to the beat divider network **17** to selectively change the voltage applied to a portion of the beat divider network, thereby enabling the network **17** to divide by four or divide by three as desired. The output of the beat divider network **17** is delivered to certain ones of the plurality of pulse amplifiers **18** and to the input of a ring counter **20**, the network **17** serving as an exemplary source of pulses.

The ring counter **20** is a direct-coupled self-biasing circuit which, in the preferred embodiment, has eight stages. The ring counter **20** may have more or less than eight stages.

The ring counter **20** is biased such that seven of the eight stages are conducting in the saturated mode of operation and one stage is non-conducting at all times. A pulse from the beat divider network **17** will cause the non-conducting stage to become conductive and the following stage to become non-conductive.

The eight stages of the ring counter are divided into two groups, one group containing the odd number stages and the other group containing the even number stages.

Connected to the ring counter **20** is a time switch **21** which enables the ring counter to generate a 4/4 4 time or a three-fourths time depending upon the type of rhythm being reproduced by the rhythm sound generator. By way of example, the ring counter **20** is an eight stage counter wherein the output of the last stage is fed back to the input of the first stage thereby allowing the ninth pulse from the beat divider network **17** to restart the count-by-eight cycle. With the time switch **21** in the open position, as shown on the drawing, the ring counter will produce eight pulses in sequence. However, when the time switch **21** is in the closed position, the first two stages of the ring counter are bypassed, thereby converting the ring counter into a count-by-six circuit. This feature enables the ring counter **20** to generate both 4/4 4 and three-fourths time counts for the various types of music being reproduced.

The plurality of outputs of the ring counter **20** are connected to still another group of pulse amplifiers **18** and to a bar counter **22**. Each time the ring counter **20** produces the eighth pulse of the count by eight sequences of operation, it generates an output pulse at the input of the bar counter **20**. The output of the bar counter is decoded by a series of logic circuits and applied to a matrix assembly **23**. Also connected to the bar counter **20** is a reset switch **24** which resets the bar counter to the zero count.

Also connected to the matrix assembly **23** are the outputs of the pulse amplifiers **18**. The matrix assembly **23** is constructed primarily of resistors which are direct current coupled to the pulse amplifiers and bar counter.

The output of the matrix assembly **23** is connected to a selector switch assembly **26** and therefrom to an instrument sound generator **27**. The selector switch **26** connects the proper matrices within the matrix assembly **23** to the respective ones of a plurality of instrument driver circuits **28**. The instrument driver circuits **28** are connected to one or more of a plurality of instrument generator circuits **29**. The output of the instrument generator circuits are then applied to mixing amplifiers **30**.

The output of the mixing amplifiers is connected to an audio amplifier (not shown) through a coupling circuit comprising a voltage divider network which is formed by resistor **31** and a potentiometer. A capacitor **33** has one end thereof connected to the movable contactor of the potentiometer **32** and the other end thereof connected to one end of the resistance element of the potentiometer **32**. The audio signal passing through the capacitor **33** and the movable contactor of the potentiometer **32** is delivered to a shielded cable **34** through a resistor **36** and a coupling capacitor **37**. The output of the mixing amplifiers **30** is connected to the coupling circuit through a shielded cable **38**. Connected to the junction of the movable contact of the potentiometer **32** and the capacitor **33** is a switch **39** which is connected to ground potential. When the switch **39** is closed, the audio signal from the mixing amplifiers **30** is grounded to mute the output of the rhythm sound device.

FIG. 2 is a detailed schematic diagram of the time-point generator **10** of FIG. 1 and is divided into two segments FIG. 2*a* and FIG. 2*b*. The tempo oscillator **11** is designated generally on FIG. 2 by reference numeral **40** and its construction and operation are described in detail in the parent application. The tempo oscillator comprises the components **41–44**.

The tempo oscillator is operated as a free-running unijunction relaxation oscillator which produces pulses at its outlet. A potentiometer **46** is connected to a voltage divider network **47** comprising a potentiometer **48** and a resistor **49**, which jointly correspond to the elements **12–16**. The pulses produced by the tempo oscillator are the basic timing signals for the musical rhythm sound producing device. By varying the resistance of the potentiometer **46**, the operating frequency of the oscillator is changed. The maximum frequency of the tempo oscillator **41** is pre-adjusted by the calibration resistor **48**.

Pulse signal information is taken from the emitter junction of the transistor **41** and delivered to a pulse amplifier stage **50**. The pulse amplifier stage **50** comprises one of the pulse amplifiers **18**, shown in FIG. **1**, and comprises the components **51–56**, whose construction and operation are described in detail in the parent application. A pulse signal is thus obtained at the output terminal T_1.

All of the pulse amplifiers used in the time-point generator are constructed and operate in substantially the same manner as that of the pulse amplifier **50**.

The pulse signal information developed across the load resistor **42** of the tempo oscillator circuit **40** is delivered to the first of a series of divider networks or flip-flop circuits **57**, **58**, **59**, and **60**. Each of the flip-flop circuits **57–60** is constructed and operates in substantially the same manner and include elements **61–70** coupled together by coupling capacitors **71–74**, as set forth in the parent application.

The flip-flop stages **57–60** are each a two-stage direct-coupled amplifier with positive feedback. Two pulses applied to the input of the flip-flop stage will produce a single pulse at the output thereof. As each stage **57–60** operates in the same manner, the total division accomplished by the stages between the tempo oscillator and the output of stage **60** is **16**.

The output of flip-flop stage **58** is coupled to the input of stage **59** and to a pulse amplifier circuit **76** through a coupling capacitor **77** and a resistor **78**. The pulse amplifier circuit **76** operates in substantially the same manner as that of the pulse amplifier circuit **50**. A negative going pulse at the output of flip-flop stage **58** will render the transistor of the pulse amplifier **76** nonconductive to produce a positive going pulse at the output terminal T_2 thereof. Similarly, the output of flip-flop stage **59** is coupled to the input of stage **60** and to a pulse amplifier stage **79** to produce a pulse at the output terminal T_3 of the pulse amplifier. Also, the output of flip-flop stage **60** is coupled to a pulse amplifier stage **82** through a coupling capacitor **83** and a resistor **84** to produce a pulse at the output terminal T_4 of the pulse amplifier **82**. The flip-flop stage **60** has a second output terminal thereof connected to a pulse amplifier stage **86** through a coupling capacitor **87** and a resistor **88**, and to a feedback amplifier circuit **89**. The feedback amplifier **89** is connected to the second output of flip-flop stage **60** through a resistor **90**, and therefore is direct current coupled to the flip-flop stage **60**. The output of the feedback amplifier **89** is connected to the input of one of the transistors of the flip-flop stage **59** through a coupling capacitor **91** and a resistor **92**.

The feedback amplifier **89** includes a transistor **93** which has the base electrode thereof connected to a positive voltage source through a biasing resistor **94**. Also connected to the positive voltage source is the collector electrode of transistor **93** through a load resistor **96**. The base of transistor **93** is connected to the triplet switch **19**, shown in FIG. **1**, through a resistor **97**. The operation of the feedback amplifier is detailed in the parent application.

In operation, when the triplet switch **19** is in the closed position, the last two flip-flop stages **59** and **60** operate in their normal mode to divide by four. On the other hand, when the switch **19**, of FIG. **1** is in the open position, the total count capacity of the last two flip-flops **59** and **60** is reduced from four counts to three counts. The output of the last flip-flop stage **60** is then non-symmetrical in a ration of 2:1 or divided at third intervals rather than in halves.

The pulses produced at the output of flip-flop stage **60** are applied to circuit points **98** and **99**, which are connected to circuit points **98*a*** and **99*a*** which are signal input terminals of an eight stage ring counter. Although the present embodiment is an eight stage ring counter, a ring counter having any number of stages may be provided in accordance with the principles of this invention.

According to this invention a single transistor is used in each stage of the ring counter **20**. The ring counter **20** comprises transistors **100**, **101**, **102**, **103**, **104**, **105**, **106**, and **107**. The emitter electrode of each transistor is connected to ground potential while the collector electrode thereof is connected to a positive voltage source through a corresponding load resistor **108**, **109**, **110**, **111**, **112**, **113**, **114** and **115** respectively. It will be noted that each stage of the ring counter is constructed in substantially the same manner.

The circuit point **98a** from the output of the beat divider network **60**, is connected to the base electrodes of transistors **100**, **102**, **104**, and **106** through corresponding resistors **116**, **117**, **118**, and **119** respectively. Similarly, the circuit point **99*a*** is connected to the base electrode of transistor **101**, **103**, **105**, and **107** through corresponding resistors **120**, **121**, **122**, and **123** respectively.

The collector electrode of transistor **100** is coupled to the base electrode of transistor **101** through a resistor **124** and a capacitor **126**, while the collector electrode of transistor **101** is coupled to the base electrode of transistor **102** through a resistor **127** and a capacitor **128**. The outputs of the remaining transistors **102–107** are coupled to the corresponding down stage transistors through resistive capacitive networks comprising resistors **129**, **131**, **133**, **136**, **138**, and **140** and capacitors **130**, **132**, **134**, **137**, **139**, and **141** respectively.

The collector of transistor **100** is direct current coupled to the base electrode of transistors **102**, **104**, and **106** through resistors **142**, **143**, and **144** respectively. The collector of transistor **101** is direct current coupled to the base electrode of transistors **103**, **105**, and **107** through resistors **146**, **147**, and **148** respectively. The collector of transistor **102** is direct current coupled to the base electrode of transistors **100**, **104**, and **106** through resistors **149**, **150**, and **151** respectively. The collector of transistor **103** is direct current coupled to the base electrode of transistors **101**, **105** and **107** through resistors **152**, **153** and **154** respectively. The

collector electrode of transistor **104** is direct current coupled to the base electrode of transistors **100**, **102**, and **106** through resistors **157**, **156** and **158** respectively. The collector electrode of transistor **105** is direct current coupled to the base electrode of transistors **101**, **103**, and **107** through resistors **160**, **159** and **161** respectively. Similarly, the collector electrode of transistor **106** is direct current coupled to the base electrode of transistors **100**, **102**, and **104** through resistors **164**, **163**, and **162** respectively, and the collector electrode of transistors **107** is direct current coupled to the base electrode of transistors **101**, **103** and **105** through resistors **168**, **167** and **166** respectively. It will be noted that the output of the last resistor **107** is coupled back to the input of the first transistor **100** through the resistor **140** and capacitor **141**.

In operation, the biasing of each of the transistors **100–107** of the ring counter is arranged such that seven of the transistors are operated in the saturated mode of operation while only one of the transistors is non-conductive. The transistors **100**, **102**, **104**, and **106** form one group of count circuits while transistors **101**, **103**, **105**, and **107** form a second group of count circuits. In each group of transistors the base electrode of each transistor is connected to the collector electrodes of the other three transistors in the group. The interconnecting resistors and the collector load resistor of each stage in the group are sized such that any three stages of the group will be held in the saturated mode of operation if the remaining stage is in the cut off condition. The transistor which is in the cut off mode of operation will remain cut off as long as the collector voltage of the remaining three saturated transistors remains below the voltage necessary to bias the transistor on.

Each base electrode of transistors **100–107** is coupled to the circuit points **98***a* and **99***a* to receive drive pulses therefrom. The drive pulses are developed at the output of the flip-flop stage **60** of the beat dividers. When the second stage of the flip-flop **60** is in the saturated mode of operation, substantially no drive pulse is delivered to the non-conductive transistor of the group of transistors **100**, **102**, **104** and **106**. On the other hand, when the second stage of flip-flop circuit **60** is rendered non-conductive, a positive pulse is applied to the circuit point **98***a* to drive the non-conductive transistor of the group **100**, **102**, **104**, and **106** into the saturated mode of operation thereby placing all of the transistors in the group in the saturated mode. Therefore, the transistor being rendered conductive produces an output pulse through the resistor capacitor coupling network between each of the transistor stages, and the following stage, which is one of the transistors of the second group, is rendered conductive. That is, when the voltage on the circuit points **98***a* and **99***a* causes a previously cut off transistor to be rendered conductive, the drop in collector voltage, applied through the resistor capacitor coupling network to the base of the succeeding saturated transistor, will cause this transistor to be cut off. As the voltage on the circuit point **99***a* is removed due to the saturated condition of the first stage of flip-flop circuit **60**, the stage which is rendered non-conductive remains non-conductive and holds the other transistors in the group in the saturated mode of operation.

The non-conductive mode of operation is then shifted from one transistor to another and from one group to another as the output of flip-flop circuit **60** changes state. That is, the stage in each group of transistors of the ring counter becomes non-conductive in turn in response to the successive output pulses of the flip-flop circuit **60**. During the time each of the transistors is non-conductive, the voltage on the collector electrode thereof goes positive while the voltage developed at the base electrode thereof goes negative. Therefore, either of the voltages developed at each of the transistor stages of the ring counter can be used as an output pulse.

In each of the resistor capacitor coupling networks between the successive transistors of the ring counter, the resistor functions as a voltage divider with the resistance networks connected to the base of the preceding stage such that the voltage swing at the base is a fraction of the voltage swing of the collector. The collector voltage swing is thus allowed to be several times the maximum base emitter reverse voltage rating which is quite small in some transistors. This circuit arrangement allows the voltage at the collector electrode to rise sharply when the transistor is cut off. This action drives the other transistors in the group more quickly into the saturated mode of operation and reduces the possibility of spurious operation.

The number of stages in the ring counter can be increased or decreased by changing the number of stages in each group. Also, the ring counter can be arranged such that all but one of the transistors is in the saturated mode.

The output of transistor **100** is connected to a terminal T_6 and to a pulse amplifier **170** which, in turn, is connected to a terminal T_7. The transistor **101** is connected to a terminal T_8 and to a pulse amplifier **171** which, in turn, is connected to a terminal T_9. The transistor **102** is connected to a terminal T_{10} and to a pulse amplifier **172** which, in turn, is connected to a terminal T_{11}. The transistor **103** is connected to a terminal T_{12} and to a pulse amplifier **173** which, in turn, is connected to a terminal T_{13}. Similarly, transistors **104**, **105**, **106** and **107** are connected to terminal T_{14}, T_{16}, T_{18}, and T_{20} and to pulse amplifiers **174**, **176**, **177** and **178** respectively. The pulse amplifiers **174**, **176**, **177** and **178** are connected to output terminals T_{15}, T_{17}, T_{19} and T_{21} respectively. At each of the output terminals represented by a square, there is produced a gating pulse while at each of the output terminals represented by a circle there is produced a pulse signal output. The terminals T_6–T_{21} are arranged for direct current coupling to one or more matrices of the matrix assembly **23**, shown in FIG. 1. Also, each of the pulse amplifiers **170**, **171**, **172**, **173**, **174**, **176**, **177** and **178** is constructed and operate in substantially the same manner as the pulse amplifier **50** connected to the tempo oscillator **40**.

The output of the last transistor **107** of the ring counter is connected to the base electrode of transistor **102** through a line **179**, a capacitor **180**, the switch **21**, shown in FIG. 1, and a resistor **181**. When the switch **21** is in the closed position, connecting resistor **181** to capacitor **180**, the feedback of transistor **107** is coupled to transistor **102** rather than to transistor **100** thereby decreasing the numerical size of the ring

counter from eight stages to six stages. This feature enables the time-point generator of the present invention to produce both 4/4 4 time pulses and three-fourths time pulses necessary for musical arrangements by using the same electronic circuitry.

The output of the last transistor **107** of the ring counter is also coupled to the input of a series of flip-flop circuits **182**, **183**, and **184**. The flip-flop circuits **182–184** are constructed in substantially the same manner as flip-flop circuit **58** and operate similarly thereto.

The first stage of flip-flop circuit **182** is direct current coupled to a terminal T_{22} and to the base of two transistors **186** and **187** through resistors **188** and **189** respectively. The transistors **186** and **187** form NAND gate circuits. The output of the second stage of the flip-flop circuit **182** is connected to a terminal T_{23}.

The first stage of the flip-flop circuit **183** is direct current coupled to transistor **186** through a resistor **190** and to transistor **187** through a resistor **191**. The second stage of the flip-flop circuit **183** is capacitively coupled to the input of flip-flop circuit **184**. The first stage of flip-flop circuit **184** is direct current coupled to transistor **187** through a resistor **192**.

The output of transistor **187** is direct current coupled to the base electrode of a transistor **193** through a resistor **194**. The transistors **186**, **187**, and **193** are connected to a positive voltage source through load resistors **196**, **197**, and **198** respectively. The pulse or gate voltage developed at the load resistors is applied to terminals T_{24}, T_{25}, and T_{26}. The output pulse developed at terminal T_{26} will be opposite that developed at terminal T_{25} due to the circuit arrangement of transistors **187** and **193**. When transistor **187** is in the saturated mode of operation, transistor **193** is cut off thereby producing a positive pulse at terminal T_{26}. On the other hand, when transistor **187** is cut off, bias is applied to transistor **193** sufficient to cause the transistor to be saturated and thereby applying ground potential or negative gate pulse to terminal T_{26}.

The output of the second stage of the flip-flop circuit **182** and the output of the first stages of flip-flop circuits **183** and **184** are connected to a switching circuit **199** through diodes **200**, **201**, and **202**. The switching circuit **199** includes a transistor **203** which has its emitter electrode connected to ground potential and the base electrode thereof connected to a positive voltage source through a resistor **204**. The collector electrode of transistor **203** is connected to the positive voltage source through a load resistor **206**. A capacitor **207** is connected across the bias resistor **204**. The base electrode of transistor **203** is connected to the reset switch **24**, of FIG. **1**, through a resistor **208**.

Closing the switch **24** resets the flip-flop stages **182–184** which form the bar counters.

The bar counter formed by the three flip-flops **182–184** has a total count capacity of eight which is a musically correct bar structure. Each time the ring counter produces an output pulse at the last stage thereof it triggers the first flip-flop stage **182** of the bar counter. Flip-flop circuits **183** and **184** follow the first stage **182** and accumulate a total of eight different states of operation. In this way the bar counter keeps track of the number of cycles through which the ring counter passes up to eight cycles and then repeats the operation. The output of the bar counter is described by the NAND gates connected thereto to produce positive gate pulses during every second, fourth, and eighth bar. These gates are used to effect electrical changes in the matrix assembly **23**, of FIG. **1**, to introduce pattern changes during every second, fourth and eighth bar.

Since a musical flourish usually occurs during the eighth bar, the bar counter is reset to the seventh bar position. This is accomplished by pulling the appropriate collectors of the flip-flop circuits **182**, **183**, and **184** down through diodes **200**, **201**, and **202** to force the bar counter to assume the seventh bar position. The operation of the reset drive for the flip-flop circuits **182–184** is further explained in the parent application.

A transistor **210** is connected to the last transistor **107** of the ring counter through a resistor **211**. The transistor **210** is connected to a transistor **212** and to a lamp **213**. The transistor **210** and **212** and lamp **213** form an indicating circuit which produces a visual light pulse during predetermined time intervals. The light pulse is used as a downbeat indicator for the person who is using the rhythm sound device for accompaniment. Transistors **210** and **212** are arranged in a Darlington configuration to develop a high gain.

Although the preferred embodiments of the present invention have been disclosed herein in detail, it will be understood that variations and modifications may be effected without departing from the spirit and scope of the novel concepts of this invention.

I claim:

1. A ring counter for counting successive pulse signals, comprising:

a. at least three stages connected in a ring, each of said stages comprising:

1. a single bipolar transistor, said transistor being the sole active element in said stage,
2. a set of resistors connecting the collector of said transistor to the bases of the transistors of the other stages,
3. a reactive coupling from the collector of said transistor to the base of the succeeding transistor,
4. a resistive load connected to the collector of said transistor and adapted to be connected to a source of potential, and
5. the emitter of said transistor being connected to a voltage reference,

whereby all but one of the transistors remains conductive; and

b. input terminal means coupled to the bases of said transistors for receiving the pulse signals, said one transistor when nonconductive being always rendered conductive in response to the next one of said pulse signals, and the following transistor being thereby rendered nonconductive so that one count is obtained each time that any of said stages becomes nonconductive; and

c. output terminal means coupled to at least one of said stages.

2. A ring counter for counting successive pulse signals, comprising:

a. an even number of at least four stages connected in a ring, alternate ones of the successive stages comprising a first group and the other stages com-

prising a second group, each of said stages comprising:

1. a single bipolar transistor, said transistor being the sole active element in said stage,
2. a set of resistors connecting the collector of said transistor to the bases of the transistors of the other stages in the same group,
3. a reactive coupling from the collector of said transistor to the base of the succeeding transistor in the other group,
4. a resistive load connected to the collector of said transistor and adapted to be connected to a source of potential, and
5. the emitter of said transistor being connected to a voltage reference, whereby all but one of the transistors remains conductive; and

b. two input terminal means coupled to the bases of said transistors for receiving the pulse signals, said one transistor when nonconductive being always rendered conductive in response to the next one of said pulse signals, and the following transistor being thereby rendered nonconductive so that one count is obtained each time that any of said stages becomes nonconductive; and

c. output terminal means coupled to at least one of said stages.

3. A ring counter according to claim 2 wherein the total number of transistors in the ring counter is eight and the total count capacity is eight, and further including circuit means connected between the last of said transistors and the third transistor for changing the count capacity from eight to six.

* * * * *