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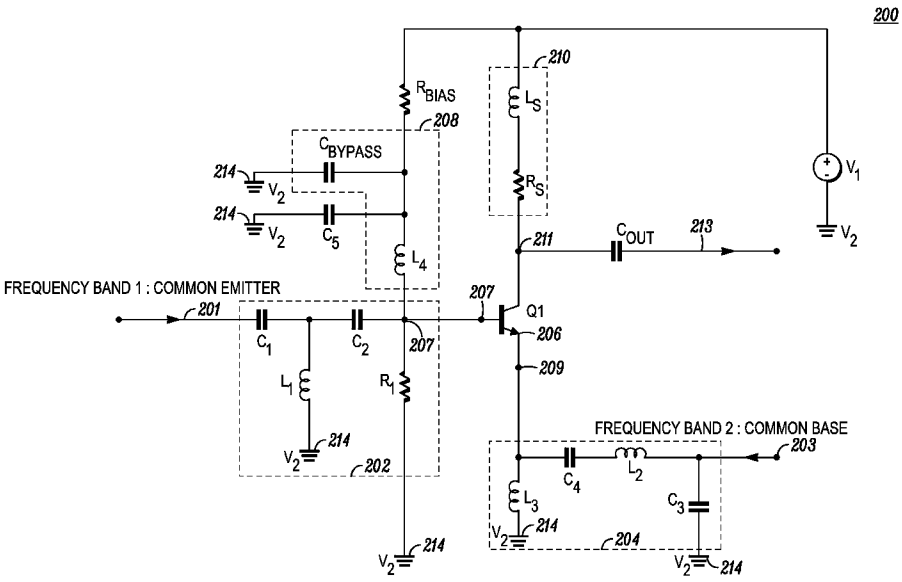
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(54) **Title:** DUAL INPUT LOW NOISE AMPLIFIER FOR MULTI-BAND OPERATION



(57) **Abstract:** A dual input low noise amplifier (LNA) for multi-band frequency operation is disclosed. The dual input LNA simultaneously operates in two amplifier configurations for the two inputs (201 and 203), of a first frequency band and a second frequency band, to produce a common output (213). Matching networks (202 and 204) receive and pass the inputs (201 and 203) to a transistor device (Ql). The transistor device is coupled to a series resonant circuit (208) at a first input node (207) to ground AC signal energy from the second input node (209) of the transistor device. The grounding causes the transistor device to simultaneously amplify and combine the signals at the first and the second input nodes to produce the common output of the first frequency band and the second frequency band at a common output node (213) of the transistor device.

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DUAL INPUT LOW NOISE AMPLIFIER FOR MULTI-BAND OPERATION

Field of the Invention

[0001] The present invention generally relates to low noise amplifiers (LNAs), and more specifically to a dual input LNA for multi-band frequency operation.

Background

[0002] Low noise amplifiers (LNAs) are widely used in front-end receivers in various wireless communication devices. These LNA devices are used for boosting power of received signals without introducing significant noise or distortion on the received signals. LNAs are variously coupled to other front-end receiver components, such as antennas, preselectors, mixers and switching networks, in different configurations for different receiver architectures. The use and topology of LNAs, and the receiver architecture within which the LNAs are integrated, vary for various communication devices, such as two-way radios, mobile radios and cell phones.

[0003] The ability for communication devices to communicate over several frequency bands is becoming increasingly prevalent. Present multi-band receivers utilize band select switches, in conjunction with LNAs and preselectors, to select a signal of particular frequency band for demodulation. Some receivers support as many as five bands (VHF, UHF1, UHF2, 700MHz and 800 MHz) which can result in excessive loss due to the required switching. These losses can degrade receiver sensitivity and may result in intermodulation distortion. Furthermore, the receivers utilizing band select switches cannot be used to simultaneously demodulate signals of different frequency bands. Parts count, board area, power

consumption, controller and logic complexity, and cost also present challenges when designing multi-band receivers.

[0004] Approaches have been suggested to overcome the utilization of band select switches. A resistive combiner may be used instead of switches to combine signals of different frequency bands from LNAs. While the resistive combiner reduces the logic complexity, it also results in front-end insertion loss and receiver sensitivity degradation. Additionally, using the resistive combiner, instead of a band select switch, does not significantly reduce the parts count or board area of a communication device.

[0005] Accordingly, it would be desirable to have an LNA capable of providing multi-band frequency operation without the aforementioned issues.

Brief Description of the Figures

[0006] The accompanying figures, where like reference numerals refer to identical or functionally similar elements throughout the separate views and which together with the detailed description below are incorporated in and form part of the specification, serve to further illustrate various embodiments and to explain various principles and advantages all in accordance with the present invention.

[0007] FIG. 1 is a block diagram illustrating a dual input low noise amplifier (LNA) in accordance with some embodiments of the invention;

[0008] FIG. 2 is a circuit schematic diagram illustrating the dual input LNA combiner in accordance with some embodiments of the invention;

[0009] FIG. 3 is a flow chart of method for operating the dual input LNA in accordance with some embodiments of the invention;

[0010] FIG. 4 is a block diagram illustrating a front-end receiver utilizing the dual input LNA in accordance with some embodiments of the invention;

[0011] FIG. 5 is an example of a graph of simulated noise factor for the dual input LNA in accordance with some embodiments of the invention;

[0012] FIG. 6 is an example of a graph of simulated isolation values between ports of the dual input LNA in accordance with some embodiments of the invention;

[0013] FIG. 7 is an example of a graph of simulated return loss values for ports of the dual input LNA in accordance with some embodiments of the invention; and

[0014] FIG. 8 is an example of a graph of simulated gain values for different amplifier configurations of the dual input LNA in accordance with some embodiments of the invention.

[0015] Skilled artisans will appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description

[0016] Before describing in detail embodiments that are in accordance with the present invention, it should be observed that the embodiments reside primarily in a dual input Low noise amplifier (LNA) for amplifying and switchlessly

combining signals of different frequency band. The dual input LNA of the present invention provides a dual-band signal which can be utilized in a demodulator block for a multi-band receiver. Accordingly, the system and method components have been represented where appropriate by conventional symbols in the drawings, showing only those specific details that are pertinent to understanding the embodiments of the present invention so as not to obscure the disclosure with details that will be readily apparent to those of ordinary skill in the art having the benefit of the description herein.

[0017] In this document, relational terms such as first and second, top and bottom, and the like may be used solely to distinguish one entity or action from another entity or action without necessarily requiring or implying any actual such relationship or order between such entities or actions. The terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus. An element proceeded by “comprises …a” does not, without more constraints, preclude the existence of additional identical elements in the process, method, article, or apparatus that comprises the element.

[0018] Briefly, in accordance with the present invention, there is provided herein a dual input LNA for amplifying and switchlessly combining signals of different frequency band. The dual input LNA formed in accordance with the present invention includes a transistor device, wherein two input nodes of the transistor device receive input signals of different frequency bands. A series resonant circuit is coupled to one of the input nodes for grounding alternate current (AC) signal energy from the frequency band received at the other input node. Consequently, a dual, simultaneous amplifier configuration is realized and the transistor device simultaneously amplifies the received input signals and provides a common dual-

band output at a third node, also referred to as a common output node, of the transistor device. The common dual-band output signal eliminates the requirement for switching between signals of different frequency bands for demodulation. Furthermore, a method and receiver utilizing the dual input LNA are provided.

[0019] FIG. 1 is a block diagram illustrating a dual input LNA 100 in accordance with some embodiments of the invention. The dual input LNA 100 is preferably incorporated within a multi-band receiver (not shown). A first signal 101 of a first frequency band and a second signal 103 of second frequency band, such as RF signals of different frequency bands, provide inputs for the dual input LNA 100. The dual input LNA 100 provides an output signal 113 of the first frequency band and the second frequency band as a common output to a demodulator block for a multi-band receiver. Hence, the dual input LNA 100 may be incorporated within the multi-band receiver to simultaneously amplify and combine the first signal 101 and the second signal 103 thereby eliminating the need for a band select switch.

[0020] The dual input LNA 100 includes a first circuit henceforth referred to as first matching network 102, a second circuit henceforth referred to as second matching network 104, a transistor device 106, , and a series resonant circuit 108. At the input for the dual input LNA, the first signal 101 is provided to the first matching network 102 and simultaneously, the second signal 103 is provided to the second matching network 104. The first matching network 102 is coupled to a first node 107 of the transistor device 106 and the second matching network 104 is coupled to a second node 109 of the transistor device 106. The series resonant circuit is coupled to the first node 107 of the transistor device 106. The output signal 113 is an output at a third node 111 (also referred to as a common output node) of the transistor device 106. The dual input LNA 100 further comprises series resistor inductor (RL) circuit 110 (also referred to as a broadband biasing

circuit), and an output capacitor C_{OUT}. The series RL circuit 110 is coupled to the third node 111. The output capacitor is also coupled to the third node 111 thereby providing the output signal 113 at the common output of the dual input LNA 100.

[0021] Operationally, the first matching network 102 is configured for receiving and passing the first signal 101 to the first node 107 of the transistor device 106. The second matching network 104 is configured for receiving and passing the second signal 103 to the second node 109 of the transistor device 106. The first and the second matching networks, 102 and 104, are configured to simultaneously provide an input impedance match and an optimum noise match for the inputs of the first and the second frequency bands respectively. As a result of the input impedance matching and optimal noise match by the matching networks, the desired return loss, isolation, and noise figure values are obtained at the first and the second nodes, 107 and 109. A more detailed discussion of the return loss, isolation, and noise figure values is provided in the discussion of FIGs 5 through 8.

[0022] Hence, the first signal 101 is received at the first node 107 and the second signal 103 is received at the second node 109. Subsequently, a portion of the alternating current (AC) signal energy of the second signal 103 of the second frequency band is passed to the first node 107. The series resonant circuit 108 which is coupled between first node 107 of the transistor device 106 and an AC ground 114 is configured to have resonant frequency within the second frequency band. As a result, the first node of the transistor is tied to a common power rail, or in other words the AC ground 114. The series resonant circuit 108 effectively and exclusively grounds alternating current (AC) signal energy of the second frequency band at the first node 107.

[0023] The first signal 101 is amplified as the transistor device 106 operates as a transistor amplifier with a common node configuration for the input at the first node 107. The transistor device 106 is designed to simultaneously operate as

a transistor amplifier with a common node configuration for the input at the second node 109. Amplified output signals for the two common node configurations appear at the third node 111 of the transistor device 106 and thus, are combined to form the output signal 113 of the first and the second frequency band. Hence, the transistor device 106 operates as a switchless device which simultaneously amplifies and combines inputs at the first node and the second node to produce the output signal 113.

[0024] Furthermore the series RL circuit 110 is coupled between a DC biasing source V_1 to provide a resistive load at the third node 111. Hence the series RL circuit 110 results in stable output impedance over a wide frequency range for the output signal 113. The output capacitor C_{OUT} blocks the direct current (DC) component of the output signal 113 and provides the output signal 113 at the common output of the dual input LNA.

[0025] In the described embodiments, the matching networks 102 and 104 may be circuits with capacitors, resistors and inductors designed to provide the input impedance match for particular frequency bands. In the described embodiments, the series resonant circuit 108 may be a series inductor capacitor (LC) resonant circuit configured to have a resonant frequency within the second frequency band. Similarly, the transistor device 106 may be a bipolar junction device (BJT) or a field effect transistor (FET). Additionally, the transistor device 106 may be an N-type (NPN or NMOS) device or a P-type (PNP or PMOS) device. The potential for DC biasing sources V_1 and V_2 depends upon the type (a N-type or a P-type) of the transistor device used.

[0026] FIG. 2 is a circuit schematic diagram illustrating the dual input LNA in accordance with some embodiments of the invention. In the illustrated embodiment of the dual input LNA 200, a transistor device 206 is an NPN device Q1 with a base 207, an emitter 209, and a collector 211. A first matching network 202 is provided which includes capacitors C_1 and C_2, an inductor L_1, and a resistor

R_1. The capacitors C_1 and C_2, the inductor L_1 and resistor R_1 are variously coupled and designed to provide input impedance match and optimum noise match for a first input 201 of the first frequency band. Similarly, a second matching network 204 is provided which includes capacitors C_3 and C_4, inductors L_3, and L_4. The capacitors C_3 and C_4, and the inductors L_3 and L_4 are variously coupled and designed to provide input impedance match and optimum noise match for a second input 203 of the second frequency band. A series resonant circuit 208 is also provided which includes a capacitor C_{BYPASS} and an inductor L_4 series connected between the base and an AC ground 214. The dual input LNA 200 also includes the series RL circuit 210 (a resistor R_S and an inductor L_S), a biasing resistor R_{BIAS}, the output capacitor C_{OUT}, a bypass capacitor C_5 and the DC biasing sources V_1 and V_2 (V_2 being 0 volts for NPN).

[0027] Operationally, the first matching network 202 provides the first input 201 to the base 207 of Q_1 and simultaneously, the second matching network 204 provides the second input 203 to the emitter 209 of Q_1. The series resonant circuit 208 AC grounds the base as the resonant frequency of the series connected L_4 and C_{BYPASS} is within the second frequency band. As a result, the first input 201 sees a common emitter configuration, and the second input 203 sees a common base configuration. Both common emitter and common base configurations operate simultaneously to provide a common output 213 at the collector 211. Hence, Q_1 operates as a common emitter amplifier for the first input 201 at the base 207 and as a common base amplifier for the second input 203 at the emitter 209 causing Q_1 to produce the common output 213 at the collector.

[0028] Operationally, the dual input LNA 200 includes the series RL circuit 210 (R_S and L_S) which is used as a resistive load for equalizing the output impedance versus frequency at the collector and providing a stable gain over a wide range of frequencies. For instance, in a case where the inputs are in the Very High Frequency (VHF) band of 150 - 200 MHz and Radio Frequency band of

around 800 MHz, the series RL circuit 210 is ideally designed to provide stable output impedance over a range from 50 MHz to 900 MHz.

[0029] Operationally, the dual input LNA 200 further includes a large resistor R_{BIAS} for providing a drive current for Q_1 at the base 207. Due to the high resistor value, R_{BIAS} does not have any impact on the series resonant circuit 208. Further, C_5 is used for grounding AC signal energy of the spurious frequency components at the base for optimizing the linearity of the dual input LNA 200.

[0030] According to some of the other embodiments, the dual input LNA may include a FET with a gate, a drain and a source. For the FET, the gate provides the first input and the source provides the second input. The series resonant circuit AC grounds the gate and as a result, the first input sees a common source configuration and the second input sees a common gate configuration. Both common source and common gate configurations operate simultaneously to provide a common output at the drain. Additionally, the RL circuit is coupled to the drain. Hence, the FET operates as a common source amplifier for the first signal at the gate and as a common gate amplifier for the second signal at the source causing the FET to produce the output signal at the drain. Hence, the FET operates as a switchless device which simultaneously amplifies and combines inputs at the gate and the source to produce the common output at the drain.

[0031] FIG. 3 is a flow chart of operating the dual input LNA 100 in accordance with some embodiments of the invention. The method 300 is initialized in simultaneous steps 301 and 302. Step 301 includes receiving and passing the first signal of the first frequency band to the first node of the transistor device. The step of receiving and passing the first signal involves operating the first matching network in the first frequency band so as to provide input impedance matching and optimum noise matching across the first frequency band. Simultaneously, step 302 includes receiving and passing the second signal of a second frequency band to a second node of the transistor device. The step of

receiving and passing the second signal involves simultaneously operating the second matching network in the second frequency band so as to provide input impedance matching and optimum noise matching across the second frequency band.

[0032] Subsequent to receiving and passing the first and the second signals, step 303 includes grounding AC signal energy of the second frequency band at the first node. The step 303 of grounding the AC signal energy of the second frequency band involves resonating the series resonant circuit at the resonant frequency within the second frequency band. Hence, the transistor device is configured to simultaneously operate in the common node amplifier configurations at the first and the second nodes. As a result of the step 303, in step 304, the method 300 includes simultaneously amplifying and combining the first signal and the second signal to produce an output signal of the first frequency band and the second frequency band at the common output node of the transistor device. The step 304 of simultaneously amplifying and combining involves switchlessly combining and amplifying the inputs at the first node and the second node to produce the output signal at the common output node. Additionally, the method 300 may also include a step of bypassing the undesired low frequency products resulting from driving multiple RF signals into a non-linear device for linearizing gain of the dual input LNA 100.

[0033] FIG. 4 is a block diagram illustrating a front-end receiver 400 utilizing the dual input LNA in accordance with some embodiments of the invention. The front-end receiver 400 includes preselector blocks 410 for bandlimiting the received signal. In the illustrated embodiment, two separate preselector blocks 410 provide two filtered signals of different frequency bands, typically RF signals, to the dual input LNA 420. The dual input LNA 420 is used for amplifying and switchlessly combining two filtered signals 417 and 419 received from the preselector blocks 410 to provide a dual-band output signal 421 to a demodulator

block 440. The demodulator block 440 down converts and subsequently digitizes dual-band signal 421 to provide an output 445 for digital demodulation (not shown).

[0034] An antenna 402 receives RF signals and passes these signals to a DIPLEXR block 404. The DIPLEXR block 404 subsequently passes signals 403 and 405 to the two separate preselector blocks 410. Each of the preselector blocks 410 filters the signals 403 and 405 using at least one filtering stage 406 designed for a different frequency band. As illustrated, each of the separate preselector blocks 410 may use several identical filtering stages 406 cascaded in series to remove the spurious frequency components and imaging effects from the signals 403 and 405.

[0035] Subsequently, the dual input LNA 420 simultaneously amplifies and combines the filtered signals 417 and 419 to provide the dual-band signal 421. The use of the dual input LNA 420 eliminates the requirement for a band select switch 430 currently used in the multi-band receivers. The dual-band signal 421 is provided to the demodulator block 440. In the demodulator block 440, the signal 421 is down converted to an intermediate frequency (IF) by the mixer 422 and is subsequently bandlimited to the IF band and amplified using a bandpass filter 424 and an amplifier 426. The signal 427 is subsequently digitized using a digitizer block 428 and the digitized output 445 is provided to the digital demodulation block (not shown).

[0036] According to some of the embodiments, each of the filtering stages 406 may comprise a bandpass filter 408 for bandlimiting the signals 405 and 403 to a particular frequency band. In some of the other embodiments, each of the filtering stages 406 may comprise at least two bandpass filters 408 cascaded in parallel for selectively switching, using switches 414, between different frequency bands. However, any combination of the above-mentioned filtering stages 406 may be used in the preselector blocks 410. For instance, in the illustrated

embodiment, the filtering stages 406 for filtering the signal 403 utilizes two parallel connected filters 408 and switches 414. Simultaneously, the filtering stage 406 for filtering the signal 405 utilizes a single filter 408.

[0037] In some of the other embodiments, the receiver may include a first preselector block generating a first filtered signal of the first frequency band from a received signal, a second preselector block generating a second filtered signal of the second frequency band from the received signal, and a dual input LNA for amplifying and switchlessly combining the first filtered signal and the second filtered signal to provide a dual-band output signal to the demodulator block.

[0038] Although not shown, several dual input LNAs may be utilized in a multi-band receiver. The multi- band receiver may include a plurality of dual input LNAs wherein each of the plurality of dual input LNAs amplifies and switchlessly combines two filtered signals received from separate preselector blocks to provide a dual-band output signal. Such multi-band receiver may also include at least one combiner which combines each of the dual-band output signals from the plurality of dual input LNAs to provide a multi-band output to the demodulator block. While combiners may be required for the multi-band receiver, the need for switching in such a multi-band receiver is reduced by half in comparison to the conventional multi-band receivers.

[0039] Further, it will be understood by a person skilled in the art that the demodulator block 440 is shown only for illustrative purposes and it may be implemented using other demodulator architectures. In some of the embodiments, a digital processor may be used to perform the task of down converting and digitizing the signal 421 from the dual input LNA 420.

[0040] Besides combining the two filtered signals in the front-end receiver, the dual input LNA is also designed to provide an optimal gain, a desired noise factor and a reduced return loss at the desired frequency bands to improve the

receiver performance. Furthermore, as different ports of a single transistor device are used for the inputs and the common output, the dual input LNA also achieves desired isolation between the input and output ports.

[0041] FIGs. 5, 6, 7 and 8 are example graphs of simulated values for the dual input LNA 200 in accordance with some embodiments of the invention. The schematic and graphs are provided as a visualization of improvement in simulated values achievable with the dual input LNA formed in accordance with some of the embodiments. In the simulation, the first signal of 800 MHz frequency band is provided at the base as an input for the common emitter configuration and the second signal of a 150 -200 MHz frequency band is provided at the emitter as an input for the common base configuration. The matching networks of the dual input LNA 200 are designed to provide input impedance match and optimum noise match for the first signal and the second signal.

[0042] FIG. 5 is an example of a graph 500 of simulated noise factor for the dual input LNA 200 in accordance with some embodiments of the invention. The graph 500 represents the noise factor in decibels (dB) (also known as noise figure) along the y-axis and the frequency of the input in MHz along the x-axis. Curve 502 illustrates simulated noise factor values over a range of frequency for the dual input LNA operating in the common emitter configuration. As illustrated, the simulated noise factor value of under 2dB is observed for the first signal of the frequency band at around 800 MHz. Hence, the simulated values indicate optimum noise match for the first matching network for the frequency band at around 800MHz.

[0043] FIG. 6 is an example of a graph 600 of simulated isolation values between ports of the dual input LNA 200 in accordance with some embodiments of the invention. The graph 600 represents the isolation in dB along the y-axis and the frequency of the input in GHz along the x-axis. As the matching networks do not introduce a significant amount of noise, the simulated isolation values for the

transistor device and the dual input LNA are identical. Hence, curves of the graph 600 show the simulated isolation values representing the amount of the signal leaking from one port of the transistor device to the other port of the transistor device over a range of input frequency.

[0044] For input ports, curve 602 represents the simulated values for isolation of the emitter (the input port for the second signal) from the base (the input port for the first signal) and curve 606 represents the simulated values for isolation of the base from the emitter. Similarly, curve 604 represents the simulated values for isolation of the base from the collector (the common output port) and curve 608 represents the simulated values for isolation of the emitter from the collector. As illustrated, the dual input LNA offers better than 20dB isolation between all ports and, specifically, better than 40dB for the input ports over the desired frequency bands of the first and the second signals. Hence, the isolation characteristics of the dual input LNA eliminate the requirement for use of isolation filters while designing the LNAs.

[0045] FIG. 7 is an example of a graph 700 of simulated return loss values for ports of the dual input LNA 200 in accordance with some embodiments of the invention. The graph 700 represents the return loss values in dB along the y-axis and the frequency of the input in GHz along the x-axis. The return loss values may be used as an indicator for the input impedance match for the first and the second matching networks as the return loss value represents the ratio of the power of the reflected signal to the power of the input signal. Hence, a low return loss value for the matching networks at a particular frequency represents good input impedance match.

[0046] Curve 702 represents the simulated return loss values for the first matching network with the input seeing the common emitter configuration at the base. Curve 702 shows a return loss of below -20 dB for the desired frequency band above 800 MHz. Similarly, curve 704 represents the simulated return loss

values for the second matching network with the input seeing the common base configuration at the emitter. Curve 704 shows a return loss of about -28 dB for the desired frequency band around 150 MHz. For the output impedance matching, curve 706 shows stable return loss values of about -10dB is observed. The stable return loss is an indicator of stable output impedance due to the resistive loading of the collector by the series RL circuit. Hence, while the return loss values for the collector are not low, the series RL circuit does provide stable output impedance at the collector over a wide frequency band.

[0047] FIG. 8 is an example of a graph 800 of simulated gain values for different amplifier configurations of the dual input LNA 200 in accordance with some embodiments of the invention. The graph 800 represents the gain values in dB along the y-axis and the frequency of the input in GHz along the x-axis. Curve 802 represents the simulated gain values for the common emitter configuration at the base and curve 804 represents the simulated gain values for the common base configuration at the emitter. The curve 802 shows maximum gain of about 10 dB for the common emitter configuration at the desired frequency band of around 800 MHz. Simultaneously, the curve 804 shows maximum gain of about 0 dB for the common base configuration at the desired frequency band of around 150 -200 MHz. Hence, the dual input LNA is configured to simultaneously operate in the two different amplifier configurations to provide the desired gain for inputs, of the desired frequency bands, at the base and the emitter.

[0048] Hence, there has been provided a dual input LNA particularly useful in the multi-band receivers. The dual input LNA of the present invention avoids the use of band select switches and thus, achieves a power efficient and robust design for the multi-band receivers. By utilizing a series resonant circuit in the dual input LNA, simultaneous amplifier configuration for two inputs is provided to produce a common output. Hence, by utilizing the dual input LNA of the present invention, the problems associated with switching are avoided. Additionally, input

impedance and optimal noise match for the two inputs is achieved. Furthermore, the use of a single transistor device in the dual input LNA significantly improves isolation between various nodes of the dual input LNA.

[0049] In the foregoing specification, specific embodiments of the present invention have been described. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention. The benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. The invention is defined solely by the appended claims including any amendments made during the pendency of this application and all equivalents of those claims as issued.

Claims

1. A dual input low noise amplifier (LNA) comprising:

a transistor device;

a first circuit configured for receiving and passing a first signal of a first frequency band to a first node (Base or Gate) of the transistor device;

a second circuit configured for receiving and passing a second signal of a second frequency band to a second node (Emitter or Source) of the transistor device; and

a series resonant circuit coupled between the first node of the transistor device and a ground thereby effectively and exclusively grounding alternating current (AC) signal energy of the second frequency band and causing the transistor device to simultaneously amplify and combine the first signal and the second signal to produce an output signal of the first frequency band and the second frequency band at a common output node of the transistor device.

2. The dual input LNA of claim 1 further comprising a series resistor inductor (RL) circuit coupled between a biasing source and the common output node of the transistor device for providing stable output impedance over a frequency range for the output signal.

3. The dual input LNA of claim 1, wherein the first circuit is a first matching network configured to provide an input impedance match and an optimum noise match for an input signal of the first frequency band and wherein the second circuit is a second matching network configured to simultaneously provide the input impedance match and the optimum noise match for an input signal of the second frequency band.

4. The dual input LNA of claim 1, wherein the series resonant circuit is a series inductor capacitor (LC) resonant circuit configured to have a resonant frequency within the second frequency band.

5. The dual input LNA of claim 4 further comprising a bypass capacitor coupled between a common node of a capacitor and an inductor in the series LC resonant circuit and the ground for optimizing linearity of the dual input LNA.

6. The dual input LNA of claim 5 further comprising a bias resistor coupled between the common node and a biasing source for providing a drive current at the first node.

7. The dual input LNA of claim 1, wherein the transistor device is one of: a bipolar junction transistor (BJT) and a field effect transistor (FET).

8. The dual input LNA of claim 1, wherein the transistor device is one of: a N-type device and a P-type device.

9. The dual input LNA of claim 7, wherein the transistor device is a switchless device which simultaneously amplifies and combines inputs at the first node and the second node to produce the output signal at the common output node.

10. The dual input LNA of claim 9, wherein the BJT operates as a common emitter amplifier for the first signal at the first node and as a common base amplifier for the second signal at the second node causing the BJT to produce the output signal at the common output node.

11. The dual input LNA of claim 9, wherein the FET operates as a common source amplifier for the first signal at the first node and as a common gate amplifier for the second signal at the second node causing the FET to produce the output signal at the common output node.

12. A method of operating a dual input low noise amplifier (LNA) comprising:

receiving and passing a first signal of a first frequency band to a first node of a transistor device;

receiving and passing a second signal of a second frequency band to a second node of the transistor device;

grounding AC signal energy of the second frequency band at the first node; and

simultaneously amplifying and combining the first signal and the second signal to produce an output signal of the first frequency band and the second frequency band at an common output node of the transistor device

13. The method of claim 12, wherein the receiving and passing the first signal further comprises operating a first circuit in the first frequency band so as to provide input impedance matching and optimum noise matching across the first frequency band and wherein the receiving and passing the second signal further comprises simultaneously operating a second circuit in the second frequency band so as to provide input impedance matching and optimum noise matching across the second frequency band.

14. The method of claim 12, wherein grounding AC signal energy of the second frequency band further comprises resonating a series resonant circuit for a resonant frequency within the second frequency band.

15. The method of claim 12, further comprising bypassing undesired frequency bands received as inputs at the first node and the second node for linearizing gain of the dual input LNA.

16. The method of claim 12, wherein the simultaneously amplifying and combining further comprises switchlessly combining and amplifying inputs at the first node and the second node to produce the output signal at the common output node.

17. A dual-band receiver including:

a dual input low noise amplifier (LNA) amplifying and switchlessly combining two filtered signals received from separate preselector blocks to provide a dual-band output signal to a demodulator block.

18. The dual-band receiver of claim 17, wherein each of the separate preselector blocks comprises at least one filtering stage providing one of the two filtered signals, each of the at least one filtering stage cascaded in series.

19. The dual-band receiver of claim 18, wherein the at least one filtering stage of at least one of the separate preselector blocks further comprises at least two filters cascaded in parallel for selectively switching to a different frequency band for the two filtered signals.

20. A dual-band receiver comprising:

a first preselector block generating a first filtered signal of a first frequency band from a received signal;

a second preselector block generating a second filtered signal of a second frequency band from the received signal; and

a dual input low noise amplifier (LNA) for amplifying and switchlessly combining the first filtered signal and the second filtered signal to provide a dual-band output signal to a demodulator block.

21. The dual-band receiver of claim 20, wherein the first and the second preselector blocks comprise at least one filtering stage providing the first and the second filtered signal, each of the at least one filtering stages cascaded in series.

22. The dual-band receiver of claim 21, wherein the at least one filtering stage of the first preselector block further comprises at least two filters cascaded in parallel for selectively switching to a different frequency band.

23. A multi-band receiver comprising:

a plurality of dual input low noise amplifiers (LNAs);

wherein each of the plurality of dual input LNAs amplifies and switchlessly combines two filtered signals received from separate preselector blocks to provide a dual-band output signal; and

wherein at least one combiner combines each of the dual-band output signals to provide a multi-band output to a demodulator block.

24. The multi-band receiver of claim 23, wherein each of the separate preselector blocks comprises at least one filtering stage providing one of the two filtered signals, each of the at least one filtering stages cascaded in series.

25. The multi-band receiver of claim 24, wherein the at least one filtering stage of at least one of the separate preselector blocks further comprises at least two filters cascaded in parallel for selectively switching to a different frequency band for the two filtered signals.

26. A low noise amplifier (LNA), comprising:

a bipolar junction device (BJT) having a base, a emitter and a collector, the base providing a first input and the emitter providing a second input;

the first input seeing a common emitter configuration;

the second input seeing a common base configuration, both common emitter and common base configurations operating simultaneously;

a series resonant circuit AC grounding the base;

a broadband biasing circuit coupled to the collector; and

a common output taken from the collector.

27. The LNA of claim 26, wherein the broadband biasing circuit comprises a series resistor inductor (RL) circuit.

28. A low noise amplifier (LNA), comprising:

a field effect transistor (FET) having a gate, a drain and a source, the gate providing a first input and the source providing a second input;

the first input seeing a common source configuration;

the second input seeing a common gate configuration, both common source and common gate configurations operating simultaneously;

a series resonant circuit AC grounding the gate;

a broadband biasing circuit coupled to the drain; and

a common output taken from the drain.

29. The LNA of claim 28, wherein the broadband biasing circuit comprises a series resistor inductor (RL) circuit.

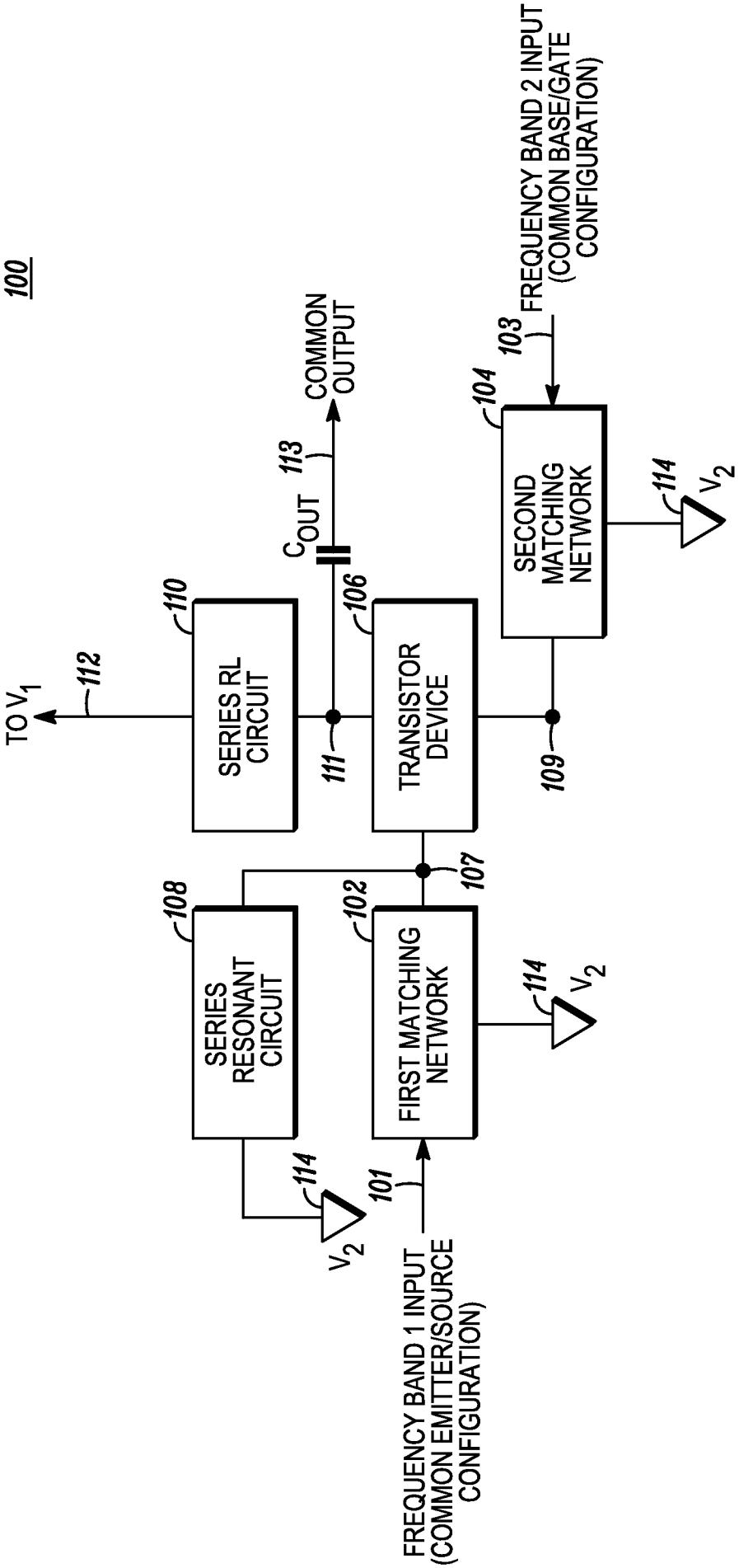

100
FREQUENCY BAND 2 INPUT (COMMON BASE/GATE CONFIGURATION)
103
104
SECOND MATCHING NETWORK
114
V_2
COMMON OUTPUT
113
C_{OUT}
110
SERIES RL CIRCUIT
106
TRANSISTOR DEVICE
TO V_1
112
111
109
107
108
SERIES RESONANT CIRCUIT
102
FIRST MATCHING NETWORK
114
V_2
114
V_2
101
FREQUENCY BAND 1 INPUT (COMMON EMITTER/SOURCE CONFIGURATION)

FIG. 1

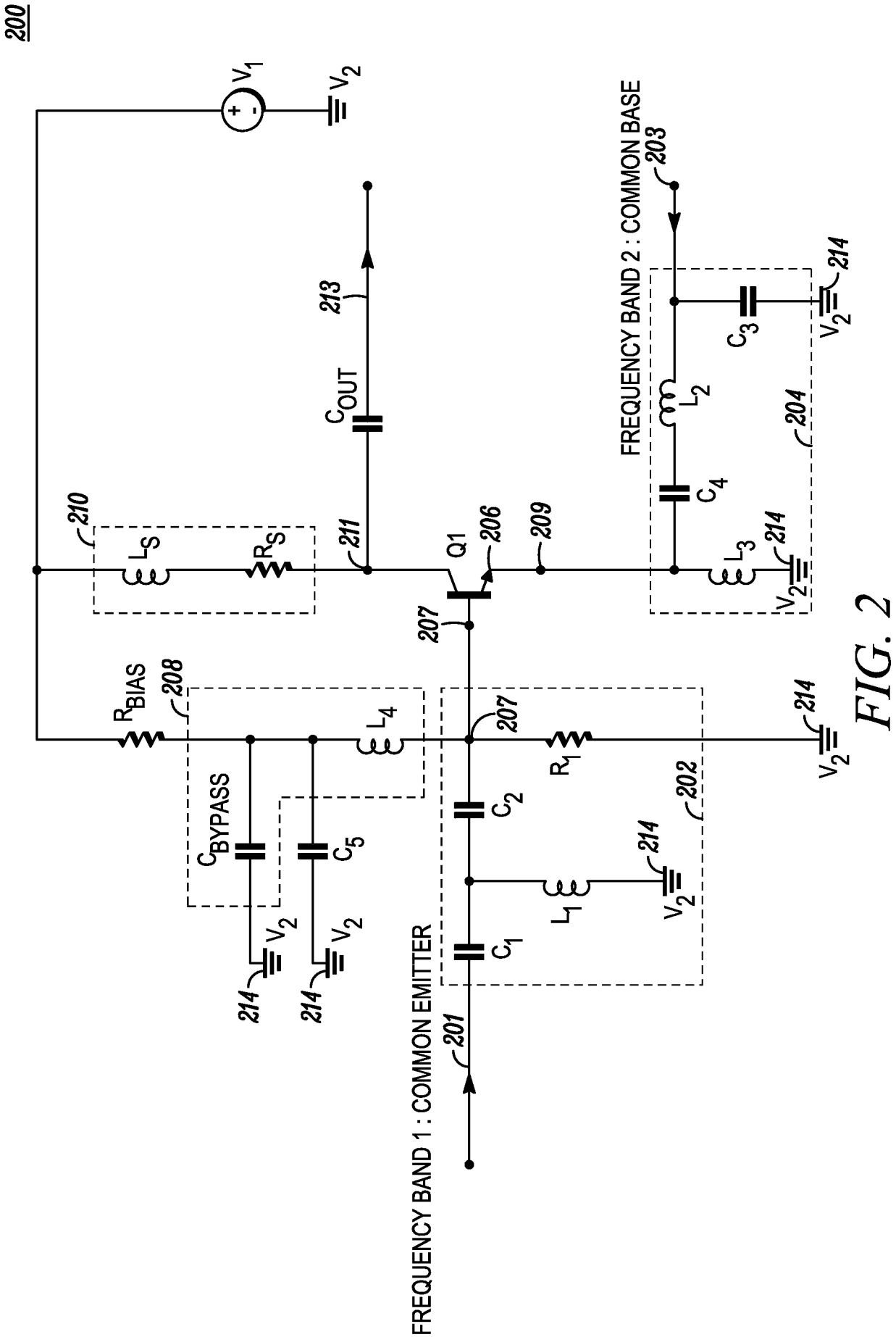

200
V1
V2
213
COUT
210
LS
RS
211
Q1
206
209
207
FREQUENCY BAND 2 : COMMON BASE
203
C3
214
L2
204
C4
L3
RBIAS
208
L4
R1
202
CBYPASS
C5
C2
L1
C1
FREQUENCY BAND 1 : COMMON EMITTER
201

FIG. 2

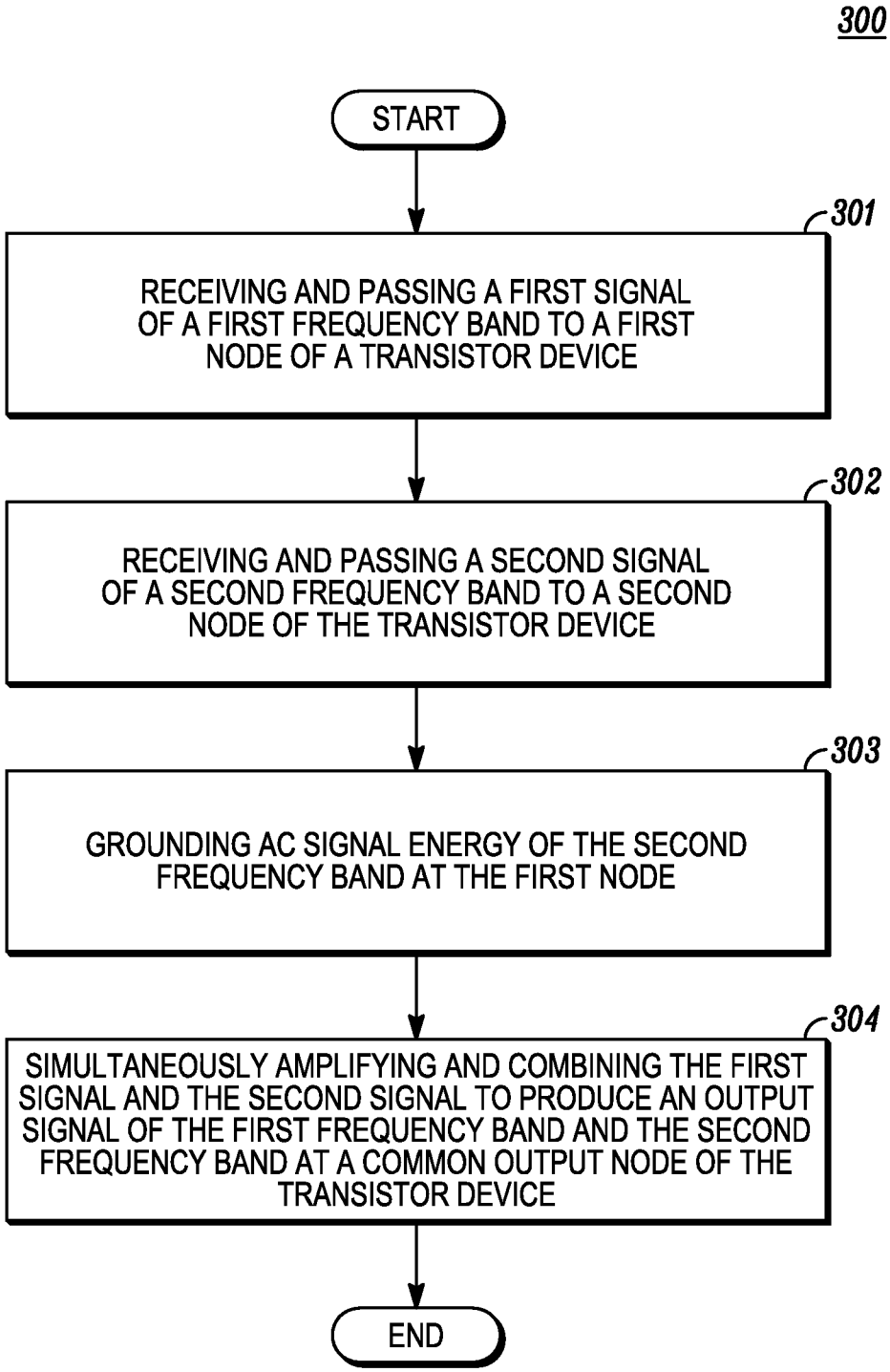

300
START
301
RECEIVING AND PASSING A FIRST SIGNAL OF A FIRST FREQUENCY BAND TO A FIRST NODE OF A TRANSISTOR DEVICE
302
RECEIVING AND PASSING A SECOND SIGNAL OF A SECOND FREQUENCY BAND TO A SECOND NODE OF THE TRANSISTOR DEVICE
303
GROUNDING AC SIGNAL ENERGY OF THE SECOND FREQUENCY BAND AT THE FIRST NODE
304
SIMULTANEOUSLY AMPLIFYING AND COMBINING THE FIRST SIGNAL AND THE SECOND SIGNAL TO PRODUCE AN OUTPUT SIGNAL OF THE FIRST FREQUENCY BAND AND THE SECOND FREQUENCY BAND AT A COMMON OUTPUT NODE OF THE TRANSISTOR DEVICE
END

FIG. 3

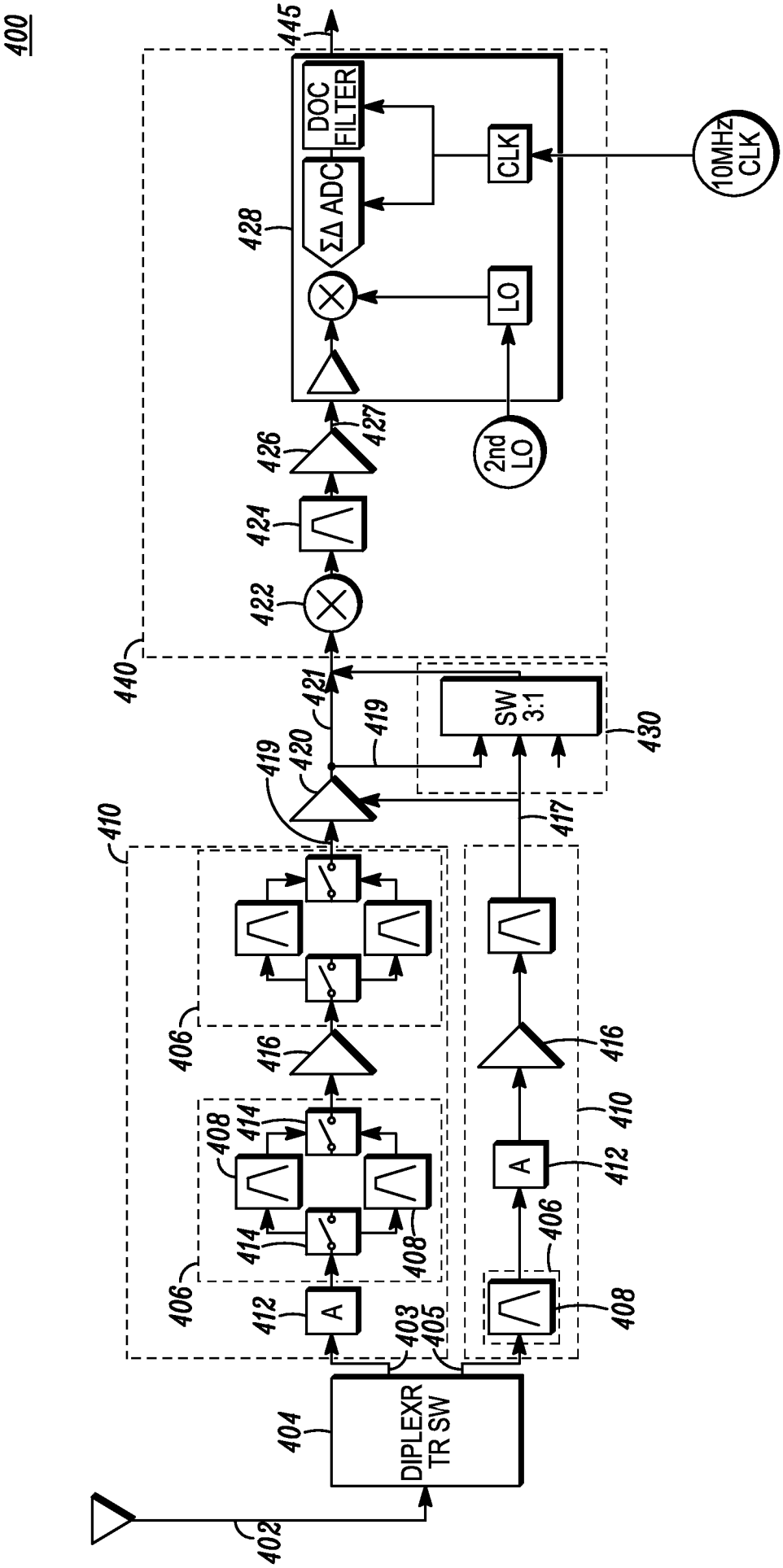

400
445
DOC FILTER
ΣΔ ADC
CLK
10MHz CLK
428
LO
2nd LO
426
427
424
422
440
421
419
420
SW 3:1
430
417
410
406
416
414
408
412
A
403
405
404
DIPLEXR TR SW
402

FIG.4

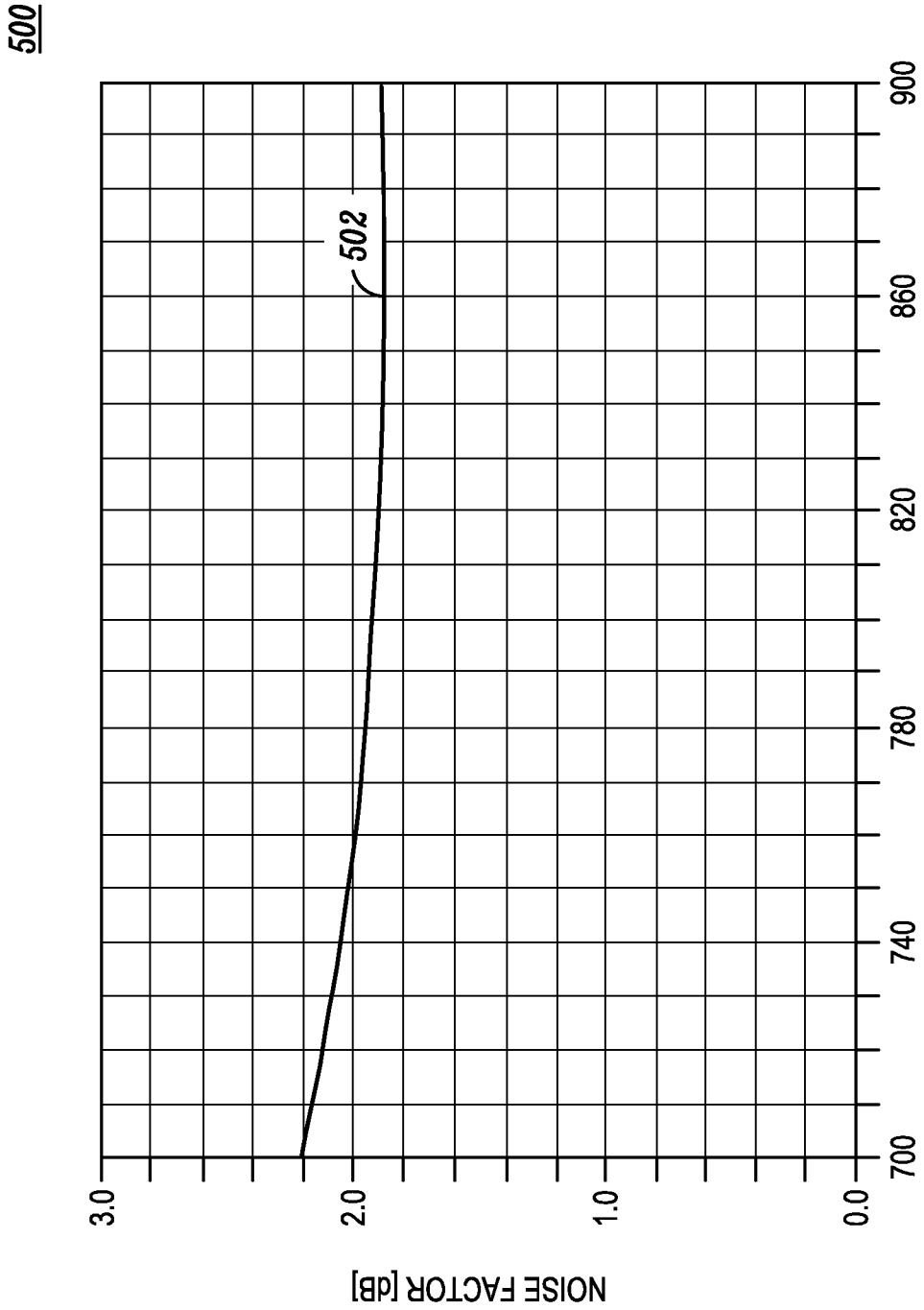


FIG. 5

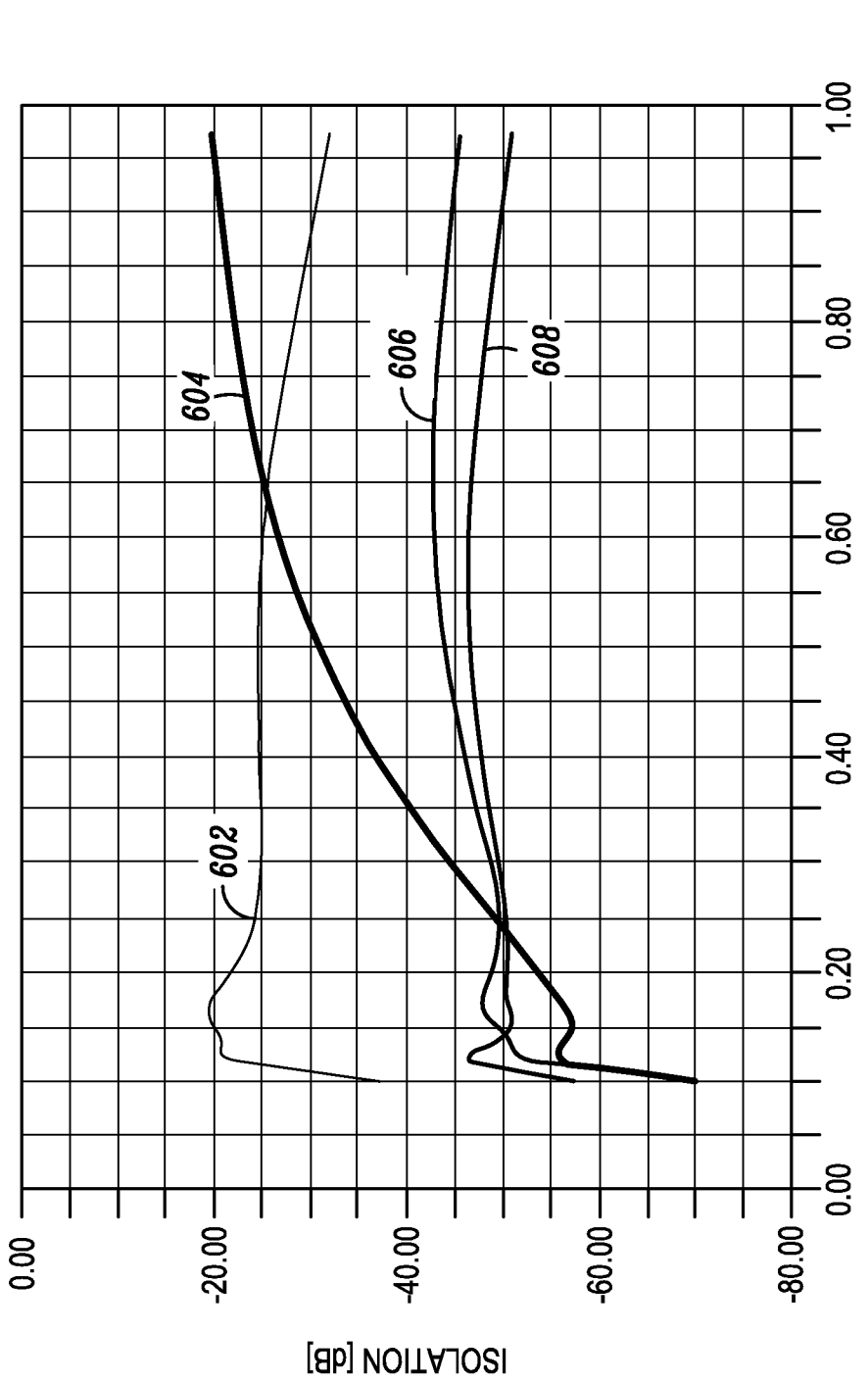

600
0.00
-20.00
-40.00
-60.00
-80.00
ISOLATION [dB]
0.00
0.20
0.40
0.60
0.80
1.00
F [GHz]
602
604
606
608

FIG. 6

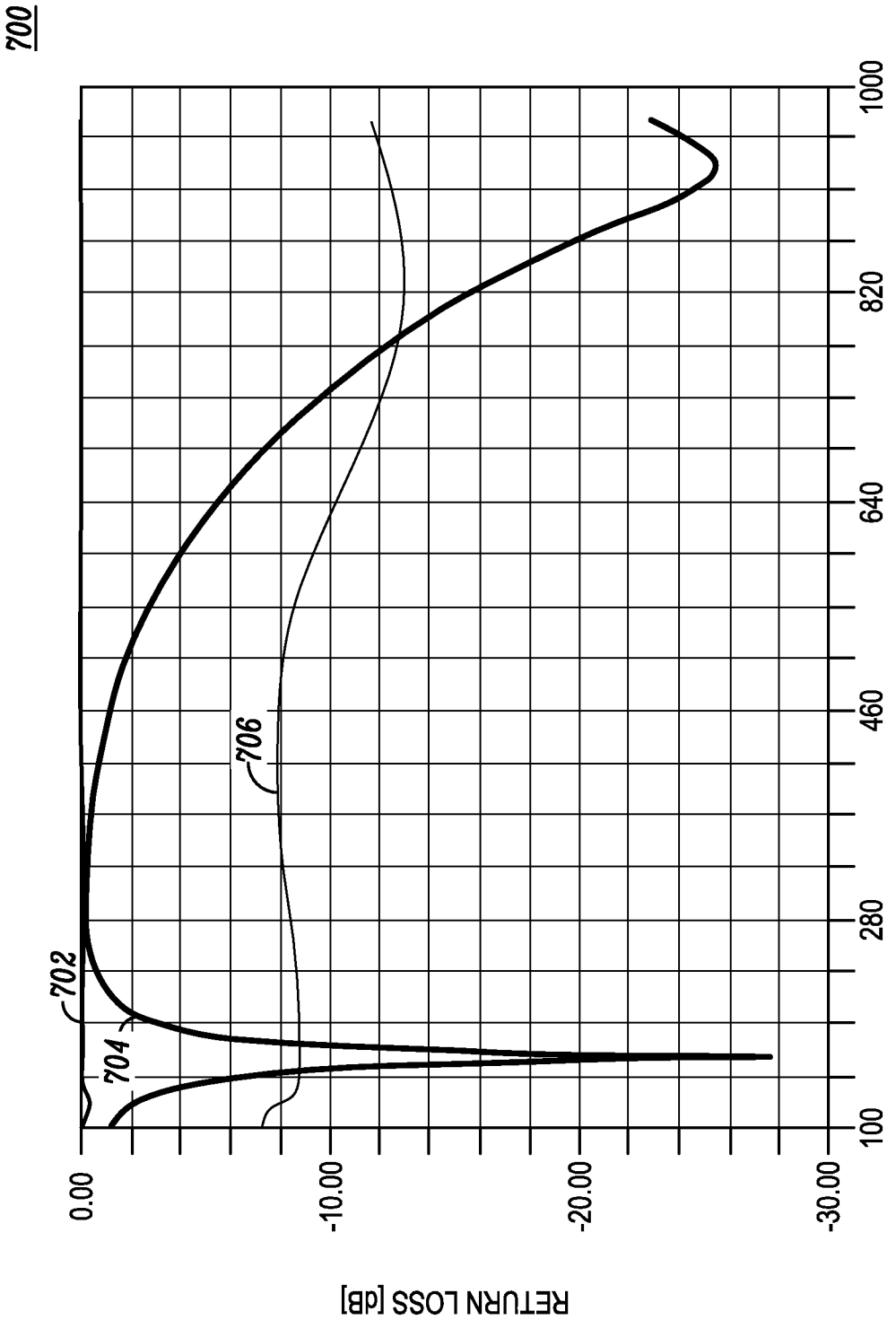

700
0.00
-10.00
-20.00
-30.00
RETURN LOSS [dB]
100
280
460
640
820
1000
F [MHz]
702
704
706

FIG. 7

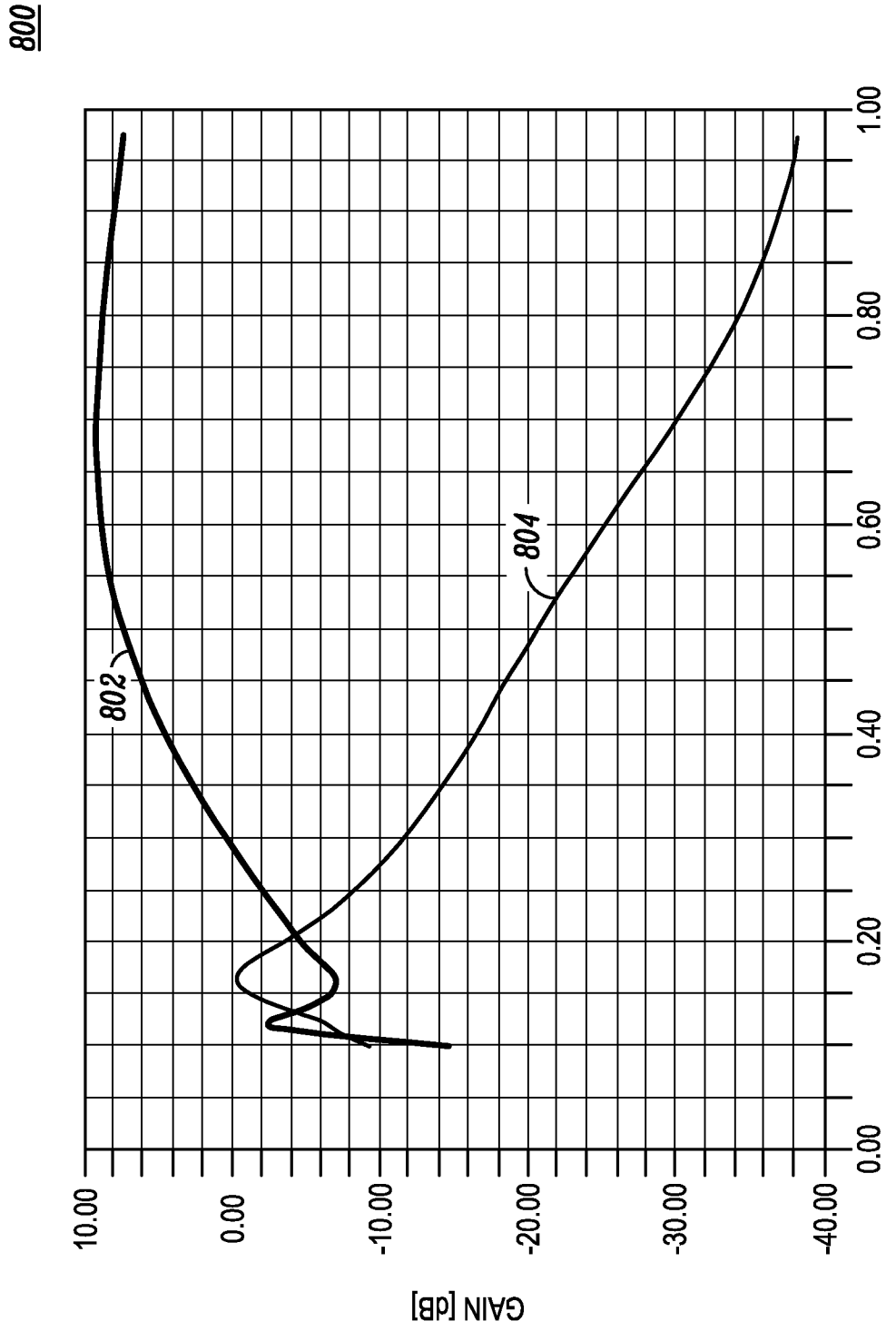

800
802
804
10.00
0.00
-10.00
-20.00
-30.00
-40.00
GAIN [dB]
0.00
0.20
0.40
0.60
0.80
1.00
F [GHz]

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/054058

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/189 H03H11/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03H H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	DE 10 99 590 B (STANDARD ELEKTRIK LORENZ AG) 16 February 1961 (1961-02-16) the whole document	1,3-21, 26,28 2,23-25, 27,29
Y	BO SHI ET AL: "A CMOS Receiver Front-End for 3.1-10.6 GHz Ultra-Wideband Radio" MICROWAVE CONFERENCE, 2006. 36TH EUROPEAN, IEEE, PI, 1 September 2006 (2006-09-01), pages 1829-1832, XP031005961 ISBN: 978-2-9600551-6-0 page 1830; figure 2	2,27,29

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 June 2008	02/07/2008

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Dietsche, Stefan

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/054058

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	SUNDERARAJAN S MOHAN ET AL: "Bandwidth Extension in CMOS with Optimized On-Chip Inductors" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 35, no. 3, 1 January 2000 (2000-01-01), XP011061203 ISSN: 0018-9200 page 347; figure 1c	2,27,29
X	US 3 727 140 A (NIETO C ET AL) 10 April 1973 (1973-04-10) column 1, line 3 - column 3, line 45; figure 1	17-22
X	DE 10 53 588 B (TELEFUNKEN GMBH) 26 March 1959 (1959-03-26) column 2, line 25 - column 4, line 9; figure 2	17-21
A	DE 18 01 843 A1 (SIEMENS AG) 4 June 1970 (1970-06-04) figure 4	20
Y	WO 2005/088849 A (QUORUM SYSTEMS INC [US]; MALONE LAWRENCE JARRETT [US]; CHRISTENSEN LON) 22 September 2005 (2005-09-22) page 11, line 5 - line 32; figure 3	23-25
Y	US 2006/012442 A1 (SHINBO JIRO [JP] ET AL) 19 January 2006 (2006-01-19) figures 6,7	23-25

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2008/054058

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers allsearchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search reportcovers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-16, 26-28

   Particular dual-input LNA with series resonant circuit connected between a first input node (base/gate of the amplifying transistor) and ground

1.1. claims: 17-25

   Multi-band receiver comprising at least one dual-input LNA for amplifying and combining filtered signals

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