



- (51) International Patent Classification:
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)
- (21) International Application Number:
PCT/US2014/057637
- (22) International Filing Date:
26 September 2014 (26.09.2014)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
61/883,158 26 September 2013 (26.09.2013) US
61/883,942 27 September 2013 (27.09.2013) US
61/887,153 4 October 2013 (04.10.2013) US
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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,

[Continued on next page]

(54) Title: ESTIMATION OF EFFECTIVE CHANNEL LENGTH FOR FINFETS AND NANO-WIRES

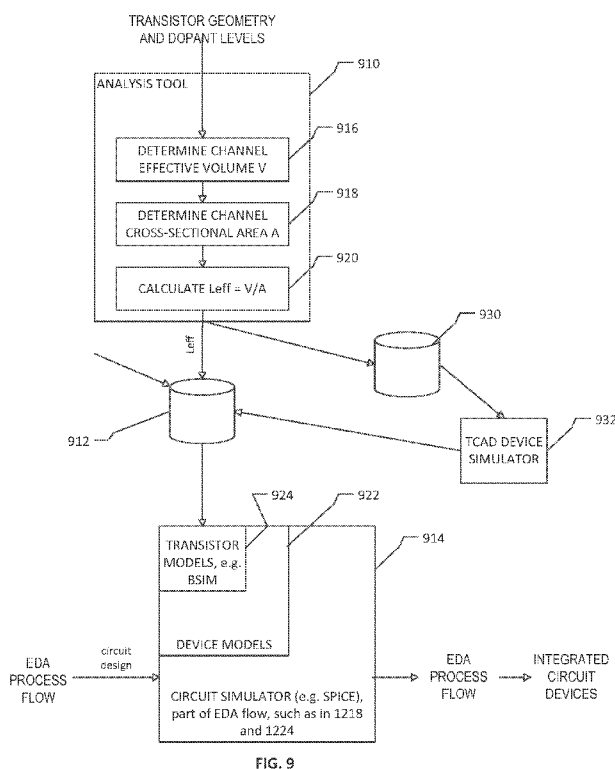


FIG. 9

(57) Abstract: Roughly described, a system for estimating an effective channel length of a 3D transistor having a gate length below 20 nm involves estimating an effective volume of the channel and a cross-sectional area of the channel, and estimating the effective channel length as the ratio of effective volume to cross-sectional area. Preferably the effective volume is estimated as the sum of the Voronoi volumes within containing boundaries of the channel, excluding those volumes having a dopant concentration above the source/drain dopant concentration at the carrier injection point. The containing boundaries can be identified using geometry data describing the transistor, particularly the data identifying inner surfaces of the gate dielectric. The estimated effective channel length can be used in TCAD level analysis of the transistor and calculating characteristics of the transistor or as needed for circuit simulation.



TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

ESTIMATION OF EFFECTIVE CHANNEL LENGTH FOR FINFETS AND NANO-WIRES

CROSS-REFERENCE TO OTHER APPLICATIONS

[0001] Applicants hereby claim the benefit under 35 U.S.C. 119(e) of the following U.S. provisional applications:

- U.S. Application No. 61/883,158, filed 26 September 2013 (Attorney Docket No. SYNPNP 2380-1);
- U.S. Application No. 61/883,942, filed 27 September, 2013 (Attorney Docket No. SYNPNP 2382-1); and
- U.S. Application No. 61/887,153, filed 04 October 2013 (Attorney Docket No. SYNPNP 2386-1).

[0002] All the above provisional applications are hereby incorporated by reference herein for their teachings.

BACKGROUND

[0003] It is desirable in many cases to have accurate estimate of the channel length for the short channel transistors like FinFETs and nano-wires. It is used to compare transistors to each other, to characterize the short channel effects, to characterize the direct source-to-drain tunneling, to model ballistic mobility, which is directly proportional to the channel length, etc. The gate length is easy to measure or extract from a geometry database, as it is defined by the gate patterning mask and subsequent deposition of the gate dielectric and the gate. However, the physical gate length is not a useful value for determining many critical characteristics of a transistor. More important is to know the effective channel length, which is defined as the average distance from source junction to drain junction. The effective channel length can be smaller than the gate length, same, or larger, depending on how transistor is built. Current practice is for engineers to take a close look at the transistor and estimate its effective channel length based on a number of factors. It is desirable to have an algorithm that can reliably

determine the effective channel length and exclude human errors and human-to-human variation due to the different "eye-balling" approaches.

SUMMARY

[0004] According to the invention, instead of direct measurement of the effective channel length, roughly described, the effective channel length for the FinFETs and nano-wires with arbitrary junction shapes is determined automatically based on integrated values such as area and volume and therefore is robust and insensitive to fluctuations in geometry and doping. Roughly described, the effective channel length of a 3D transistor having a gate length below 20 nm involves estimating an effective volume of the channel and a cross-sectional area of the channel, and estimating the effective channel length as the ratio of effective volume to cross-sectional area. Preferably the effective volume is estimated as the sum of a plurality of sub-volumes within containing boundaries of the channel, excluding those sub-volumes having a dopant concentration above the source/drain dopant concentration at the carrier injection point. The containing boundaries can be identified using geometry data describing the transistor, particularly the data identifying inner surfaces of the gate dielectric. The estimated effective channel length can be used in TCAD level analysis of the transistor and calculating characteristics of the transistor as needed for circuit simulation.

[0005] The algorithm can be applied either to continuum doping profiles that are defined in terms of concentrations at each point in space, or to atomistic representation of the doping atoms, which can be preferred when transistors are scaled such that only a few atoms determine their behavior. In an embodiment, the algorithm handles both doped channels and undoped channels by using the concept of threshold source/drain doping level that is independent of the channel doping. Atomistic representation of the source/drain doping often exhibits non-contiguous, "spotty" dopant distributions, which are especially difficult to evaluate by eye-balling the structure. However, the concept of "effective channel volume" easily handles it. The invention is most beneficial for three-dimensional transistor bodies such as FinFETs, dual and tri-gate transistors and nanowires. Aspects of this approach can be applied to any three-dimensional transistor with tight gate control, including transistor bodies made up of 2-dimensional channel materials such as graphene, BN, MoS₂, WSe₂, and including carbon nano-tubes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The invention will be described with respect to specific embodiments thereof, and reference will be made to the drawings, in which:

Fig. 1 is an idealized drawing of a planar MOSFET transistor.

Fig. 2 is a drawing of a planar MOSFET transistor with curved junctions.

Fig. 3 is a perspective view of a model of a FinFET.

Fig. 4 is a drawing of a FinFET transistor with curved junctions.

Fig. 5 illustrates a planar MOSFET with an atomistic view of doping in the source, channel, and drain.

Fig. 6 depicts a FinFET with atomistic doping in the source, drain, and channel-stop region below the channel.

Fig. 7 depicts top views of two FinFET samples with different randomized atomistic doping distributions.

Fig. 8 depicts a cross-cut view of the FinFET of Fig. 3.

Fig. 9 illustrates modules in a system according to the invention.

Fig. 10 is an example flow chart detail of the module in Fig. 9 for determining channel effective volume V .

Fig. 11 is an example flow chart detail of the module in Fig. 9 for determining channel cross-sectional area.

Fig. 12 depicts a simplified representation of an illustrative digital integrated circuit design flow.

Fig. 13 is a simplified block diagram of a computer system that can be used to implement aspects of the invention.

DETAILED DESCRIPTION

[0007] The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

[0008] During the development and advancement of fabrication processes, as well as at other times, new transistor structures are developed. The new structures can differ from prior structures in many ways, such as by channel material, doping materials and profiles, scaling, gate and gate dielectric materials, source/drain shapes and so on. They can also differ in more

fundamental ways, such as the ways in which FinFETs, dual and tri-gate transistors, nanowires, SOI transistors, ultra-thin body transistors, 2-dimensional channel transistors and carbon nanotubes differ from conventional planar transistors. Before these transistors are put into production, they are analyzed to determine their circuit level parameters such as their I-V curves, threshold voltage V_{th} , electron and hole mobility, leakage currents, output resistance, capacitance, small signal characteristics, and so on. These parameters are used to compare transistor structures to others, as well as being provided to circuit simulators so that circuits that use such transistors can be modeled.

[0009] Conventionally, effective channel length L_{eff} is extracted from a geometric model of a transistor by drawing a line parallel to the current flow somewhere inside the channel and determining intersections of that line with the source junction and the drain junction. This works fine if the source junction is flat and is parallel to the drain junction, as is shown on Fig. 1. This approach is not completely automatic, as it typically requires the human to choose where to draw the line.

[0010] However, the junctions are usually curved, as illustrated on Fig. 2. Depending on where the line is drawn, the effective channel length is different. In a planar MOSFET, typically the line is drawn close to the gate dielectric, where most of the current is flowing, giving effective channel length of L_1 . The L_2 and L_3 values typically are ignored, as there is no significant current flow.

[0011] For FinFETs and nano-wire transistors, current is flowing throughout the entire channel, so the simple approach that works for the planar MOSFET is no longer valid. Typical FinFET geometry is depicted in Fig. 3. It includes a channel region 310, and source and drain regions 312, 314 on opposite ends of the channel region longitudinally. The channel ideally is a body of undoped silicon, and the source and drain regions are doped with dopant atoms. FinFET cross-section along the channel is shown on Fig. 4, with the current flowing throughout the entire channel. Here, all possible effective channel length measurements are meaningful, including L_1 , L_2 , and L_3 . The overall effective channel length can be determined by taking multiple measurements that equally represent all parts of the channel and averaging them. This is possible to accomplish with the conventional approach, although it becomes laborious.

[0012] As the transistor sizes keep shrinking with each subsequent technology node, they contain fewer and fewer lattice atoms, approximately 3 times less with each generation. This means that specific locations of separate doping atoms can determine a transistor's behavior. Fig. 5 illustrates a planar MOSFET with an atomistic view of doping in the source 512, channel 510, and drain 514. Fig. 6 depicts a FinFET with atomistic doping in the channel 610, source 612,

drain 614, and channel-stop region 616 below the channel. The source/drain dopants in Fig. 6 are As atoms (dark circles), and the channel-stop dopants are shown as light circles. The channel is undoped silicon in this image, except for unintended dopant atoms randomly diffusing into the channel either from the source or from the drain or from the channel-stop region.

[0013] Fig. 7 shows top view of two FinFET samples 721 and 722 with different randomized atomistic dopant distributions. In sample 721 the channel, source and drain are indicated as 710A, 712A and 714A, respectively. In sample 722 the channel, source and drain are indicated as 710B, 712B and 714B, respectively. The conventional approach breaks down for atomistic doping, because the measuring lines randomly bump into the atoms and give inaccurate results.

[0014] Fig. 9 shows a system which can resolve the issues of curved and spotty junctions and also eliminate any need for the human to choose where to draw the measuring lines and therefore make it completely automatic. In the illustrated embodiment, the system is organized as an analysis tool 910 which generates a set of parameters including the effective gate length L_{eff} , which are then written to a database 912 and used for simulating electrical behavior of the transistor in a circuit. The tool can execute a process that accepts a transistor specification as input, where the transistor specification includes transistor geometry and dopant distribution or distributions. Using the transistor specification, the process can generate parameters such as L_{eff} .

[0015] The database 912 typically contains model information for a large number of components offered to designers for the particular fabrication process, including several different types of transistors. The model information for each component is made available to circuit simulators such as a SPICE tool 914, for use in simulating the electrical performance of an input circuit design.

[0016] The calculated value of L_{eff} can be used additionally or instead for other purposes. For example, it can be written into a memory region or database 930, and retrieved by a TCAD device simulator 932 for detailed TCAD level analysis of the transistor. An accurate value of L_{eff} is useful for example to provide yet more parameter values for a transistor model in a circuit simulator. The calculated value for L_{eff} can be used, for example, in the ballistic mobility model. A tool which performs such TCAD level analysis is Sentaurus Device, available from Synopsys, Inc., and described in Synopsys, Sentaurus Device, Datasheet (2007), incorporated by reference herein and available at http://www.synopsys.com/Tools/TCAD/CapsuleModule/sdevice_ds.pdf (visited 2013-10-03). Transistor parameters output by the TCAD device simulator 932 can, like L_{eff} itself, be written into the database 912 for use in transistor models by a circuit simulator 914.

[0017] The databases 912 and 930 are stored on one or more non-transitory computer readable media. As used herein, no distinction is intended between whether a database is disposed "on" or "in" a computer readable medium. Additionally, as used herein, the term "database" does not necessarily imply any unity of structure. For example, two or more separate databases, when considered together, still constitute a "database" as that term is used herein. Thus in Fig. 9, the databases 912 and 930 are also sometimes referred to herein in combination as "a database".

Analysis Tool

[0018] The analysis tool 910 has stored accessibly thereto, a data set stored in one or more files in a non-transitory computer readable medium. The computer readable medium may be a stand-alone component or may be part of one or more other computer systems. Alternatively, the data set may be provided in the form of a data stream. The data set describes, among other things, the geometry and dopant profile of the transistor to be analyzed. Preferably the data set is provided to the tool in a predetermined data interchange format, such as is generated by TCAD. Preferably the format uses a 3D mesh to organize the data set, in which each node indicates among other things the material and the doping level at that position in the structure. More specifically, each node of the mesh has node information associated with it, which indicates among other things the material and dopant concentrations within a volume that contains the node. For example, in the FinFET of Fig. 3, a 3D grid (not shown) is imposed on the structure, with each node of the grid identifying information about the Voronoi volume that contains the node. In the illustrations of Figs. 3, 6 and 7, for example, an undoped volume in the channel is indicated at the corresponding node as containing pure silicon. A volume in the source or drain region is indicated as containing silicon with a high concentration of source/drain dopant atoms (arsenic in Figs. 6 and 7). Volumes containing gate dielectric (not shown), are indicated as containing oxide. By comparing the oxide content of volumes with neighboring volumes, it is possible to determine the surface interface of the channel with the surrounding gate dielectric. Note that the mesh need not be uniform. Additionally, the length of the gate oxide in the transistor longitudinal dimension as reflected in the data set is one of several ways in which the data set indicates what the gate length is of the transistor.

[0019] The analysis tool 910 can be invoked using an application program interface (API), in which a script or other software program, running on a computer system, invokes the tool 910 and identifies the input data to it. In one embodiment the transistor information is specified to the program by a user identifying, through a command line or through a graphical user interface

(GUI), a file that contains the input data. In one embodiment the file that contains the input data may be generated by a fabrication process simulator, such as Sentaurus Process, available from Synopsys, Inc., from detailed information about the fabrication process to be used to fabricate the transistor. In an embodiment the fabrication process simulator operates according to any of the techniques described in U.S. Patent Application No. 14/479,070, filed 5 September 2014 (Attorney Docket No. SYNPN 2474-2), incorporated by reference herein.

[0020] The analysis tool 910 generates as output the effective channel length L_{eff} of the input transistor structure. It may also generate other transistor parameters as output. In one embodiment the output is returned to the caller of the API, which can display the output to a user, or write it to the database 912, or provide it as input through another API to the circuit simulator 914. In another embodiment any of these dispositions of the output can be performed by the analysis tool 912 itself.

[0021] The operation performed by the analysis tool includes the calculation of L_{eff} from the transistor input data. Referring to Fig. 9, the calculation involves determining an effective volume V of the channel (step 916), determining a cross-sectional area A for the channel (step 918), and calculating $L_{eff}=V/A$ (step 920). In all flowcharts herein, the logic of the flow chart can be implemented using processors programmed using computer programs stored in memory accessible to the computer systems and executable by the processors, by dedicated logic hardware, including field programmable integrated circuits, or by combinations of dedicated logic hardware and computer programs. Each block in the flowchart describes logic that can be implemented in hardware or in software running on one or more computing processes executing on one or more computer systems as described herein. In one embodiment, each step of the flow chart illustrates the function of a separate module of software. In another embodiment, the logic of the step is performed by software code routines which are distributed throughout more than one module. As with all flowcharts herein, it will be appreciated that many of the steps can be combined, performed in parallel or performed in a different sequence without affecting the functions achieved. In some cases, as the reader will appreciate, a re-arrangement of steps will achieve the same results only if certain other changes are made as well. In other cases, as the reader will appreciate, a re-arrangement of steps will achieve the same results only if certain conditions are satisfied. Furthermore, it will be appreciated that the flow charts herein show only steps that are pertinent to an understanding of the invention, and it will be understood that in a specific embodiment, numerous additional steps for accomplishing other functions for that embodiment can be performed before, after and between those steps shown.

[0022] Fig. 10 illustrates an example method for determining the channel effective volume V . In step 1010, the geometric data modeling the transistor geometry is analyzed to find a rough volumetric region that contains the channel. It is preferable to err on the large size so as to include at least the entire actual channel. FinFETs (including dual gate and tri-gate versions), nano-wire transistors, gate-all-around transistors, and 2-dimensional transistors with graphene, BN, MoS₂, or WSe₂, all include in the transistor structure a thin gate dielectric surrounding the channel. Therefore, to find a rough volumetric region containing the channel in these types of transistors, an embodiment can find the thin gate dielectric, and identify the volume inside whose surfaces are interfaces to this dielectric. More specifically, the following sub-method can be used:

[0023] 1. Find the minimum EOT (Equivalent Oxide Thickness) in the structure. This can be determined by surveying the geometry data to find surfaces where oxide meets other materials. Since the geometry data is preferably not idealized, but rather is generated by a TCAD simulation of a series of fabrication process steps, it will be appreciated that the surfaces will not be simple planes.

[0024] 2. Find all adjacent semiconductor surface where EOT does not exceed the minimum EOT plus some predetermined margin. It is possible that because of the non-ideal fabrication process, the minimum EOT may be smaller than an idealized thickness, for example in corners or at the edges of layers. The margin is chosen to be large enough to capture most or all of the gate dielectric, though thicker than the minimum. The margin is chosen also to be small enough to ensure that oxide regions which are contained in the structure for other reasons are excluded. For example the margin can be 20% of the minimum EOT.

[0025] 3. The obtained surface sheathes the channel, leaving open the source side and the drain side. For bulk FinFETs, it also leaves open the bottom surface of the channel – see, for example, Fig. 8. The system completes the bottom surface by a plane that is parallel to the main (longitudinal) axis of the channel (see step 1110 in Fig. 11), and the source and drain ends of the channel are completed by planes that are perpendicular to the main axis of the channel.

[0026] The volumetric region bounded by the surfaces found in step 1010 is only a rough enclosure of the effective channel, which as previously mentioned typically does not have flat surfaces. The boundaries of this rough enclosure are sometimes referred to herein as "containing boundaries" of the channel.

[0027] In step 1012 the effective volume V of the contained effective channel is calculated. This can be accomplished by calculating the sum of Voronoi volumes of all the mesh nodes in the volumetric region determined in step 1010, for only those of the nodes whose doping level is

below a predetermined value C^* . C^* is chosen as a source/drain dopant concentration at the interface between channel and source or drain. Preferably C^* is equal to the source/drain dopant concentration at the carrier injection point. Preferably $C^*=2 \times 10^{19} \text{ cm}^{-3}$, per Taur, Y., CMOS design near the limit of scaling, IBM J. RES. & DEV., Vol. 46 No. 2/3, pp. 213-222 (2002), incorporated by reference herein. For spotty atomistic doping, choosing a threshold like C^* will omit volumes having source/drain dopants that have trickled into the channel, but will count all adjacent volume around such dopants, which is the desired behavior.

[0028] It will be appreciated that one of the purposes of finding containing boundaries of the channel is to ensure that the summation of Voronoi volumes in step 1012 covers at least the effective volume of the channel, but excludes regions of the structure which are isolated from the effective volume of the channel but which the dopant concentration criterion might fail to exclude by itself. Other methods to find appropriate containing boundaries that will accomplish this purpose will be apparent to the reader.

[0029] Fig. 11 illustrates an example method for determining channel cross-sectional area. It involves, in step 1110, finding the main axis of the rough volumetric region found in step 1010. To ensure electrostatic integrity of the transistor, its channel length should be considerably larger than its channel width. Therefore, the longer dimension of the volume determined in step 1010 defines the main axis of the channel, the direction of the current flow.

[0030] In step 1112, a longitudinal position along the main axis is chosen which is deemed to have a cross-sectional area that is "typical" for the channel. For a typical device, in which the channel has a roughly constant width and depth along at least the longitudinally central portion of its length, a good position to choose is the centroid of the volumetric region from step 1010. Thus, this step can involve calculating the coordinates of the centroid of the volumetric region from step 1010.

[0031] Next, in step 1114, the cross-sectional area A of the rough channel volume from step 1110 is calculated, at the longitudinal position from step 1112. This can involve determining the plane passing through the centroid and perpendicular to the main axis, and calculating the area of that plane. Note that if the channel width or height varies along its length, then an embodiment can calculate the cross-sectional area at several longitudinal positions along the channel main axis, and average them to determine A .

[0032] As mentioned, once values have been obtained for V and A , the effective channel length can be calculated as $L_{\text{eff}}=V/A$.

Circuit Simulator

[0033] Circuit simulators are well known. Examples of such tools are different versions of SPICE, described in the following documents incorporated by reference herein: Nagel and Pederson, SPICE (Simulation Program with Integrated Circuit Emphasis), EECS Department, University of California, Berkeley (1973) (available at <http://www.eecs.Berkeley.edu/Pubs/TechRpts/1973/ERL-382.pdf>, visited 2013-10-02); Nagel, Laurence W., SPICE2: A Computer Program to Simulate Semiconductor Circuits, EECS Department, University of California, Berkeley (1975) (available at <http://www.eecs.berkeley.edu/Pubs/TechRpts/1975/ERL-520.pdf>, visited 2013-10-02); and Quarles, Thomas L., Analysis of Performance and Convergence Issues for Circuit Simulation, EECS Department, University of California, Berkeley (1989) (available at <http://www.eecs.berkeley.edu/Pubs/TechRpts/1989/ERL-89-42.pdf>, visited 2013-10-02), all incorporated by reference herein. Roughly described, a circuit simulator takes a circuit design as input (typically in the form of a netlist, indicating each component of the circuit and the network by which they are interconnected), and calculates a variety of kinds of information about the circuit. In the embodiment of Fig. 9, the circuit simulator 914 is used for example in steps 1218 and/or 1224 of the typical EDA flow in Fig. 12 discussed hereinafter.

[0034] Circuit simulators such as SPICE include device models 922, which model the behavior of the various components that are used in a circuit. One example device model which is commonly used for transistors, is the Berkeley Short-channel IGFET Model (BSIM) family of models. The BSIM4 version of the model is described for example in Mohan V. Dunga et. al., BSIM4.6.0 MOSFET Model User's Manual, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley (2006), incorporated by reference herein. It can be seen that the model uses L_{eff} in the calculation of a large number of transistor parameters, including:

- the calculation of I-V profiles;
- V_{th} change due to SCE and DIBL
- drain current I_{ds} in the subthreshold region
- mobility
- saturation voltage V_{dsat}
- the Early voltage due to substrate current
- transient currents $i_D(t)$, $i_G(t)$ and $i_S(t)$
- flicker noise
- and many others.

[0035] In all the equations, BSIM uses a geometrical approximation of L_{eff} , which does not necessarily correspond to a true effective channel length. In an embodiment, the value for L_{eff} calculated by the analysis tool 910 is provided to the BSIM model which then uses it in place of its own geometrical approximation.

Design Process Flow

[0036] As mentioned, the circuit simulator 914 (Fig. 9) can be used as part of an overall EDA design process flow. Fig. 12 shows a simplified representation of an illustrative digital integrated circuit design flow. At a high level, the process starts with the product idea (step 1200) and is realized in an EDA (Electronic Design Automation) software design process (step 1210). When the design is finalized, it can be taped-out (step 1227). At some point after tape out, the fabrication process (step 1250) and packaging and assembly processes (step 1260) occur resulting, ultimately, in finished integrated circuit chips (result 1270). An example physical fabrication flow is described in Integrated Circuit Engineering Corp., Basic Integrated Circuit Technology Reference Manual, Section 2, Basic Integrated Circuit Manufacturing, pp. 2-1 through 2-112 (1993) incorporated by reference herein.

[0037] The EDA software design process (step 1210) is itself composed of a number of steps 1212 -1230, shown in linear fashion for simplicity. In an actual integrated circuit design process, the particular design might have to go back through steps until certain tests are passed. Similarly, in any actual design process, these steps may occur in different orders and combinations. This description is therefore provided by way of context and general explanation rather than as a specific, or recommended, design flow for a particular integrated circuit.

[0038] A brief description of the component steps of the EDA software design process (step 1210) will now be provided.

[0039] System design (step 1212): The designers describe the functionality that they want to implement, they can perform what-if planning to refine functionality, check costs, etc. Hardware-software architecture partitioning can occur at this stage. Example EDA software products from Synopsys, Inc. that can be used at this step include Model Architect, Saber, System Studio, and DesignWare® products.

[0040] Logic design and functional verification (step 1214): At this stage, the VHDL or Verilog code for modules in the system is written and the design is checked for functional accuracy. More specifically, the design is checked to ensure that it produces correct outputs in response to particular input stimuli. Example EDA software products from Synopsys, Inc. that

can be used at this step include VCS, VERA, DesignWare®, Magellan, Formality, ESP and LEDA products.

[0041] Synthesis and design for test (step 1216): Here, the VHDL/Verilog is translated to a netlist. The netlist can be optimized for the target technology. Additionally, the design and implementation of tests to permit checking of the finished chip occurs. Example EDA software products from Synopsys, Inc. that can be used at this step include Design Compiler®, Physical Compiler, DFT Compiler, Power Compiler, FPGA Compiler, TetraMAX, and DesignWare® products.

[0042] Netlist verification (step 1218): At this step, the netlist is checked for compliance with timing constraints and for correspondence with the VHDL/Verilog source code. Example EDA software products from Synopsys, Inc. that can be used at this step include Formality, PrimeTime, and VCS products.

[0043] Design planning (step 1220): Here, an overall floor plan for the chip is constructed and analyzed for timing and top-level routing. Example EDA software products from Synopsys, Inc. that can be used at this step include Astro and Custom Designer products.

[0044] Physical implementation (step 1222): The placement (positioning of circuit elements) and routing (connection of the same) occurs at this step, as can selection of library cells to perform specified logic functions. Example EDA software products from Synopsys, Inc. that can be used at this step include the Astro, IC Compiler, and Custom Designer products.

[0045] Analysis and extraction (step 1224): At this step, the circuit function is verified at a transistor level, this in turn permits what-if refinement. Example EDA software products from Synopsys, Inc. that can be used at this step include AstroRail, PrimeRail, PrimeTime, and Star-RCXT products.

[0046] Physical verification (step 1226): At this step various checking functions are performed to ensure correctness for: manufacturing, electrical issues, lithographic issues, and circuitry. Example EDA software products from Synopsys, Inc. that can be used at this step include the Hercules product.

[0047] Tape-out (step 1227): This step provides the “tape out” data to be used (after lithographic enhancements are applied if appropriate) for production of masks for lithographic use to produce finished chips. Example EDA software products from Synopsys, Inc. that can be used at this step include the IC Compiler and Custom Designer families of products.

[0048] Resolution enhancement (step 1228): This step involves geometric manipulations of the layout to improve manufacturability of the design. Example EDA software products from Synopsys, Inc. that can be used at this step include Proteus, ProteusAF, and PSMGen products.

[0049] Mask data preparation (step 1230): This step provides mask-making-ready “tape-out” data for production of masks for lithographic use to produce finished chips. Example EDA software products from Synopsys, Inc. that can be used at this step include the CATS(R) family of products.

[0050] **Parallel flow.** The integrated circuit manufacturing flow includes a parallel flow, as follows:

[0051] (1) Develop individual process steps for manufacturing the integrated circuit. This can be modeled with EDA tools such as the Synopsys tools “Sentaurus Process”, “Sentaurus Topography”, and “Sentaurus Lithography”. The input information here includes process conditions like temperature, reactor ambient, implant energy, etc. The output information includes the change in geometry or doping profiles or stress distribution.

[0052] (2) Integrate the individual process steps into the complete process flow. This can be modeled with EDA tools such as the Synopsys tool “Sentaurus Process”. The input information here includes the collection of the process steps in the appropriate sequence. The output includes the geometry, the doping profiles, and the stress distribution for the transistors and the space in between the transistors.

[0053] (3) Analyze performance of the transistor manufactured with this process flow. This can be done with EDA tools such as the Synopsys tool “Sentaurus Device”. The input information here includes the output of step (2) and the biases applied to transistor terminals. The output information includes the currents and capacitances for each bias combination. Aspects of the invention can be used for example in this step.

[0054] (4) If necessary, modify the process steps and the process flow to achieve the desired transistor performance. This can be done iteratively by using tools such as the Synopsys tools mentioned above.

[0055] Once the process flow is ready, it can be used for manufacturing multiple circuit designs. The EDA flow 1212-1230 will be used for this purpose. The parallel flow described here typically is used at a foundry to develop a process flow that can be used to manufacture designs. A combination of the process flow and the masks 1230 are used to manufacture any particular circuit. If the integrated circuit is manufactured at an IDM (integrated device manufacturer) company instead of the combination of a fables company and a foundry, then both parallel flows described above are done at the same IDM company.

Hardware implementation

[0056] Fig. 13 is a simplified block diagram of a computer system 1310 that can be used to implement any of the methods and processes herein.

[0057] Computer system 1310 typically includes a processor subsystem 1314 which communicates with a number of peripheral devices via bus subsystem 1312. These peripheral devices may include a storage subsystem 1324, comprising a memory subsystem 1326 and a file storage subsystem 1328, user interface input devices 1322, user interface output devices 1320, and a network interface subsystem 1316. The input and output devices allow user interaction with computer system 1310. Network interface subsystem 1316 provides an interface to outside networks, including an interface to communication network 1318, and is coupled via communication network 1318 to corresponding interface devices in other computer systems. Communication network 1318 may comprise many interconnected computer systems and communication links. These communication links may be wireline links, optical links, wireless links, or any other mechanisms for communication of information, but typically it is an IP-based communication network. While in one embodiment, communication network 1318 is the Internet, in other embodiments, communication network 1318 may be any suitable computer network.

[0058] The physical hardware component of network interfaces are sometimes referred to as network interface cards (NICs), although they need not be in the form of cards: for instance they could be in the form of integrated circuits (ICs) and connectors fitted directly onto a motherboard, or in the form of macrocells fabricated on a single integrated circuit chip with other components of the computer system.

[0059] User interface input devices 1322 may include a keyboard, pointing devices such as a mouse, trackball, touchpad, or graphics tablet, a scanner, a touch screen incorporated into the display, audio input devices such as voice recognition systems, microphones, and other types of input devices. In general, use of the term "input device" is intended to include all possible types of devices and ways to input information into computer system 1310 or onto computer network 1318.

[0060] User interface output devices 1320 may include a display subsystem, a printer, a fax machine, or non-visual displays such as audio output devices. The display subsystem may include a cathode ray tube (CRT), a flat panel device such as a liquid crystal display (LCD), a projection device, or some other mechanism for creating a visible image. The display subsystem may also provide non visual display such as via audio output devices. In general, use of the term "output device" is intended to include all possible types of devices and ways to output information from computer system 1310 to the user or to another machine or computer system.

[0061] Storage subsystem 1324 stores the basic programming and data constructs that provide the functionality of certain embodiments of the present invention. For example, the various modules implementing the functionality of certain embodiments of the invention may be stored in storage subsystem 1324. In particular, software code modules implementing the various flow chart steps described herein may be stored in storage subsystem 1324. These software modules are generally executed by processor subsystem 1314. The database 912 also may be stored in the storage subsystem 1324.

[0062] Memory subsystem 1326 typically includes a number of memories including a main random access memory (RAM) 1330 for storage of instructions and data during program execution and a read only memory (ROM) 1332 in which fixed instructions are stored. File storage subsystem 1328 includes persistent non-transitory memory storing computer programs, databases and other resources to configure the data processing systems as tool for determining the effective channel length of transistors, and for storing the results, and for making use of the results in circuit simulations, and for performing many other steps in the EDA process. The tool can include an API configured to use input parameter sets (such as those identifying a transistor structure and doping profile), and to perform the procedures of the tool using the input parameter sets. The file storage subsystem 1328 may include for example a hard disk drive, a floppy disk drive along with associated removable media, a CD ROM drive, an optical drive, or removable media cartridges. The databases and modules implementing the functionality of certain embodiments of the invention may have been provided on a computer readable medium such as one or more CD-ROMs, and may be stored by file storage subsystem 1328. The host memory 1326 contains, among other things, computer instructions which, when executed by the processor subsystem 1314, cause the computer system to operate or perform functions as described herein. As used herein, processes and software that are said to run in or on "the host" or "the computer", execute on the processor subsystem 1314 in response to computer instructions and data in the host memory subsystem 1326 including any other local or remote storage for such instructions and data.

[0063] Bus subsystem 1312 provides a mechanism for letting the various components and subsystems of computer system 1310 communicate with each other as intended. Although bus subsystem 1312 is shown schematically as a single bus, alternative embodiments of the bus subsystem may use multiple busses.

[0064] Computer system 1310 itself can be of varying types including a personal computer, a portable computer, a workstation, a computer terminal, a network computer, a television, a mainframe, a server farm, or any other data processing system or user device. Due to the ever

changing nature of computers and networks, the description of computer system 1310 depicted in Fig. 13 is intended only as a specific example for purposes of illustrating the preferred embodiments of the present invention. Many other configurations of computer system 1310 are possible having more or less components than the computer system depicted in Fig. 13.

[0065] In addition, while the present invention has been described in the context of a fully functioning data processing system, those of ordinary skill in the art will appreciate that the processes herein are capable of being distributed in the form of a computer readable medium of instructions and data and that the invention applies equally regardless of the particular type of signal bearing media actually used to carry out the distribution. As used herein, a computer readable medium is one on which information can be stored and read by a computer system. Examples include a floppy disk, a hard disk drive, a RAM, a CD, a DVD, flash memory, a USB drive, and so on. The computer readable medium may store information in coded formats that are decoded for actual use in a particular data processing system. A single computer readable medium, as the term is used herein, may also include more than one physical item, such as a plurality of CD ROMs or a plurality of segments of RAM, or a combination of several different kinds of media. As used herein, the term does not include mere time varying signals in which the information is encoded in the way the signal varies over time.

[0066] As used herein, a given signal, event or value is "responsive" to a predecessor signal, event or value if the predecessor signal, event or value influenced the given signal, event or value. If there is an intervening processing element, step or time period, the given signal, event or value can still be "responsive" to the predecessor signal, event or value. If the intervening processing element or step combines more than one signal, event or value, the signal output of the processing element or step is considered "responsive" to each of the signal, event or value inputs. If the given signal, event or value is the same as the predecessor signal, event or value, this is merely a degenerate case in which the given signal, event or value is still considered to be "responsive" to the predecessor signal, event or value. "Dependency" of a given signal, event or value upon another signal, event or value is defined similarly.

[0067] As used herein, the "identification" of an item of information does not necessarily require the direct specification of that item of information. Information can be "identified" in a field by simply referring to the actual information through one or more layers of indirection, or by identifying one or more items of different information which are together sufficient to determine the actual item of information. In addition, the term "indicate" is used herein to mean the same as "identify".

[0068] The applicant hereby discloses in isolation each individual feature described herein and any combination of two or more such features, to the extent that such features or combinations are capable of being carried out based on the present specification as a whole in light of the common general knowledge of a person skilled in the art, irrespective of whether such features or combinations of features solve any problems disclosed herein, and without limitation to the scope of the claims. The applicant indicates that aspects of the present invention may consist of any such feature or combination of features.

[0069] The foregoing description of preferred embodiments of the present invention has been provided for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. In particular, and without limitation, any and all variations described, suggested or incorporated by reference herein with respect to any one embodiment are also to be considered taught with respect to all other embodiments. The embodiments described herein were chosen and described in order to best explain the principles of the invention and its practical application, thereby enabling others skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use contemplated.

We claim:

CLAIMS

1. A system for estimating an effective channel length of a transistor, the system comprising:

a data processor;

a source of a data set for the data processor, the data set describing a dopant profile of a three-dimensional transistor having a semiconductor body, the data set also identifying a gate length for the transistor which is no greater than 20 nm; and

a computer readable medium coupled to the data processor, the computer readable medium having stored thereon in a non-transitory manner a plurality of software code portions defining logic for:

estimating, in dependence upon the data set, an effective volume V of the channel of the transistor,

determining a cross-sectional area A of the channel of the transistor, and

estimating the effective channel length of the transistor as the ratio of V to A .

2 The system of claim 1, wherein the data set further identifies surfaces of gate dielectric material adjacent to the semiconductor body, and wherein estimating an effective volume comprises:

identifying containing boundaries of the channel in dependence upon the surfaces of gate dielectric material adjacent to the semiconductor body as identified in the data set; and

determining the effective volume in dependence upon the dopant profile within the containing boundaries as described in the data set.

3 The system of claim 2, wherein the data set describes source/drain dopant concentration within each of a plurality of sub-volumes within the semiconductor body,

and wherein determining the effective volume in dependence upon the dopant profile comprises summing all of the sub-volumes which are within the containing boundaries and whose source/drain dopant concentration is below a predetermined value.

4. The system of claim 1, wherein the data set describes source/drain dopant concentration within each of a plurality of sub-volumes within the semiconductor body, and wherein estimating an effective volume comprises:

identifying containing boundaries of the channel; and

summing all of the sub-volumes which are within the containing boundaries and whose source/drain dopant concentration is below a predetermined value.

5. The system of claim 4, wherein the predetermined value is the source/drain dopant concentration at a carrier injection point at an interface of channel and a member of the group consisting of source and drain.

6. The system of any of claims 4-5, wherein the source/drain dopant concentration of at least one of the sub-volumes which are within the containing boundaries, exceeds the predetermined value.

7. The system of claim 1, wherein the data set further identifies surfaces of gate dielectric material adjacent to the semiconductor body, and wherein determining a cross-sectional area A of the channel of the transistor comprises:

choosing a particular longitudinal position along the channel; and

calculating a cross-sectional area of the channel at the particular longitudinal position in dependence upon the surfaces of gate dielectric material identified in the data set.

8. The system of claim 7, wherein the particular longitudinal position is the centroid of a volumetric region determined by identifying containing boundaries of the channel in dependence upon the surfaces of gate dielectric material adjacent to the semiconductor body as identified in the data set.

9. The system of any of claims 1-8, wherein the plurality of software code portions further define logic for writing the effective channel length into a database.

10. The system of any of claims 1-9, wherein the plurality of software code portions further define logic for simulating a circuit design that uses the transistor, including calculating a characteristic of the transistor in dependence upon the effective channel length estimated in the step of estimating the effective channel length of the transistor.

11. The system of any of claims 1-9, wherein the plurality of software code portions further define logic for performing a detailed TCAD level analysis of the transistor using the effective channel length from the estimated effective channel length.

12. The system of claim 11, wherein performing a detailed TCAD level analysis of the transistor comprises a member of the group consisting of:

calculating an I-V profile of the transistor;

determining values for drain current I_{ds} in the subthreshold region of the transistor;

determining electron or hole mobility in the channel of the transistor;

determining the saturation voltage V_{dsat} of the transistor;

determining the Early voltage of the transistor due to substrate current;

determining transient currents $i_D(t)$, $i_G(t)$ and $i_S(t)$ of the transistor; and

determining flicker noise in the transistor.

13. A method for estimating an effective channel length of a transistor, comprising the steps of:

providing, to a computer system, a data set describing a dopant profile of a three-dimensional transistor having a semiconductor body, the data set also identifying a gate length for the transistor which is no greater than 20 nm;

the computer system estimating, in dependence upon the data set, an effective volume V of the channel of the transistor;

determining a cross-sectional area A of the channel of the transistor; and

estimating the effective channel length of the transistor as the ratio of V to A .

14 The method of claim 13, wherein the data set further identifies surfaces of gate dielectric material adjacent to the semiconductor body, and wherein estimating an effective volume comprises:

the computer system identifying containing boundaries of the channel in dependence upon the surfaces of gate dielectric material adjacent to the semiconductor body as identified in the data set; and

determining the effective volume in dependence upon the dopant profile within the containing boundaries as described in the data set.

15 The method of claim 13, wherein the data set describes source/drain dopant concentration within each of a plurality of sub-volumes within the semiconductor body,

and wherein determining the effective volume in dependence upon the dopant profile comprises summing all of the sub-volumes which are within the containing boundaries and whose source/drain dopant concentration is below a predetermined value.

16. The method of claim 13, wherein the data set describes source/drain dopant concentration within each of a plurality of sub-volumes within the semiconductor body, and wherein estimating an effective volume comprises:

identifying containing boundaries of the channel; and

the computer system summing all of the sub-volumes which are within the containing boundaries and whose source/drain dopant concentration is below a predetermined value.

17. The method of claim 16, wherein the predetermined value is the source/drain dopant concentration at a carrier injection point at an interface of channel and a member of the group consisting of source and drain.

18. The method of any of claims 16-17, wherein the source/drain dopant concentration of at least one of the sub-volumes which are within the containing boundaries, exceeds the predetermined value.

19. The method of claim 13, wherein the data set further identifies surfaces of gate dielectric material adjacent to the semiconductor body, and wherein determining a cross-sectional area A of the channel of the transistor comprises:

choosing a particular longitudinal position along the channel; and

calculating a cross-sectional area of the channel at the particular longitudinal position in dependence upon the surfaces of gate dielectric material identified in the data set.

20. The method of claim 19, wherein the particular longitudinal position is the centroid of a volumetric region determined by identifying containing boundaries of the channel in dependence upon the surfaces of gate dielectric material adjacent to the semiconductor body as identified in the data set.

21. The method of any of claims 13-20, further comprising writing the effective channel length into a database.

22. The method of any of claims 13-21, further comprising a computer system simulating a circuit design that uses the transistor, including calculating a characteristic of the transistor in dependence upon the effective channel length estimated in the step of estimating the effective channel length of the transistor.

23. The method of any of claims 13-22, further comprising the step of performing a detailed TCAD level analysis of the transistor using the effective channel length from the step of estimating the effective channel length.

24. The method of claim 23, wherein performing a detailed TCAD level analysis of the transistor comprises a member of the group consisting of:

calculating an I-V profile of the transistor;

determining values for drain current I_{ds} in the subthreshold region of the transistor;

determining electron or hole mobility in the channel of the transistor;

determining the saturation voltage V_{dsat} of the transistor;

determining the Early voltage of the transistor due to substrate current;

determining transient currents $i_D(t)$, $i_G(t)$ and $i_S(t)$ of the transistor; and

determining flicker noise in the transistor.

25. A system for estimating an effective channel length of a transistor, comprising:
a data processor; and

storage accessible by the processor, the data processor configured to perform the steps of:

- receiving at an API input data describing aspects of a transistor;
- estimating the effective channel length of the transistor in dependence upon the input data; and
- outputting the estimated effective channel length,

wherein estimating the effective channel length of the transistor in dependence upon the input data includes:

- estimating an effective volume V of the channel of the transistor;
- determining a cross-sectional area A of the channel of the transistor; and
- estimating the effective channel length of the transistor as the ratio of V to A .

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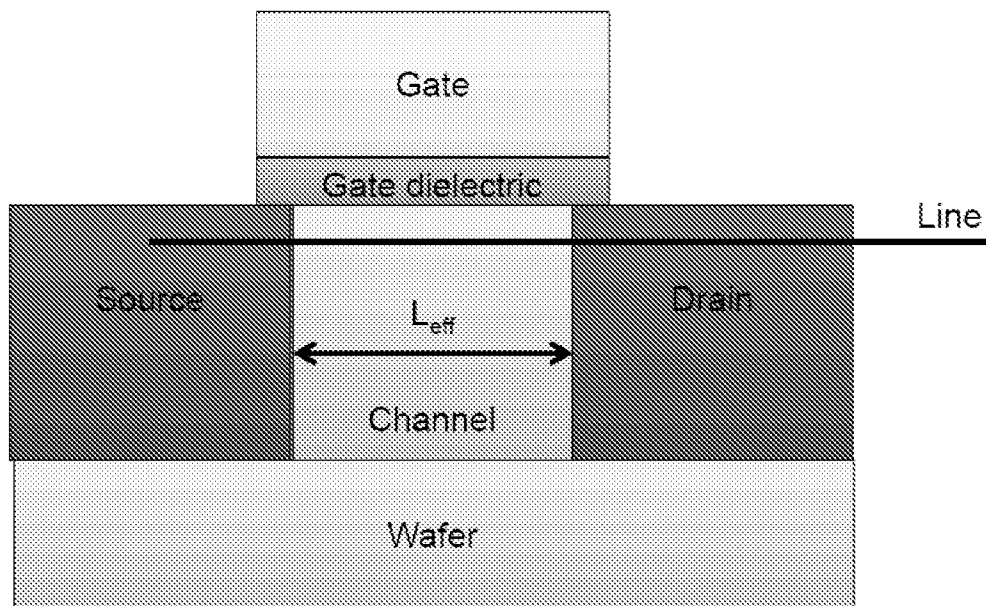
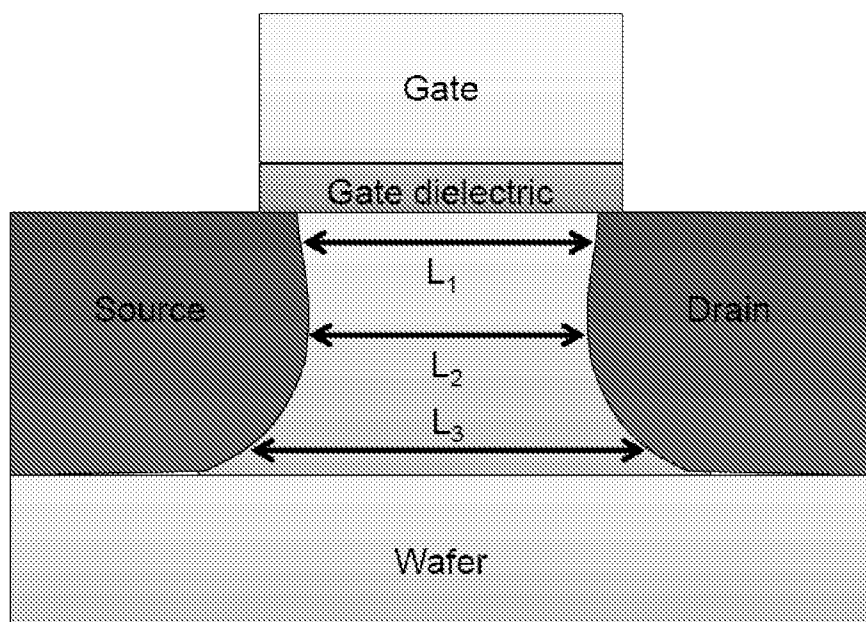
Fig. 1 Transistor with Parallel Junctions**Fig. 2 Transistor with Curved Junctions**

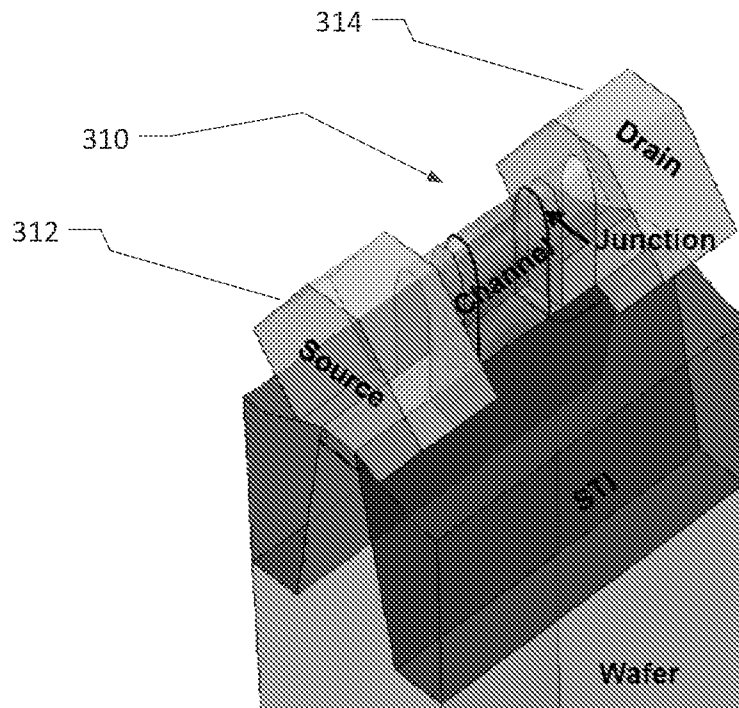
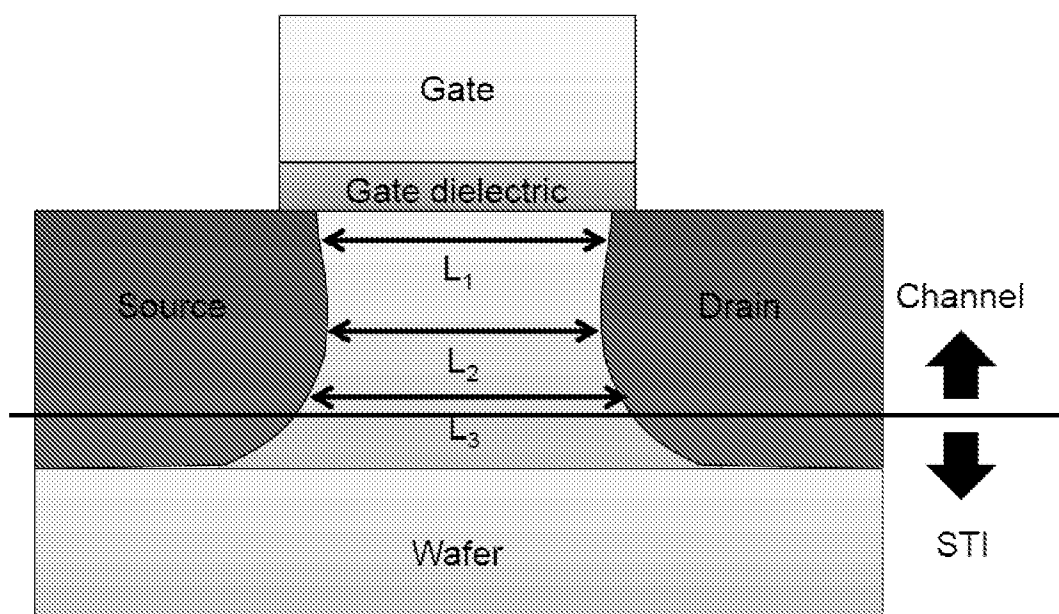
Fig. 3 FinFET Overview**Fig. 4 FinFET Cut Along Channel**

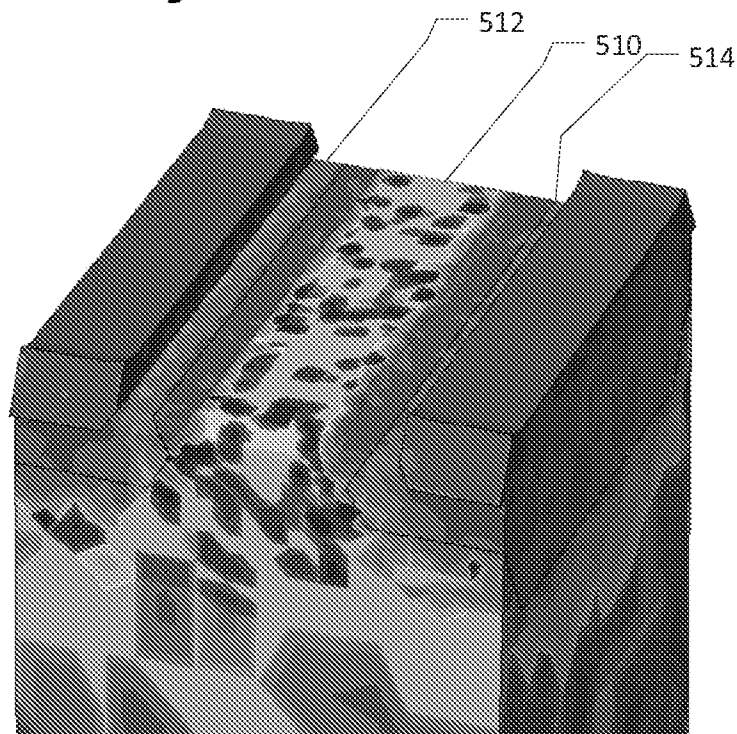
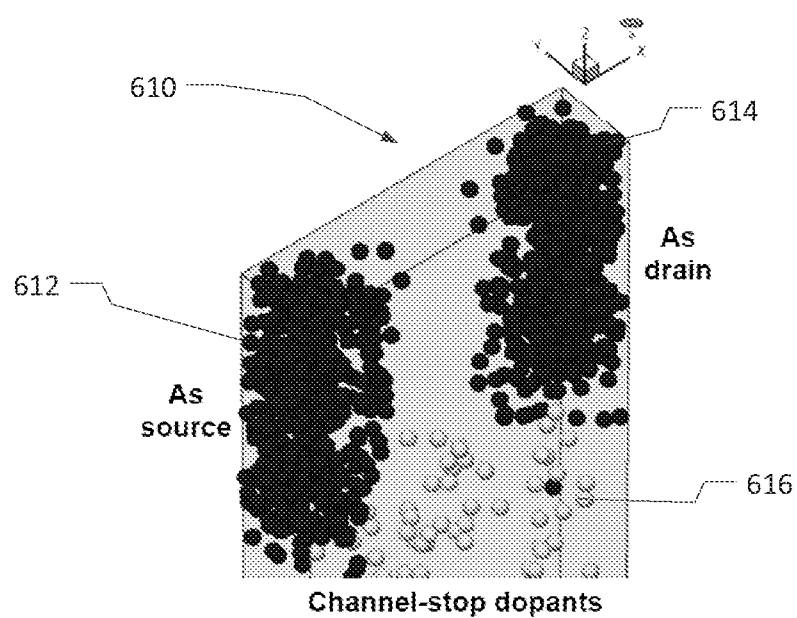
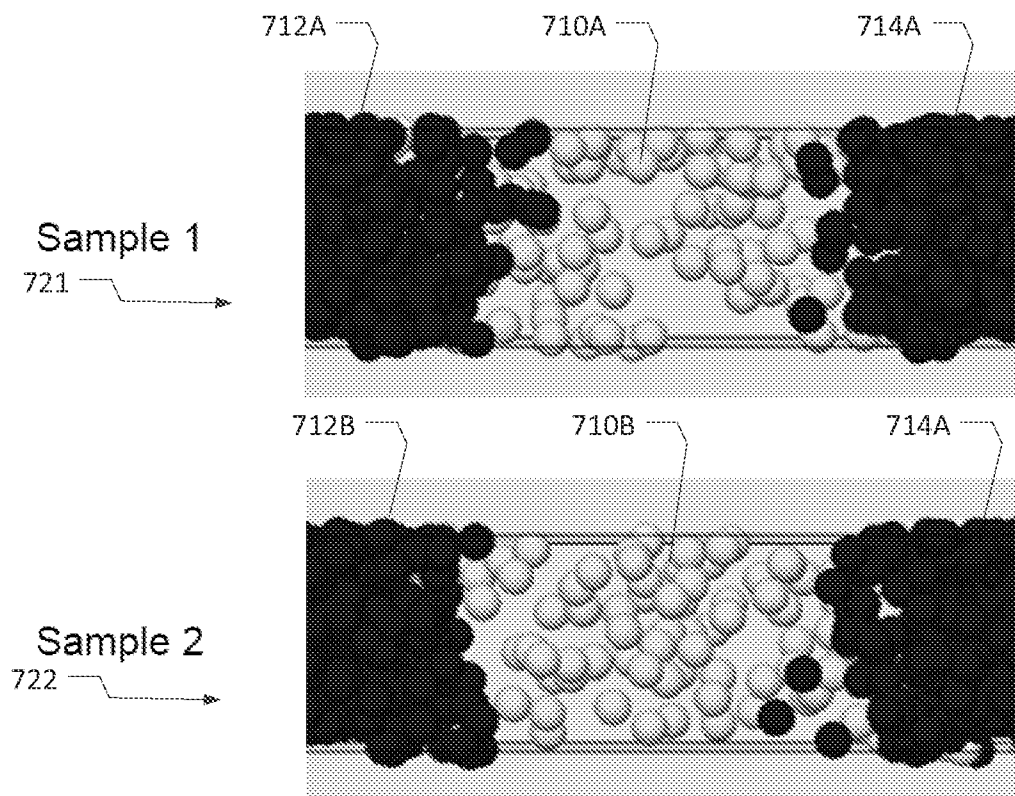
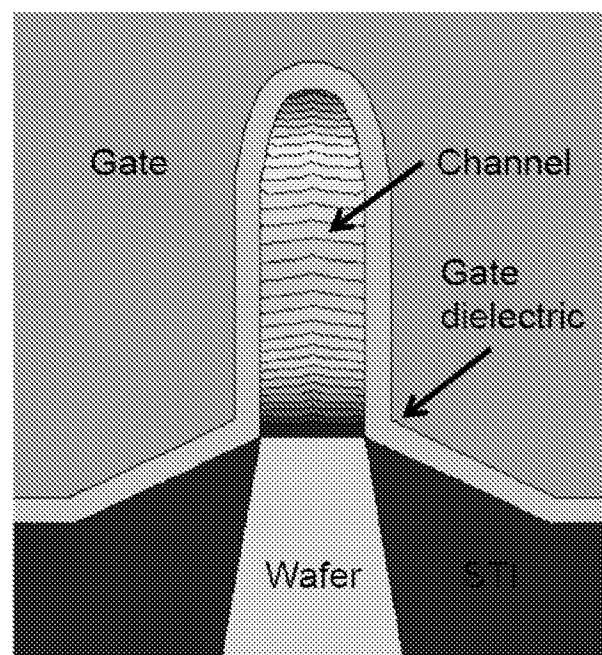
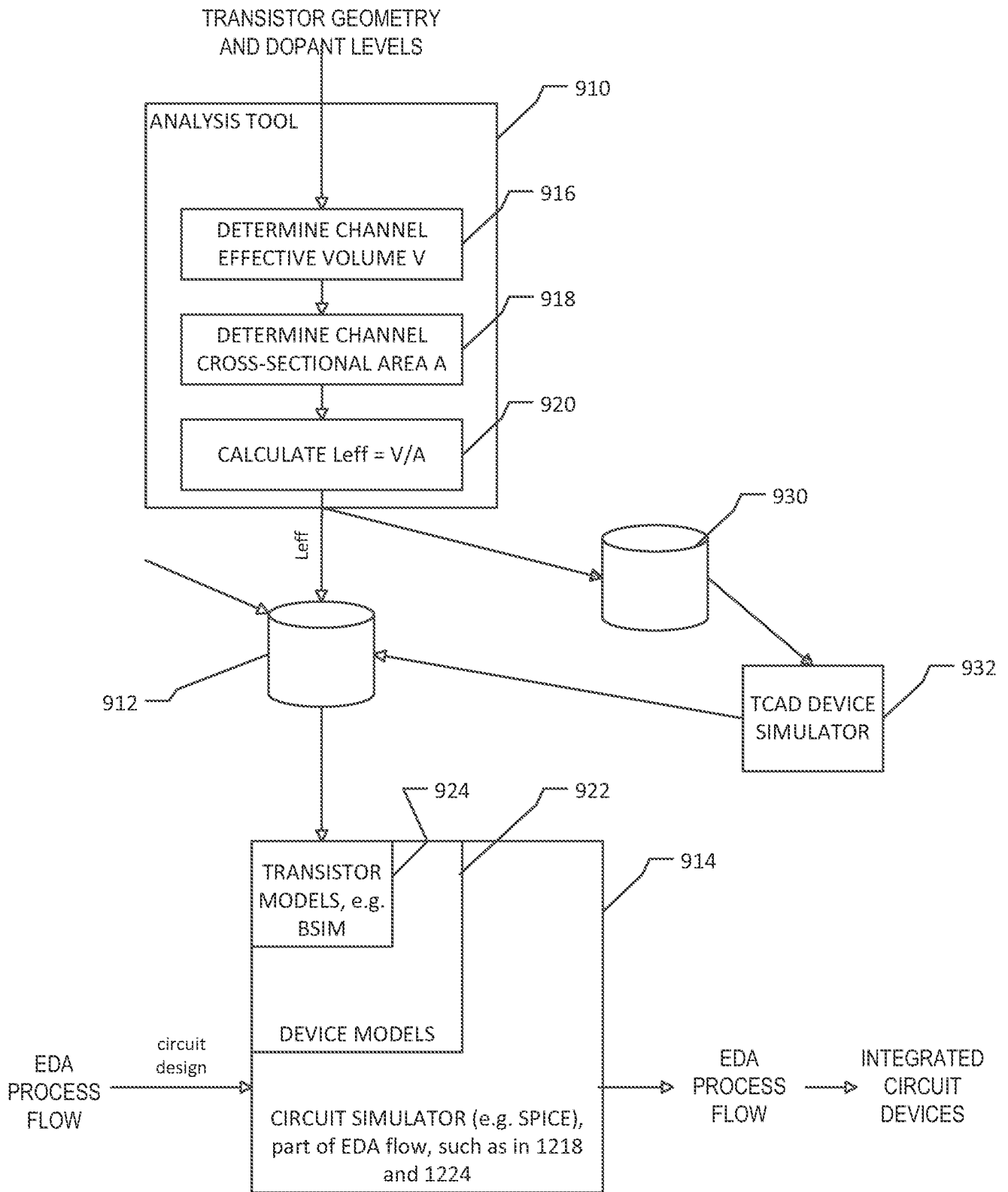
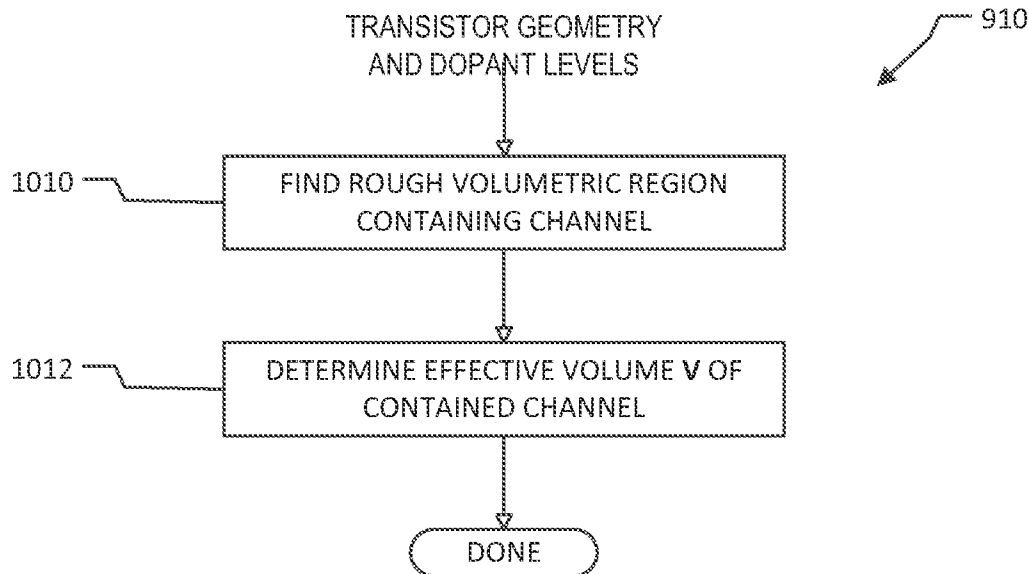
Fig. 5 “Noisy” Atomistic Junctions**Fig. 6 FinFET with Atomistic Doping**

Fig. 7 FinFET Top View**Fig. 8 FinFET Cut Across Channel**

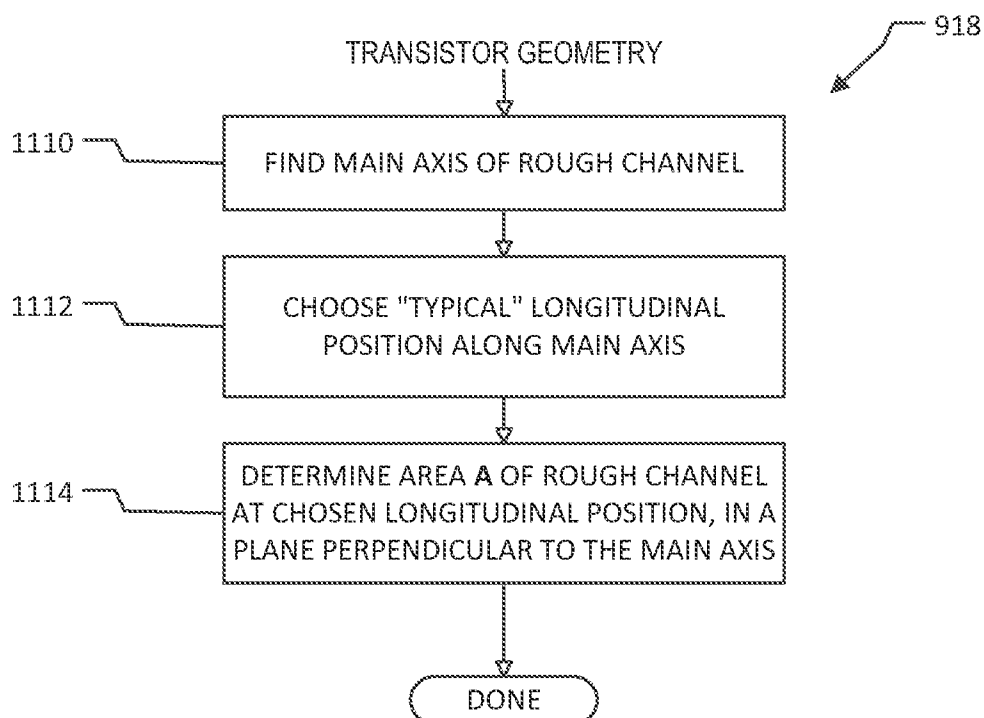
**FIG. 9**

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DETERMINE CHANNEL EFFECTIVE VOLUME V
EXAMPLE METHOD

**FIG. 10**

DETERMINE CHANNEL CROSS-SECTIONAL AREA
EXAMPLE METHOD

**FIG. 11**

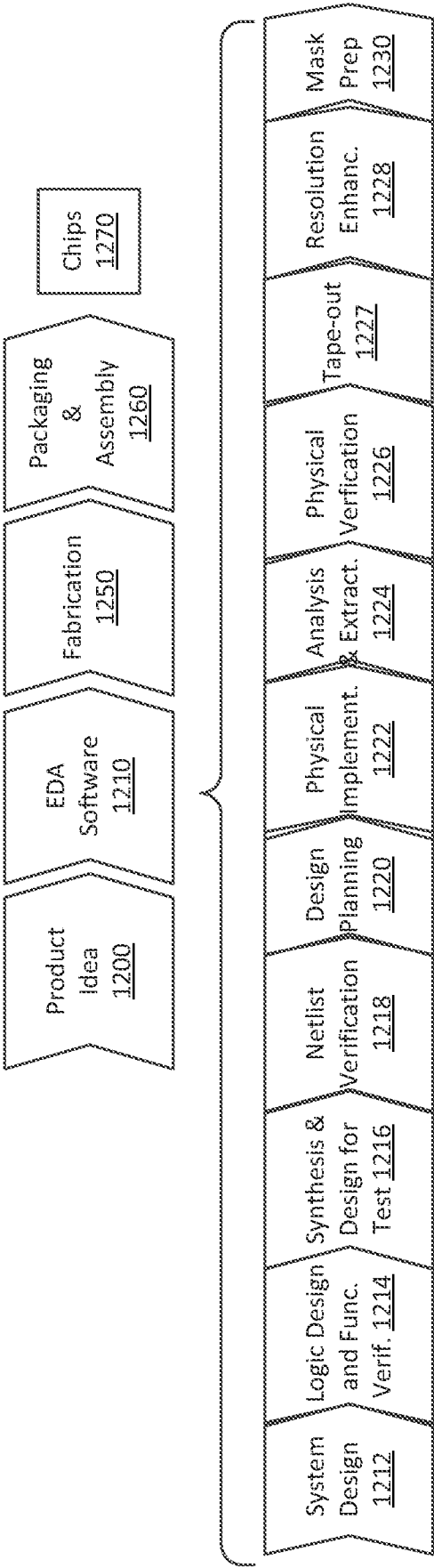
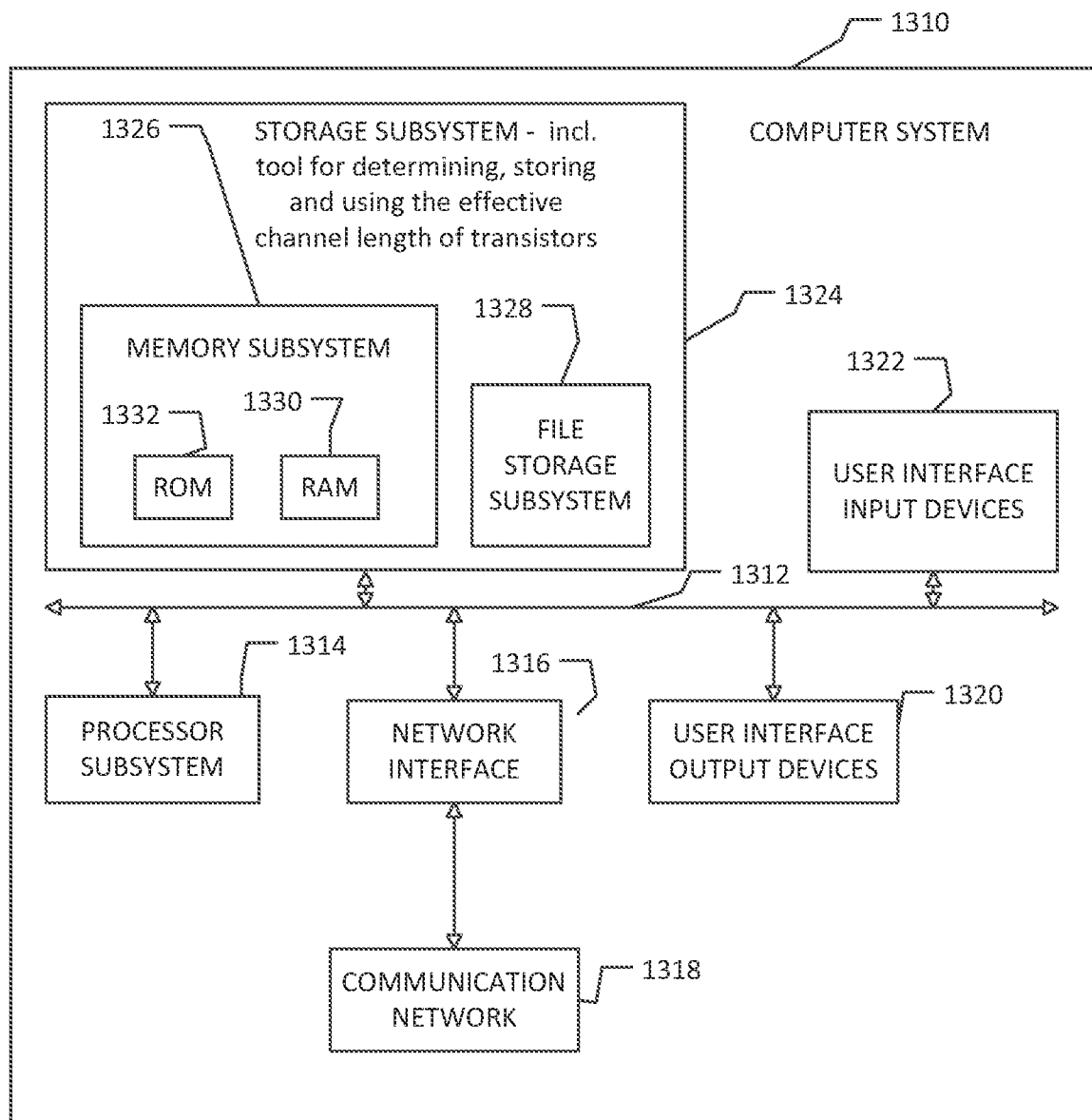


FIG. 12

**FIG. 13**

INTERNATIONAL SEARCH REPORTInternational application No.
PCT/US2014/057637**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 12, 24
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claims 12, 24 are unclear because they refer to multiple dependent claims which do not comply with PCT Rule 6.4(a).
3. ☒ Claims Nos.: 9-11, 21-23
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/057637**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/78(2006.01)i, H01L 21/336(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 29/00; G01R 31/00; G11C 11/34; H01L 29/786; H01L 29/772; H01L 21/66; H01L 23/58; H01L 21/336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: effective channel length, dopant profile, effective volume, cross-sectional area

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002-0142495 A1 (AKIHIRO USUJIMA) 03 October 2002 See abstract, claims 1-8 and figures 1-9.	1-8, 13-20, 25
A	WO 02-058158 A2 (ADVANCED MICRO DEVICES, INC.) 25 July 2002 See abstract, claims 1-3 and figures 2a-3c.	1-8, 13-20, 25
A	US 2012-0228615 A1 (HIDEKI UOCHI) 13 September 2012 See abstract, claims 1-4 and figures 2A-9C.	1-8, 13-20, 25
A	US 2005-0281086 A1 (TOSHIO KOBAYASHI et al.) 22 December 2005 See abstract, claim 1 and figures 1-5.	1-8, 13-20, 25
A	US 2006-0038171 A1 (RYOJI HASUMI et al.) 23 February 2006 See abstract, claims 1-8 and figures 1-15.	1-8, 13-20, 25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

05 January 2015 (05.01.2015)

Date of mailing of the international search report

05 January 2015 (05.01.2015)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/057637

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