DIGITAL VEHICLE DETECTOR

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ABSTRACT

A vehicle detection and traffic control system employing a plurality of detection loops at different locations, such as adjacent a roadway or street intersection, or the like, each controlling the period of a respective oscillator. The oscillator outputs are sequentially scanned by a time-sharing system and digital data corresponding to their periods is stored in respective digital memories. The digital signals from the oscillators are compared with previously stored digital signals and the comparison data thus derived is decoded and may provide commands to operate traffic lights. Manually adjustable sensitivity and timing circuits are provided. Likewise, a drift correction circuit is provided for the oscillators, responding to the comparison data.

12 Claims, 13 Drawing Figures
**Drift Compensation Section**

- Serial % Gain from Fig. 6
- Serial Memory Word from Fig. 11
- New Memory Data
- Borrow

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### Decision Logic

<table>
<thead>
<tr>
<th>Result</th>
<th>Cause</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse</td>
<td>Number of counts accumulated in memory since last pulse = serial timer setting</td>
<td>Issue one drift-compensation pulse</td>
</tr>
<tr>
<td>No pulse</td>
<td>Above not true</td>
<td>None</td>
</tr>
</tbody>
</table>

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**Fig. 10**

- Plug-in matrix or other switch assembly for presetting channel gain
- Switching means for presetting desired presence timer setting
- Seconds
- Minutes

**Fig. 11**

- Binary bit count
- Operator controls (each channel)
- Serial absolute gain

**Fig. 12**

- Multiplexer assembly
- Serial timer setting
This invention relates to vehicle detectors, and more particularly to systems for detecting the presence of motor vehicles of various types adjacent critical areas, such as at intersections between heavily travelled roads and cross roads with less traffic, and employing the detection signals for controlling traffic lights in a manner to increase the efficiency of handling traffic and to minimize delay.

A main object of the invention is to provide a novel and improved vehicle detection and traffic control system which is reliable in operation, which greatly increases the efficiency of handling traffic, as compared with previously employed systems, and which avoids confusion between detection signals obtained from nearby respective detection units forming part of the overall system pattern.

A further object of the invention is to provide an improved vehicle detection and control system which employs digital memories rather than analog memories and which therefore has much higher precision than systems previously employed, which employs a time-sharing arrangement to prevent confusion between cooperative spaced units of the system, and which includes means for adjusting the sensitivity of the elements, for adjusting the time factors involved in the operation of the elements, and for automatically compensating for drift caused by changes in environmental conditions in the area in which the system is installed.

A still further object of the invention is to provide an improved vehicle detection and traffic control system which is relatively easy to install, which employs completely passive detection loop elements, which can detect vehicles of different types, and which is compensated automatically for changes in physical conditions such as temperature and other types of weather conditions, and for changes in supply voltage, or the like.

Further objects and advantages of the invention will become apparent from the following description and claims, and from the accompanying drawings, wherein:

FIG. 1 is a diagrammatic plan view of an intersection between a major traffic road or highway and a cross road, employing an improved vehicle detection and traffic light control system according to the present invention.

FIG. 2 is a diagrammatic plan view of one type of vehicle detection loop assembly which may be employed in a system according to the present invention.

FIG. 3 is a diagrammatic plan view of another type of vehicle detection loop assembly which may be employed in the system of the present invention.

FIG. 4 is a diagram of a typical vehicle detection and traffic control system according to the present invention, showing the electrical parts thereof in block form.

FIG. 5 is a block diagram showing the data acquisition section of a system such as that illustrated in FIG. 4.

FIG. 6 is a block diagram of the main arithmetic section forming part of a system such as that shown in FIG. 4.

FIG. 7 is a diagram illustrating the operating sequence of the oscillators in the system of FIG. 4.

FIG. 8 is a block diagram of the auxiliary arithmetic section forming part of the system of FIG. 4.

FIG. 9 is a block diagram of the presence timer section forming part of the system of FIG. 4.

FIG. 10 is a block diagram of a drift compensation section which may form part of a system such as that illustrated in FIG. 4.

FIG. 11 is a partial block diagram showing manually adjustable elements for adjusting the channel gain and the presence timer setting in a system such as that shown in FIG. 4.

FIG. 12 is a fragmentary perspective view of a portion of a vehicle detection loop assembly adapted to be installed in a roadway in a vehicle detection and traffic control system according to the present invention.

FIG. 13 is a partial block diagram giving a more detailed showing of how the decoding data may be derived at the input side of a decision logic section in the system of FIG. 6 or FIG. 8.

The present invention is directed in general to the detection of metal objects, and more specifically to the detection of vehicles on a road. Traffic control systems depend on the information obtained from vehicle detectors to increase the efficiency of moving traffic with a minimum of delay. As the volume of vehicles increases, the complexity of phasing increases, and the need for better vehicle detection systems becomes an important requirement.

Many types of vehicle detection methods have been employed, such as sonar, microwave, infra-red, the use of magnetometers, and the use of inductance loops. The method employing inductance loops has been the one most widely accepted in the trade. This widespread acceptance is due to the large and precise area over which vehicle detection can be effectively accomplished. In addition, the loops of wire installed in the streets are completely passive and therefore very reliable.

As intersections handle more traffic with increased phasing, a problem arises from the presence of many vehicle oscillators at the same intersection. If two vehicle detectors happen to utilize the same operating frequency an error in detection will result. The prior art at the present time utilizes analog memories to determine the status of changes in inductance due to the relationships of vehicles to pick-up loop inductors. Also, analog memory systems drift due to time, temperature and weather changes, voltage changes, and the like, and these factors can cause errors in time call status. Thus, the traffic trade has a very real need for a reliable vehicle detection system which overcomes these problems.

A prime purpose of the present invention is to provide a satisfactory solution to these problems.

The configuration of the inductor loop installed in the street is an important consideration for obtaining the maximum inductance change caused by vehicles passing in proximity to said loop inductor. A loop configuration which will control the magnetic field in a manner to provide maximum mutual inductive coupling for either horizontal or vertical polarized metal objects will allow the accurate detection of either standard vehicles or motor bikes. Existing loop designs normally utilize a single rectangular geometry which is horizontally polarized only. For the utilization of traffic-actuated signal controllers, the ability to obtain accurate detection of all classes of vehicles becomes a design goal for all traffic signal applications. Rectangular loops will emit horizontally polarized electromagnetic waves, which will provide good mutual inductance cou-
pling to vehicles, which also represent horizontally polarized shorted-turn receivers.

The vehicle receiver reflects an electrical loading similar to a shorted turn, relative to the driven loop in the street. A single rectangular loop design will give good performance for cars, but very poor mutual inductive coupling for motor bikes, which represent vertically polarized receivers. The present invention aims to provide a solution to this problem. The solution consists in utilizing special two-coil configurations, as will be presently described, these configurations being so polarized as to provide a controlled magnetic field which will provide both good vertical and horizontal mutual inductive coupling to all classes of motor vehicles or bikes. The present invention covers the considerations in layout for either a single lane or a double lane approach. This invention also includes a method by which a loop can be installed on an existing highway without sawcuts or requiring asphalt lifts for placement.

In accordance with the present invention, the loop inductors are connected to respective different-frequency oscillators which are sequentially cyclically energized in a time-sharing sequence, and readings corresponding to oscillator frequency, phase shift, or period (indicating channel loop inductance values) are obtained, converted into digital form, and stored in respective digital memories associated with the loop inductors, rather than being stored in analog memories as in past practice.

One of the most important shortcomings of previously employed systems was frequency contamination among many loop amplifiers at the same location, causing false cross-calling of the associated vehicle detectors. The system of the present invention overcomes this problem by having only the controlled oscillator on at any instant in time.

The system of the present invention also overcomes disadvantages of earlier systems by providing rapid auto-tuning to minimize the need for adjustment by technicians, and provides automatic adjustment for changes in environmental conditions, whereby to maintain optimum vehicle detection accuracy.

One of the unique features of the present invention that significantly and materially makes it advantageous over previously employed systems is the use of digital memories. The digital memory for the inductance type metal detector is important due to the small changes in inductance which must be accurately logged. A typical change of inductance in vehicle detection may range from 1.0 percent to as low as 0.01 percent. This may be close to the resolution limit for analog memories, with a drift rate, caused by temperature changes, humidity changes, etc., which exceeds the resolution limit. It is probably for these reasons that earlier systems have had difficulty in achieving a high degree of reliability. In contrast to this, the digital memory is absolutely accurate, with a resolution limited only by the means employed in reading the inductance. A digital memory can have a resolution of from 1 part in 1,000 to 1 part in 1,000,000 with no degradation due to environmental factors. In addition to this feature, in the system of the present invention sensitivity per loop is easily controlled in accordance with the assigned amount of resolution per channel. Furthermore, in the system of the present invention the digital memory can be pre-set for the purpose of dumping errors caused by stalled vehicles on loops, over a preset time period.

Referring to the drawings, FIG. 1 shows a vehicle 11 prior to proceeding over a loop assembly 12 located on the street near the intersection of a cross street 13 with a main highway 14, with a traffic light assembly 15 provided at the intersection. The loop assembly 12 is connected to one of the oscillators 16 shown in FIG. 4.

FIG. 2 shows one form of detection loop assembly 12 which may be employed. The assembly comprises a relatively wide rectangular horizontal outer double loop 17 and a relatively narrow horizontal inner double loop 18 arranged substantially coplanar and connected in parallel with their magnetic fields aiding; the loops are placed to define three rectangles, namely, 1A, 1B and 1C. FIG. 3 shows another form of detection loop assembly 12', providing the same result, comprising two substantially identical horizontal double loops 17' and 18' placed in overlapping substantially coplanar relationship, and also connected in parallel with their magnetic fields aiding, likewise defining three rectangles 2A, 2B and 2C.

The loop assembly may be embedded in a relatively flat body of molded material, such as Fiberglas, shaped in the manner illustrated in FIG. 12, or other suitable highly durable molded material. The body preferably has tapered edges as shown. The assembly forms a prefabricated unit which may be bonded to the road surface at its desired location by means of suitable bonding cement.

FIG. 4 shows in general block form the electrical components of a typical vehicle detector, combined with traffic light control means, which may be associated with traffic intersections such as that shown in FIG. 1. In the typical arrangement of FIG. 4 there are four detection loops 12, corresponding to those shown in FIG. 1, each being connected to a different-frequency oscillator 16, the oscillators being sequentially cyclically keyed, for example, by a rotary switch assembly 21 driven from suitable time-sharing motor drive means 22 forming part of a generalized signal comparison and control unit 20, various portions of which will be presently described. One of the oscillators 16 is more specifically illustrated in FIG. 5, to which further reference will shortly be made.

FIG. 7 illustrates the operating sequence of the keying of the respective oscillators 12 in a typical 4-channel system. Thus, the oscillators are cyclically energized sequentially for respective time periods corresponding to the elongated blocks 23 shown in FIG. 7, each oscillator being turned on as soon as the preceding oscillator is turned off, with a short delay thereafter, shown at 24 for stabilization before the comparison means 20 measures the oscillator period, which occurs in the time segment 25. Comparison means 20 performs its computations in the final small time segment 26 immediately before the oscillator is turned off.

For the given channel, the power is turned on, the oscillator is allowed to operate for the time period 24 to stabilize, and then a precise measurement is made of the oscillator period (during time segment 25) by gating a precision crystal frequency from a crystal clock 27 through a gate 31 into a binary counter 28. The output of the oscillator 16 is supplied to the gate 31 through a frequency divider 32. At the end of the frequency measurement period 25, the number which has accumulated in the binary counter 28 is scanned by a
multiplexer 33 and formatted into a serial digital word which is used for further computations. After all computations are complete on a given channel, the power to the associated oscillator is turned off, and operation proceeds to the next channel. After all channels have been serviced, the operation starts over again at the first channel and again goes through each channel, one by one. In detail, referring to FIG. 5, a binary channel address is received by element 34, one of four decoders defining the channel to be operated at the particular moment. An output signal from this decoder 34 turns on the loop oscillator 16. A signal from the loop oscillator is passed to the frequency divider 32, which averages the oscillator period over a longer time interval, typically 64 counts. The output of divider 32, representing this averaged oscillator period, is gated (by gate 31) with the precision crystal clock 27 and passed to the binary counter 28. After a stabilization period 24, the reset signal will be removed from the binary counter 28 and it will accumulate a count proportional to the period of the loop oscillator 16. When it is through counting, the multiplexer 33 will scan the contents of the binary counter and provide a serial output word at line 35 which is proportional to the oscillator period, and therefore is proportional to the square root of the loop inductance.

Returning to the generalized system shown in FIG. 4, and for the present to a generalized discussion thereof, the block 20 provides a comparison and control means for turning the oscillators on sequentially. It also includes the sequencing and control means such that the appropriate oscillator is scanned and a coded serial reading is taken and stored in the appropriate memory 40 of a digital memory. The comparison means can either be of the frequency, phase shift, or time interval measuring type for indicating a channel inductance value. Control means 20 computes the difference between the present and previous readings of the digital memory segment 40. The block 20 subjects this difference to further conditioning by digital sensitivity block 70 and digital timer block 80, and determines whether a signal that channel is to be issued. If the resultant difference is sufficient, the control block 20 will issue a call for that channel through a decoder 50, and it will be decoded and will be passed to an amplifier 60 and will appear at the output of the amplifier. Block 90 represents a comparator circuit which determines if the new reading is different from the old reading and which will apply a drift correction factor to the digital memory segment 40.

The control means 20 also is responsive to individual channel settings of sensitivity from block 70 or presence for memory from block 80. Although FIG. 4 shows four loop oscillators, it is to be understood that the number of loop oscillators in a system under the concept of the present invention could be expanded to the use of 20 or more, depending on the required application.

Block 50 will maintain the respective loop calls, showing whether metal objects are over a loop or whether the metal object has left the loop detection zone.

Amplifiers 60 provide a means of providing the proper interfaces for respective data collection systems. Elements 60 may provide transistor solid state current sinking, relay isolated interface, or variations, as dictated by the required conditions. The control and comparison means 20 can be run at different speeds so that sampling time can be optimized for either high sensitivity or high sample rate, for determining the period the metal object is over a loop.

The main arithmetic section, in block 20 and shown in FIG. 6, performs all the computations necessary to determine whether there is a car over a loop and whether or not a call should be made to the traffic controller 15 being serviced by the loop detector. Serial data from output line 35 of the data acquisition section (FIG. 5) is compared with stored data in a binary memory 40. This comparison is performed by a subtractor 41. The outputs of this subtraction process are used by the decision logic device 42 to determine whether or not there is a car in the loop 12, and what memory corrections should be made. If the incoming data from line 35 is the same (the subtraction result is zero) as the data stored in the memory 40, this indicates a normal quiescent state, with no car in the loop and no memory correction required. If the incoming data from line 35 is larger in magnitude than the memory date (the subtraction result is negative), this indicates an increase in oscillator period, or a decrease in oscillator frequency, which would indicate that a car is leaving the loop. Under these conditions the memory will be changed to match the date. If, on the other hand, the incoming serial data from line 35 is smaller in magnitude than the memory date (Result: + - ), this indicates that cars may be arriving, and decisions then must be based upon how much smaller is this data. The difference between the serial data from line 35 and the memorized data that will be allowed before action is taken is defined as the "gain," and is a parameter which can be established by the equipment user at the control panel by operating a manual control device, such as by inserting a suitable plug-in element in a switching matrix as shown in FIG. 11, or by operating a suitable switch device. This gain is formatted into a serial binary word in the output line 43 of a multiplexer 44. It is desirable that the gain term in line 43 be a constant percentage of the serial data being utilized from the loop. Therefore, the gain term from line 43 is multiplied by the binary serial number from line 35 in the serial multiplier 45. The resulting small binary number in output line 46, proportional to percentage gain, is subtracted from the output of subtractor 41 in a subtractor 47. The results of this subtraction appear in a line 48, supplying it to the decision logic device 42.

If the output of subtractor 47 is negative, a car may be arriving, but the signal change may not yet be large enough to exceed the established gain threshold. No output action will be taken, but the memory data will be allowed to decrease only by one binary count each computational cycle. This establishes the maximum rate at which a car may creep into the detection loop without causing the threshold to be exceeded.

If the output of subtractor 47 is positive (Result: + + ), the threshold has been exceeded, namely, a car definitively has arrived. A call will be issued at output line 49, and corrections will cease to be made to the memory in order that it may hold memorized the previous value until the car goes away. A signal will be issued at output line 51 to the presence timer 80 (FIG. 9) in order to time-out the length of time a car is allowed to indicate its presence within the loop. This timer can be preset (see FIG. 11) by the equipment user to times from 0.1 sec. to 20 minutes, and is used to remove a
call from a channel after the timer has run out, even through a car may still be in the loop. The output line 52 of the timer setting device shown in FIG. 11 is gated to a 14-bit binary decrementing counter (FIG. 9) comprising a 14-bit serial binary memory 53 and a subtractor 54. Under normal operation, one bit will be subtracted from the memory on each computation cycle, resulting in the binary decrementing counter operation.

A serial binary word in line 52, representing the desired maximum setting, is brought in from the control panel adjusting device (FIG. 11). This maximum timer setting will be inserted in the memory 53 in place of its current number under control of the memory correction logic device 55 whenever commanded by the main arithmetic unit (FIG. 6) at output line 51 or by the auxiliary arithmetic unit (FIG. 8) at an output line 56. Whenever neither arithmetic unit is commanding the timer to be reset to maximum, the timer will run, decreasing towards zero. A decision logic device 57 watches the output of subtractor 54 and detects when the timer reaches zero. At this time a timer-equals-zero signal will be issued at the output line 58 and the memory 53 will cease decrementing.

Referring to FIG. 6, the timer-equals-zero signal, at an output line 59, enters a memory correction logic device 61 and causes the serial data from the traffic loop to be placed in memory 40 in place of the memory's previous contents. This erases all prior indication of a car in the loop, and the channel is reverted to a normal quiescent state, ready for additional traffic if it should arrive.

The auxiliary arithmetic section shown in FIG. 8 provides a valuable new function. With previous traffic detectors there was no means to distinguish between a car stalled in a loop and a long cue of cars travelling over the loop. When a car is stalled in the loop, it is desirous to have the presence timer (FIG. 9) time-out and therefore remove a call from the intersection traffic controller. On the other hand, with a long cue of cars travelling over the loop, it is not desirous for the timer to time-out, but rather the call should continue being placed to the controller from that traffic movement. The auxiliary arithmetic section in effect watches for traffic movement within the loop while a call is in effect, and resets the presence timer to maximum whenever such traffic movement occurs. Operation is very similar to that of the main arithmetic section (FIG. 6) except that when the threshold is exceeded, a single pulse output occurs in line 56 which resets the presence timer 80. Referring to FIG. 8, serial data in line 35 is compared with data in a line 62 from a binary memory device 63, in subtractor 64. The results are used by a decision logic device 65. The desired gain for determining whether a threshold has been exceeded is usually different for the auxiliary function than for the main function. Therefore, a serial percentage gain signal from line 46 is brought in and multiplied by a decision gain change signal in a line 66 in a serial multiplier 67 before being furnished to the second subtractor 68. The output of subtractor 68 is furnished by a line 69 to decision logic device 65 and is then utilized in a manner similar to that of the main arithmetic section to determine whether or not to reset the timer to maximum and to reset the memory 63.

FIG. 10 illustrates a computation device utilized to correct for drift in a loop inductor during the time that a car is present on the loop and the presence timer is running. Should a car go away before the timer runs out, it is important that the main arithmetic section recapture normal operation and remove a call to the intersection controller. The drift compensation section of FIG. 10 provides a small negative drift to the main memory to assure that this occurs. The rate at which the main memory can be drifted is proportional to the gain setting and inversely proportional to the timer setting, that is, it can be drifted for very low gains, wherein a large absolute gain number is used in the main arithmetic section. A greater drift can be allowed, on the other hand, for very long timer settings; a lesser drift can be allowed per unit of time. The desired drift function then is proportional to gain divided by timer setting. A 14-bit memory 71 in conjunction with a subtractor 72 is operated as a binary decrementing counter and is decremented each computational cycle by the binary serial percentage gain from the line 46. A borrow from the subtractor 72 is compared by bygate 73 with the serial timer setting signal from line 52. The result will be a pulse output whenever the decrementing counter borrows past the pulse position of the serial timer setting binary word (from line 52). The resulting output, at output line 74, from a decision logic device 75, which receives the bygate resultant signal from the bygate output line 76, will be (gain) pulses, for each timer setting. These pulses are applied to the drift compensation input of the main arithmetic section (FIG. 6), resulting in decreasing the memory value by one count each time a drift compensation pulse is applied, thereby providing a downward drift rate proportional to gain divided by timer setting.

FIG. 11 schematically illustrates the operating panel controls for gain and timer settings previously mentioned. A suitable switching device, such as a plug-in matrix assembly 77, is provided for presetting the gain in each channel. Thus, for each channel a manually changeable plug-in diode assembly 101 may be employed with the matrix, to place the appropriate diode in the channel circuit, corresponding to a desired preset gain. The setting of the matrix assembly 101 is an equivalent switching device, is scanned by multiplexer 98 and is formatted into a binary signal word, carried on output line 43, proportional to the desired setting. Similar plug-in matrix switching assemblies may be employed in the presence timer presetting assembly 78 for establishing the desired presence timer setting for each channel. The output of the control assembly 78, which may be in accordance with a setting for seconds or minutes of a two-position manually operated selector switch 81, is scanned by a multiplexer 79 and is formatted into a serial binary word, appearing at the output line 52, proportional to the desired binary timer setting. The serial gain and serial timer settings are then presented to the arithmetic sections of the system in the manner previously described.

FIG. 13 is a more detailed showing of how the decoding data is achieved in connection with the decision logic device 42 of FIG. 6, or in connection with the corresponding decision logic device 65 of FIG. 8. Thus, as shown in FIG. 13, the "change in period" data from subtractor 41 is fed through a "zero detector" 102 to the corresponding input of decision logic device 42; this data is also fed through a "less than zero" detector 103 to a corresponding input of device 42 through an "OR" gate 104 which also receives the signal from "zero detector" 102. The data in line 48 from sub-
tractor 47 is fed through a “less than zero” detector 105 to the corresponding input of device 42, and the signals from detectors 103 and 105 are supplied to a corresponding input of device 42 through an “AND” gate 106.

While a specific embodiment of an improved vehicle detection and traffic control system has been disclosed in the foregoing description, it will be understood that various modifications within the spirit of the invention may occur to those skilled in the art. Therefore it is intended that no limitations be placed on the invention except as defined by the scope of the appended claims.

What is claimed is:

1. In combination with a plurality of traffic lanes leading to an intersection, a vehicle detection and traffic control system comprising a plurality of detection loops mounted in respective traffic lanes for inductive conduction with vehicles approaching the intersection, respective oscillators operatively connected to the loops so that said loops control the periods of the oscillators and so that said periods are changed by vehicles on said lanes approaching said intersection, time-sharing means to sequentially scan the oscillator outputs, means to derive data corresponding to the periods of the oscillators, respective memories associated with the oscillators, means to store the time-shared data in said respective memories, means to compare data furnished to the memories with previously stored data therein and to derive comparison data, traffic signal means, and means including time-sharing decoding means to furnish commands to said traffic signal means in accordance with the comparison data.

2. The vehicle detection and traffic control system of claim 1, and wherein the derived, stored and comparison data is in digital form.

3. The vehicle detection and traffic control system of claim 2, and means to prevent commands to said traffic signal means unless said comparison data exceeds a predetermined lower limit digital value.

4. The vehicle detection and traffic control system of claim 3, and means for variably presetting said lower limit value.

5. The vehicle detection and traffic control system of claim 3, and means to limit the length of time that a vehicle is allowed to indicate its presence over a loop and maintain a command to said traffic signal means.

6. The vehicle detection and traffic control system of claim 3, and means to substitute the last-derived digital comparison data for the previously stored digital comparison data in the associated memory after a predetermined time period and to terminate its command to said traffic signal means.

7. The vehicle detection and traffic control system of claim 6, and means for variably presetting said time period.

8. The vehicle detection and traffic control system of claim 6, and wherein said substitution means comprises a decrementing digital presence timer settable to a maximum timing value, and means to set said timer to a maximum responsive to the detection of movement of a vehicle over a loop, whereby to maintain its command during said timing value while such movement continues.

9. The vehicle detection and control system of claim 8, and means to provide a small negative drift to said associated memory, comprising a binary decrementing counter decremented each computational cycle and connected to said memory and including means to provide a downward drift rate proportional to said lower limit value divided by the timer setting.

10. The vehicle detection and traffic control system of claim 1, wherein the derived, stored and comparison data is in digital form, means to prevent commands to said traffic signal means unless said comparison data exceeds a predetermined lower limit digital value, and means to substitute the last-derived digital comparison data for the previously stored digital comparison data in the associated memory after a predetermined time period and to terminate its command to said traffic signal means, wherein said substitution means comprises a decrementing digital presence timer settable to a maximum timing value, means to set said timer to maximum responsive to the detection of movement of a vehicle to a position over a loop, whereby to maintain its command during said timing value, means to terminate said command at the end of said maximum timing value if no further movement of the vehicle occurs, and means to reset said timer to maximum when the vehicle resumes movement before the end of said maximum timing value.

11. The vehicle detection and traffic control system of claim 1, wherein each detection loop comprises an inductor arranged to define a plurality of adjacent elongated detection areas extending in the direction of the associated traffic lane.

12. The vehicle detection and traffic control system of claim 11, and wherein each detection loop is arranged to define three elongated side-by-side detection areas.

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