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(54) **Title:** CIRCUITRY AND METHOD FOR REDUCING AREA AND POWER OF A PIPELINE ADC

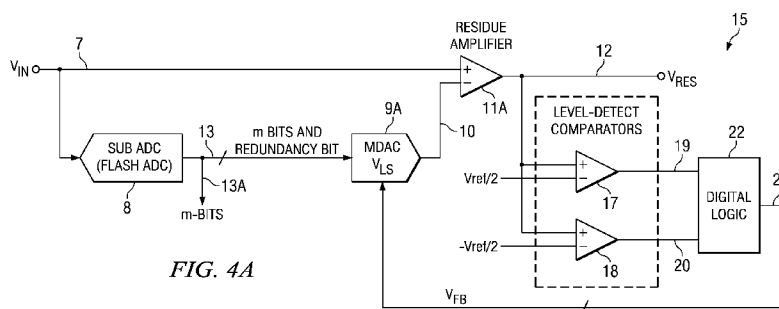


FIG. 4A

(57) **Abstract:** A pipeline ADC (analog-to-digital converter) (14) includes a residue amplifier (7) for applying a first residue signal (V_{res1}) to a first input of a residue amplifier (11A) and to an input of a sub-ADC (8) for resolving a predetermined number (m) of bits and producing a redundancy bit in response to the first residue signal. A level-shifting MDAC (9A) converts the predetermined number of bits and the redundancy bit to an analog signal (10) on the a second input of the residue amplifier, which amplifies the difference between the first residue signal and the analog signal to generate a second residue signal (V_{res2}). The MDAC causes the residue amplifier to shift the second residue signal back within a predetermined voltage range ($\pm V_{ref}/2$) by the end of the amplifying if the second residue signal is outside of the predetermined voltage range.

CIRCUITRY AND METHOD FOR REDUCING AREA AND POWER OF A PIPELINE ADC

[0001] This relates generally to improvements which increase the linearity of pipeline ADCs (analog-to-digital converters), and more particularly to improvements which substantially reduce the number of “next stage comparators” and the amount of integrated circuit chip area and power dissipation of pipeline ADCs.

BACKGROUND

[0002] A pipeline ADC includes a sequence of pipeline ADC stages. FIG. 1 shows a single conventional pipeline ADC stage 1 wherein an analog input signal V_{IN} is applied by conductor 7 to the input of a sub-ADC 8 and to the (+) input of a residue amplifier 11. Sub-ADC 8 typically is implemented by means of a flash ADC. The digital output of sub-ADC 8 is applied to the input of a conventional multiplier DAC (MDAC) 9, the output of which is applied to the (-) input of residue amplifier 11, which produces a residue voltage V_{RES} on conductor 12. A residue plot for pipeline ADC stage 1 is shown in FIG. 2. (A flash ADC typically includes a string of equal resistors connected in series as a voltage divider between a pair of reference voltages to generate individual reference voltages on various circuit nodes or tap points between the respective resistors. Each individual reference voltage may be connected to the (+) input of a corresponding comparator, and the (-) input of each comparator may be connected to an analog input voltage. The comparator outputs provide a digital representation of the analog input voltage.)

[0003] In the operation of a conventional pipeline ADC there is just one amplification phase, which is called a hold phase because it is accomplished by means of a sample/hold circuit wherein V_{IN} is sampled during a sample phase and amplified during a hold phase. The accuracy with which the sampling and amplification needs to be performed depends on the resolution of the pipeline ADC.

[0004] Various errors generated in the known pipeline ADCs cause nonlinear operation thereof. One source of error is random input offset voltages of the flash comparators of the various stages. Another source of error is random input-referred input offset voltages of the

residue amplifiers of the various stages. Yet another error is due to variations in the series-connected resistors of the flash ADCs.

[0005] The sub-ADC 8 of FIG. 1 typically generates m bits of sub-ADC code, plus a redundancy bit, if needed, to allow correction of some of the above errors. A known technique for eliminating the effect of the foregoing sources of error on the linearity of a pipeline ADC is referred to as providing “redundancy” in the various pipeline ADC stages. The redundancy is accomplished by providing sub-ADCs with a larger number of bits than the number of bits to be resolved by the various stages, respectively. For example, addition of one or more redundancy bits to the sub-ADC in each pipeline ADC stage except the first stage introduces redundancy, and the redundancy is effective to correct sub-ADC errors generated in the previous stage. For example, if the sub-ADC of a stage of the pipeline ADC is required to resolve 3 bits, then providing a fourth bit introduces redundancy by providing one additional bit of resolution in the sub-ADC of the next pipeline ADC stage. The redundancy provides additional range for the swing of the residue amplifier output voltage, and that additional range is used to correct for the error generated in the previous stage. However, the redundancy bit is not used as part of the sub-ADC code generated by that sub-ADC. (In an ideal circuit, the sub-ADC would not have any error so no redundancy bit would be required.)

[0006] An ideal pipeline ADC stage that resolves n effective bits has an n -bit sub-ADC and therefore 2^n comparators in the sub-ADC. The gain of the residue amplifier of the stage also needs to be 2^n . However, in the presence of redundancy of 1-bit, the sub-ADC resolution has to be increased to $(n+1)$ bits and therefore the number of comparators has to be increased to 2^{n+1} . The residue amplifier gain still remains equal to 2^n . In other words, the gain of the residue amplifier is reduced by a factor of $\frac{1}{2}$ as compared to the resolution of the sub-ADC. Since the gain of the residue amplifier is reduced by half, its output voltage V_{RES} then will have a dynamic range that spans $\pm V_{ref}/2$, rather than $\pm V_{ref}$ as in the ideal case wherein there are no errors in the sub-ADC comparators. The extra dynamic range between $-V_{ref}$ and $-V_{ref}/2$ and between $+V_{ref}/2$ and $+V_{ref}$ corresponds to be the actual “redundancy” that is “used” to correct errors in the sub-ADC comparators of the pipeline ADC stage. In summary, the pipeline ADC stage with redundancy requires double the number of comparators in the sub-ADC as compared to an ideal pipeline ADC stage.

[0007] The ideal pipeline ADC stage which has no errors from the sub-ADC requires ideal comparators that have zero input-referred offset. Since this is not achievable in practice, redundancy is added, as explained above, in the conventional pipeline ADC stage. Redundancy makes the design of the sub-ADC feasible, but the comparator input offset specification is still “tight” enough to necessitate use of a preamplifier stage in each of the comparators to amplify the comparator input signal before it is passed on to a latch that makes the comparator decision. The preamplifier stage in each comparator requires undesirably large amounts of additional chip area and power dissipation. This limitation is especially large for ADCs having higher than 10-bit resolution.

[0008] A drawback of using a redundancy bit in a pipeline ADC stage is that the number of flash ADC comparators in the pipeline ADC stage must be doubled.

[0009] Since the residue voltage V_{RES} produced by the residue amplifier of each pipeline ADC stage needs to be able to swing accurately between $\pm V_{ref}$, the first stage (or first few stages) of a high-resolution pipeline ADC requires the residue amplifier of each such stage to have high DC gain and high bandwidth. Unfortunately, this complicates the design of the residue amplifier of each pipeline ADC stage. A technique that has been used to solve the design complications is referred to as “reference scaling”, and is disclosed in commonly assigned US patent 7,161,521 entitled “Multi-Stage Analog to Digital Converter Architecture” issued January 9, 2007 to Nandi et al.; this patent is entirely incorporated herein by reference. In the reference scaling technique, the gain of the residue amplifier of the flash ADC of each pipeline ADC stage following the first stage is reduced further by a factor of 2. The gain of the residue amplifier for a pipeline ADC stage that resolves n “effective” bits is made equal to 2^{n-1} , instead of 2^n . In this way, the output swing of the residue amplifier is reduced by a factor of 2. In the presence of sub-ADC errors, the maximum output swing of the residue amplifier is limited to $\pm V_{ref}/2$, as compared to $\pm V_{ref}$ in case of the conventional stage. (The output swing of an ideal pipeline stage is $\pm V_{ref}/4$ when the reference scaling technique is used, as opposed to $\pm V_{ref}/2$ for a conventional stage.)

[0010] When reference scaling is used, the residue amplifier output voltage has to swing between $\pm V_{ref}/2$. This allows design of the residue amplifier to be substantially simplified. However, a disadvantage of reference scaling is that the input offset specification requirements are substantially increased for the flash ADC comparators in the sub-ADC of the next pipeline

ADC stage. That makes it necessary to use substantially larger, substantially more power-consuming comparator circuitry. Reference scaling reduces residue amplifier output voltage swing, and also reduces the DC gain and bandwidth requirements of the residue amplifier. Unfortunately, this tightens the input offset specification requirement of the flash ADC comparators of the following stage. The next pipeline ADC stage requires 2^{m+1} comparators to span an input range from $-V_{ref}/2$ to $+V_{ref}/2$, where m is the number of bits to be resolved by that pipeline ADC stage. In the absence of the previously mentioned error sources, only 2^m comparators spanning $-V_{ref}/2$ to $+V_{ref}/2$ would be needed. For example, a 12-bit ADC having four 3-bit pipeline ADC stages arranged in a 3-3-3-3 configuration would require a total of 56 flash ADC comparators. If reference scaling is used, the cost and power dissipation of the pipeline ADC would be substantially increased because each flash ADC comparator would need to be composed of substantially larger, substantially more power-consuming circuitry. Although the reference scaling architecture solves the previously mentioned problems caused by large residue amplifier output voltage swings, reference scaling does not change the requirement of doubling the number of flash ADC comparators if redundancy bits are introduced.

[0011] FIG. 3 is a copy of FIG. 7A of above-mentioned patent 7,161,521, and illustrates a conventional flash ADC 8 which may be used as the sub-ADC in block 8 of FIG. 1. Flash ADC 8 includes comparators 710-1 through 710- 2^{q+1} are connected to comparators 710-1 and $2^{q+2}+1$ equal resistors 730A-730Z. Flash ADC 8 is assumed to be generating a q -bit sub-code based on a differential reference input REFP-REFM which is equal to V_{ref} . Resistors 730A-730Z operate as a resistor ladder network which divides the foregoing reference voltage V_{ref} into equal voltage steps. The resistor ladder network generates 2^{q+2} levels, the 2^{q+1} level middle half of which are connected to the (+) inputs of comparators 710-1 through 710- 2^{q+2} . Note that one-fourth of the generated 2^{q+2} levels located on each side, respectively, of the middle half are not connected to any comparator inputs. (It should be understood that 2^q comparators and 2^{q+1} resistors, would be required in the case of a single-ended implementation.) Comparators 710-1 through 710- 2^{q+1} provide a q -bit sub-code by comparing the differential analog input signal InpP-InpM with the corresponding 2^{q+1} middle half levels generated by the resistor ladder network. As a result, the differential analog input signal InpP-InpM is compared within the dynamic range of REFP/2 and REFM/2. The output of the flash ADC comparators represents a sub-code generated by

sub-ADC 8.

[0012] There is a need for an accurate, linear pipeline ADC which requires substantially less integrated circuit chip area and power dissipation than prior pipeline ADCs that have otherwise essentially similar performance.

[0013] There also is a need for an accurate, linear pipeline ADC which avoids problems associated with pipeline ADCs that utilize reference scaling.

[0014] There also is a need for a technique for reducing the difficulty of designing the components of a high-resolution pipeline ADC.

SUMMARY

[0015] It is an object of the invention to provide an accurate, linear pipeline ADC and method which require substantially less integrated circuit chip area and power dissipation than prior pipeline ADCs that have otherwise essentially similar performance.

[0016] It is another object of the invention to provide an accurate, linear pipeline ADC which avoids problems associated with pipeline ADCs that utilize reference scaling.

[0017] It is another object of the invention to provide a technique for reducing the difficulty of designing the sub-ADC of a high-resolution pipeline ADC.

[0018] It is another object of the invention to provide a technique for reducing the number of comparators required in the flash ADC of a next pipeline ADC stage in a pipeline ADC when redundancy bits are used.

[0019] It is another object of the invention to provide an improved way of limiting the output voltage swing of a residue amplifier to voltage to levels between $\pm V_{ref}/2$ without using the known reference scaling technique.

[0020] In accordance with one embodiment, the invention provides a pipeline ADC (analog-to-digital converter) (14) which includes a residue amplifier (7) for applying a first residue signal (V_{res1}) to a first input of a residue amplifier (11A) and to an input of a sub-ADC (8) for resolving a predetermined number (m) of bits and producing a redundancy bit in response to the first residue signal. A level-shifting MDAC (9A) converts the predetermined number of bits and the redundancy bit to an analog signal (10) on a second input of the residue amplifier, which amplifies the difference between the first residue signal and the analog signal to generate a second residue signal (V_{res2}). The MDAC causes the residue amplifier to shift the second residue signal back within a predetermined voltage range ($\pm V_{ref}/2$) by the end of the amplifying

if the second residue signal is outside of the predetermined voltage range.

[0021] In one embodiment, the invention provides a pipeline ADC (analog-to-digital converter) (14) including a pipeline ADC stage (15) including a residue amplifier (11A) having a first (+) input coupled to receive a first residue signal (e.g., V_{res1}) of a previous ADC stage (e.g., 15-1 or 15-2). A first sub-ADC (8) has an input coupled to receive the first residue signal (V_{res1}) for resolving a predetermined number (m) of bits and producing the predetermined number (m) of bits and a redundancy bit in response to the first residue signal (V_{res1}). A first DAC (digital-to-analog converter) (9A) converts the predetermined number (m) of bits and the redundancy bit to an analog signal (10) applied to a second (-) input of the residue amplifier (11A). The DAC (9A) has a level-shifting input (V_{LS}) for receiving a feedback signal (V_{FB}), the residue amplifier (11A) amplifying a difference between the residue signal (V_{res1}) and the analog signal (10) to generate a second residue signal (V_{res2}). Level-detect circuitry (17,18,22) receives the second residue signal (V_{res2}) and generates the first feedback signal (V_{FB}) if the second residue signal (V_{res2}) is outside of a predetermined voltage range ($\pm V_{ref}/2$) so as to cause the first DAC (9A) to shift the second residue signal (V_{res2}) back within the predetermined voltage range ($\pm V_{ref}/2$) by the end of the amplifying. In one embodiment, the previous ADC stage is essentially the same as the pipeline ADC stage (15). In one embodiment, the predetermined voltage range is equal to one half of a reference voltage (V_{ref}) applied to the DAC (9A).

[0022] In one embodiment, the previous ADC stage is a first ADC stage (15-1) of the pipeline ADC (14). In one embodiment, the sub-ADC (8) includes 2^m comparators the outputs of which produce the resolved bits, where m is an effective number of bits resolved by the pipeline ADC stage, excluding the redundancy bit. In one embodiment, the first sub-ADC (8) is a m bit flash-ADC. In one embodiment, the DAC (9A) includes an MDAC (multiplying DAC).

[0023] In one embodiment, the level-detect circuitry (17,18,22) includes first (17) and second (18) comparators each having an output coupled to an input of a logic circuit (22), a first input (+) of each of the first (17) and (18) comparators being coupled to the second residue signal (V_{res2}), a second input (-) of the first comparator (17) being coupled to a first reference voltage ($+V_{ref}/2$) which corresponds to an upper end of the predetermined voltage range ($\pm V_{ref}/2$), a second input (-) of the second comparator (18) being coupled to a second reference voltage ($-V_{ref}/2$) which corresponds to a lower end of the predetermined voltage range

($\pm V_{\text{ref}}/2$), an output of the logic circuit (22) providing the feedback signal (V_{FB}). In one embodiment, the level-detect circuitry (17,18,22) operates in accordance with the truth table:

if $-V_{\text{ref}}/2 < V_{\text{res}}(\text{coarse}) < V_{\text{ref}}/2$, then $V_{\text{FB}} = \text{zero}$ (so that V_{RES} is not shifted);

if $V_{\text{ref}}(\text{coarse}) > V_{\text{ref}}/2$, then $V_{\text{FB}} = -V_{\text{ref}}$ (so that V_{RES} is shifted by $-V_{\text{ref}}$); and

if $V_{\text{ref}}(\text{coarse}) < -V_{\text{ref}}/2$, then $V_{\text{FB}} = +V_{\text{ref}}$ (so that V_{RES} is shifted by $+V_{\text{ref}}$),

where V_{ref} is a reference voltage of the pipeline ADC (14), $V_{\text{res}}(\text{coarse})$ is a pre-amplified value of the second residue signal (V_{res2}), and V_{FB} is the feedback signal.

[0024] In one embodiment, the comparators of the sub-ADC (8) are dynamic comparators. In one embodiment, the residue amplifier (11A), the DAC (9A), and sample/hold circuitry are combined in a single circuit module (32).

[0025] In one embodiment, the amplifying includes a pre-amplification phase without shifting the value of the second residue signal (V_{res2}) in response to the feedback signal (V_{FB}), followed by a main amplification phase which includes shifting of the second residue signal (V_{res2}) in response to the feedback signal (V_{FB}) to keep the second residue signal (V_{res2}) within the predetermined voltage range ($\pm V_{\text{ref}}/2$). In one embodiment, the pre-amplification phase occurs with substantially lower accuracy than the main amplification phase.

[0026] In one embodiment, the level-shifting circuitry (64,60A,60B) has an input (23) coupled to the first input (31A,31B) of the residue amplifier (11A). The level-shifting circuitry (64,60A,60B) causes the residue amplifier (11A) to produce:

a zero level shift of an output (OUTP-OUTM) of the residue amplifier (11A) in response to a "0" level of the feedback signal (V_{FB}),

a first polarity level shift ($+V_{\text{ref}}$) of the output (OUTP-OUTM) of the residue amplifier (11A) in response to a "1" level of the feedback signal (V_{FB}), and

a second polarity level shift ($-V_{\text{ref}}$) of an output (OUTP-OUTM) of the residue amplifier (11A) in response to a "-1" level of the feedback signal (V_{FB}).

[0027] In one embodiment, the invention provides a method of operating a pipeline ADC (analog-to-digital converter) (14) including a pipeline ADC stage (15), the method including applying a first residue signal (e.g., V_{res1}) to a first (+) input of a residue amplifier (11A) and to an input of a sub-ADC (8) for resolving a predetermined number (m) of bits; operating the sub-ADC (8) to produce the predetermined number (m) of resolved bits and a redundancy bit in response to the first residue signal (e.g., V_{res1}); converting the predetermined number (m) of

resolved bits and the redundancy bit to an analog signal (10) and applying the analog signal (10) to a second (-) input of the residue amplifier (11A); amplifying the difference between the first residue signal (V_{res1}) and the analog signal (10) to generate a second residue signal (V_{res2}); and if the second residue signal (V_{res2}) is outside of a predetermined voltage range ($\pm V_{ref}/2$), then causing the residue amplifier (11A) to shift the second residue signal (V_{res2}) back within the predetermined voltage range ($\pm V_{ref}/2$) by the end of the amplifying phase. In one embodiment, the method includes operating level-detect circuitry (17,18,22) in accordance with the truth table:

if $-V_{ref}/2 < V_{res}(\text{coarse}) < V_{ref}/2$, then $V_{FB} = \text{zero}$ (so that V_{RES} is not shifted);

if $V_{res}(\text{coarse}) > V_{ref}/2$, then $V_{FB} = -V_{ref}$ (so that V_{RES} is shifted by $-V_{ref}$); and

if $V_{res}(\text{coarse}) < -V_{ref}/2$, then $V_{FB} = +V_{ref}$ (so that V_{RES} is shifted by $+V_{ref}$),

where V_{ref} is a reference voltage of the pipeline ADC (14), $V_{res}(\text{coarse})$ is a pre-amplified value of the second residue signal (V_{res2}), and V_{FB} is the feedback signal.

[0028] In one embodiment, the method includes utilizing a DAC (digital-to-analog converter) (9A) having a level-shifting input (23) to shift the second (-) input of the residue amplifier (11A) so as to superimpose a level shift on the second residue signal (V_{res2}) so as to shift it back within the predetermined voltage range.

[0029] In one embodiment, the method includes providing 2^{m-1} comparators in the sub-ADC (8).

[0030] In one embodiment, the invention provides a pipeline ADC (analog-to-digital converter) (14), including means (7) for applying a first residue signal (e.g., V_{res1}) to a first (+) input of a residue amplifier (11A) and to an input of a sub-ADC (8) for resolving a predetermined number (m) of bits; means (710-1,2...730A,B... in FIG. 3) in the sub-ADC (8) for producing the predetermined number (m) of bits and a redundancy bit in response to the first residue signal (e.g., V_{res1}); means (9A) for converting the predetermined number (m) of bits and the redundancy bit to an analog signal (10) and applying the analog signal (10) to a second (-) input of the residue amplifier (11A); means (FIG. 7A) for amplifying the difference between the first residue signal (V_{res1}) and the analog signal (10) to generate a second residue signal (V_{res2}); and means (17,18,22,9A) for causing the residue amplifier (11A) to shift the second residue signal (V_{res2}) back within the predetermined voltage range ($\pm V_{ref}/2$) by the end of the amplifying if the second residue signal (V_{res2}) is outside of a predetermined voltage range

($\pm V_{ref}/2$).

BRIEF DESCRIPTION OF THE DRAWINGS

- [0031] FIG. 1 is a block diagram of a conventional pipeline ADC stage.
- [0032] FIG. 2 is a residue plot of the conventional pipeline ADC stage of FIG. 1.
- [0033] FIG. 3 is a diagram of a sub-ADC which may be used in block 8 of FIG. 1.
- [0034] FIGS. 4A is a block diagram of a pipeline ADC stage in accordance with the invention.
- [0035] FIG. 4B is a block diagram of a pipeline ADC including a sequence of the pipeline ADC stages shown in FIG. 4A.
- [0036] FIG. 5A is a timing diagram for the pipeline ADC stage of FIG. 4A.
- [0037] FIG. 5B is a similar timing diagram for the pipeline ADC stage of FIG. 4A, but corresponding to FIGS. 7A and 7B.
- [0038] FIG. 5C is a similar timing diagram for the pipeline ADC stage of FIG. 4A, but corresponding to FIG. 8.
- [0039] FIG. 6 is a plot of the residue curve of the pipeline ADC stage of FIG. 4A for both pre-amplification and main-amplification.
- [0040] FIG. 7A is a detailed schematic diagram of the residue amplifier in block 11A.
- [0041] FIG. 7B is a more detailed schematic diagram of the residue amplifier in block 11A which illustrates level shift circuitry associated with the circuitry shown in Fig7A.
- [0042] FIG. 8 is a detailed schematic diagram of a dynamic comparator circuit which may be utilized in blocks 17 and 18 of FIG. 4A.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

- [0043] An improvement to conventional “pipeline ADC stages” for a pipeline ADC is provided which avoids the need to double the number of flash ADC comparators of a “next” pipeline ADC stage when redundancy bits are used to improve the linearity of the pipeline ADC. The improvement is accomplished by using residue voltage level detecting circuitry which detects an out-of-range excursion of the residue voltage and accordingly provides feedback that shifts the residue voltage back into the desired range for each pipeline ADC stage following the first stage.
- [0044] FIG. 4A shows a new pipeline ADC stage 15 wherein analog input signal V_{IN} (which typically is the residue voltage of a previous pipeline ADC stage) is applied by conductor

7 to the input of a sub-ADC 8 and also to the (+) input of a residue amplifier 11A. Sub-ADC 8 may be implemented by means of a flash ADC 8, which is commonly used in conventional pipeline ADCs. Flash ADC 8 in FIG. 4A is similar to the one shown in Prior Art FIG. 3 except that the number of resistors is equal to $2^{q+1}+1$, as there are no untapped resistors at the top and bottom of the resistor string. The total number of comparators in sub-ADC 8 of FIG. 4A is equal to 2^{q+1} . In accordance with the embodiment of the invention shown in FIG. 4A, the number of comparators is reduced by half, ie., to 2^q , whereas the resistor string is the same as in Prior Art FIG. 3, and this is applicable for the flash ADC of all stages of the pipeline ADC except the first stage.

[0045] In FIG. 4A, the digital output of sub-ADC 8 is applied via bus 13 to the input of a MDAC 9A, the output conductor 10 of which is connected to the (-) input of residue amplifier 11A. MDAC 9A also receives a feedback signal V_{FB} produced on conductor or bus 23 by level-detect circuitry including residue-level-detect comparators 17 and 18 and digital logic circuit 22. Residue amplifier 11A produces an output voltage or residue voltage V_{RES} on conductor 12, which is connected to the (+) inputs of comparators 17 and 18. The (-) inputs of comparators 17 and 18 are connected to comparator threshold voltages $V_{ref}/2$ and $-V_{ref}/2$, respectively. A residue plot for pipeline ADC stage 15 is shown in FIG. 6. Subsequently described FIGS. 7A and 7B clarify how the feedback levels $\pm V_{ref}$ are superimposed on the normal output of MDAC 9A.

[0046] Pipeline ADC stage 15 of FIG. 4A helps to avoid costs/drawbacks associated with using the prior art reference scaling technique by connecting output 12 of residue amplifier 11A to the (+) inputs of level-detect comparators 17 and 18, which have input threshold voltages set at $-V_{ref}/2$ and $+V_{ref}/2$, respectively. In the presence of amplified errors generated in the previous stage, if V_{RES} swings beyond $\pm V_{ref}/2$, then one of level-detect comparators 17 and 18 switches and causes logic circuitry 22 to accordingly send a level-shifting feedback voltage V_{FB} to MDAC 9A via bus 23. The outputs 19 and 20 of level-detect comparators 17 and 18, respectively, are applied to inputs of digital logic 22, the output 23 of which is connected to a level-shift input V_{LS} input of level-shifting MDAC 9A. The feedback voltage V_{FB} produced in response to level-detect comparators 17 and 18 is used to prevent V_{RES} from going outside of the range between $\pm V_{ref}/2$.

[0047] Level-detect comparators 17 and 18 detect whether residue amplifier output

voltage V_{RES} is between $\pm V_{ref}/2$ (and therefore also detect whether V_{RES} is higher than $+V_{ref}/2$ or lower than $-V_{ref}/2$). Digital logic circuit 22 produces no feedback on bus 23 if V_{RES} is between $\pm V_{ref}/2$. However, if V_{RES} is less than $-V_{ref}/2$, then digital logic circuit 22 produces a $+V_{ref}$ level on feedback bus 23. If V_{RES} is greater than $+V_{ref}/2$, then digital logic circuit 22 produces a $-V_{ref}$ level on feedback bus 23. That is, digital logic circuit 22 operates in accordance with the following truth table:

Table 1

if $-V_{ref}/2 < V_{res}(\text{coarse}) < V_{ref}/2$, then $V_{FB} = \text{zero}$ (so that V_{RES} is not shifted);
 if $V_{ref}(\text{coarse}) > V_{ref}/2$, then $V_{FB} = -V_{ref}$ (so that V_{RES} is shifted by $-V_{ref}$); and
 if $V_{ref}(\text{coarse}) < -V_{ref}/2$, then $V_{FB} = +V_{ref}$ (so that V_{RES} is shifted by $+V_{ref}$).

[0048] This means that the final residue amplifier output V_{RES} at the end of the amplification process is not shifted at all, and always remains within the range $\pm V_{ref}/2$, as indicated by the solid line curve in the residue plot of FIG. 6. The feedback voltage V_{FB} keeps V_{RES} between $\pm V_{ref}/2$, and thereby avoids the need to double the number of flash-ADC comparators in the next stage (if redundancy bits are used in each pipeline ADC stage), since there is no need for flash ADC comparators to detect tap point voltages of the resistor network having values between V_{ref} and $V_{ref}/2$ and values between $-V_{ref}/2$ and $-V_{ref}$. The digital logic 63 shown in subsequently described FIG. 7A produces digital level signals -1, 0 and +1 as feedback. Additional decoding circuitry 64 in the MDAC 9A, as indicated in FIG. 7B, converts those digital signals to an equivalent voltage level shifts of $+V_{ref}$, 0 or $-V_{ref}$.

[0049] FIG. 4B shows a N-bit pipeline ADC 14 composed of 4 pipeline ADC stages 15-1,2,3,4 each having the basic configuration shown in FIG. 4A. Stages 15-1,2,3, are assumed to resolve p, q, r, and s bits, respectively, where N is equal to $p+q+r+s$. (In the example described herein, N is equal to 12 and each of p, q, r, and s is equal to 3.) The input conductor 7-1 of input stage 15-1 receives input voltage V_{IN} which is to be converted to a digital representation by N-bit pipeline ADC 14. Stage 15-1 generates a p-bit digital code on digital bus 21-1, and also generates a residue voltage V_{res1} on conductor 7-2, which is connected to the analog input of pipeline ADC stage 15-2. Similarly, stage 15-2 generates a q-bit digital code on digital bus 21-2, and also generates a residue voltage V_{res2} on conductor 7-3, which is connected to the analog input of pipeline ADC stage 15-3. Stage 15-3 generates a r-bit digital code on digital bus 21-3, and also generates a residue voltage V_{res3} on conductor 7-4, which is connected to the analog

input of pipeline ADC stage 15-4. (Note that V_{res1} , V_{res2} ,... are particular values of V_{RES} generated by a residue amplifier 11A as in FIG. 4A.) The last stage 15-4 generates a s-bit digital code on digital bus 21-4, and also generates an internal residue voltage V_{res4} (not shown). Each of stages 15-1,2,3,4 is biased by a reference voltage V_{ref} . The resolved p, q, r, and s bits constitute the digital representation of V_{IN} .

[0050] In one example, a redundancy bit is provided in each of stages 15-2,3,4 in FIG. 4B, in order to eliminate the ADC nonlinearity caused by the previously mentioned error sources. However, the redundancy bits are not resolved by the various pipeline ADC stages and do not appear on bus 21-1,2,3,4 as part of the N-bit output generated by pipeline ADC 14.

[0051] FIG. 5A shows a timing diagram for pipeline ADC stage 15 of FIG. 4A and pipeline ADC 14 of FIG. 4B. The SAMPLE signal is input to sample/hold circuitry (shown in FIGS. 7A and 7B) which samples the signals produced by the flash ADCs 8 of the various pipeline ADC stages. The SAMPLE phase is the interval during which the analog input to the ADC stage is, in effect, sampled. The HOLD phase is the entire time interval which is available for performing amplification of the residue voltages V_{res1} , V_{res2} ,... of the various pipeline ADC stages. Each overall residue amplification process includes a “course” pre-amplification operation followed by a “fine” main amplification operation.

[0052] FIG. 7A illustrates an implementation in which MDAC 9A, the previously mentioned sample and hold circuitry, and residue amplifier 11A are integrated into a single circuit “module”. Referring to FIG. 7A, residue amplifier 11A and MDAC 9A shown in pipeline ADC 15 of FIG. 4A are combined, along with suitable sample/hold circuitry, in a single circuit or “module” 32. Module 32 functions similarly to a sample and hold amplifier along with a built-in DAC function. Residue amplifier 11A in FIG. 7A includes an operational amplifier 30 having its (+) input connected by conductor 31A to one terminal of a feedback capacitor 40A of capacitance C. The other terminal of feedback capacitor 40A is connected by conductor 43A to one terminal of each of switches 42A and 45A. The other terminal of switch 42A is connected by conductor 46A to a (+) output of operational amplifier 30, which produces a (+) output signal OUTP on conductor 46A. The other terminal of switch 45A is connected to a conductor 47 which receives a common mode reference voltage REFCM. Similarly, the (-) input of operational amplifier 30 is connected by conductor 31B to one terminal of a feedback capacitor 40B of capacitance C. The other terminal of feedback capacitor 40B is connected by conductor

43B to one terminal of each of switches 42B and 45B. The other terminal of switch 42B is connected by conductor 46B to a (-) output of operational amplifier 30, which produces a (-) output signal OUTM on conductor 46B. The other terminal of switch 45B is connected to REFCM conductor 47.

[0053] Module 32 in FIG. 7A also includes 2^m switching circuits 33-1, 2...33- 2^m , each of which includes a sampling capacitor 38A of capacitance C having one terminal connected to conductor 31A and another terminal connected by a corresponding conductor 37A to one terminal of each of switches 34A, 35A, and 36A, where m is the number of bits resolved by the pipeline ADC stage 15 that contains module 32. Switch 34A is controlled by clock signal Ph1, and switches 35A and 36A are controlled by Ph2. The other terminal of switch 34A is connected to receive a corresponding input signal INP, which is the (+) input of the ADC stage which goes into both flash sub-ADC 8 and residue amplifier 11A as shown in FIG. 4A. The other terminal of switch 35A is connected to receive either a (+) reference signal REFP or a (-) reference signal REFM, depending on the flash sub-ADC output which is decoded through the digital logic 63 shown in FIG. 7A. The other terminal of switch 36A is connected by conductor 47 to receive REFCM.

[0054] Similarly, module or circuit 32 in FIG. 7A also includes 2^m switching circuits 39-1, 2...39- 2^m , each of which includes a sampling capacitor 38B having one terminal connected to conductor 31B and another terminal connected by a corresponding conductor 37B to one terminal of each of switches 34B, 35B, and 36B. Switch 34B is controlled by Ph1, and switches 35B and 36B are controlled by Ph2. The other terminal of switch 34B is connected to receive a corresponding (-) input signal INM, which is the (-) input of the ADC stage which goes into both flash sub-ADC 8 and residue amplifier 11A as shown in FIG. 4A. The other terminal of switch 35B is connected to receive either (+) reference signal REFM or (-) reference signal REFP depending on the flash sub-ADC output which is decoded through digital logic 63.

[0055] Ph2 in the MDAC circuitry is same as the “HOLD” phase of timing diagram of FIG. 5A. Depending on the output from flash ADC 8 (FIG. 4A), capacitor 38A is connected either to REFP, REFM or REFCM through switches 35A and 36A. This also applies to capacitor 38B. The other terminal of switch 36B is connected by conductor 47 to receive REFCM.

[0056] In this example, the flash ADC 8 of each pipeline ADC stage contains the module 32 of FIG. 7A and produces m “effective” bits to be resolved, and each stage except the first also

includes one redundancy bit. The m “effective” bits and the redundancy bit appear on digital bus 13A (FIG. 4A). Digital bus 13A is provided as an input to the digital logic circuit 63 that also is included in module 32. Ph1 is the same as “SAMPLE” phase of FIG. 5A and Ph2 is the same as “HOLD” phase of FIG. 5A. The input signal INP is sampled on capacitor 38A and INM is sampled on capacitor 38B, for all of the MDACs 33-1 through 33-2^m and 39-1 through 39-2^m during the sample phase Ph1. During hold phase Ph2, the capacitor 38A or 38B of a particular MDAC is connected to REFP, REFM or REFCM in response to the control signal 65 produced by digital logic 63, depending on the output of the flash sub-ADC 8. (Recall that the same input $INP-INM=V_{IN}$ goes to flash sub-ADC 8.) The feedback capacitors 40A and 40B are connected to REFCM during sample phase Ph1. Therefore, a “0” is differentially sampled onto feedback capacitors 40A and 40B. In the hold phase Ph2, feedback capacitors 40A and 40B are connected to the output conductors 46A and 46B of operational amplifier 30. By writing equations for the charges on all of the feedback capacitors 40A and 40B and MDAC capacitors 38A and 38B in the sample phase and the hold phase and then equating the total charge during a sample phase to the total charge during a hold phase, subsequently described Equation (1) is obtained for OUTP-OUTM, which is the residue output V_{RES} of the combined MDAC and residue amplification stage 32 shown in FIG. 7A.

[0057] The analog input signals INP and INM (which are represented by V_{IN} in the simplified diagrams of FIGS. 4A and 4B) generated by the previous pipeline ADC stage are sampled on corresponding sampling capacitors 38A and 38B of capacitance C during phase Ph1. The MDAC conversion function is achieved by using either REFP/REFM or REFCM during phase Ph2.

[0058] Equation (1) set forth below for V_{RES} defines a combined gain and DAC function. Note that OUTP-OUTM is also represented by V_{RES} in FIG. 4A and by V_{res} in FIG. 4B. As explained above, the input signal INP-INM (V_{IN} in FIGS. 4A and 4B) is sampled on all of the sampling capacitors 33-1 through 33-2^m and 39-1 through 39-2^m. Therefore, $G=2^m$ is obtained as the coefficient for INP-INM. In the hold phase Ph2, REFP, REFM or REFCM is connected to each MDAC capacitor depending on the flash ADC output. This gives the coefficient k in Equation (1) for the reference term REFP-REFM, which is equal to V_{ref} . The residue amplifier output voltage V_{RES} is represented by the expression

$$\text{Eqn. (1)} \quad V_{\text{RES}} = \text{OUTP} - \text{OUTM} = G \cdot (\text{INP} - \text{INM}) - k \cdot (\text{REFP} - \text{REFM}),$$

where $G = 2^m$, $k = -2^m, -2^{m-1}, -2^{m-2}, \dots, -1, 0, 1, \dots, 2^{m-2}, 2^{m-1}, 2^m$, depending on the digital output received from flash ADC 8 by the MDAC circuitry in FIG. 7A, the analog output of which is applied to the (-) input of residue amplifier 11A. Ph1 phase is the same as “SAMPLE” and Ph2 phase is the same as “HOLD” of the timing diagram in FIG. 5B.

[0059] Referring to FIG. 7B, module 32 includes MDACs 33-1 and 39-1 of MDAC circuitry 9A and residue amplifier 11A of FIG. 7A. MDAC 9A also includes level-shifting circuits 60A and 60B, and further includes digital decoding logic 63 for generating control signals 65 for all of the MDAC switches that are turned on, i.e., closed, during phase Ph2. MDAC 9A also includes digital decoding logic circuit 64 for generating control signals 66 for all level-shifting circuit switches that are on, i.e., closed, during phase Ph2. Level-shifting circuit 60A includes a level-shifting capacitor 68A of capacitance $C_L = C$ connected between conductor 31A and one terminal of each of switches 61A, 62A, and 63A. The other terminal of switch 61A is connected to common mode reference voltage REFCM. The other terminal of switch 62A is connected to either REFP or REFM, depending on the output of sub-ADC 8. The other terminal of switch 61A is connected to REFCM. Similarly, level-shifting circuit 60B includes a level-shifting capacitor 68B of capacitance C_L connected between conductor 31B and one terminal of each of switches 61B, 62B, and 63B. The other terminal of switch 61B is connected to REFCM. The other terminal of switch 62B is connected to either REFP or REFM, depending on the output of sub-ADC 8. The other terminal of switch 61B is connected to REFCM.

[0060] The above mentioned level-shifting function is based on feedback signal V_{FB} from the two-level residue-voltage-detecting comparators 17 and 18 (FIG. 4A), and is accomplished by using level-shifting capacitors 68A and 68B of capacitance C_L shown in FIG. 7B. During sample phase Ph1, the level-shifting capacitor nodes 70A and 70B are connected to common mode reference voltage REFCM. Therefore, operational amplifier 30 samples a differential voltage of zero across level-shifting capacitors 68A and 68B during main amplification phase Ph2a as shown in FIG. 5B. Level-shifting capacitors 68A and 68B are connected to REFP, REFM or REFCM, which are generated by decoding logic 64 on the basis of feedback signal V_{FB} from the two-level detect comparators 17 and 18 in FIG. 4A. This results in operation according to the following truth table:

if $V_{FB} = '0'$, the top and bottom capacitors level-shifting capacitors 68A and 68B are connected to REFCM during Ph2a. This results a level shift of zero to the output OUTP–OUTM produced by residue amplifier 11A,

if $V_{FB} = '1'$, the top and bottom capacitors level-shifting capacitors 68A and 68B are connected to REFCM during Ph2a. This results in a level shift of “+Vref” to the output OUTP–OUTM produced by residue amplifier 11A, and

if $V_{FB} = '-1'$ the top and bottom capacitors level-shifting capacitors 68A and 68B are connected to REFM and REFP, respectively, during Ph2a. This results a level shift of zero to the output OUTP–OUTM produced by residue amplifier 11A.

[0061] FIG. 8 illustrates a dynamic flash ADC comparator circuit 25 which may be used in flash ADC comparators 710-1, 710-2^{q-1}, 710-2^q and 710-2^{q+1} shown in Prior Art FIG. 3. Dynamic comparator circuit 25 includes a latch circuit 53 and associated switched capacitor input circuitry. Latch circuit 53 includes P-channel MOS transistors MP1 and MP2 and N-channel MOS transistors MN1 and MN2 and also includes switches 57A and 57B controlled by a clock signal Ph-3. The sources of transistors MP1 and MP2 are connected by switch 57A to V_{DD} , and the sources of transistors MN1 and MN2 are connected by switch 57B to V_{SS} . The gates of transistors MP1 and MN1 are connected to conductor 54A, on which the (+) output signal OUTP of dynamic comparator 25 is generated. Similarly, the gates of transistors MP2 and MN2 are connected to conductor 54B, on which the (-) output signal OUTM of dynamic comparator 25 is generated. The drains of transistors MP1 and MN1 are connected to conductor 54B, and the drains of transistors MP2 and MN2 are connected to conductor 54A.

[0062] The associated switched capacitor input circuitry of dynamic comparator circuit 25 in FIG. 8 includes switches 55A, 55B, 56A and 56B all controlled by clock signal Ph1, and also includes switches 58A and 58B which both are controlled by clock signal Ph2. Conductor 54A is connected to one terminal of switch 55A and one terminal of sampling capacitor 52A. The other terminal of switch 55A is connected to the input common mode voltage INCM, which sets the common mode voltage on the other terminal of capacitor 52A based on the common mode voltage of the output signals OUTP and OUTM of latch circuit 53. Latch circuit 53 makes decisions during phase Ph3, as indicated in the timing diagram of FIG. 5C. The other terminal of capacitor 52A is connected by conductor 51A to one terminal of each of switches 56A and 58A. The other terminal of switch 56A is connected to the (+) input of dynamic comparator 25, and

the other terminal of switch 58A is connected to receive the (+) reference signal REFP.

[0063] Similarly, conductor 54B is connected to one terminal of switch 55B and one terminal of sampling capacitor 52B. The other terminal of switch 55B is connected to the input common mode voltage INCM, which sets the common mode voltage on the other terminal of capacitor 52B based on the common mode voltage of the output signals OUTP and OUTM of latch circuit 53. Latch circuit 53 makes decisions during phase Ph3, as indicated in the timing diagram of FIG. 5C. The other terminal of capacitor 52B is connected by conductor 51B to one terminal of each of switches 56B and 58B. The other terminal of switch 56A is connected to the (+) input of dynamic comparator 25, and the other terminal of switch 58B is connected to receive the (+) reference signal REFM.

[0064] In operation, each of the inputs INP and INM of dynamic comparator 25 in FIG. 8 are sampled onto sampling capacitors 52A and 52B, respectively, during phase Ph1 in FIG. 5C. The references REFP and REFM are applied to sampling capacitors 52A and 52B, respectively, during phase Ph2. Latch 53 is enabled by clock signal phase Ph3 just before the end of phase Ph2, and makes a switching decision based on the relative difference between the differential input voltage $INP-INM$ and the differential reference voltage $REFP-REFM$. Note that $INP-INM$ is the input V_{IN} of FIG. 4A, but $REFP-REFM$ is not the same as V_{ref} and is different for each dynamic comparator 25, depending on the tap of the flash ADC resistor ladder (FIG. 3) to which that dynamic comparator 25 is connected.

[0065] To summarize, a cost/drawback of introducing a redundancy bit into a sub-ADC is that it adds one extra bit of resolution to each flash ADC 8, and that means the number of flash ADC comparators of the next pipeline ADC stage 15 must be doubled. One purpose of the invention is to reduce the number of comparators required in the flash ADC 8 of the next pipeline ADC stage 15 when redundancy bits is used. Another purpose of the invention is to limit output voltage swing of residue amplifier 11A to voltage levels between $\pm V_{ref}/2$ without using the previously described reference scaling, because even though reference scaling limits the residue amplifier output voltage swing to $\pm V_{ref}/2$, it also decreases the input offset specification and increases the area and power consumption required by that the flash ADC comparators.

[0066] As previously indicated, the residue amplification process in pipeline ADC stage 15 includes a pre-amplification operation followed by a main amplification operation. First, the

pre-amplification begins at the beginning of the HOLD phase indicated in the timing diagrams of FIGS. 5A-C, and consists of a “coarse” amplification by residue amplifier 11A to obtain a “coarse” value of V_{RES} , which is referred to as $V_{res}(\text{coarse})$. If errors are being generated in the previous stage, $V_{res}(\text{coarse})$ will swing either above $V_{ref}/2$ or below $-V_{ref}/2$. This condition is detected by one of level-detect comparators 17 and 18 and causes digital logic circuit 22 (FIG. 4A) to generate a value of feedback voltage V_{FB} equal to $+V_{ref}$ or $-V_{ref}$ on bus 23. The “coarse” pre-amplification operation requires less accuracy than the “fine” main amplification operation, and involves larger residue amplifier output voltage swings. Therefore, the same residue amplifier may be used both to provide the more accurate main amplification and the less accurate coarse pre-amplification. Consequently, the additional residue amplifier output voltage swing that occurs during the pre-amplification phase does not necessitate incurring any additional cost in the form of more complex, more accurate residue amplifier circuitry.

[0067] After completion of the pre-amplification phase, residue amplifier 11A then operates to generate a much more accurate value of V_{RES} , referred to as $V_{res}(\text{fine})$, based on the feedback voltage V_{FB} derived from level-detect comparators 17 and 18. If V_{RES} swings beyond $\pm V_{ref}/2$ during pre-amplification, then the feedback signal V_{FB} on bus 23 causes MDAC 9A to impose a level shift on its output 10 in FIG. 4A (or between conductors 31A and 31B FIG. 7B) so that residue amplifier 11A produces a corresponding level shift onto V_{RES} during the main amplification phase. This prevents the final value of $V_{res}(\text{fine})$ from going beyond the range $\pm V_{ref}/2$. This is accomplished by operation of level-detect comparators 17 and 18 and logic circuit 22 in accordance with the truth table previously set forth in Table 1. Therefore, the final residue amplifier output V_{RES} at the end of the amplification process always remains within the $\pm V_{ref}/2$ range, as indicated by the solid line curve in the residue plot of FIG. 6.

[0068] Referring to FIG. 6, the residue curve for $V_{RES}=V_{res}(\text{fine})$ in pipeline ADC stage 15 is indicated by the solid line segments A, B, D, E, and F. The residue curve for $V_{RES}=V_{res}(\text{coarse})$ during pre-amplification is indicated by the dashed lines including line segments C and G, where $V_{res}(\text{coarse})$ may go beyond $\pm V_{ref}/2$ (and in the worst case may reach either of the values $\pm V_{ref}$). In pipeline ADC stage 15 of FIG. 4A, the “pre-amplification residue voltage” $V_{RES}=V_{res}(\text{coarse})$ generated during the pre-amplification phase follows solid line segment A, dashed line segment C, solid line segments D and E, part of segment F, and dashed line segment G.

[0069] The accuracy specification of pipeline ADC 14 will always require $V_{RES}=V_{res}(\text{fine})$ to be within the $\pm V_{ref}/2$ as indicated by the solid-line residue curve shown in FIG. 6. The dashed line is the residue voltage plot during pre-amplification, and the solid line is the residue voltage plot during main amplification. During the pre-amplification operation, part of dashed-line section C goes higher than $+V_{ref}/2$, causing digital logic 22 in FIG. 4A to kick in and generate a V_{FB} value of $-V_{ref}$ which causes a downward level shift in the value of V_{RES} during the main amplification operation. This causes V_{RES} to be less than $+V_{ref}/2$ during the main amplification operation. This downward level shift therefore causes V_{RES} to follow the solid line in FIG. 6 (no portion of which exceeds $+V_{ref}/2$) during the main amplification operation. Similarly, during the pre-amplification operation, part of dashed-line section C goes lower than $-V_{ref}/2$, causing digital logic 22 in FIG. 4A to kick in and generate a V_{FB} value of $+V_{ref}$ which causes a upward level shift in the value of V_{RES} during the main amplification operation. This upward level shift therefore causes V_{RES} to be greater than $-V_{ref}/2$ during the main amplification operation. This upward level shift causes V_{RES} to follow the solid line in FIG. 6 (no portion of which is less than $-V_{ref}/2$) during the main amplification operation.

[0070] Table 2 below conveys the same basic information as previously mentioned Table 1, but uses the foregoing terms “ $V_{res}(\text{coarse})$ ” and “ $V_{res}(\text{fine})$ ” as shown in the residue plot of FIG. 6.

Table 2

if $-V_{ref}/2 < V_{res}(\text{coarse}) < V_{ref}/2$, then $V_{FB} = \text{zero}$ (so that $V_{res}(\text{fine}) = V_{RES}$);
 if $V_{res}(\text{coarse}) > V_{ref}/2$, then $V_{FB} = -V_{ref}$ (so that $V_{res}(\text{fine}) = V_{RES} - V_{ref}$); and
 if $V_{res}(\text{coarse}) < -V_{ref}/2$, then $V_{FB} = +V_{ref}$ (so that $V_{res}(\text{fine}) = V_{RES} + V_{ref}$).

[0071] Thus, the overall residue amplification is performed in two steps. In the pre-amplification step, a coarse pre-amplification of the residue is performed, with substantially less accuracy than is required during the main amplification step. During the main amplification step, residue amplifier 11A needs to amplify with a higher level of accuracy determined by the resolution of pipeline ADC 14 (FIG. 4B), such that the output voltage swing V_{RES} of residue amplifier 11A never goes above $V_{ref}/2$ or below $-V_{ref}/2$. This avoids the problems caused by excessive output swings of the residue amplifiers of prior art pipeline ADC stages. Also, the number of flash ADC comparators 8 in each “next” pipeline ADC stage 15 in pipeline ADC 14 is reduced by half. Furthermore, the required input offset voltage specification of the flash ADC

comparators of each “next” pipeline ADC stage is substantially reduced compared to the input offset specification required in the flash ADCs of a conventional pipeline ADC.

[0072] In one implementation of pipeline ADC 14 in FIGS. 4A and 4B, only a single pair of level-detect comparators is needed and it is shared by all of the pipeline ADC stages which follow the input stage 15-1. In this implementation the waveforms in the timing diagram of FIG. 6 are successively applied to each pipeline ADC stage. In another implementation, a single residue amplifier is shared between all of the pipeline ADC stages. For example, if pipeline ADC 14 (FIG. 4B) is a 12-bit ADC which includes 4 stages each having 3 bits, the analog input V_{IN} of pipeline ADC 14 is sampled, and then an entire ADC conversion process is performed. Only after that complete conversion by pipeline ADC 14 has been completed can V_{IN} be sampled again. That allows the single residue amplifier to be shared across all four stages of the pipeline ADC. However, this arrangement does not allow sharing of level-detect comparators.

[0073] In another implementation, the first stage 15-1 of pipeline ADC 14 samples the input V_{IN} and amplifies the residue. While the residue amplifier of the first stage 15-1 is amplifying its residue, the next stage 15-2 of pipeline ADC 14 is sampling the residue output of first stage 15-1. Once the amplification of the first stage residue is complete, the second stage of pipeline ADC 14 then amplifies its own residue, and simultaneously first stage 15-1 operates to sample V_{IN} again. In this implementation, a single residue amplifier can not be shared between all the stages of pipeline ADC 14. However, a first residue amplifier may be shared between the first and second pipeline ADC stages, and second residue amplifier may be shared between the third and fourth pipeline ADC stages, and so forth. In any case, every stage must have its own MDAC and flash-ADC.

[0074] An advantage of pipeline ADC stage 15 of FIG. 4A is that the residue amplifier input offset voltage can individually be less than the value $LSB/2$, and all of the other errors summed together also can be less than $LSB/2$. This is contrast to a conventional pipeline ADCs, in which all errors, including comparator input offset and residue amplifier input offset IR voltage drop variations, etc., in combination must not exceed the $LSB/2$ value of the pipeline ADC stage. This reduces the input offset requirement of the flash-ADC comparators and also of the residue amplifier.

[0075] Using dynamic comparator 25 of FIG. 8 results in substantially reduced integrated circuit chip area and substantially reduced power dissipation of pipeline ADC 14.

Only switching power during latch operation is consumed, whereas both static power and switching power are consumed by a conventional comparator which includes a preamplifier stage. Dynamic comparators may be used in the flash ADCs, which further reduces integrated circuit chip area and power dissipation, and also reduces switching power because a reduced number of clock signal lines is required in the pipeline ADC.

[0076] An advantage of pipeline ADC stage 15 FIG. 4A is that the residue voltage V_{RES} never swings outside of the range $\pm V_{ref}/2$. This means half of the comparators can be removed from the flash-ADC of the next stage, which saves a substantial amount of integrated circuit chip area and eliminates a substantial amount of power dissipation. For example, in a 12-bit ADC with a “(3-3-3-3)” split of the 12 bits between 4 pipeline ADC stages 15, only 36 flash-ADC comparators are needed, rather than the 56 flash-ADC comparators that would be needed if the level-detect comparators and associated digital circuitry are not used. (Note that the reduction in hold time available during the main amplification phase is compensated to some extent by the reduced capacitive loading by the reduced the number of flash ADC comparators required in the subsequent pipeline ADC stage.)

[0077] In a conventional pipeline ADC, all errors (comparator offset, amplifier offset, IR voltage drop and others) combined together must not exceed $LSB/2$ of the pipeline ADC. In contrast, in pipeline ADC stage 15 of FIG. 4A, residue amplifier input offset can individually be less than $LSB/2$ and all others errors summed together can be less than $LSB/2$. This reduces the offset spec of the sub-ADC comparators and allows dynamic comparators (without preamplifiers) to be used in the flash ADCs thereby reducing integrated circuit chip area and power consumption, and also reducing switching power due to a reduced number of clock lines in the pipeline ADC.

[0078] Although the disclosed pipeline ADC stage and technique provide an effective alternative to the prior art reference scaling technique, the two techniques may be combined to achieve the advantages of a reduced number of required flash ADC comparators, reduced residue amplifier output swing, and reduced DC gain and bandwidth of the residue amplifier, for example, in a very low supply voltage application. In that case, reference scaling could be used to limit the residue amplifier output swing to the range $\pm V_{ref}/4$, although some of the advantage achieved by reducing the flash-ADC comparator input offset requirements would be lost. Although the flash-ADC as a practical matter is almost always a flash-ADC, it could be another

type of ADC.

[0079] Those skilled in the art will appreciate that modifications may be made to the described embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS:

What is claimed is:

1. A pipeline ADC (analog-to-digital converter) including a pipeline ADC stage, comprising:
 - (a) a residue amplifier having a first input coupled to receive a first residue signal of a previous ADC stage;
 - (b) a first sub-ADC having an input coupled to receive the first residue signal for resolving a predetermined number of bits and producing the predetermined number of bits and a redundancy bit in response to the first residue signal;
 - (c) a first DAC (digital-to-analog converter) for converting the predetermined number of bits and the redundancy bit to an analog signal applied to a second input of the residue amplifier, the DAC having a level-shifting input for receiving a feedback signal, the residue amplifier amplifying a difference between the residue signal and the analog signal to generate a second residue signal; and
 - (d) level-detect circuitry receiving the second residue signal and generating the first feedback signal if the second residue signal is outside of a predetermined voltage range so as to cause the first DAC to shift the second residue signal back within the predetermined voltage range by the end of the amplifying.
2. The pipeline ADC of claim 1 wherein the previous ADC stage is essentially the same as the pipeline ADC stage.
3. The pipeline ADC of claim 1 wherein the previous ADC stage is a first ADC stage of the pipeline ADC.
4. The pipeline ADC of claim 1 wherein the sub-ADC includes 2^m comparators the outputs of which produce the resolved bits, where m is an effective number of bits, excluding the redundancy bit, resolved by the pipeline ADC stage.
5. The pipeline ADC of claim 4 wherein the first sub-ADC is a m bit flash-ADC.
6. The pipeline ADC of claim 1 wherein the DAC includes an MDAC (multiplying DAC).
7. The pipeline ADC of claim 1 wherein the level-detect circuitry includes first and second comparators each having an output coupled to an input of a logic circuit, a first input of each of the first and second comparators being coupled to the second residue signal, a second

input of the first comparator being coupled to a first reference voltage which corresponds to an upper end of the predetermined voltage range, and a second input of the second comparator being coupled to a second reference voltage which corresponds to a lower end of the predetermined voltage range, an output of the logic circuit providing the feedback signal.

8. The pipeline ADC of claim 1 wherein the level-detect circuitry operates in accordance with the truth table

if $-V_{\text{ref}}/2 < V_{\text{res}}(\text{coarse}) < V_{\text{ref}}/2$, then $V_{\text{FB}} = \text{zero}$ (so that V_{RES} is not shifted);

if $V_{\text{ref}}(\text{coarse}) > V_{\text{ref}}/2$, then $V_{\text{FB}} = -V_{\text{ref}}$ (so that V_{RES} is shifted by $-V_{\text{ref}}$); and

if $V_{\text{ref}}(\text{coarse}) < -V_{\text{ref}}/2$, then $V_{\text{FB}} = +V_{\text{ref}}$ (so that V_{RES} is shifted by $+V_{\text{ref}}$),

where V_{ref} is a reference voltage of the pipeline ADC, $V_{\text{res}}(\text{coarse})$ is a pre-amplified value of the second residue signal, and V_{FB} is the feedback signal.

9. The pipeline ADC of claim 1 wherein the predetermined voltage range is equal to one half of a reference voltage applied to the DAC.

10. The pipeline ADC of claim 5 wherein the comparators of the sub-ADC are dynamic comparators.

11. The pipeline ADC of claim 1 wherein the residue amplifier, the DAC, and sample/hold circuitry are combined in a single circuit module.

12. The pipeline ADC of claim 11 wherein the amplifying includes a pre-amplification phase without shifting the value of the second residue signal in response to the feedback signal, followed by a main amplification phase which includes shifting of the second residue signal in response to the feedback signal to keep the second residue signal within the predetermined voltage range.

13. The pipeline ADC of claim 12 wherein the pre-amplification phase occurs with substantially lower accuracy than the main amplification phase.

14. The pipeline ADC of claim 1 including level-shifting circuitry having an input coupled to the first input of the residue amplifier, the level-shifting circuitry causing the residue amplifier to produce

a zero level shift of an output of the residue amplifier in response to a "0" level of the feedback signal,

a first polarity level shift of the output of the residue amplifier in response to a "1" level of the feedback signal, and

a second polarity level shift of an output of the residue amplifier in response to a “-1” level of the feedback signal.

15. A method of operating a pipeline ADC (analog-to-digital converter) including a pipeline ADC stage, the method comprising:

- (a) applying a first residue signal to a first input of a residue amplifier and to an input of a sub-ADC for resolving a predetermined number of bits;
- (b) operating the sub-ADC to produce the predetermined number of resolved bits and a redundancy bit in response to the first residue signal;
- (c) converting the predetermined number of resolved bits and the redundancy bit to an analog signal and applying the analog signal to a second input of the residue amplifier;
- (d) amplifying the difference between the first residue signal and the analog signal to generate a second residue signal; and
- (e) if the second residue signal is outside of a predetermined voltage range, then causing the residue amplifier to shift the second residue signal back within the predetermined voltage range by the end of the amplifying phase.

16. The method of claim 15 wherein step (e) includes operating level-detect circuitry in accordance with the truth table

if $-V_{\text{ref}}/2 < V_{\text{res}}(\text{coarse}) < V_{\text{ref}}/2$, then $V_{\text{FB}} = \text{zero}$ (so that V_{RES} is not shifted);

if $V_{\text{ref}}(\text{coarse}) > V_{\text{ref}}/2$, then $V_{\text{FB}} = -V_{\text{ref}}$ (so that V_{RES} is shifted by $-V_{\text{ref}}$); and

if $V_{\text{ref}}(\text{coarse}) < -V_{\text{ref}}/2$, then $V_{\text{FB}} = +V_{\text{ref}}$ (so that V_{RES} is shifted by $+V_{\text{ref}}$),

where V_{ref} is a reference voltage of the pipeline ADC, $V_{\text{res}}(\text{coarse})$ is a pre-amplified value of the second residue signal, and V_{FB} is the feedback signal.

17. The method of claim 16 wherein step (c) includes utilizing a DAC (digital-to-analog converter) having a level-shifting input to shift the second input of the residue amplifier so as to superimpose a level shift on the second residue signal so as to shift it back within the predetermined voltage range.

18. The method of claim 15 including repeating steps (a) through (e) for a next pipeline ADC stage.

19. The method of claim 15 including providing 2^{m-1} comparators in the sub-ADC.

20. A pipeline ADC (analog-to-digital converter), comprising:

- (a) means for applying a first residue signal to a first input of a residue amplifier and

to an input of a sub-ADC for resolving a predetermined number of bits;

(b) means in the sub-ADC for producing the predetermined number of bits and a redundancy bit in response to the first residue signal;

(c) means for converting the predetermined number of bits and the redundancy bit to an analog signal and applying the analog signal to a second input of the residue amplifier;

(d) means for amplifying the difference between the first residue signal and the analog signal to generate a second residue signal; and

(e) means for causing the residue amplifier to shift the second residue signal back within the predetermined voltage range by the end of the amplifying if the second residue signal is outside of a predetermined voltage range.

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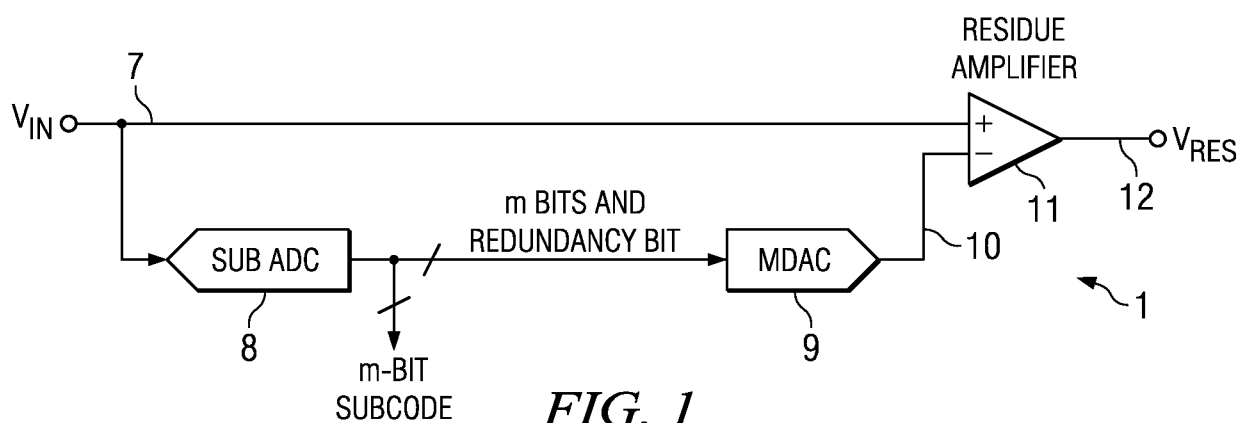


FIG. 1
(PRIOR ART)

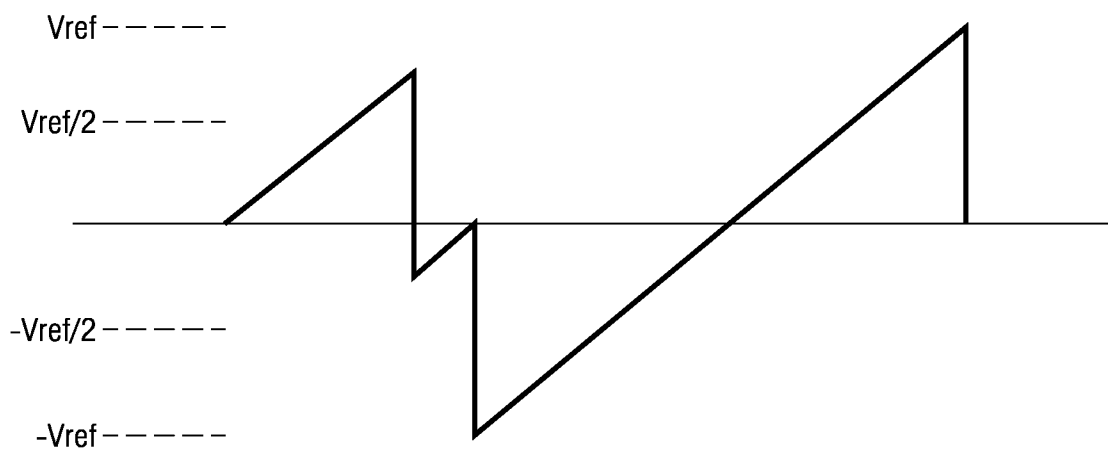
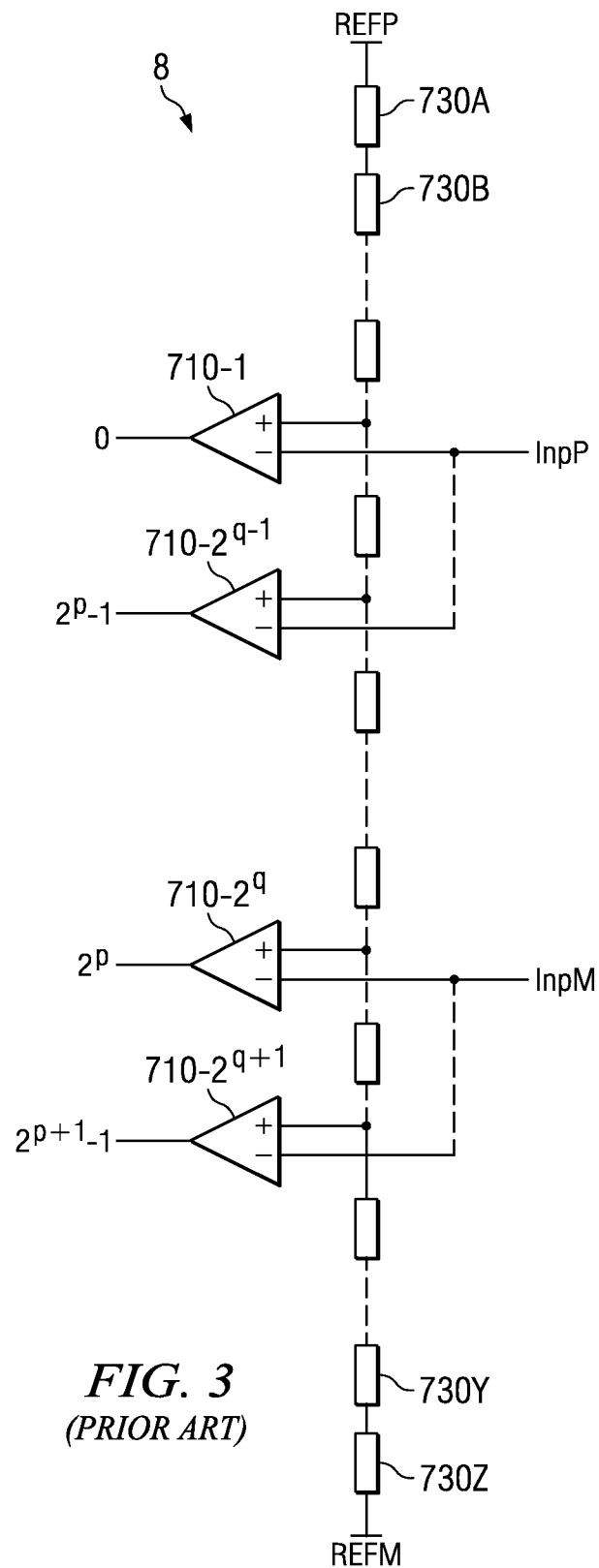


FIG. 2
(PRIOR ART)

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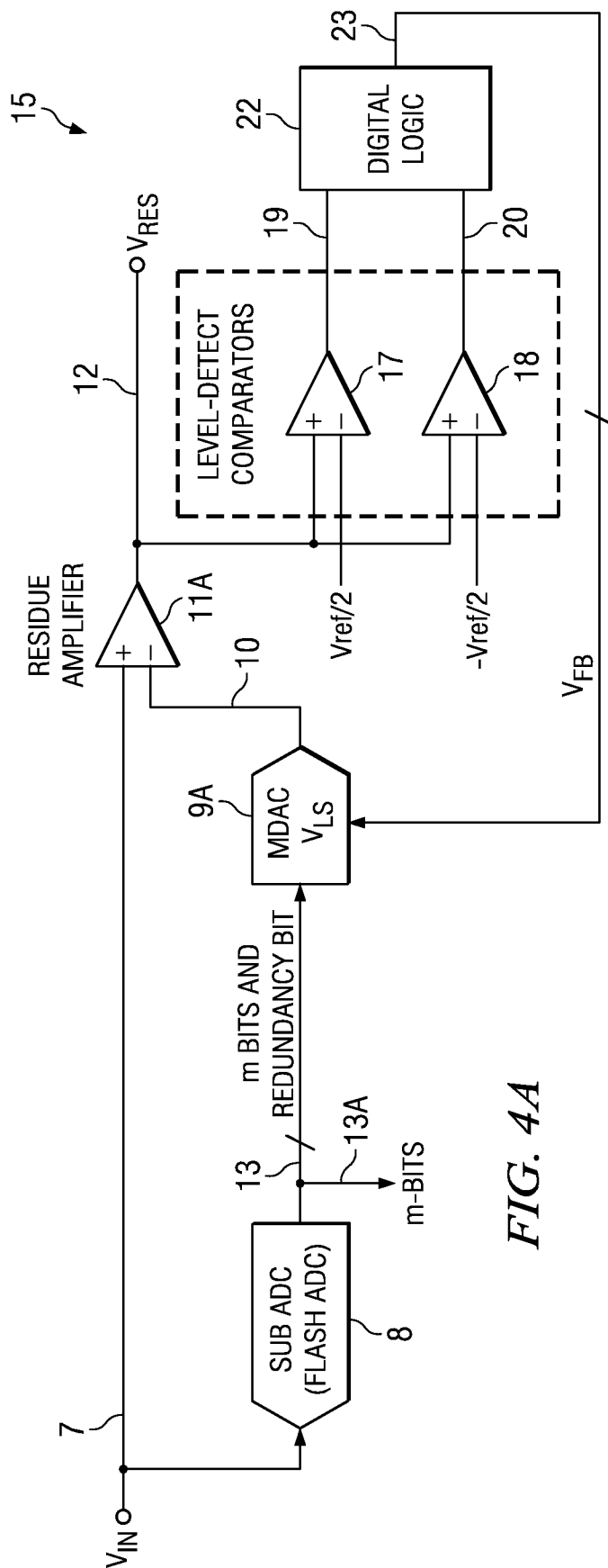


FIG. 4A

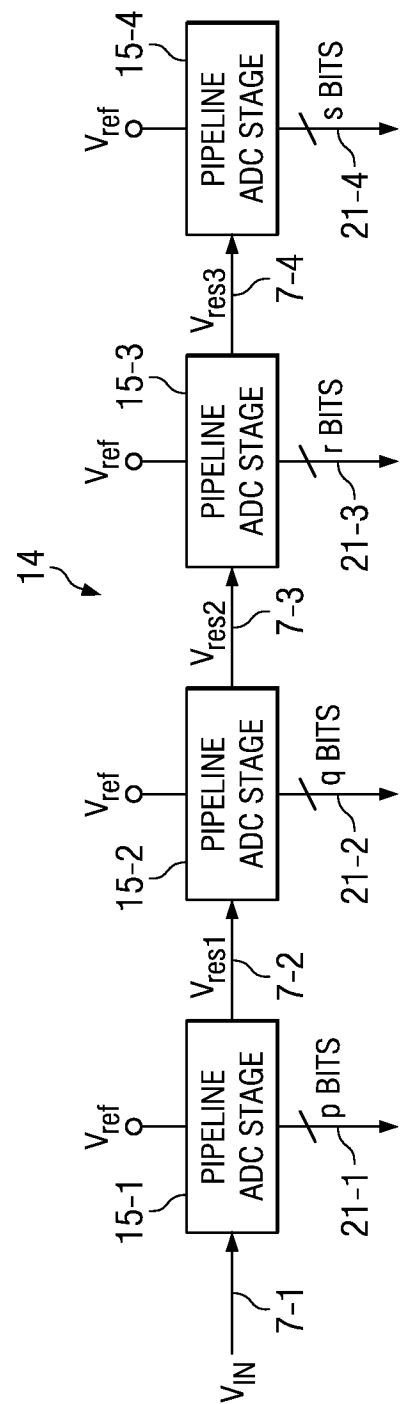


FIG. 4B

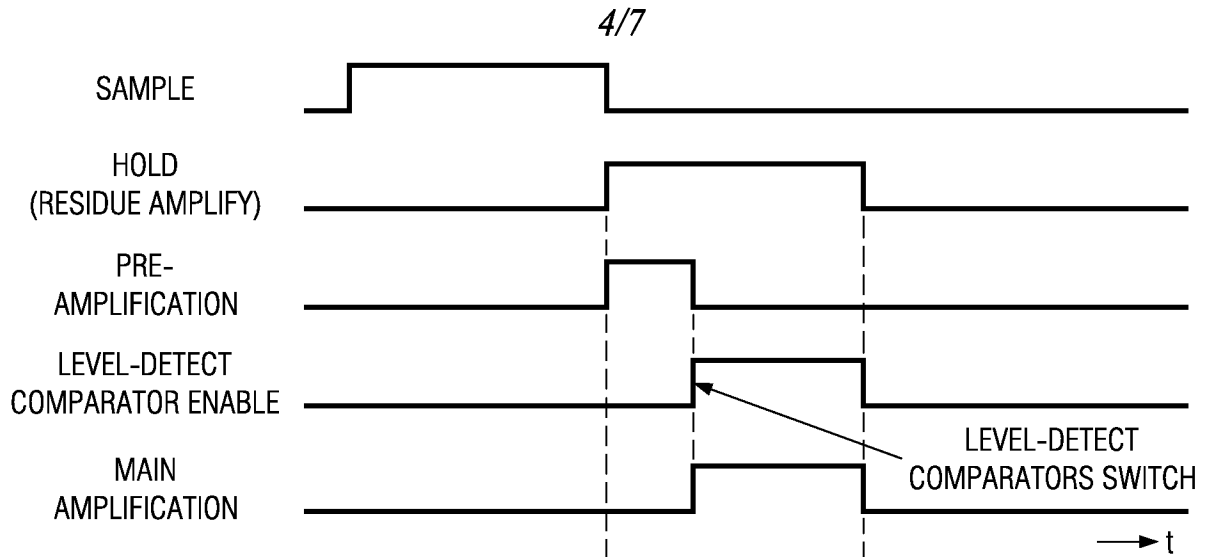


FIG. 5A

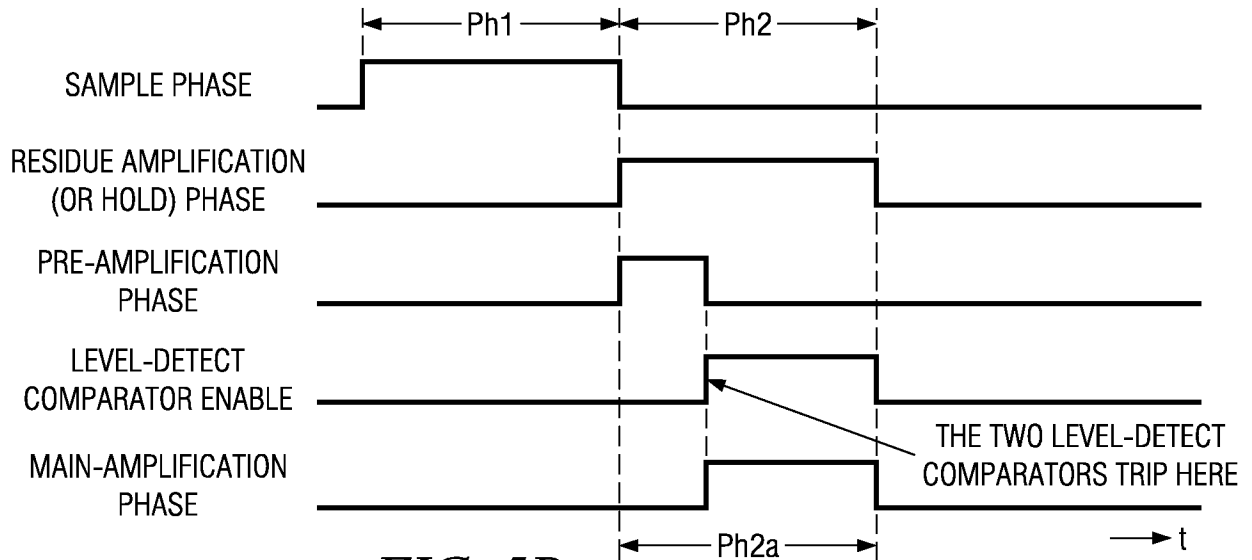


FIG. 5B

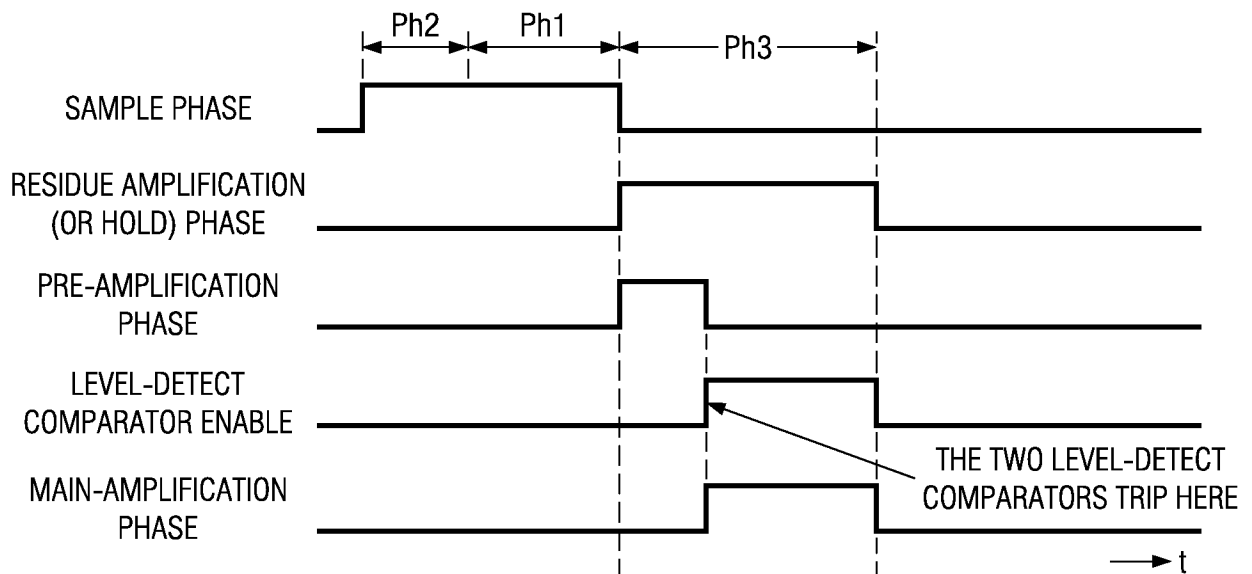


FIG. 5C

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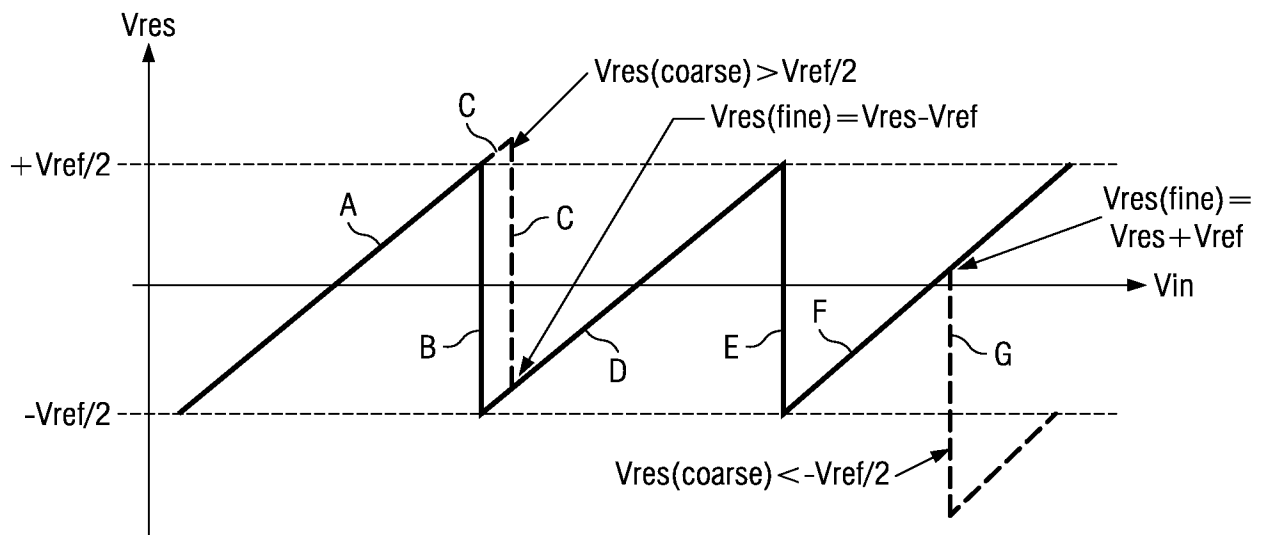


FIG. 6

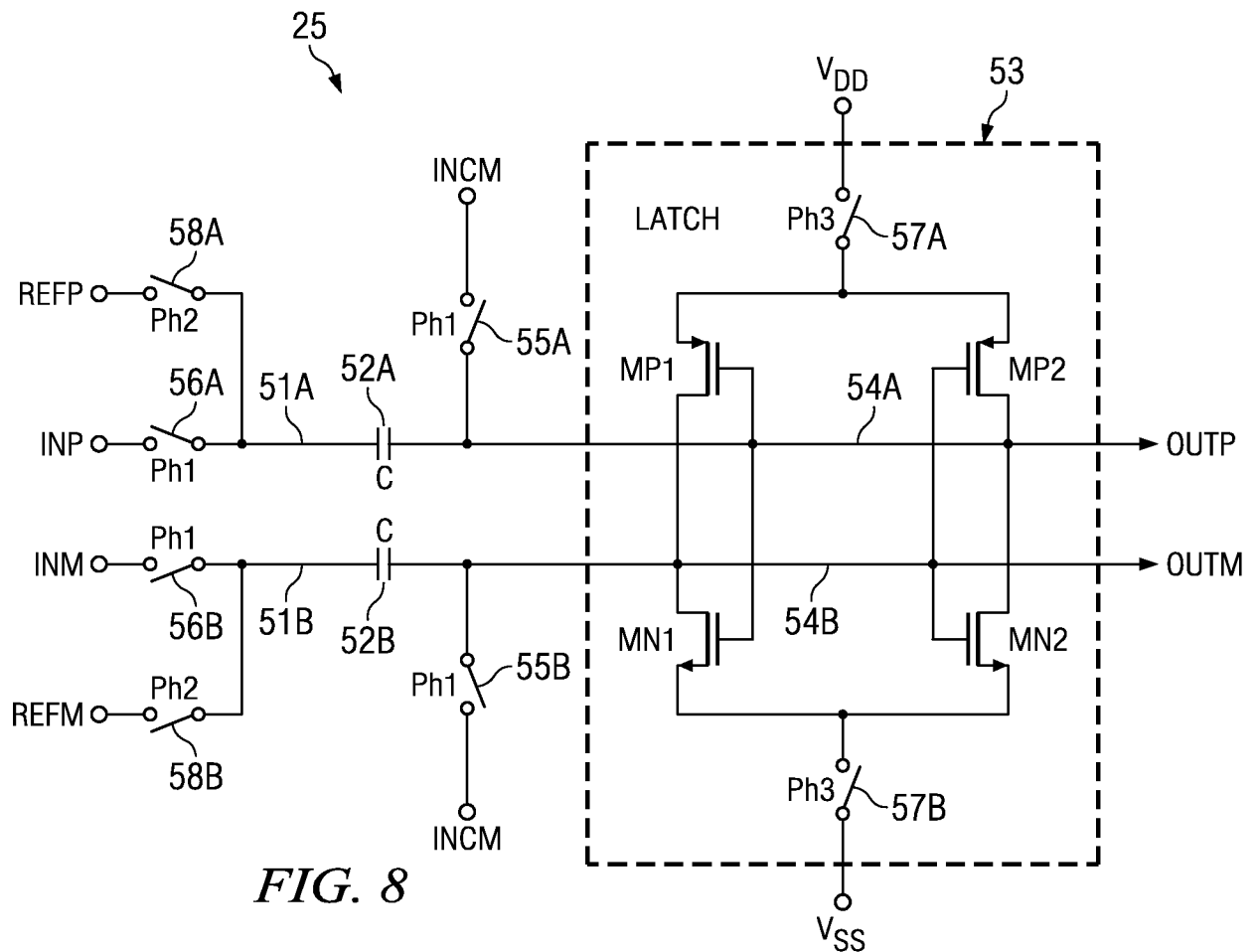


FIG. 8

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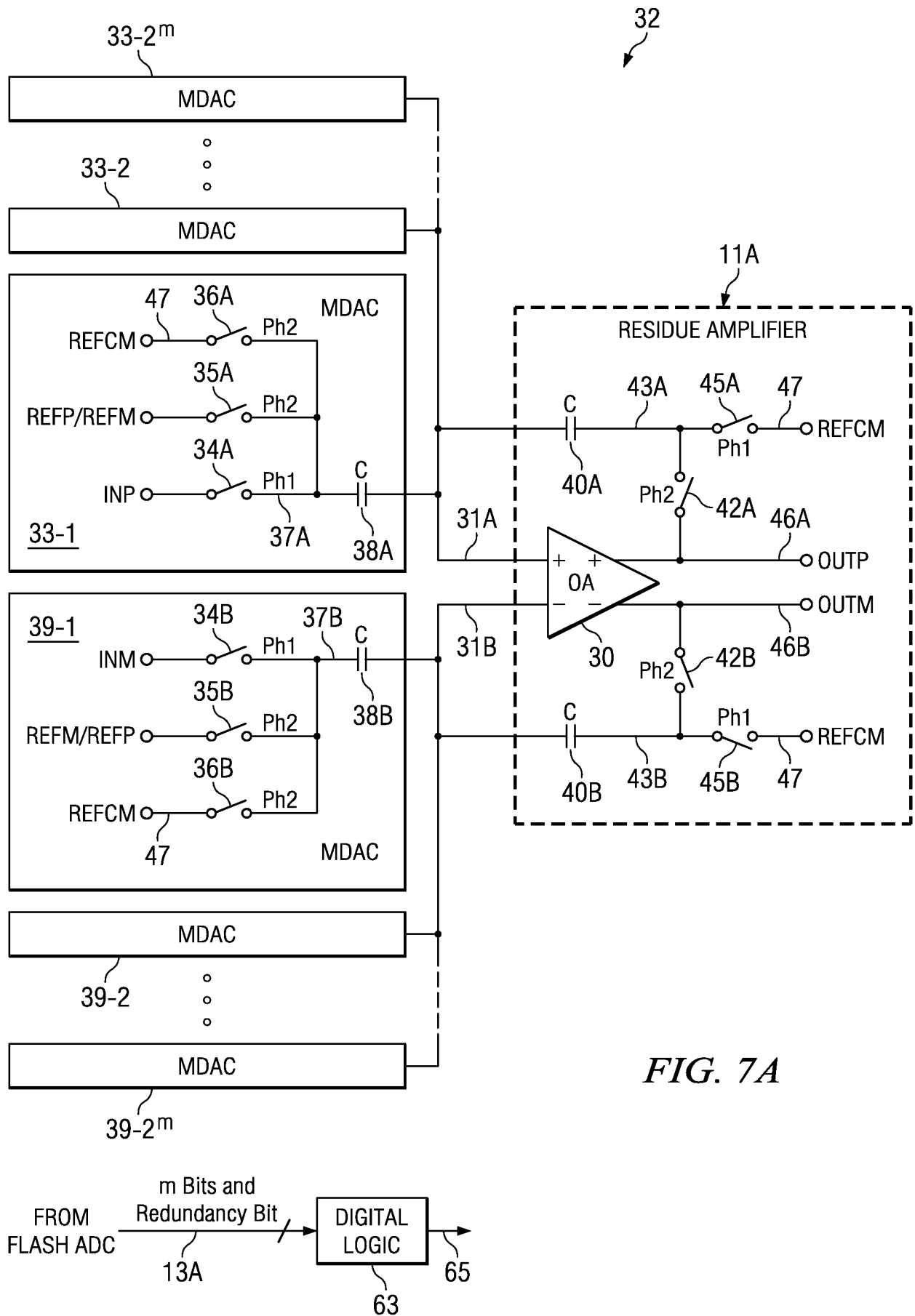
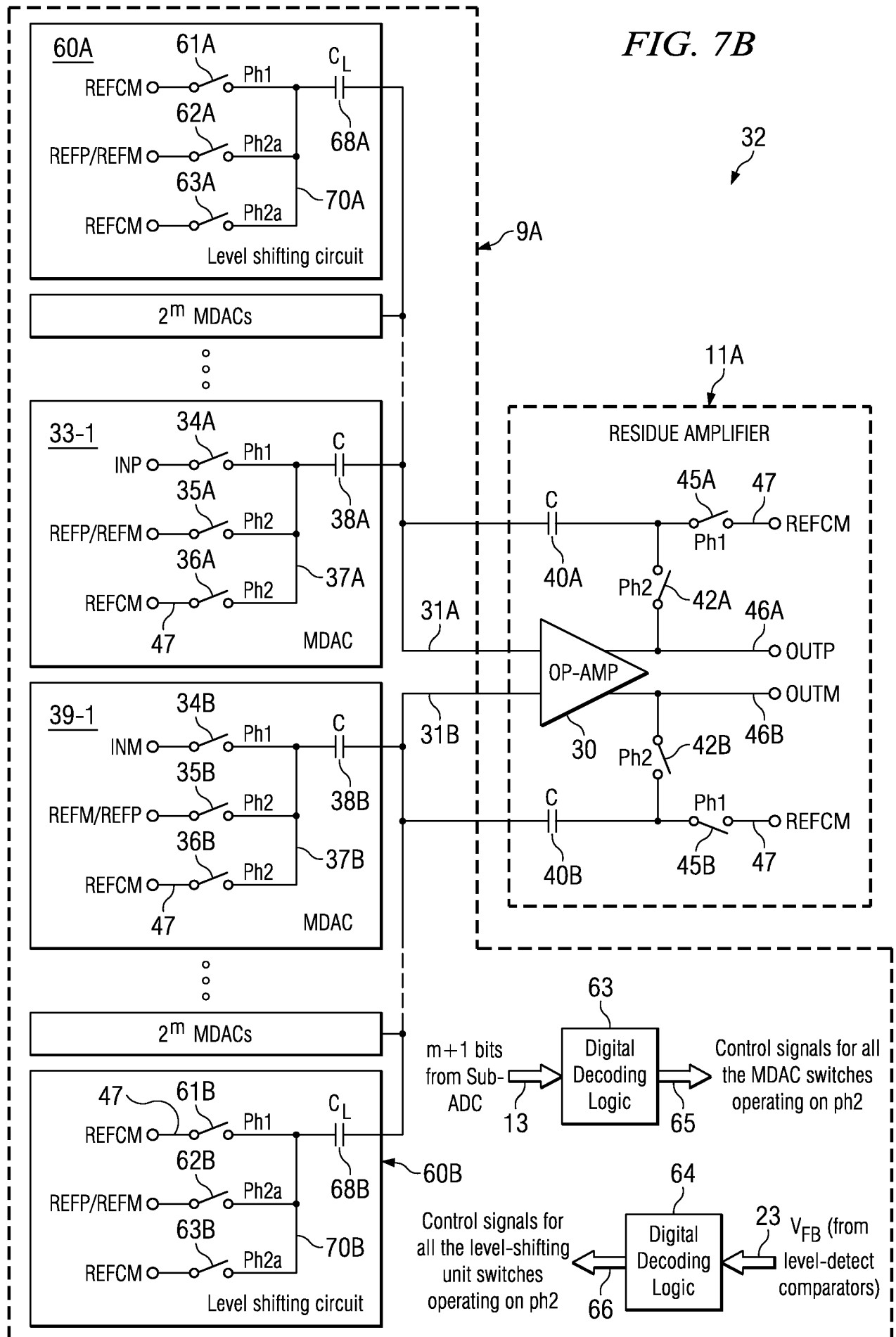


FIG. 7A

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FIG. 7B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/057811**A. CLASSIFICATION OF SUBJECT MATTER****H03M 1/12(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03M 1/12; H03M 1/10; H03M 1/06; H03M 1/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:ADC(analog to digital converter), pipeline, residue amplifier, redundancy bit, linearity, level-shifting, voltage range**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006-0227025 A1 (KAMAL EL-SANKARY et al.) 12 October 2006 See paragraphs 5-7, 69-70; claims 33-35; and figures 8B, 8C.	1-20
A	US 7372391 B1 (MATTHEW COURCY et al.) 13 May 2008 See column 6, lines 11-77; claim 1; and figure 6.	1-20
A	US 2005-0275571 A1 (JOHNNY BJORNSEN) 15 December 2005 See paragraphs 14-18; claims 1-4; and figure 4.	1-20
A	US 2005-0242982 A1 (JOHN B. HUGHES) 03 November 2005 See paragraphs 7-9, 53, 56-62; and figure 12.	1-20
A	US 2006-0114144 A1 (COLIN GERARD LYDEN et al.) 01 June 2006 See paragraphs 93-95; and figures 10a, 10b, 22.	1-20

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

06 December 2013 (06.12.2013)

Date of mailing of the international search report

09 December 2013 (09.12.2013)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/057811

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US 2005-0275571 A1	15/12/2005	US 7129866 B2	31/10/2006
US 2005-0242982 A1	03/11/2005	AT 360919 T AU 2003-281643 A1 AU 2003-281643 A8 CN 1669224 A CN 1669224 CO DE 60313481 D1 DE 60313481 T2 EP 1552614 A2 EP 1552614 B1 GB 0216897 D0 JP 2005-534221 A US 7002505 B2 WO 2004-010586 A2 WO 2004-010586 A3	15/05/2007 09/02/2004 09/02/2004 14/09/2005 01/10/2008 06/06/2007 10/01/2008 13/07/2005 25/04/2007 28/08/2002 10/11/2005 21/02/2006 29/01/2004 21/05/2004
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