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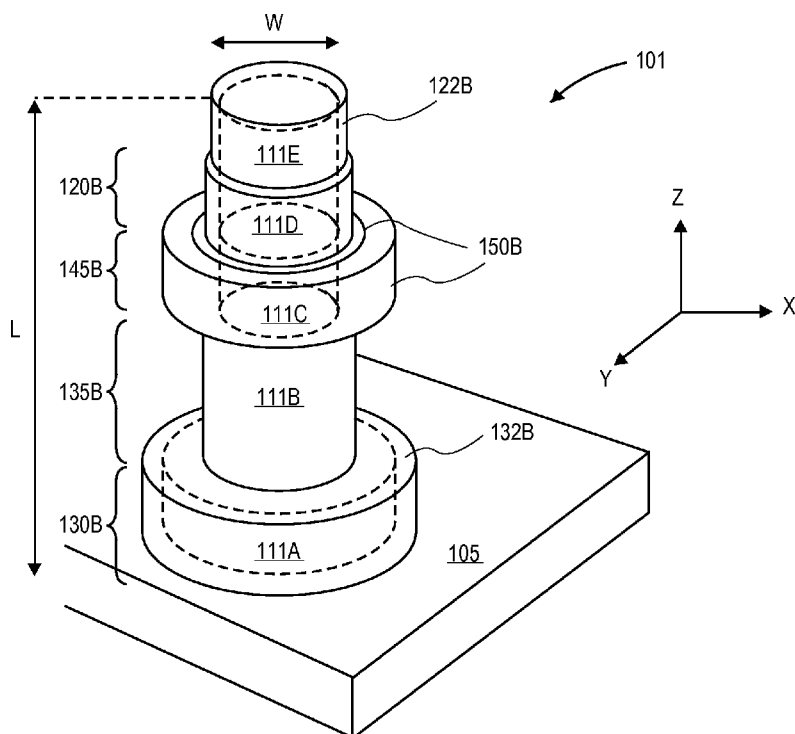
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(54) Title: PATTERNING OF VERTICAL NANOWIRE TRANSISTOR CHANNEL AND GATE WITH DIRECTED SELF ASSEMBLY



(57) Abstract: Directed self-assembly (DSA) material, or di-block co-polymer, to pattern features that ultimately define a channel region a gate electrode of a vertical nanowire transistor, potentially based on one lithographic operation. In embodiments, DSA material is confined within a guide opening patterned using convention lithography. In embodiments, channel regions and gate electrode materials are aligned to edges of segregated regions within the DSA material.

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**PATTERNING OF VERTICAL NANOWIRE TRANSISTOR CHANNEL AND GATE
WITH DIRECTED SELF ASSEMBLY**

TECHNICAL FIELD

Embodiments of the invention generally relate to transistor fabrication for microelectronics, and more particularly pertain to patterning of a vertical nanowire transistor using directed self-assembly (DSA).

BACKGROUND

In vertically oriented transistors, well-controlled material layer thickness define functional lengths, such as gate length (L_g), and material composition may be advantageously tailored to achieve band gap and mobility differentiation. Current drive can also be continuously scaled by lithographic patterning of the channel width (W_g) and corresponding cross-section of the nanowire. However, in practical applications, one may need to print nanowire features (e.g., holes) on the order of 15nm or less in diameter while having very good critical dimension (CD) uniformity, good circularity, and of minimal feature pitch for highest density. In addition the channel pattern must be accurately aligned to the gate stack and contact metallization.

Lithographic printing of holes less than 15nm with sufficient CD uniformity, circularity, and pitch is beyond the capability of known ArF or EUV resist. Techniques whereby holes are printed larger and then shrunk fail to achieve desired pitches (e.g., <30nm). Such pitches are also below the resolution of even two mask patterning techniques, and as such would require at least three mask patterning steps along with a very aggressive shrink process employing an expensive lithography toolset.

Techniques to pattern a vertical nanowire transistor to dimensions below 15nm and pitches below 30nm, which are manufacturable at lower cost are therefor advantageous.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention are illustrated by way of example, and not limitation, in the figures of the accompanying drawings in which:

Figure 1 is an isometric illustration of a vertical nanowire transistor, in accordance with an embodiment;

Figure 2 is a flow diagram illustrating a method of forming a vertical nanowire transistor, in accordance with an embodiment;

Figures 3A, 3B, 3C, 3D, and 3E illustrate plan views of single-channel structures formed as operations in the method of Figure 2 are performed, in accordance with an embodiment;

Figures 4A, 4B, 4C, 4D, and 4E illustrate cross-sectional views of the structures illustrated in Figure 3A-3E, in accordance with an embodiment;

Figures 5A, 5B, 5C, 5D, 5E, and 5F illustrate plan views of single-channel structures formed as operations in the method of Figure 2 are performed, in accordance with an embodiment;

Figures 6A, 6B, 6C, 6D, 6E, and 6F illustrate cross-sectional views of the structures illustrated in Figure 5A-5D, in accordance with an embodiment;

Figures 7A, 7B, and 7C illustrate plan views of dual-channel structures formed as operations in the method of Figure 2 are performed, in accordance with an embodiment;

Figures 8A, 8B, and 8C illustrate cross-sectional views of the structures illustrated in Figure 7A-7C, in accordance with an embodiment;

Figures 9A, 9B, 9C, 9D, and 9E illustrate cross-sectional views of single-channel structures formed as operations in the method of Figure 2 are performed, in accordance with an embodiment;

Figures 10A, 10B, 10C, 10D, 10E, 10F and 10G illustrate cross-sectional views of single-channel structures formed as operations in the method of Figure 2 are performed, in accordance with an embodiment;

Figure 11 is a functional block diagram of a mobile computing platform employing non-planar transistors, in accordance with an embodiment of the present invention; and

Figure 12 illustrates a functional block diagram of computing device in accordance with one embodiment.

DETAILED DESCRIPTION

In the following description, numerous details are set forth. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without these specific details. In some instances, well-known methods and devices are shown in block diagram form, rather than in detail, to avoid obscuring the present invention. Reference throughout this specification to “an embodiment” or “in one embodiment” means that a particular feature, structure, function, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrase “in an embodiment” in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the two embodiments are not structurally or functionally exclusive of the other.

The terms “coupled” and “connected,” along with their derivatives, may be used herein to describe structural relationships between components. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, “connected”

may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" may be used to indicate that two or more elements are in either direct or indirect (with other intervening elements between them) physical or electrical contact with each other, and/or that the two or more elements co-operate or interact with each other (e.g., as in a cause an effect relationship).

The terms "over," "under," "between," and "on" as used herein refer to a relative position of one material layer with respect to other layers. As such, for example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in direct contact with that second layer.

Figure 1 is an isometric illustration of an exemplary vertical nanowire transistor 101, which may be fabricated in accordance with embodiments of the present invention. For the vertical nanowire transistor 101, a semiconductor nanowire is vertically oriented with respect to the substrate 105 so that the longitudinal length L is along the z dimension (perpendicular to a surface plane of the substrate 105) and the width W defines an area of the substrate 105 occupied by the nanowire. As for a laterally oriented transistor, the vertical transistor 101 comprises one or more semiconductor materials along the longitudinal length L corresponding to functional regions of the transistor including the channel region 145B disposed between an extrinsic source/drain region 135B, source/drain region 130B and source/drain region 120B. Depending on the embodiment a drain of the transistor 101 may be "down," on the substrate 105, or the transistor may be inverted to have "source down." In the vertical form, the transistor 101 has critical dimensions, such as channel length and L_g (i.e., portions of the longitudinal length L) defined by material layer thickness, which can be very well-controlled (e.g., to 5-10 Å) by either epitaxial growth processes, implantation processes, or deposition processes.

Generally, substrate 105 and the first and second semiconductor material layers 111C, 111B may be any known in the art including group IV materials (e.g., Si, Ge, SiGe), III-N materials (e.g., GaN, AlGaN, etc.), or group III-V materials (e.g., InAlAs, AlGaAs, etc.). The drain/source regions 130B, 120B are of semiconductor material layers 111A, 111D, which may be the same material as for the channel region 145B, or a different material. The source/drain contact 122B may include a semiconductor 111E disposed on the source/drain region 120, such as a p+ tunneling layer and/or a highly doped (e.g., n+) low band gap capping layer. A low resistivity ohmic contact metal may further be included in the source contact 122B.

The transistor 101 includes a gate stack 150B coaxially wrapping completely around the nanowire within the channel region 145B. Similarly, the source/drain contacts 122B and 132B are also illustrated as coaxially wrapping around the source/drain regions 120B, 130B, though

they need not. Disposed between the gate stack 150B, a first dielectric spacer (not depicted) is disposed on the source/drain contact 132B and coaxially wraps completely around the extrinsic source/drain region 135B along a first longitudinal length. A second dielectric spacer 156 is disposed on the gate stack 150B and coaxially wraps completely around the source/drain region 120B along a second longitudinal length with the source/drain contact 132B disposed on the second dielectric spacer.

Figure 2 is a flow diagram illustrating a method 201 of forming a vertical nanowire transistor, such as the transistor 101, in accordance with an embodiment. Generally, the method 201 entails employing a directed self-assembly (DSA) material, such as a di-block co-polymer, to pattern features that ultimately define a channel region of a vertical nanowire transistor based on one lithographic operation, potentially without need for a scanner.

The method 201 begins with lithographically patterning a guide opening in a mask layer at operation 205. The guide opening is to provide an edge that a DSA material aligns to, and is more particularly a closed polygon, and advantageously curved, and more particularly circular. Any number of guide openings may be concurrently printed at operation 205, for example a 1-D or 2-D array of guide openings may be printed using any conventional lithographic process known in the art. As used herein, a 1-D array entails a row or column of guide openings with minimum pitch between adjacent ones in the row or column dimension and more than minimum pitch between adjacent rows or columns, while a 2-D array entails rows and columns of guide openings with minimum pitch between all guide openings in both row and column dimensions. The size and shape of the guide can be changed to allow more than one channel hole to be patterned in a given guide layer opening as for example Figure 7b.

Figures 3A-3D illustrate plan views of a single-channel transistor structure formed as operations in the method 201 are performed, in accordance with an embodiment. A circular guide opening 315 is shown in Figure 3A, and represents one repeating unit for a 1-D or 2-D array that is printed at operation 205. Figures 4A-4D illustrate cross-sectional views of the structures illustrated in Figure 3A-3D, respectively, along the A'-A line depicted in Figure 3A. In the exemplary embodiment, the circular guide opening 315 has a critical dimension (CD1) of no more than 20nm with the polygon edge 306 defining a hole 305 (Figure 4A) through a thickness of the mask 340, which may be a photoresist or hardmask material. Any conventional resist formulation suitable for the lithography tool employed may be utilized in photoresist embodiments. The mask 340 is disposed over a semiconductor layer having a z-height thickness (T1) corresponding to a desired transistor channel length (Lg) that is to provide the channel region of the nanowire transistor. For the exemplary embodiment illustrated in Figure 4A, the mask 340 is disposed directly on the channel semiconductor layer 315 (e.g., single crystalline silicon, SiGe, etc.), although an intervening material layer, such as a hardmask material layer

(e.g., SixNy, SiO₂, etc.), may be disposed between the photoresist layer 340 and channel semiconductor layer 315.

Returning to Figure 2, the method 201 continues with operation 210 where the DSA material is deposited into the guide opening(s) formed at operation 205. In preparation for application of the DSA material the surface of layer 315 may be treated so that it is equally attractive/repulsive to the polymer A and polymer B. As shown in Figure 3B and 4B, a DSA material 350 fills the guide opening 315 and is contained by the guide opening edges 306. The DSA material 350 generally comprises at least first and second polymers (i.e., a polymer A and a polymer B). When applied over the substrate, for example by spin coating, the polymers A and B are in an intermixed state. Beyond the basic chemistry of the polymers A and B, the polymers A and B may each be chosen to have desired distribution of molecular weights and the DSA material 350 may be selected to have a desired polymer A-to-polymer B ratio (A:B), as a function of the geometry and CD of the guide operation 315 and the desired CD of the transistor channel region. While any DSA material known in the art may be utilized, in the exemplary embodiment one of the polymer A and polymer B is present in a photoresist employed as the mask 340. For example, where the mask 340 comprises polystyrene, polymer A or polymer B is also polystyrene. In one such embodiment, the other of the polymers is PMMA (poly(methyl methacrylate)).

The method 201(Figure 2) continues with operation 215 where the DSA material is segregated into interior and exterior polymer regions. Segregation of the polymer A from the polymer B occurs while the DSA material 350 is annealed at an elevated temperature for a duration sufficient to permit adequate migration of the polymers, as a function of the dimensions of the guide opening 315, and the molecular weights of the polymers, etc. With the guide opening 315 enclosing the DSA material 350, segregation can be engineered so as one of the polymers (e.g., polymer A) migrates away from the guide edge 306 while the other of the polymers (e.g., polymer B) migrates toward the guide edge 306. An interior polymer region 350A comprising predominantly a first polymer is then completely surrounded by an exterior polymer region 350B comprising predominantly a second polymer. In the exemplary embodiment shown in Figures 3C and 4C, the interior polymer region 350A is spaced apart from the guide opening edge to have a diameter of CD₂, reduced from that of CD₁. For appropriately chosen DSA constituents, under layer and guide opening edge surface properties, the interior polymer region 350A form integer numbers of substantially identical cylinders or spheres embedded within the exterior polymer region 350B. While in the exemplary single channel embodiment illustrated in Figures 3A-3E a single interior polymer region 350A is formed, multiples of such regions may be formed where the guide opening is sized sufficiently large in at least one dimension. With the segregation mechanics being a well-controlled function of the co-

polymer properties of the DSA material, the interior polymer region(s) maintain a consistent distance from each other and from the guide opening edges. As such, the interior polymer region 350A is effectively self-aligned to the guide opening edge 306.

Following the bake and/or cure performed at operation 215, the method 201 continues to operation 220 where a semiconductor channel region of the transistor is defined within the interior of the guide opening by removing one of the interior and exterior polymer regions selectively to the other. In the exemplary embodiment illustrated in Figures 3D and 4D, the exterior polymer region 350B is removed (e.g., dissolved) selectively to the interior polymer region 350A. As further shown, the exterior polymer region 350B is also removed selectively to the mask 340 such that two edges are defined at operation 220: an edge of the interior polymer region 350A, and the guide opening edge 306 with the edge of the interior polymer region 350A being self-aligned to the guide opening edge 306.

An annular trench 375 is then etched through the channel semiconductor layer 315 and the interior polymer region 350A removed, along with the mask 340. The exposed portion of the channel semiconductor layer 325 may be recessed with any etch process known in the art for the given semiconductor material (Si, SiGe, etc.), to form a sidewall of a channel region 315A associated with the transistor Lg aligned with an edge of the interior polymer region 350A. As used herein, "aligned" permits some nominal etch bias (positive or negative) to be incurred which may change the CD of the channel region 315A from that of CD2, but the dimension of the channel region 315A is nevertheless based on that of the interior polymer region 350A and as such, significantly smaller than the dimension of the guide opening (CD1). For example, the sidewalls of the channel region 315A may be aligned to the interior polymer region 350A with an anisotropic etch through the channel region 315A followed by an isotropic etch that recesses the sidewalls of the channel region 315A relative to the CD of the interior polymer region 350A. In one embodiment where the guide opening CD1 is less than 20nm, the channel region 315A has a CD2 of less than 15nm. The trench 375 may be stopped on an underlying semiconductor material 310 (e.g., single crystalline Si, SiGe, Ge, etc.), on a basis of compositional etch selectivity or on the basis of a timed etch, for example. Depending on the embodiment, the underlying semiconductor material 310 is either already heavily doped to a particular conductivity typed, may be doped upon its exposure, or is partially removed and regrown as a doped material. In the embodiment illustrated in Figures 3D and 4D, the semiconductor material 310 heavily doped to function as a source/drain region (e.g., source/drain region 111A and/or extrinsic source/drain region 111B in Figure 1).

With the semiconductor channel region defined at operation 220, the method 201 continues with depositing a gate material over a sidewall of the semiconductor channel region at operation 225. Generally, any gate dielectric deposition process known in the art may be

performed, including deposition of a sacrificial gate dielectric which is to be subsequently replaced later in the fabrication process (e.g., as in a conventional “gate-last” type process flow). However, in the exemplary embodiment, at operation 225, a non-sacrificial high-k (e.g., > 9) gate dielectric 380 is deposited on the semiconductor surface exposed at the bottom of the trench 375 and on the trench sidewalls 380A and 380B. As one example, a metal oxide, such as but not limited to HfO₂, or ZrO₂, is deposited by atomic layer deposition at operation 225 as the gate dielectric 380.

The method 201 then completes with operation 230 where the semiconductor channel region 315A is surrounded with a gate electrode material. In the exemplary embodiment, operation 230 comprises filling the cylindrical trench 375 with a gate electrode material 390. The gate electrode material 390 may include any conventional gate electrode material, such as but not limited to polysilicon, a work function metal, and/or a fill metal. Techniques known in the art, such as but not limited to deposition and polish, may be utilized to planarize the gate electrode material 390 with the channel region 315A, or an overlying hardmask layer. As shown in Figures 3E and 4E, the gate dielectric 380 electrically isolates the gate electrode material 390 from the channel region 315A, as well as from the underlying source/drain region 310 and peripheral semiconductor material 315B. Notably, the dimensions of the gate electrode material 390 are therefore fully self-aligned to the guide opening edge 306 as well as self-aligned to the channel region 315A with only the z-height thickness of the gate electrode material 390 left to vary as a function of the desired transistor channel length. The vertical transistor can then be completed with conventional techniques (e.g., deposition or epitaxial growth of the source/drain semiconductor 111D, on the exposed surface of the semiconductor channel region 315A, deposition of contact metallization, etc.).

Figures 5A-5F illustrate plan views of single-channel structures formed as operations in the method 201 are performed, in accordance with an alternate embodiment. Figures 6A-6F illustrate cross-sectional views of the structures illustrated in Figure 5A-5F, in accordance with an embodiment. Generally, in the embodiment illustrated in Figures 5A-5F, operations 205-215 are as were described in the context of Figures 3A-3D with the exception that the mask 340 is deposited on a dielectric layer 415 (e.g., Si₃N₄, SiON, SiO₂, etc.) disposed over the semiconductor layer 310. Following segregation of the co-polymers into the interior polymer region 350A and exterior polymer region 350B, at operation 220 the interior polymer region 350A is removed selectively to the exterior polymer region 350B, as is illustrated in Figures 5D and 6D. In this exemplary embodiment, the mask 340 is also removed leaving an annular mask consisting of the exterior polymer region 350B. The dielectric layer 415 is then etched to expose the underlying crystalline surface of the semiconductor material 310. As shown in Figure 6E, the operation 220 further includes removing the exterior polymer region 350B and epitaxially

growing (e.g., with MOCVD, etc.) the semiconductor channel region 315A from the exposed crystalline semiconductor surface with the dielectric layer 415 serving as a growth stopping hardmask. Given the size of the semiconductor channel region 315A (e.g., <15nm), the grown semiconductor material layer may have advantageously good crystallinity as a result of aspect ratio trapping. After formation of the semiconductor channel region 315A, the second portion of the dielectric layer 415 is recessed to form a cylindrical trench exposing a sidewall of the semiconductor channel region. In the exemplary embodiment depicted, the dielectric layer 415 is completely removed, exposing a surface of the semiconductor layer 310. For one such embodiment, the semiconductor layer 310 is appropriately doped to serve as the source/drain semiconductor region of the nanowire transistor with the channel region 315A then epitaxially grown directly a surface of the source/drain semiconductor region.

As shown in Figures 5F and 6F, the method 201 then continues through operation 225 to form the gate dielectric on the sidewalls 380A, over the semiconductor material layer 310 and on the sidewalls 380B, substantially as is described elsewhere herein in reference to Figures 3E and 4E. The gate electrode material 390 is then deposited at operation 230 to again surround the channel region 315A.

While Figures 3A-3E and 4A-4E, as well as Figure 5A-5F and 6A-6F, illustrate single channel embodiments of the method 201, Figures 7A-7C illustrate plan views of dual-channel structures formed as operations in the method 201 are performed, in accordance with an embodiment. Figures 8A-8C further illustrate cross-sectional views of the structures illustrated in Figure 7A-7C. Generally, the method 201 is practiced substantially as described elsewhere herein for single-channel embodiments with the DSA material defining two (or more) interior polymer regions, each of which becomes the basis for defining a semiconductor channel region of a vertical nanowire transistor. For such multi-channel embodiments, the DSA material is leveraged to self-align the channel regions to a surrounding gate and also reduce pitch between adjacent channel regions relative to the pitch employed to print the guide openings. In exemplary embodiments, the pitch of two adjacent channel regions is below the resolution limit of a scanner employed to print the guide openings.

Figures 7A and 8A illustrate the guide opening 315 initially patterned (e.g., printed or etched) into the mask 340 (e.g., at operation 205) is larger in a first dimension (e.g., axis B1) than in a second dimension (e.g., axis A1). Generally, the longer length B1 exceeds a threshold characteristic of the DSA material (e.g., 40nm) while the shorter length A1 does not (e.g., A1 may be approximately the diameter of a guide opening for a single-channel embodiment (e.g., less than 20nm). In embodiments, the longer length B1 is at least twice the shorter length A1. For certain surface conditions, such an elongated guide opening 315, when filled with a DSA material having proper co-polymer properties, anneals into the two interior polymer regions

350A1 and 350A2 illustrated in Figures 7B and 8B. Both of the interior polymer regions 350A1 and 350A2 are surrounded by a contiguous exterior polymer region 350B with the material properties of each segregated region being as described elsewhere herein in the context of single-channel embodiments. Upon segregation, the interior polymer regions 350A1 and 350A2 have essentially identical dimensions (e.g., CD3 as shown in Figure 8C). In the exemplary
5 embodiments where the guide opening has at least one dimension that is less than 20nm, the interior polymer regions 350A1 and 350A2 each have a width that is less than 15nm, and in further such embodiments the pitch of the interior polymer regions 350A1 and 350A2 is also less than 15nm.

10 With the plurality of interior polymer regions 350A1 and 350A2 materially distinguished from the exterior polymer region 350B, the method 201 proceeds through operations 220, 225, 230 substantially as described for single-channel embodiments (e.g., as illustrated either by Figures 3A-3E, 4A-4E) to define the channel semiconductor layer 315 into the two channel regions 315A1 and 315A2 controlled by a shared gate electrode 390 through the gate dielectrics
15 350A1 and 350A2, respectively. As such, segregation capabilities of the DSA material may be utilized to make multi-wired vertical transistors which may be individually sized for optimal gate control (reduced short channel effects) while providing a desired amount of drive current (determined by the number of discrete channels formed).

20 In embodiments, not only are the channel region and gate of a vertical transistor defined based on segregation of a DSA material, so too are other functional regions of the transistor, such as, but not limited to, the source drain regions, as illustrated by the Figures 9A-9E and 10A-10G. Figures 9A, 9B, 9C, 9D, and 9E illustrate cross-sectional views of single-channel structures formed as operations in the method of Figure 2B are performed, in accordance with an embodiment. Generally, in this exemplary embodiment, source/drain regions, as well as the
25 channel region, of a vertical nanowire transistor are regrown in regions defined by segregation of a DSA material.

Figure 9A begins at the completion of operation 215 where DSA material has been segregated in the interior polymer region 350A and exterior polymer region 350B. The substrate in this embodiment includes a dielectric layer 925 disposed over a degenerately doped
30 semiconductor layer 945, that is further disposed over a crystalline semiconductor substrate layer 903. The interior polymer region 350A is removed selectively to the exterior polymer region 350B, as described elsewhere herein, and also selectively to the mask 340, as shown in Figure 9B. An interior trench is then etched through the dielectric layer 925 and the layer 945 in the region where the interior polymer region 350A was removed to expose the semiconductor 903.
35 With the mask 340 then removed, a peripheral portion of the dielectric layer 925 is removed to leave an annular perimeter of dielectric 925 surrounding the interior trench. A selective epitaxial

process is then employed to form the nanowire transistor from the seeding surface of the exposed semiconductor substrate layer 903 within the interior trench and periphery region. As shown in Figure 9D, a first (bottom) crystalline source/drain semiconductor layer 310 is grown from the semiconductor substrate layer 903 and from the semiconductor layer 945. Regrowth of the source/drain semiconductor layer 310 may improve crystallinity in the channel region subsequently grown as advantageous defect trapping may occur in the source/drain semiconductor layer 310. Furthermore, regrowth of the source/drain semiconductor layer 310 serves to selectively form a connection to the now embedded conductive semiconductor layer 945 with crystalline or polycrystalline semiconductor formed over the semiconductor layer 945. A semiconductor channel region 315 is then epitaxially grown from the source/drain semiconductor layer 310. A second (top) source/drain semiconductor layer 320 is further grown over the semiconductor channel region 315. The regrown film is polished back to planarize against the dielectric layer 925 as a polish stop. Due to initial non-planarity between the interior trench and the periphery, the planarization process removes the regrown semiconductor in the periphery back to the bottom source/drain semiconductor layer 310 while the top source/drain semiconductor layer 320 is retaining in the interior region as a portion of the vertical nanowire transistor.

The gate dielectric is formed at operation 220 by first recessing the annular portion of the dielectric layer 925 remaining where the exterior polymer region 350B was originally disposed. This exposes a sidewall of the semiconductor channel region 315. The dielectric layer 925 may be completely recessed with an etch selective to the underlying conductive layer 945, in which case the gate dielectric formed at operation 225 serves to insulate the gate electrode material 390 from the conductive layer 945. Alternatively, the dielectric layer 925 may be recessed only partially (e.g., with a timed etch back) to increase the thickness of dielectric between the gate electrode material 390 and underlying conductive layer 945. As such, the top surface of the vertical nanowire transistor structure illustrated in Figure 9E is planarized and provides top-side access to all functional regions of the transistor for contact (e.g., silicidation) and interconnect metallization.

Figures 10A, 10B, 10C, 10D, and 10E illustrate cross-sectional views of single-channel structures formed as operations in the method of Figure 2B are performed, in accordance with an embodiment. In this exemplary embodiment, a stack of semiconductor materials including two source/drain layers and a channel layer are etched based on a DSA material. This embodiment may therefore be considered a special case of the embodiment illustrated by Figures 3A-3E, 4A-4E. Figure 10A begins with the DSA material segregated into the interior and exterior polymer regions 350A, 350B. The substrate includes a semiconductor material layer stack including compositionally distinct (through either doping or differing lattice atoms) material layers. For

the exemplary embodiment, the semiconductor material stack includes a bottom source/drain layer 1010 disposed on a substrate 1003, a channel layer 1015 disposed on the bottom source/drain layer 1010, and a top source/drain layer 1020 disposed over the channel layer 1015. Disposed over the semiconductor stack is a dielectric (hardmask) layer 1030.

5 As shown in Figure 10B, the exterior polymer region 350B is removed selectively to the interior polymer region 350A and the mask 340. An annular trench is then etched through most of the stack to expose the bottom source/drain layer 1010, as shown in Figure 10C. A dielectric spacer 1040 (Figure 10D) is formed along sidewalls of the semiconductor stacks and a silicide 1050 is formed on the exposed both source/drain layer 1010. Dielectric material 1060 is then
 10 deposited within the trench, planarized, and recessed (etched back) to a z-height (thickness) sufficient to re-expose the channel region sidewall. An isotropic etch removes the dielectric spacer 1040 and the gate dielectric 380 is deposited in the trench over the recessed dielectric material 1060 and on the channel semiconductor sidewall. The gate electrode material is then deposited in the trench, planarized with a top surface of the dielectric 1030 and then recess
 15 etched to a z-height (thickness) sufficient to control the channel region. Finally, a dielectric 1070 is deposited in the trench, planarized with the top surface of the dielectric 1030. The dielectric 1030 may then be removed selectively to the dielectric 1070 to expose the top source/drain 1020 in preparation for contact metallization. Hence, the vertically-oriented nanowire transistor with sub-lithographic wire dimensions (e.g., <15nm) are self-alignedly
 20 fabricated, along with local interconnects, on the basis of a single lithographic mask and DSA material.

Figure 11 is a functional block diagram of a SOC implementation of a mobile computing platform, in accordance with an embodiment of the present invention. The mobile computing platform 1100 may be any portable device configured for each of electronic data display,
 25 electronic data processing, and wireless electronic data transmission. For example, mobile computing platform 1100 may be any of a tablet, a smart phone, laptop computer, etc. and includes a display screen 1105, the SOC 1110, and a battery 1115. As illustrated, the greater the level of integration of the SOC 1110, the more of the form factor within the mobile computing device 1100 that may be occupied by the battery 1115 for longest operative lifetimes between
 30 charging, or occupied by memory (not depicted), such as a solid state drive, DRAM, etc., for greatest platform functionality.

The SOC 1110 is further illustrated in the expanded view 1120. Depending on the embodiment, the SOC 1110 includes a portion of a silicon substrate 1160 (i.e., a chip) upon which one or more of a power management integrated circuit (PMIC) 1115, RF integrated circuit (RFIC) 1125 including an RF transmitter and/or receiver, a controller thereof 1111, and one or
 35 more central processor core, or memory 1177. In embodiments, the SOC 1110 includes one or

more vertical nanowire transistors (FETs) in conformance with one or more of the embodiments described herein. In further embodiments, manufacture of the SOC 1110 includes one or more of the methods described herein for fabricating a vertically-oriented nanowire transistor (FET).

Figure 12 is a functional block diagram of a computing device 1200 in accordance with one embodiment of the invention. The computing device 1200 may be found inside the platform 1100, for example, and further includes a board 1202 hosting a number of components, such as but not limited to a processor 1204 (e.g., an applications processor) and at least one communication chip 1206. In embodiments, at least the processor 1204 includes a vertical nanowire transistor (FET) having structures in accordance with embodiments describe elsewhere herein, and/or fabricated in accordance with embodiments further described elsewhere herein. The processor 1204 is physically and electrically coupled to the board 1202. The processor 1204 includes an integrated circuit die packaged within the processor 1204. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

In some implementations the at least one communication chip 1206 is also physically and electrically coupled to the board 1202. In further implementations, the communication chip 1206 is part of the processor 1204. Depending on its applications, computing device 1200 may include other components that may or may not be physically and electrically coupled to the board 1202. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., RAM or ROM) in the form of flash memory or STTM, etc., a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, touchscreen display, touchscreen controller, battery, audio codec, video codec, power amplifier, global positioning system (GPS) device, compass, accelerometer, gyroscope, speaker, camera, and mass storage device (such as hard disk drive, solid state drive (SSD), compact disk (CD), and so forth).

At least one of the communication chips 1206 enables wireless communications for the transfer of data to and from the computing device 1200. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1206 may implement any of a number of wireless standards or protocols, including but not limited to those described elsewhere herein. The computing device 1200 may include a plurality of communication chips 1206. For instance, a first communication chip 1206 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second

communication chip 1206 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

It is to be understood that the above description is intended to be illustrative, and not restrictive. For example, while flow diagrams in the figures show a particular order of operations performed by certain embodiments of the invention, it should be understood that such order is not required (e.g., alternative embodiments may perform the operations in a different order, combine certain operations, overlap certain operations, etc.). Furthermore, many other embodiments will be apparent to those of skill in the art upon reading and understanding the above description. Although the present invention has been described with reference to specific exemplary embodiments, it will be recognized that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

CLAIMS

What is claimed is:

1. A method of forming a nanowire transistor on a substrate, the method comprising:
5 lithographically patterning a guide opening of a first diameter in a mask layer disposed over a source/drain semiconductor layer of the transistor;
depositing a directed self-assembly (DSA) material into the guide opening;
segregating the DSA material into an interior polymer region completely surrounded by an exterior polymer region within the guide opening;
10 defining a semiconductor channel region of the transistor within the guide opening by removing one of the interior and exterior polymer regions selectively to the other, wherein the channel region diameter and spacing from an edge of the guide opening are both defined by the DSA segregation;
removing the other of the interior and exterior polymer regions;
15 depositing a gate dielectric over the semiconductor channel region; and
surrounding the semiconductor channel region with an annular gate electrode having an outer diameter self-aligned to the guide opening.
2. The method of claim 1, wherein defining the semiconductor channel region further
20 comprises:
removing the exterior polymer region while retaining the interior polymer region to expose a portion of a channel semiconductor layer; and
recessing the exposed portion of the channel semiconductor layer to form a cylindrical trench having a channel semiconductor sidewall associated with a channel length of the transistor
25 aligned with an edge of the interior polymer region.
3. The method of claim 2, wherein the recessing exposes a source/drain semiconductor region of the transistor, and wherein the gate dielectric isolates the source/drain semiconductor region from the gate electrode material.
30
4. The method of claim 2, wherein depositing a gate dielectric over the semiconductor channel region further comprises depositing the gate dielectric into the cylindrical trench and covering the channel semiconductor sidewall; and
wherein surrounding the semiconductor channel region with the gate electrode comprises
35 filling the cylindrical trench with a gate electrode material.

5. The method of claim 1, wherein defining the semiconductor channel region further comprises:

removing the interior polymer region while retaining the exterior polymer region to expose an underlying first portion of a dielectric layer;

5 etching a trench in the exposed first portion of the dielectric layer to expose a crystalline semiconductor surface; and

epitaxially growing the semiconductor channel region from the exposed crystalline semiconductor surface; and

10 recessing a second portion of the dielectric layer adjacent to the semiconductor channel region to form a cylindrical trench exposing a sidewall of the semiconductor channel region.

6. The method of claim 5, wherein the crystalline semiconductor surface is a surface of a source/drain semiconductor region of the transistor.

15 7. The method of claim 5, wherein the crystalline semiconductor surface is a surface of an undoped or lightly doped semiconductor substrate, and wherein epitaxially growing the semiconductor channel region further comprises first growing a source/drain semiconductor region of the transistor from the surface of the semiconductor substrate and then growing the semiconductor channel region from the source/drain semiconductor region.

20

8. The method of claim 5, wherein depositing a gate dielectric over the semiconductor channel region further comprises depositing the gate dielectric into the cylindrical trench and covering the channel semiconductor sidewall; and

25 wherein surrounding the semiconductor channel region with the gate electrode comprises filling the cylindrical trench with a gate electrode material.

9. The method of claim 8, wherein the gate dielectric is deposited over the recessed second portion of the dielectric layer.

30 10. The method of claim 1, wherein lithographically patterning a guide opening further comprises printing an opening having a first diameter in a first dimension and a second diameter in a second dimension, the second diameter being at least twice the first diameter;

wherein segregating the DSA material into the interior polymer region completely surrounded by the exterior polymer region within the guide opening further comprises forming
35 first and second polymer regions, each completely surrounded by the exterior polymer region; and

wherein defining the semiconductor channel region further comprises forming a first and second channel region, each channel region having a diameter and a spacing from an edge of the guide opening defined by the DSA segregation.

- 5 11. The method of claim 1, wherein depositing the DSA material into the guide opening further comprises spin coating a DSA material comprising first and second polymeric materials; and

wherein segregating the DSA material further comprises curing the DSA material at a temperature and for a duration sufficient to permit the first polymeric material to migrate into the interior polymer portion while the second polymeric material migrates into the exterior polymer portion

10

12. The method of claim 11, wherein one of the first and second polymeric materials comprises PMMA.

15

13. The method of claim 12, wherein the other of the first and second polymeric material comprises polystyrene.

20

14. The method of claim 11, wherein the mask layer comprises one of the first and second polymeric materials.

25

15. A method of forming a nanowire transistor on a substrate, the method comprising:
lithographically patterning a guide opening of a first diameter in a mask layer disposed over a source/drain semiconductor layer of the transistor;
depositing a directed self-assembly (DSA) material into the guide opening;
segregating the DSA material into an interior polymer region completely surrounded by an exterior polymer region within the guide opening;

removing the exterior polymer region selectively to the interior polymer region to form a cylindrical trench exposing an underlying hardmask layer;

30

etching through the hardmask layer to advance the trench and expose a first semiconductor source/drain region;

etching through the exposed portion of the first semiconductor source/drain region to advance the trench and expose a semiconductor channel layer disposed below the source/drain region;

35

etching the exposed portion of the semiconductor channel layer to advance the trench and expose a semiconductor layer disposed below the semiconductor channel layer;

filling the trench with a first dielectric material and etching back the first dielectric material selectively relative to the hardmask layer to expose a sidewall of the semiconductor channel layer;

depositing a gate dielectric over the sidewall; and

5 filling the trench with a gate electrode material to surround the sidewall with an annular gate electrode having an outer diameter self-aligned to the guide opening.

16. The method of claim 15, further comprising forming a silicide of the semiconductor layer disposed below the semiconductor channel layer prior to filling the trench with the dielectric.

10

17. The method of claim 16, further comprising:

etching the gate electrode material back relative to the hardmask layer to expose a sidewall of the first semiconductor source/drain region, and

15 filling the trench with a second dielectric material and planarizing the second dielectric material to a surface of the hardmask layer;

removing the hardmask layer selectively the second dielectric material to expose a surface of the first semiconductor source/drain region; and

depositing a contact metal on the exposed surface of the first semiconductor source/drain region.

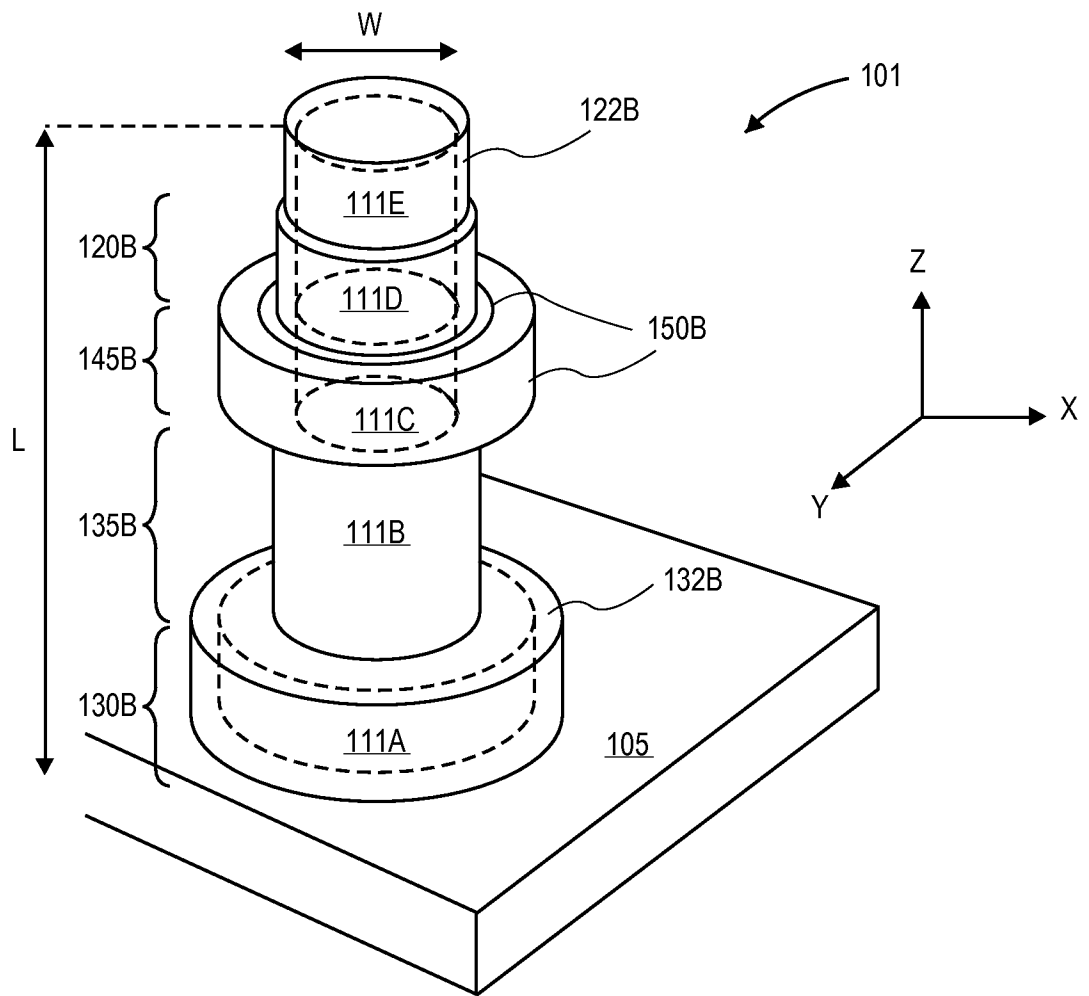
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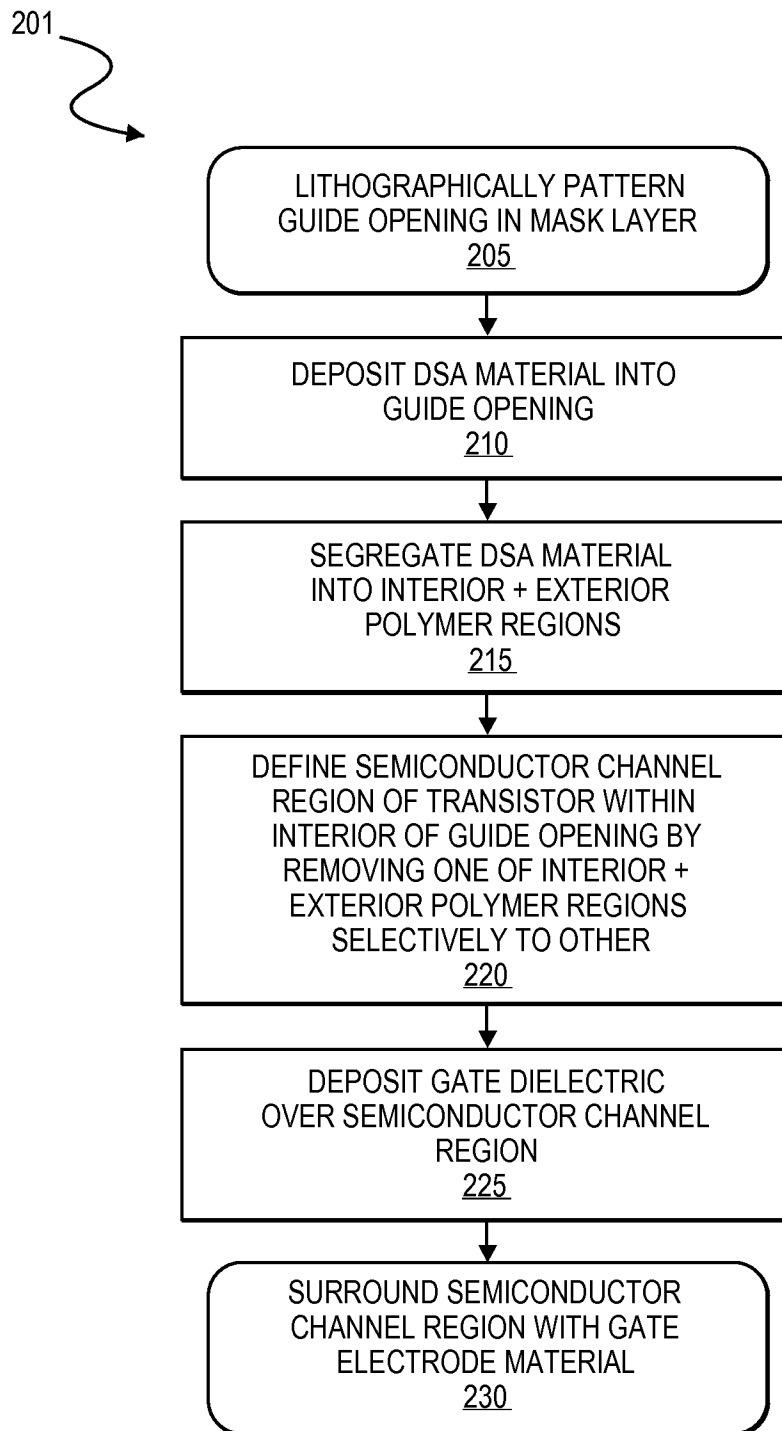
18. The method of claim 15, wherein depositing the DSA material into the guide opening further comprises spin coating a DSA material comprising first and second polymeric materials; and

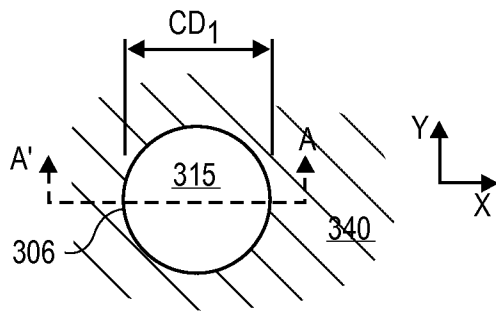
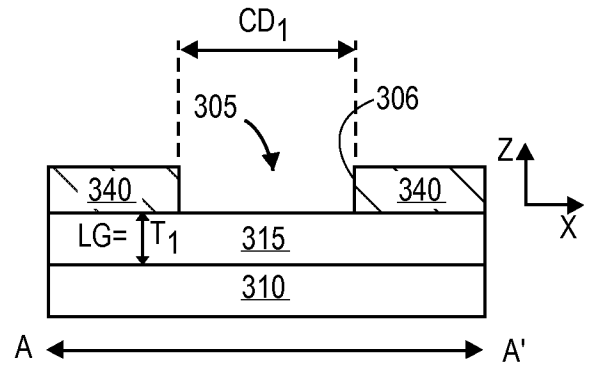
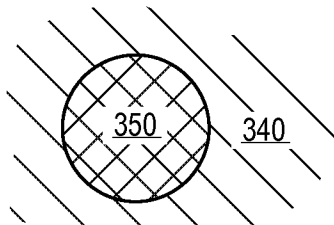
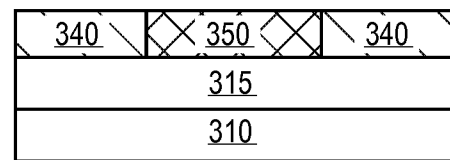
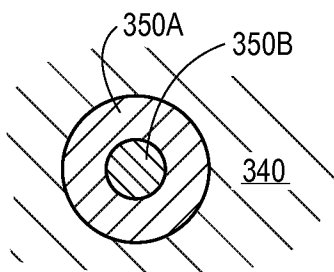
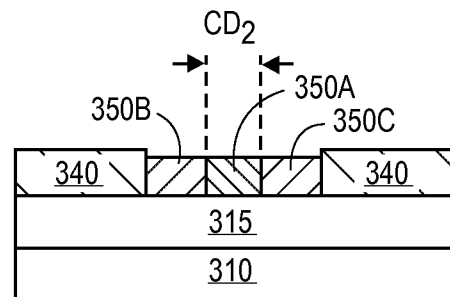
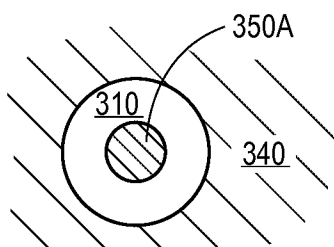
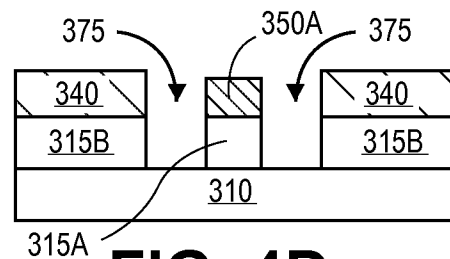
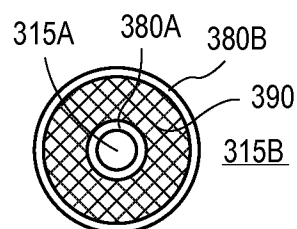
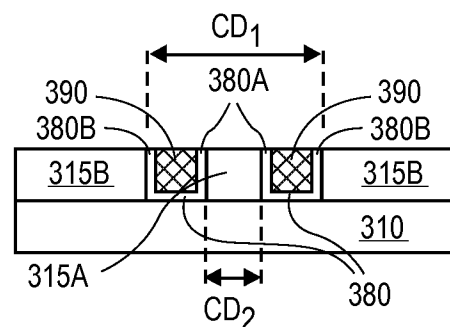
25 wherein segregating the DSA material further comprises curing the DSA material at a temperature and for a duration sufficient to permit the first polymeric material to migrate into the interior polymer portion while the second polymeric material migrates into the exterior polymer portion

19. The method of claim 18, wherein one of the first and second polymeric materials
30 comprises PMMA.

20. The method of claim 19, wherein the other of the first and second polymeric material comprises polystyrene.

**FIG. 1**

**FIG. 2**

**FIG. 3A****FIG. 4A****FIG. 3B****FIG. 4B****FIG. 3C****FIG. 4C****FIG. 3D****FIG. 4D****FIG. 3E****FIG. 4E**

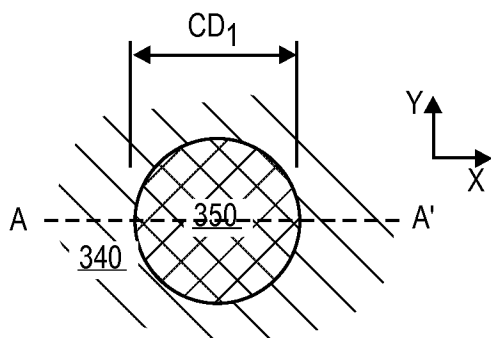


FIG. 5A

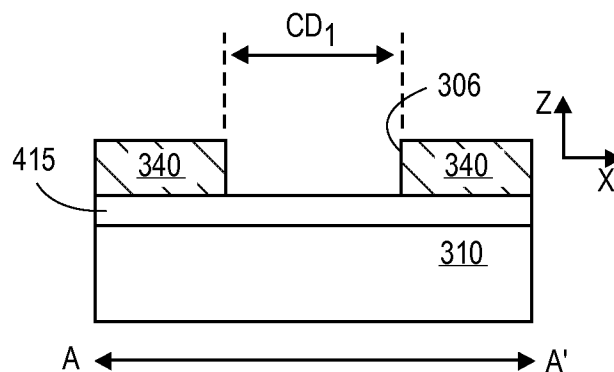


FIG. 6A

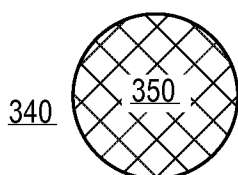


FIG. 5B

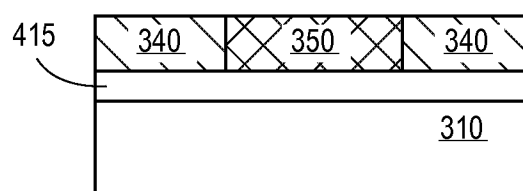


FIG. 6B

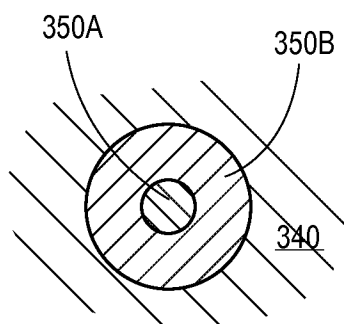


FIG. 5C

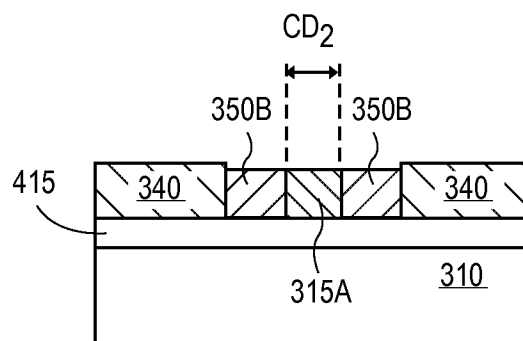


FIG. 6C

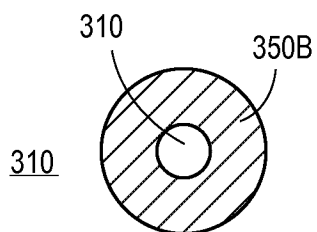


FIG. 5D

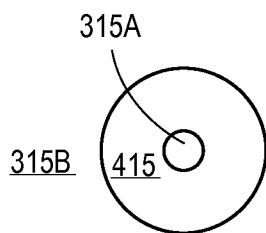


FIG. 5E

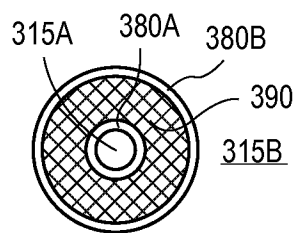


FIG. 5F

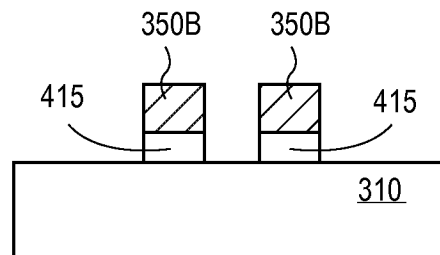


FIG. 6D

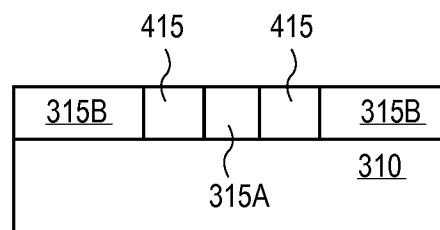


FIG. 6E

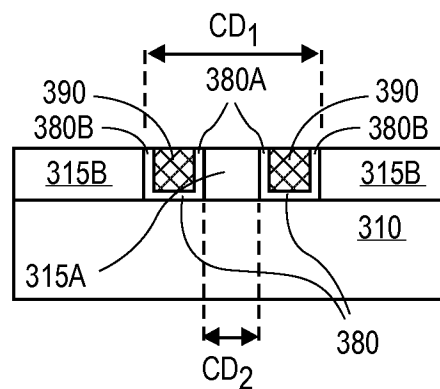


FIG. 6F

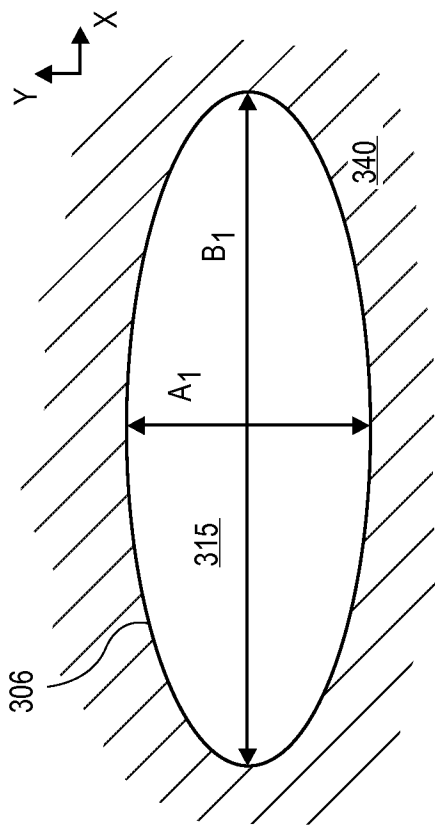


FIG. 7A

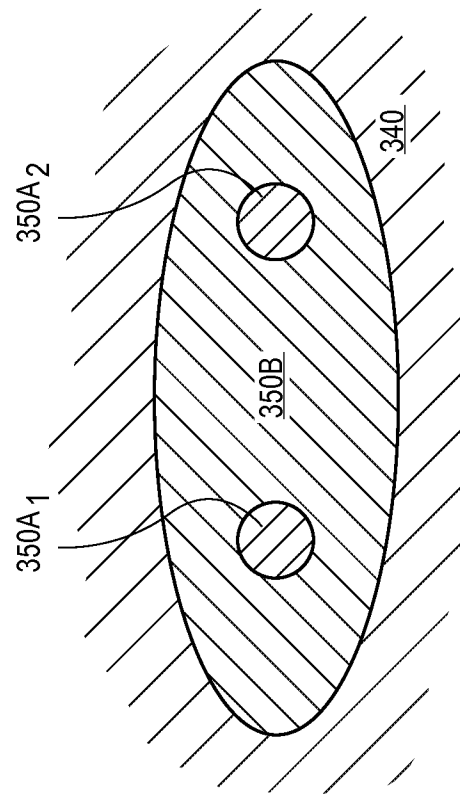


FIG. 7B

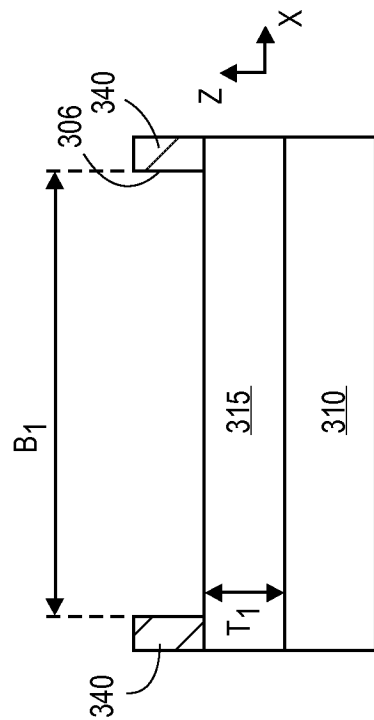


FIG. 8A

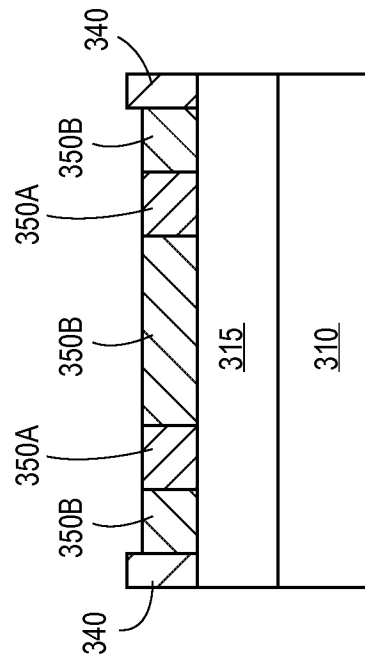


FIG. 8B

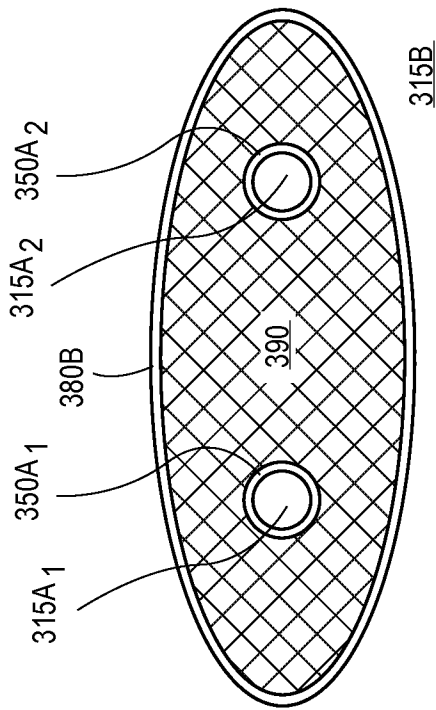


FIG. 7C

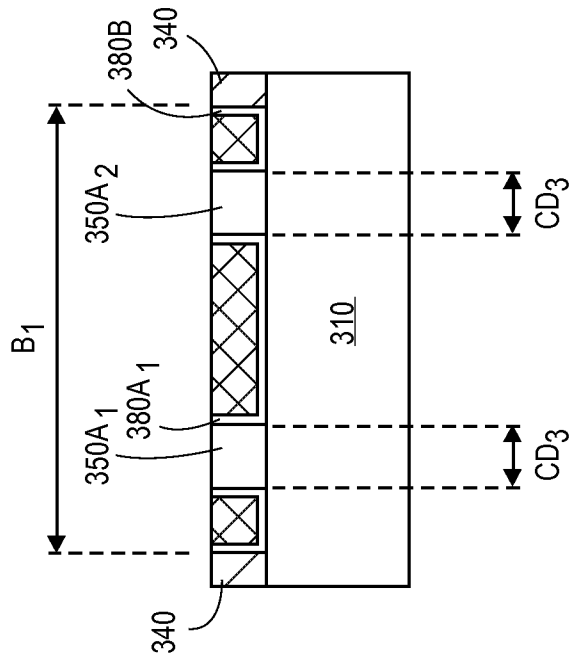


FIG. 8C

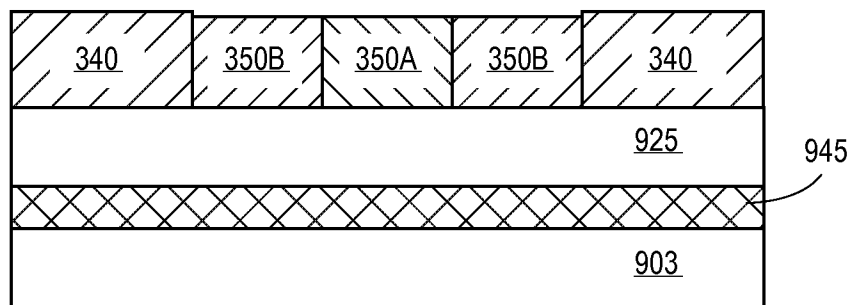


FIG. 9A

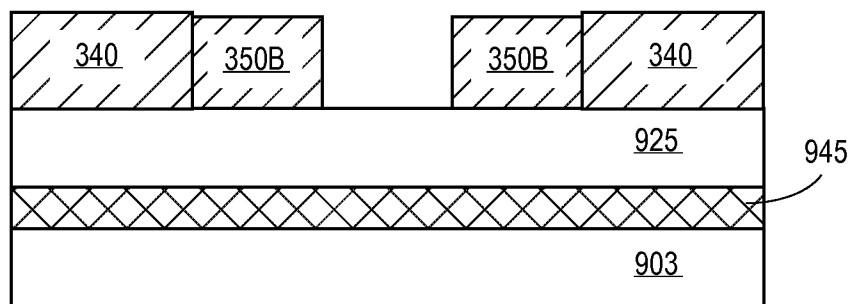


FIG. 9B

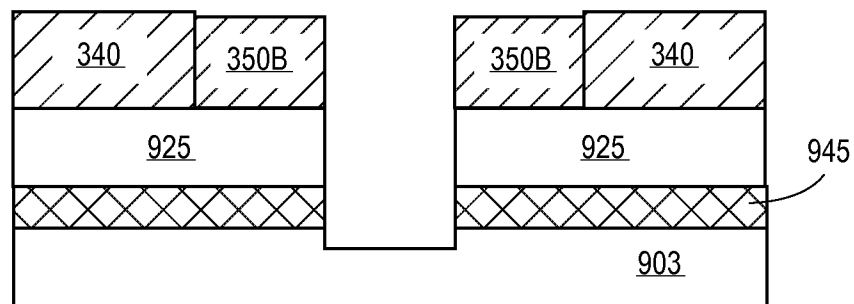


FIG. 9C

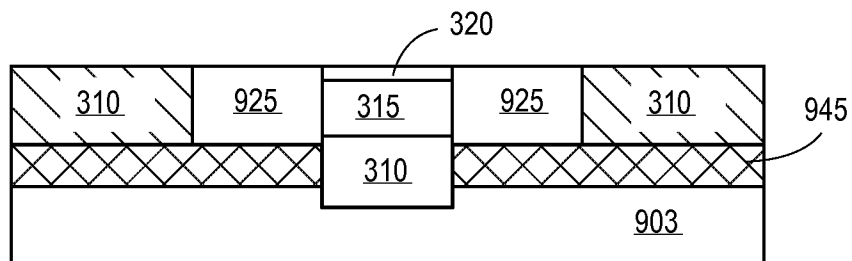


FIG. 9D

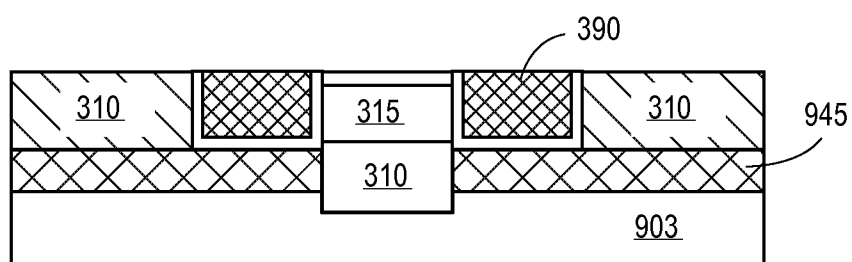


FIG. 9E

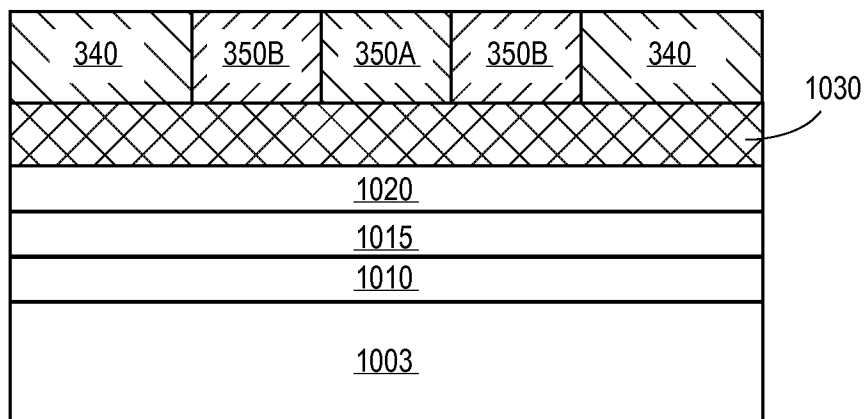


FIG. 10A

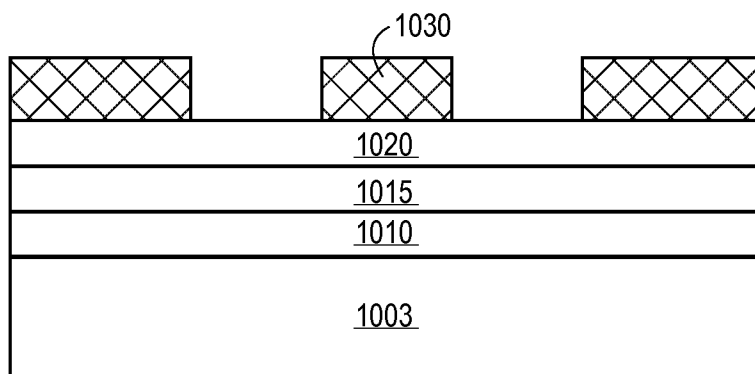


FIG. 10B

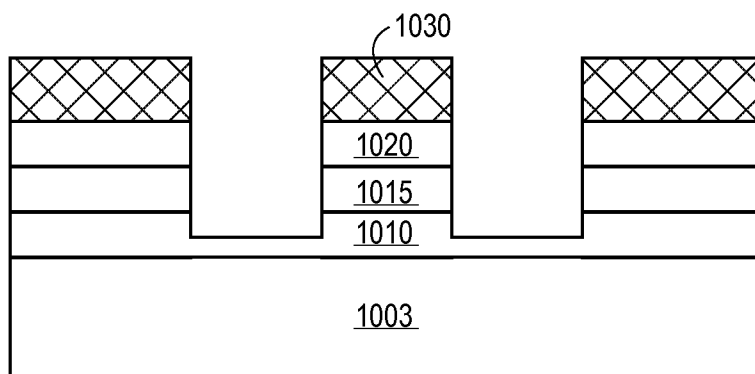


FIG. 10C

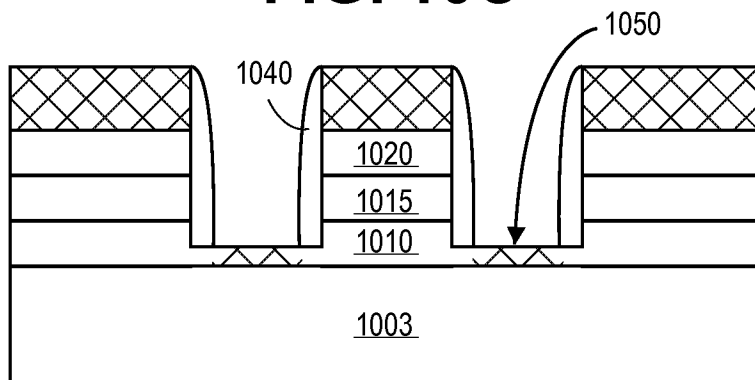


FIG. 10D

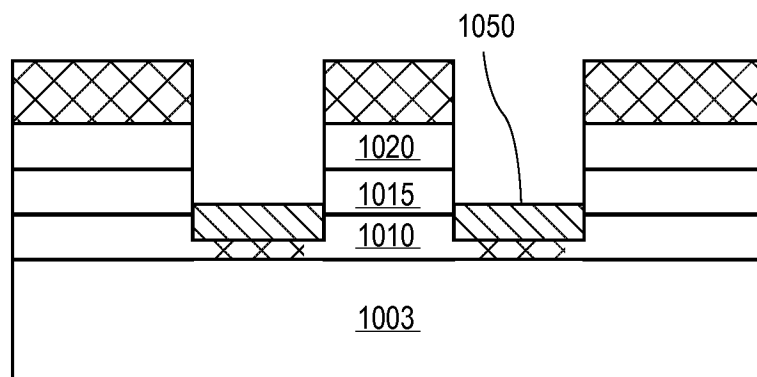


FIG. 10E

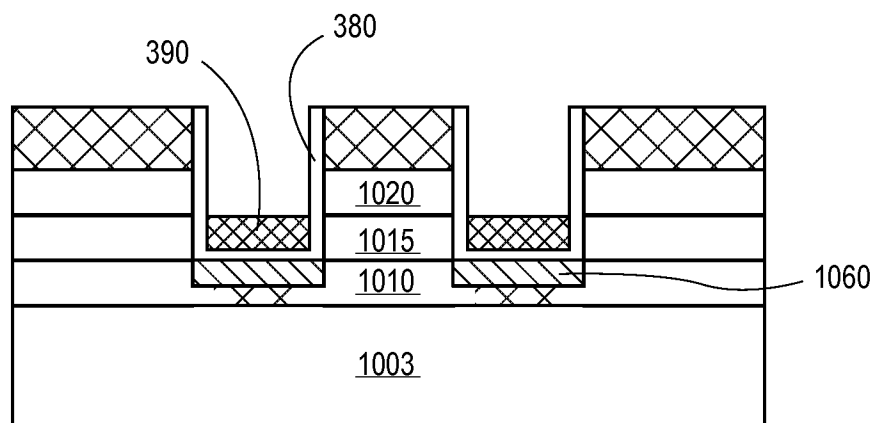


FIG. 10F

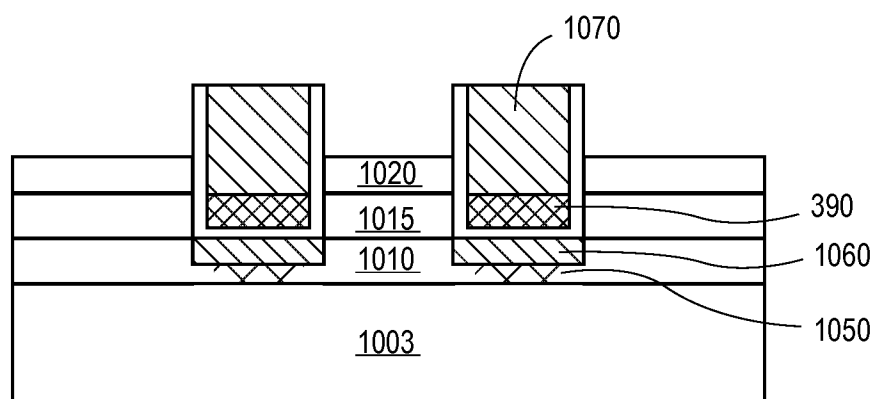
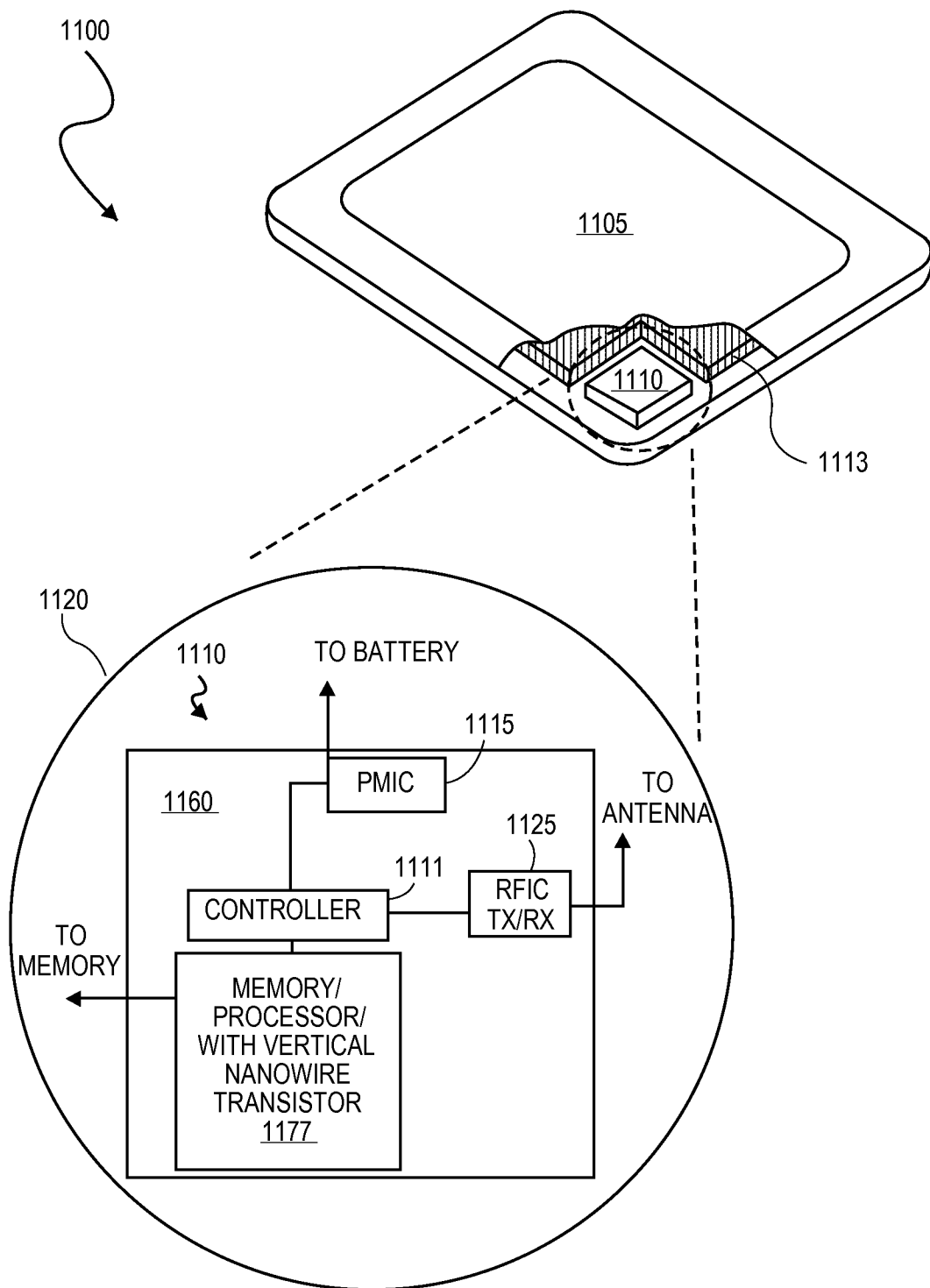


FIG. 10G

**FIG. 11**

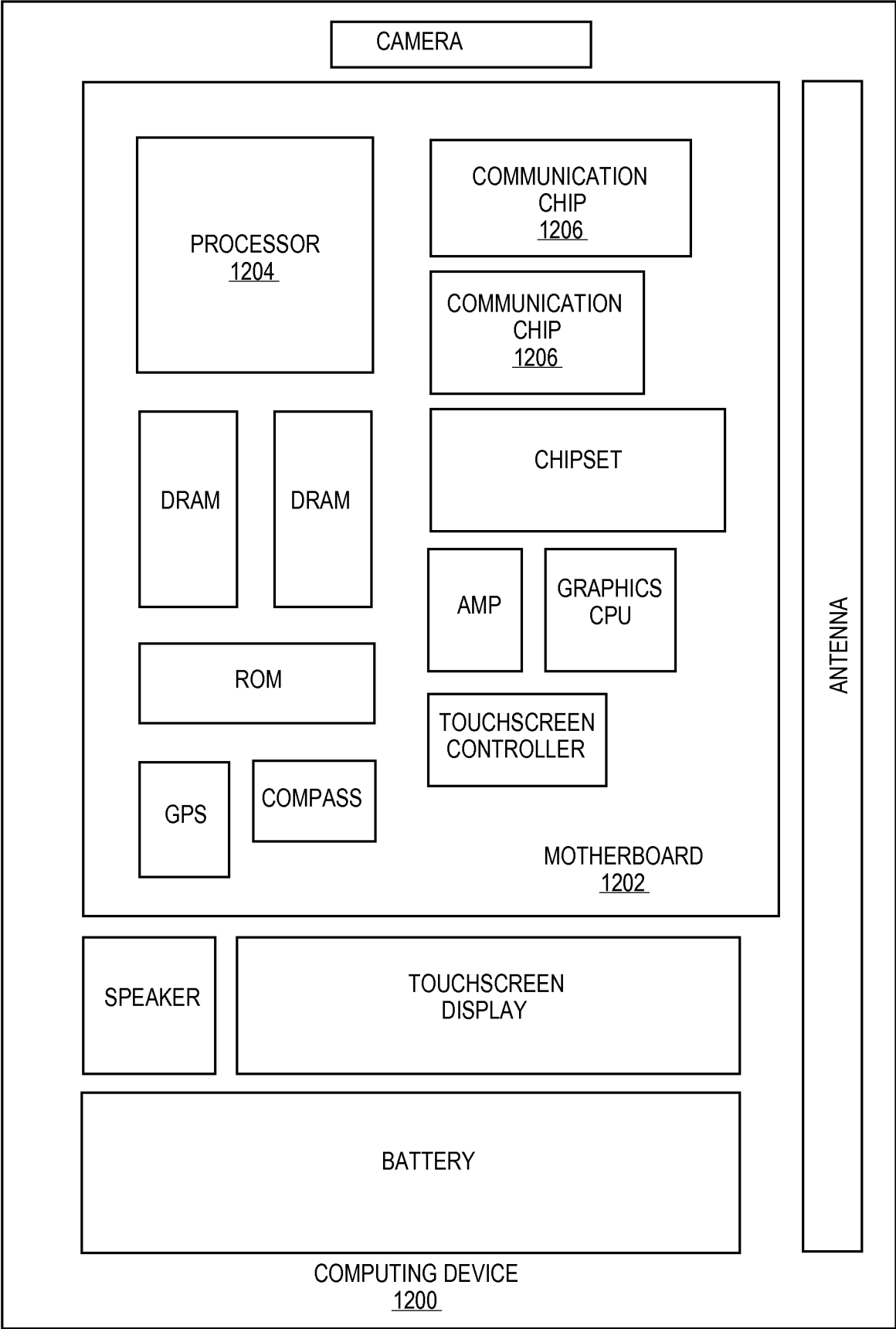


FIG. 12

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/336(2006.01)i, H01L 29/78(2006.01)i, H01L 21/027(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/336; H01L 21/84; H01L 29/772; H01L 27/108; H01L 21/8242; H01L 29/78; H01L 21/335; H01L 21/8238;
H01L 27/12; H01L 21/027

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: transistor, directed, self, assembly, gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008-0099845 A1 (HAINING YANG et al.) 01 May 2008 See abstract, paragraphs [0036]-[0080] and figures 1A-8B.	1-20
A	KR 10-2005-0019468 A (SAMSUNG ELECTRONICS CO., LTD.) 03 March 2005 See abstract, pages 3-4 and figures 2-6.	1-20
A	US 2010-0276669 A1 (SHACHAR RICHTER et al.) 04 November 2010 See abstract, paragraphs [0103]-[0106] and figures 4A-4F.	1-20
A	KR 10-2009-0054472 A (MICRON TECHNOLOGY, INC.) 29 May 2009 See abstract, paragraphs [0027]-[0032] and figures 1A-1D.	1-20
A	KR 10-2003-0050997 A (DONGBU ELECTRONICS CO., LTD.) 25 June 2003 See abstract, pages 2-3 and figures 1-3.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

25 September 2013 (25.09.2013)

Date of mailing of the international search report

25 September 2013 (25.09.2013)

Name and mailing address of the ISA/KR

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302-701, Republic of Korea

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Authorized officer

CHOI Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/046899

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