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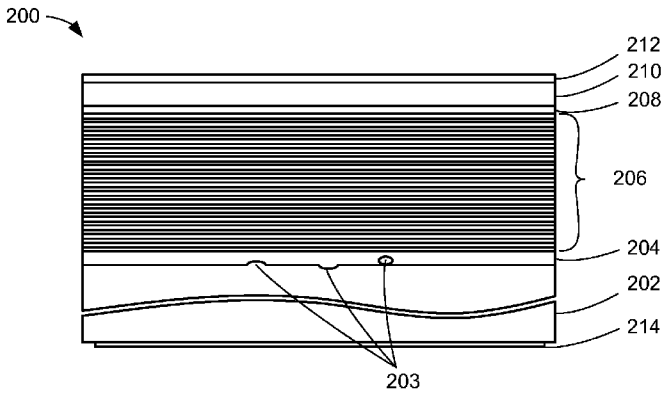

FIG. 2

(57) Abstract: An extreme ultraviolet mirror or blank production system includes: a first deposition system for depositing a planarization layer over a semiconductor substrate; a second deposition system for depositing an ultra-smooth layer over the planarization layer, the ultra-smooth layer having reorganized molecules; and a third deposition system for depositing a multi-layer stack over the ultra-smooth layer. The extreme ultraviolet blank includes: a substrate; a planarization layer over the substrate; an ultra-smooth layer over the planarization layer, the ultra-smooth layer having reorganized molecules; a multi-layer stack; and capping layers over the multi-layer stack. An extreme ultraviolet lithography system includes: an extreme ultraviolet light source; a mirror for directing light from the extreme ultraviolet light source; a reticle stage for placing an extreme ultraviolet mask blank with a planarization layer and an ultra-smooth layer over the planarization layer; and a wafer stage for placing a wafer.

WO 2014/152033 A1

ULTRA-SMOOTH LAYER ULTRAVIOLET LITHOGRAPHY MIRRORS AND BLANKS, AND MANUFACTURING AND LITHOGRAPHY SYSTEMS THEREFOR

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims the benefit of U.S. Provisional Patent Application serial number 61/786,109, filed March 14, 2013, and the subject matter thereof is incorporated herein by reference thereto.

[0002] The present application contains subject matter related to a concurrently filed U.S. Patent Application serial number 14/139,307, filed December 23, 2013, and the subject matter thereof is incorporated herein by reference thereto.

[0003] The present application contains subject matter related to a concurrently filed U.S. Patent Application serial number 14/139,371, filed December 23, 2013, and the subject matter thereof is incorporated herein by reference thereto.

[0004] The present application contains subject matter related to a concurrently filed U.S. Patent Application serial number 14/139,415, filed December 23, 2013, and the subject matter thereof is incorporated herein by reference thereto.

[0005] The present application contains subject matter related to a concurrently filed U.S. Patent Application serial number 14/139,457, filed December 23, 2013, and the subject matter thereof is incorporated herein by reference thereto.

TECHNICAL FIELD

[0006] The present invention relates generally to extreme ultraviolet lithography mirrors and blanks, and manufacturing and lithography systems for such extreme ultraviolet lithography mirrors and blanks.

BACKGROUND

[0007] Extreme ultraviolet lithography (EUV, also known as soft x-ray projection lithography) is a contender to replace deep ultraviolet lithography for the manufacture of 0.13 micron, and smaller, minimum feature size semiconductor devices.

[0008] However, extreme ultraviolet light, which is generally in the 5 to 40 nanometer wavelength range, is strongly absorbed in virtually all materials. For that reason, extreme ultraviolet systems work by reflection rather than by transmission of light. Through the use of a series of mirrors, or lens elements, and a reflective element, or mask blank, coated with a non-reflective absorber mask pattern, the patterned actinic light is reflected onto a resist-coated semiconductor wafer.

[0009] The lens elements and mask blanks of extreme ultraviolet lithography systems are coated with reflective multilayer coatings of materials such as molybdenum and silicon. Reflection values of approximately 65% per lens element, or mask blank, have been obtained by using substrates that are coated with multilayer coatings that strongly reflect light essentially at a single wavelength within a extremely narrow ultraviolet bandpass; e.g., 12 to 14 nanometer bandpass for 13 nanometer ultraviolet light.

[0010] There are various classes of defects in semiconductor processing technology which cause problems in lens elements and masks. Opaque defects are typically caused by particles on top of the multilayer coatings or mask pattern which absorb light when it should be reflected. Clear defects are typically caused by pinholes in the mask pattern on top of the multilayer coatings through which light is reflected when it should be absorbed. And phase defects are typically caused by scratches and surface variations beneath the multilayer coatings which cause transitions in the phase of the reflected light. These phase transitions result in light wave interference effects which distort or alter the pattern that is to be exposed in the resist on the surface of the semiconductor wafer. Because of the shorter wavelengths of radiation which must be used for sub-0.13 micron minimum feature size, scratches and surface variations which were insignificant before now become intolerable.

[0011] While progress has been made in reducing or eliminating particle defects and work has been done on repair of opaque and clear defects in lens elements and masks, to date nothing has been done to address the problem of phase defects. For deep ultraviolet lithography, surfaces are processed to maintain phase transitions below 60 degrees. Similar processing for extreme ultraviolet lithography is yet to be developed.

[0012] For an actinic wavelength of 13 nanometers, a 180 degree phase transition in the light reflected from the multilayer coating may occur for a scratch of as little as 3 nanometers in depth in the underlying surface. This depth gets shallower with shorter wavelengths. Similarly, at the same wavelength, surface variations more abrupt than one (1) nanometer rise over one hundred (100) nanometers run may cause similar phase transitions. These phase transitions can cause a phase defect at the surface of the semiconductor wafer and irreparably damage the semiconductor devices.

[0013] In the past, lens elements and mask blanks for deep ultraviolet lithography have generally been of glass but silicon or ultra low thermal expansion materials have been proposed as alternatives for extreme ultraviolet lithography. Whether the lens element or mask blank is of glass, ultra low thermal expansion material, or silicon, the surface of the lens element or mask blank is made as smooth as possible by mechanical polishing with an abrasive. The scratches that are left behind in such a process are sometimes referred to as "scratch-dig" marks, and their depth and width depend upon the size of the particles in the abrasive used to polish the mask blank. For visible and deep ultraviolet lithography, these scratches are too small to cause phase defects in the pattern on the semiconductor wafer. However, for extreme ultraviolet lithography, scratch-dig marks are a significant problem because they will appear as phase defects.

[0014] Due to the short illumination wavelengths required for EUV lithography the lens elements and pattern masks used must be reflective mask instead of the transmissive masks used in current lithography. The reflective mask is made up of a precise stack of alternating thin layers of molybdenum and silicon, which creates a Bragg refractor or mirror. Because of the nature of the multilayer stack and the small feature size, any imperfections in the surface of the substrate on which the multilayer stack is deposited will be magnified and impact the final product. Imperfections on the scale of a few nanometers can show up as printable defects on the finished mask and need to be eliminated from the surface of the mask blank before deposition of the multilayer stack.

[0015] Common imperfections include pits, scratches, and particles. Common cleaning techniques remove many of the particles but either generate new pits or amplify existing pits. The pits can come from the polishing or cleaning process or can be from inclusions or flaws in the substrate material itself that are exposed during the cutting and polishing process. Further polishing can be used to remove the pits at the surface, but there is a risk that new pits will be exposed or caused in the process, which limits the usefulness of using polishing alone to

smooth and planarize the substrate surface. Another method for substrate smoothing is laser or plasma annealing. These techniques melt and reflow a thin surface layer of the glass substrate, removing local defects. The problem is that they induce longer range roughness or ripples in the substrate surface and so do not provide the substrate flatness required for EUV mask blanks.

[0016] In view of the need for the increasingly smaller feature size of electronic components, it is increasingly critical that answers be found to these problems. In view of the ever-increasing commercial competitive pressures, along with growing consumer expectations, it is critical that answers be found for these problems. Additionally, the need to reduce costs, improve efficiencies and performance, and meet competitive pressures adds an even greater urgency to the critical necessity for finding answers to these problems.

[0017] Solutions to these problems have been long sought but prior developments have not taught or suggested any solutions and, thus, solutions to these problems have long eluded those skilled in the art.

SUMMARY

[0018] An embodiment of the present invention provides an extreme ultraviolet lens element or blank production system that includes: a first deposition system for depositing a planarization layer over a semiconductor substrate; a second deposition system for depositing an ultra-smooth layer over the planarization layer, the ultra-smooth layer having reorganized molecules; and a third deposition system for depositing a multi-layer stack over the ultra-smooth layer.

[0019] An embodiment of the present invention provides an extreme ultraviolet lithography system that includes: an extreme ultraviolet light source; a mirror for directing light from the extreme ultraviolet light source; a reticle stage for placing an extreme ultraviolet mask blank with a planarization layer and an ultra-smooth layer over the planarization layer; and a wafer stage for placing a wafer.

[0020] An embodiment of the present invention provides an extreme ultraviolet blank that includes: a substrate; a planarization layer over the substrate; an ultra-smooth layer over the planarization layer, the ultra-smooth layer having reorganized molecules; a multi-layer stack having an amorphous metallic layer; and capping layers over the multi-layer stack.

[0021] Certain embodiments of the invention have other steps or elements in addition to or in place of those mentioned above. The steps or element will become apparent to those

skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] FIG. 1 is an extreme ultraviolet (EUV) mirror or mask blank production system.

[0023] FIG. 2 is an EUV mask blank in accordance with an embodiment of the present invention.

[0024] FIG. 3 is an EUV mask.

[0025] FIG. 4 is a method for making the EUV mask blank with ultra-low defects.

[0026] FIG. 5 is an optical train for an EUV lithography system.

[0027] FIG. 6 is an EUV lithography system.

DETAILED DESCRIPTION

[0028] The following embodiments are described in sufficient detail to enable those skilled in the art to make and use the invention. It is to be understood that other embodiments would be evident based on the present disclosure, and that system, process, or mechanical changes may be made without departing from the scope of the present invention.

[0029] In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent that the invention may be practiced without these specific details. In order to avoid obscuring the present invention, some well-known circuits, system configurations, and process steps are not disclosed in detail.

[0030] The drawings showing embodiments of the system are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and are shown exaggerated in the drawing FIGs. Similarly, although the views in the drawings for ease of description generally show similar orientations, this depiction in the FIGs. is arbitrary for the most part. Generally, the invention can be operated in any orientation.

[0031] Where multiple embodiments are disclosed and described having some features in common, for clarity and ease of illustration, description, and comprehension thereof, similar and like features will be described with similar reference numerals.

[0032] For expository purposes, the term "horizontal" as used herein is defined as a plane parallel to the plane or surface of a lens element or mask blank, regardless of its orientation.

The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Terms, such as "above", "below", "bottom", "top", "side" (as in "sidewall"), "higher", "lower", "upper", "over", and "under", are defined with respect to the horizontal plane, as shown in the figures. The term "on" indicates that there is direct contact between elements.

[0033] The term "processing" as used herein includes deposition of material or photoresist, patterning, exposure, development, etching, cleaning, and/or removal of the material or photoresist as required in forming a described structure.

[0034] Embodiments of the present invention use various established techniques for depositing silicon, silicon oxide, and related films of compatible thermal expansion coefficient by CVD, PVD, ALD, and flowable CVD to fill the pits and bury the defects. Once deposited, the films surface maybe smooth and flat enough for further multilayer stack deposition, or may then be smoothed further using a variety of established smoothing or polishing techniques, including CMP, annealing, or ion beam polishing.

[0035] Referring now to FIG. 1, therein is shown an extreme ultraviolet (EUV) mirror or blank production system 100. The EUV mirror or blank production system 100 includes a mask blank loading and carrier handling system 102 into which mask blanks 104 are loaded. An airlock 106 provides access to a wafer handling vacuum chamber 108. In the embodiment shown, the wafer handling vacuum chamber 108 contains two vacuum chambers, a first vacuum chamber 110 and a second vacuum chamber 112. Within the first vacuum chamber 110 is a first wafer handling system 114 and in the second vacuum chamber 112 is a second wafer handling system 116.

[0036] The wafer handling vacuum chamber 108 has a plurality of ports around its periphery for attachment of various other systems. The first vacuum chamber 110 has a degas system 118, a first physical vapor deposition system 120, a second physical vapor deposition system 122, and a preclean system 124.

[0037] The second vacuum chamber 112 has a first multi-cathode source 126, a flowable chemical vapor deposition (FCVD) system 128, a cure chamber 130, and an ultra-smooth deposition chamber 132 connected to it.

[0038] In an alternative embodiment, the FCVD system 128, the cure chamber 130, and the ultra-smooth deposition chamber 132 can be in a separate system from the EUV mirror or blank production system 100.

[0039] The first wafer handling system 114 is capable of moving wafers, such as a wafer 134, among the airlock 106 and the various systems around the periphery of the first vacuum

chamber 110 in a continuous vacuum. The second wafer handling system 116 is capable of moving wafers, such as a wafer 136, around the second vacuum chamber 112 while maintaining the wafers in a continuous vacuum.

[0040] Referring now to FIG. 2, therein is shown an EUV lens element or mask blank 200 in accordance with an embodiment of the present invention. The EUV lens element or mask blank 200 has an ultra-low expansion substrate 202 of glass or silicon. The top surface of the ultra-low expansion substrate 202 has imperfections 203, such as bumps, pits, scratches, and particles, which result from chemical mechanical polishing (CMP) with an abrasive or other polishing method and handing of the substrate. The scratches that are left behind in such a process are sometimes referred to as "scratch-dig" marks, and their depth and width depend upon the size of the particles in the abrasive used to polish the EUV lens element or mask blank 200 to form a EUV mirror or mask.

[0041] It has been discovered that the imperfections in the EUV lens element or mask blank 200 can be eliminated by deposition of a planarization layer 204. The planarization layer 204 can be formed by depositing a flowable CVD film or depositing silicon, silicon oxide, or related films by CVD, PVD, or similar processes. This step buries particles, fills in scratches or indentations, and repairs other defects that are on the ultra-low expansion substrate 202.

[0042] In the case of flowable CVD films, no further processing may be required to achieve an acceptably smooth, flat surface on the ultra-low expansion substrate 202. For silicon, silicon oxide, or related films, smoothing after deposition may be required. This smoothing can be done by a variety of polishing methods including, but not limited to CMP, chemical polishing, ion beam polishing or annealing. These smoothing techniques can also be applied to the flowable CVD film if further smoothing is required.

[0043] However, the planarization layer 204 has still been found to have a roughness of up to 1.0 nm RMS.

[0044] It has been discovered that the roughness of the planarization layer 204 can be further reduced by the application of an ultra-smooth layer 205 over the planarization layer 204. The ultra-smooth is defined as a local roughness under 0.2nm RMS.

[0045] During the deposition of the ultra-smooth layer 205, there is a reorganization of the film to result in ultra-smoothness. The reorganization is due to a reflow process, a sputtering and redeposition process, or other process where the molecules of the film are reorganized to level out the surface to the ultra-smoothness.

[0046] The ultra-smooth layer 205 can impart improved mechanical and chemical properties to the surface of the planarization layer 204 to aid in the integration of the subsequent processing steps. The ultra-smooth layer 205 include films such as a high density plasma (HDP) oxide, boron doped phosphorous glass, amorphous silicon, or a metal film.

[0047] It has been found that the planarization layer 204 having a local roughness of about 0.5nm RMS can be further smoothed by the application of a HDP oxide layer to about 0.15nm RMS.

[0048] A multi-layer stack 206 of thin films is formed above the planarization layer 204 to form a Bragg reflector. Due to the transmissive nature of the optics and illuminating wavelengths used in EUV, reflective optics are used and the multi-layer stack 206 may be made of alternating layers of reflective materials, such as molybdenum and silicon, which are much thinner than the planarization layer 204 and the ultra-smooth layer 205.

[0049] It has been found that the planarization layer 204 and the ultra-smooth layer 205 can be formed in a different system from the multi-layer stack 206 because the need to maintain a vacuum between the processes is not an essential condition to forming the layers and the stack.

[0050] A capping layer 208 is formed above the multi-layer stack 206. The capping layer 208 can be a material such as ruthenium (Ru) or a non-oxidized compound thereof to help protect the multi-layer stack 206 from any chemical etchants to which the EUV mask blank 200 is exposed during mask processing. Other material such as titanium nitride, boron carbide, silicon nitride, ruthenium oxide, and silicon carbide may also be used in the capping layer 208.

[0051] An absorber layer 210 is placed over the capping layer 208. The absorber layer 210 is of a material having a high absorption coefficient for a particular frequency of EUV light (about 13.5 nm) and may be a material such chromium, tantalum or nitrides thereof.

[0052] An anti-reflective coating (ARC) 212 is deposited on the absorber layer 210. The ARC 212 can be of a material such as tantalum oxynitride or tantalum boron oxide.

[0053] A backside chucking layer 214 is formed on the rear surface of the ultra-low expansion substrate 202 for chucking the substrate in an electrostatic chuck (not shown).

[0054] Referring now to FIG. 3, therein is shown a EUV mask 300. The EUV mask 300 is square and has a pattern 302 on the top surface thereof.

[0055] Referring now to FIG. 4, therein is shown a method 400 of manufacturing an EUV mirror or mask blank. The method 400 includes: forming a planarization layer on a substrate

in a step 404; forming an ultra-smooth layer over the planarization layer in a step 406; and forming a multi-layer stack on the ultra-smooth layer in a step 408.

[0056] Referring now to FIG. 5, therein is shown an optical train 500 for an EUV lithography system. The optical train 500 has a plasma source 502 for creating the EUV light and collecting it in a collector 504. The collector 504 provides the light to a field facet mirror 508 which is part of an illuminator system 506 which further includes a pupil facet mirror 510. The illuminator system 506 provides the EUV light to a reticle 512 (which is the fully processed version of the mask blank 104 of FIG. 1), which reflects the EUV light through projection optics 514 and onto a wafer 516.

[0057] Referring now to FIG. 6, therein is shown an EUV lithography system 600. The EUV lithography system 600 includes an EUV light source area 602, a reticle stage 604 and a wafer stage 606 as adjuncts to the optical train 500.

[0058] Embodiments of the present invention planarize and smooth EUV lens element and mask blank substrates so as to remove all pits, defects, and particles on the substrate surface so that the surface is atomically flat and smooth. The idea is to deposit defect free material on the surface of the EUV lens element or mask blank substrate that can then be processed without inducing any defects to achieve an atomically flat and smooth surface.

[0059] The first step is to fill any pits that are present; this can be done by depositing a flowable CVD film or by depositing silicon, silicon oxide, or related films via CVD, PVD, or a similar process. This step will also bury particles and other defects that are on the EUV mask blank substrate surface. In the case of flowable CVD films, no further CMP or other smoothing processing would be required to achieve an acceptably smooth, flat surface on the EUV mask blank substrate.

[0060] For the silicon, silicon oxide, or related films smoothing after deposition will likely be required. This smoothing can be done by a variety of polishing methods including, but not limited to CMP, chemical polishing, ion beam polishing, or annealing. These techniques can also be applied to the flowable CVD films if further smoothing is required.

[0061] One advantage of this method is that it is substrate independent and so it can be used on a variety of substrates and qualities of substrates. It has the potential to make it possible to use glass substrates that have the required properties for EUV lens element and mask blanks but do not have atomically flat, smooth surfaces after polishing. This independence makes it possible to use different substrate suppliers and minimizes the impact of unexpected changes to the substrate preparation and polishing by the suppliers.

[0062] Embodiments of the invention provide an atomically flat, low defect, smooth surface for an EUV lens element or mask blank. However, embodiments of the invention could also be used to manufacture other types of blanks, such as for mirrors. Over a glass substrate, embodiments of the invention can be used to form an EUV mirror.

[0063] Further, embodiments of the invention can be applied to other atomically flat, low defect, smooth surface structures used in UV, DUV, e-beam, visible, infrared, ion-beam, x-ray, and other types of semiconductor lithography. Embodiments of the invention can also be used in various size structures that can range from wafer-scale to device level and even to larger area displays and solar applications.

[0064] Another approach would be to use flat highly thermally conducting surfaces to grow the multilayer stack on. Historically, glass is used as the substrate for masks, due to the transmissive nature of the optics and illuminating wavelengths used. EUV is absorbed by all materials, thus reflective optics is used. However, reflectivity is not 100% (<70% for current Mo/Si stack), and the absorbed part of the radiation will heat up the substrate. Current mask glass substrate composition is optimized to give zero thermal expansion coefficient, at the operating temperature, to avoid pattern distortion during resist exposure. If substrates more thermally conducting than glass are used, for example metallic or silicon, heat from EUV exposure can be transferred into a cooled chuck thus eliminating the need for a specialized glass. Furthermore, the mask substrate surface can be smoothed using semiconductor compatible processes such as deposition of a layer such as described above (silicon, silicon dioxide) or by CMP or a combination of both.

[0065] The resulting method, process, apparatus, device, product, and/or system is straightforward, cost-effective, uncomplicated, highly versatile, accurate, sensitive, and effective, and can be implemented by adapting known components for ready, efficient, and economical manufacturing, application, and utilization.

[0066] Another important aspect of the present invention is that it valuably supports and services the historical trend of reducing costs, simplifying systems, and increasing performance.

[0067] These and other valuable aspects of the present invention consequently further the state of the technology to at least the next level.

[0068] While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to

embrace all such alternatives, modifications, and variations that fall within the scope of the included claims. All matters hithertofore set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

What is claimed is:

1. An extreme ultraviolet lens element or blank production system comprising:

a first deposition system for depositing a planarization layer over a semiconductor substrate;

a second deposition system for depositing an ultra-smooth layer over the planarization layer, the ultra-smooth layer having reorganized molecules; and

a third deposition system for depositing a multi-layer stack over the ultra-smooth layer.

2. The system as claimed in claim 1 wherein the second deposition system causes a reflow of the molecules of the ultra-smooth layer in a sputtering and redeposition process.

3. The system as claimed in claim 1 wherein the second deposition system causes a reorganization of the molecules of the ultra-smooth layer of a high density plasma oxide.

4. The system as claimed in claim 1 wherein the second deposition system causes a reorganization of the molecules of the ultra-smooth layer of silicon, metal, or dielectric material.

5. The system as claimed in claim 1 wherein the third deposition system deposits the multi-layer stack to form an extreme ultraviolet mask blank.

6. The system as claimed in claim 1 wherein the third deposition system deposits the multi-layer stack to form an extreme ultraviolet mirror.

7. The system as claimed in claim 1 wherein the second deposition system causes the ultra-smooth layer to have a local roughness under 0.2nm RMS.

8. An extreme ultraviolet lithography system comprising:

an extreme ultraviolet light source;

a mirror for directing light from the extreme ultraviolet light source;

a reticle stage for placing an extreme ultraviolet mask blank with a planarization layer and an ultra-smooth layer over the planarization layer; and

a wafer stage for placing a wafer.

9. The system as claimed in claim 8 wherein the ultra-smooth layer has a melting reflow of the molecules of the ultra-smooth layer.

10. The system as claimed in claim 8 wherein the ultra-smooth layer has a reorganization of the molecules of the ultra-smooth layer of a high density plasma oxide.

11. The system as claimed in claim 8 wherein the ultra-smooth layer has a reorganization of the molecules of the ultra-smooth layer of silicon, metal, or dielectric material.

12. The system as claimed in claim 8 wherein a multi-layer stack forms the extreme ultraviolet mask blank.

13. The system as claimed in claim 8 wherein the multi-layer stack forms an extreme ultraviolet mirror.

14. The system as claimed in claim 8 wherein the ultra-smooth layer has a local roughness under 0.2nm RMS.

15. A method of making an extreme ultraviolet blank comprising:

forming a planarization layer over a substrate;

forming an ultra-smooth layer over the planarization layer, the ultra-smooth layer having reorganized molecules; and

forming a multi-layer stack over the ultra-smooth layer.

16. The method as claimed in claim 15 wherein forming the ultra-smooth layer reflows the molecules of the ultra-smooth layer.

17. The method as claimed in claim 15 wherein forming the ultra-smooth layer reorganizes the molecules of the ultra-smooth layer of a high density plasma oxide.

18. The method as claimed in claim 15 wherein forming the ultra-smooth layer reorganizes the molecules of the ultra-smooth layer of silicon, metal, or dielectric material.

19. The method as claimed in claim 15 wherein forming the multi-layer stack includes forming an amorphous metallic layer.

20. The method as claimed in claim 15 wherein forming the multi-layer stack includes forming an extreme ultraviolet mask blank or an extreme ultraviolet mirror.

21. The method as claimed in claim 15 wherein forming the ultra-smooth layer includes forming a surface having a local roughness under 0.2nm RMS.

22. An extreme ultraviolet blank comprising:

a substrate;

a planarization layer over the substrate;

an ultra-smooth layer over the planarization layer, the ultra-smooth layer having reorganized molecules; and

a multi-layer stack over the ultra-smooth layer.

23. The blank as claimed in claim 22 wherein the ultra-smooth layer has a reflow of the molecules of the ultra-smooth layer.

24. The blank as claimed in claim 22 wherein the ultra-smooth layer has a reorganization of the molecules of the ultra-smooth layer of a high density plasma oxide.

25. The blank as claimed in claim 22 wherein the ultra-smooth layer has a reorganization of the molecules of the ultra-smooth layer of silicon, metal, or dielectric material.

26. The blank as claimed in claim 22 wherein the multi-layer stack includes an amorphous metallic layer.

27. The blank as claimed in claim 22 wherein the multi-layer stack forms an extreme ultraviolet mask blank or an extreme ultraviolet mirror.

28. The blank as claimed in claim 22 wherein the ultra-smooth layer has a local roughness under 0.2nm RMS.

29. An extreme ultraviolet blank comprising:

a substrate;

a planarization layer over the substrate;

an ultra-smooth layer over the planarization layer, the ultra-smooth layer having reorganized molecules;

a multi-layer stack having an amorphous metallic layer; and

capping layers over the multi-layer stack.

30. The blank as claimed in claim 29 wherein the ultra-smooth layer has a reflow of the molecules of the ultra-smooth layer.

31. The blank as claimed in claim 29 wherein the ultra-smooth layer has a reorganization of the molecules of the ultra-smooth layer of a high density plasma oxide.

32. The blank as claimed in claim 29 wherein the ultra-smooth layer has a reorganization of the molecules of the ultra-smooth layer of silicon, metal, or dielectric material.

33. The blank as claimed in claim 29 wherein the multi-layer stack forms an extreme ultraviolet mask blank or an extreme ultraviolet mirror.

34. The blank as claimed in claim 29 wherein the ultra-smooth layer has a local roughness under 0.2nm RMS.

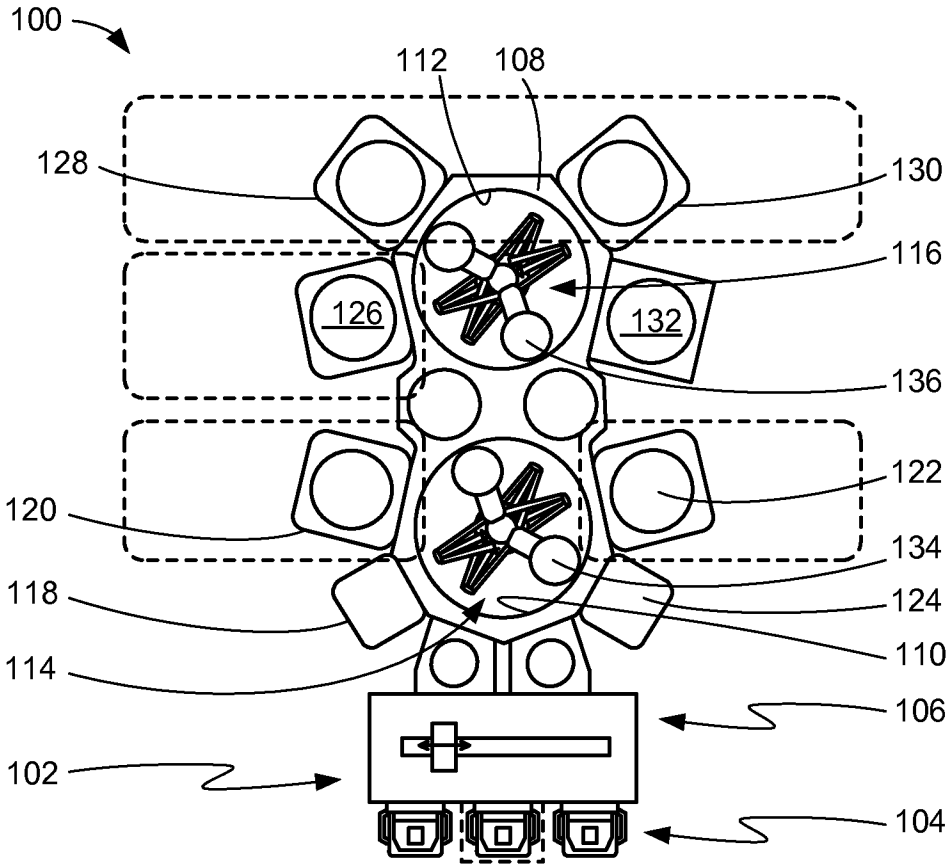
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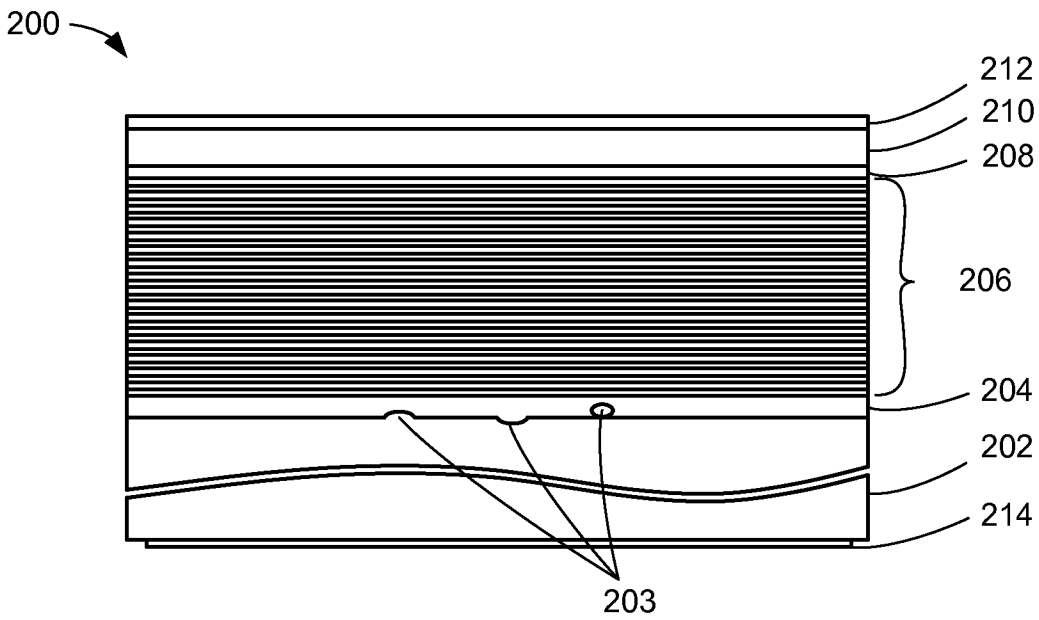
FIG. 1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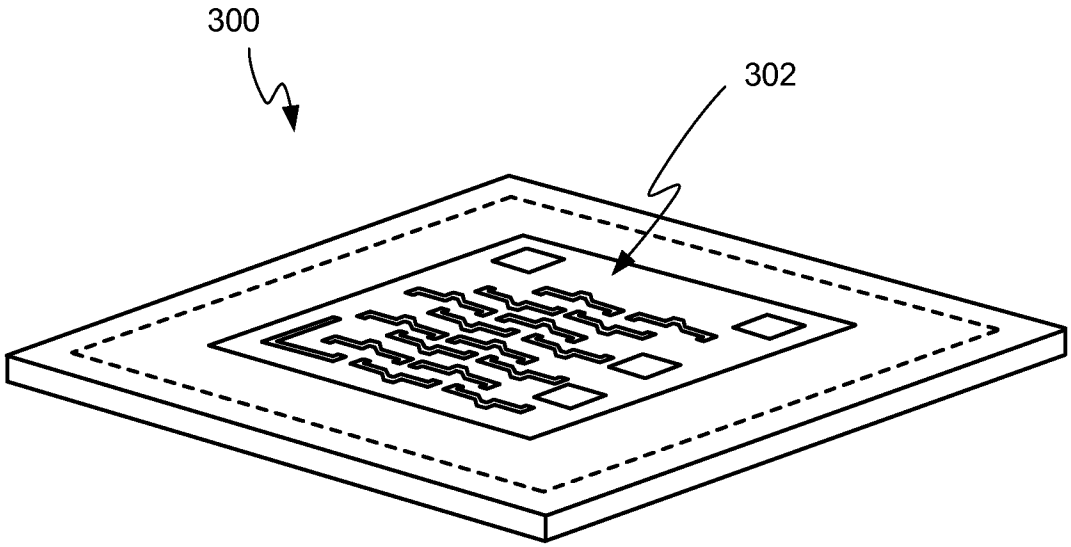
203

FIG. 2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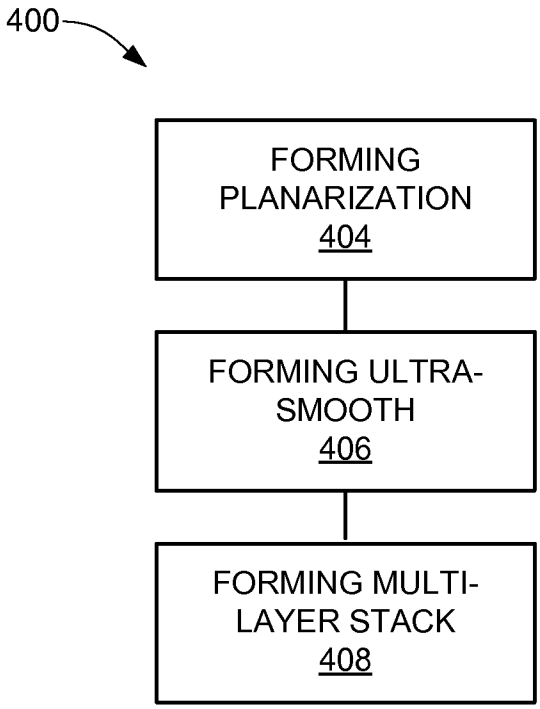
302

FIG. 3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FORMING ULTRA-SMOOTH 406
FORMING MULTI-LAYER STACK 408

FIG. 4

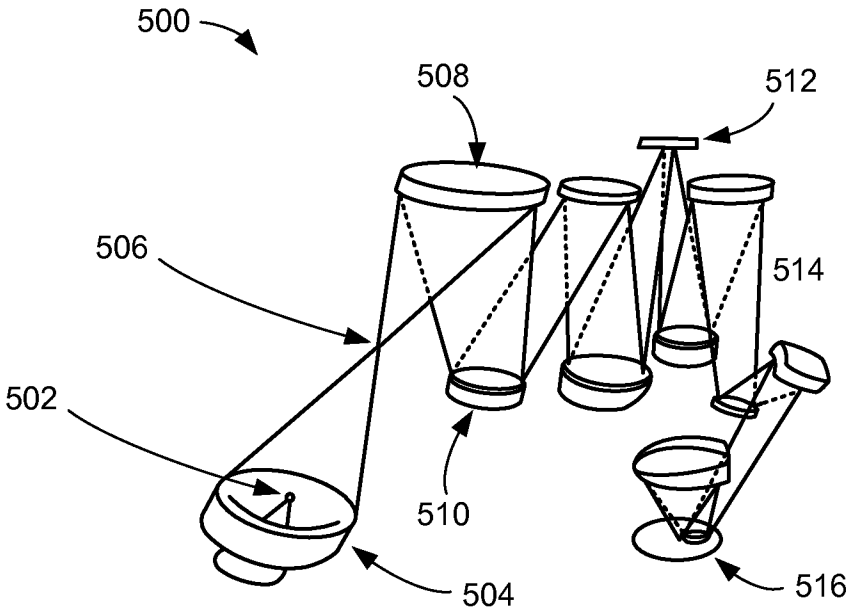

FIG. 5

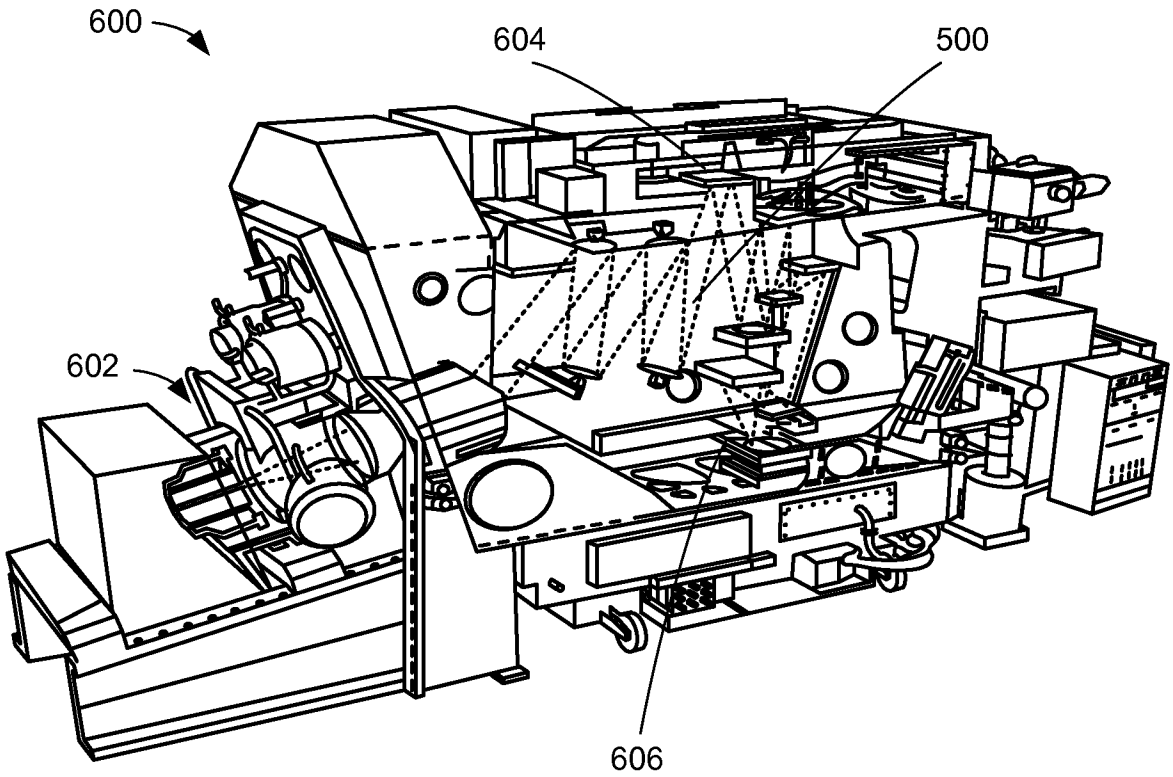

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/026844

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/027(2006.01)i, H01L 21/20(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/027; G21K 5/00; B32B 9/00; F21V 9/04; G03F 7/09; G03C 1/005; H01L 21/4763; G02B 1/10; G03C 5/00; B29C 35/08; H01L 21/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: EUV, blank, deposit, second, planar, smooth, layer, substrate and multi-layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004-0151988 A1 (PETER J. SILVERMAN) 05 August 2004 See abstract, paragraphs [0016]-[0025] and figures 1A-5B.	1-34
A	US 2006-0245057 A1 (MAARTEN MARINUS JOHANNES W. VAN HERPEN et al.) 02 November 2006 See abstract, paragraphs [0042]-[0060] and figures 2-5.	1-34
A	US 2007-0020903 A1 (TAKAKO TAKEHARA et al.) 25 January 2007 See abstract, paragraphs [0068]-[0090] and figures 4A-4B.	1-34
A	US 2005-0084773 A1 (ANTHONY C. KRAUTH) 21 April 2005 See abstract, paragraphs [0020]-[0027] and figure 1.	1-34
A	US 2004-0029041 A1 (WU-SHENG SHIH et al.) 12 February 2004 See abstract, paragraphs [0034]-[0053] and figures 3(a)-4(d).	1-34

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 September 2014 (02.09.2014)	**03 September 2014 (03.09.2014)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2014/026844

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Information on patent family members

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PCT/US2014/026844

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