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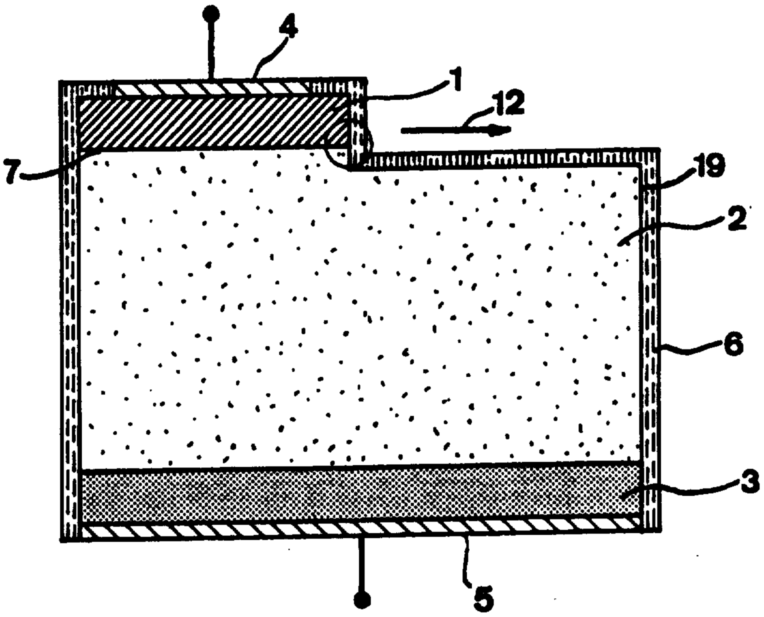
**(54) Title:** SEMICONDUCTOR DEVICE HAVING A PASSIVATION LAYER

**(57) Abstract**

A semiconductor device comprises at least one semiconductor layer (1-3) of SiC and a layer (6) applied on at least a portion of an edge surface (19) of said SiC-layer so as to passivate this edge surface portion. At least the portion of said passivation layer closest to said edge surface portion of the SiC-layer is made of a first crystalline material, and the passivation layer comprises a portion made of a second material having AlN as only component or as a major component of a crystalline alloy constituting said second material.



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# Semiconductor device having a passivation layer

## TECHNICAL FIELD OF THE INVENTION AND PRIOR ART

The present invention relates to a semiconductor device comprising at least one semiconductor layer of SiC and a layer applied on at least a portion of an edge surface of said SiC-layer so as to passivate this edge surface portion.

All types of semiconductor devices are comprised, such as for example different types of diodes, transistors and thyristors.

Such devices are in particular used in applications in which it is possible to benefit from the superior properties of SiC in comparison with especially Si, namely the capability of SiC to function well under extreme conditions. SiC has a high thermal stability due to a large band gap between the valence band and the conduction band, such that devices fabricated from said material are able to operate at high temperatures, namely up to 1000 K. Furthermore, it has a high thermal conductivity, so that SiC devices may be arranged at a high density. SiC also has a more than 5 times higher breakdown field than Si, so that it is well suited as a material in high power devices operating under conditions where high voltages may occur in the blocking state of a device.

The passivation of the edge of a device is made for different reasons and using different means. One reason for applying a passivation layer to the edge of the device is to protect a semiconductor layer or layers of the device, especially to prevent moisture and ion migration which may damage the semiconductor layer. The passivation layer may also protect the semiconductor layer against mechanical influences and dirt. Another task of a passivation layer is to stabilise the surface region of the semiconductor layer, which then has also a stabilising effect on the properties in the bulk of the semiconductor layer. In particular, the passivating layer has to shield the semiconductor layer of the device electrically with respect to the ambient, so that electrical fields from the device will not detrimentally influence surrounding devices or equipment and primarily there will be no generation of jumping sparks at the interface between the semiconductor layer and the air and no breakdown in a blocking state of the device, when the passivation layer is applied in a region of the device where the electric field is high in a blocking state of the device.

The present invention is in particular occupied with the problem to obtain a passivation adapted to the use of SiC as semiconducting material, so that especially the property of SiC to withstand high temperatures and high breakdown fields may be utilised.

$SiO_2$ has until now often been used as passivation layer, since it may easily be created by thermal oxidation, but it is not adapted for use in SiC-devices. $SiO_2$ may not withstand the high breakdown voltages which are required to be possible in the application of SiC-power devices, such a passivation layer would be partially destroyed by said extreme high voltage, and a lack of appropriate passivation of such devices would thereto not only result in a decrease of the breakdown voltage, but in an irreversible, destructive mode of electric breakdown in the device as well. Furthermore, $SiO_2$ may not be grown thick enough to hold extreme high voltages and it has also a lower dielectric constant than SiC. $SiO_2$ may also not be stable at higher temperatures, the interface between the SiC-semiconductor layer and the $SiO_2$ layer is known to be unstable at temperatures above 300°C. These drawbacks are also present in other conventional dielectrics used for passivation purposes, such as SiO and $Si_3N_4$.

It is also known that the capability to withstand high voltages in the blocking state of such a device can be improved by different geometric tricks preventing a concentration of the electric field at the edge of the device, such as bevelled edge surfaces having different inclinations. It is also known that the application of a semi-insulating material as a passivation layer in the region of a device where the electric field is high in a blocking state of the device, allows a weak leakage current to flow in the blocking state of the device, thereby smoothing out the electric field in said region.

Furthermore, all the conventional passivation layers used as passivation layers for a SiC-device will result in a comparatively high trapping density at the interface between the SiC and the passivation layer due to disorders at the interface. This will result in an unstable surface region of the device and a low stability and reliability of the function of the device in said region, leading to electric field peaks or spots having a lower breakdown field than other parts of the passivation layer. Such instabilities make it necessary to set the limit for the highest allowed voltage in the blocking state of the device considerably lower than would be possible if the interface region be just as or nearly as stable and uniformly built up as the bulk region of the device.

## SUMMARY OF THE INVENTION

The object of the present invention is to provide a semiconductor device as defined in the introduction, which has a passivation making it possible to withstand breakdown fields close to the physical limit of SiC and be thermally stable in the temperature range in which SiC-devices may operate.

This object is in accordance with the invention, obtained by making at least the portion of said passivation layer closest to said edge surface portion of the SiC-layer of a first crystalline material, and by that the passivation layer comprises a portion made of a second material having crystalline AlN as only component or as a major component of a crystalline alloy constituting said second material.

By using crystalline AlN as only component or as a major component of a crystalline alloy constituting said second material as a portion of the passivation layer, the passivation layer may withstand high breakdown fields and have a high thermal stability. AlN has nearly the same dielectric constant as SiC and is able to withstand electric fields of a greater magnitude than SiC. Furthermore, AlN is thermally stable within the possible temperature range of operation of SiC-devices and importantly has substantially the same coefficient of thermal expansion as SiC. The fact that at least the portion of the passivation layer closest to the edge surface portion of the SiC-layer is made of a crystalline material, makes a very important contribution to the capability of such a device to withstand high breakdown fields. Due to the use of a crystalline material for the passivation layer next to the SiC semiconductor layer the disorder and by that the trapping density at the interface there between is dramatically reduced with respect to the use of known passivation materials. Accordingly, the interface between the passivation layer and the semiconductor layer will get a nearly "bulk-like"-character, so that there will be no dramatic fluctuation of the electric field at the interface or in the passivation layer portion closest to said interface and this passivation layer portion will have a uniform ability to withstand electric fields, so that higher electric fields may be allowed in the blocking state of the device without any risk of the occurrence of an electrical breakdown due to an inhomogeneity in the passivation.

According to a preferred embodiment of the invention said first material of the passivation layer is substantially lattice-matched to SiC and has substantially the same coefficient of thermal expansion as SiC, which will make it possible to obtain an extreme low interface trap density with the advantages mentioned above as well as a possibility to grow thick and mechanically stable layers of said first material next to the SiC-layer.

According to another preferred embodiment of the invention said first crystalline material is said second material, i.e. a material having crystalline AlN as only component or as a major component of a crystalline alloy constituting said material is arranged closest to said edge surface portion of the SiC-layer. AlN has a 2H structure and will match under given orientations with all types of SiC polytypes, both cubic and hexagonal ones, and it has a good lattice-match with a misfit of only 0,7%.

According to another preferred embodiment of the invention said second layer is $Al_xB_{(1-x)}N$. The incorporation of B in AlN will make it possible to obtain a perfect lattice match of the second material to SiC, which will be very advantageous when said first crystalline material is said second material. In such a case a theoretical perfect lattice match may be obtained at a B-content of 4%. A content of B will also increase the bandgap and the breakdown voltage and make the material more resistent to oxidation. Thanks to the better lattice match thicker passivation layers may be grown. The boron-content could be graded in the passivation layers, so that it may be around 4% at the interface to the SiC-layer for obtaining a perfect lattice match and then gradually increase in the direction away from the interface so as to increase the resistance to oxidation thereof.

According to a further preferred embodiment of the invention said passivation layer is applied at least in a region of the device where the electric field is high in a blocking state of the device and it comprises at least two superimposed sub-layers of which one is made of said second material and another is made of a semi-insulating material allowing a weak leakage current to flow therein, in said blocking state of the device for smoothing out the electric field in said region. These characteristics will make it possible to withstand high electric fields owing to the high breakdown field and the stability of the second material defined above and the capability of the layer of the semi-insulating material to smooth out the electric field otherwise concentrated in said region.

According to a still further preferred embodiment of the invention the sub-layer applied on the SiC-layer, i.e. said first crystalline material, is made of a semi-insulating material, and the sub-layer made of said second material is arranged on the top of that semi-insulating material. This embodiment of the invention as well as a further preferred embodiment thereof, in which the sub-layer made of said second material is applied on the SiC-layer and the layer made of the semi-insulating material is arranged on the top of said second material layer, results in high breakdown fields.

According to another preferred embodiment of the invention in which the first crystalline material is said second material and the passivation layer is applied at least in a region of the device where the electric field is high in a blocking state of the device, said second material is lightly N-doped to provide electrons as free charge carriers at the interface between the SiC-layer and the layer of the second material so as to make a weak current flow at said interface in said blocking state of the device for smoothing out the electric field in said region. By using AlN as at least major component of the material at the interface between the SiC-layer and the passivation layer and doping it with donors, the band off-set of the conduction bands between AlN and SiC may be utilised to obtain electrons as free charge carriers at said interface with the same electric field smoothing out property as provided by a semi-insulating layer there. AlN has a band gap of about 6,2 eV, which is considerable larger than all polytypes of SiC, which have band gaps between 2,3 and 3,3 eV. AlN has energy band off-sets for both the conduction band and the valence band for all the SiC polytypes, which in the case of doping AlN with donors will result in a "falling down" of electrons at the interface from the AlN to the SiC conduction band at said interface. These free electrons may then be influenced by a voltage to move along said interface so as to smooth out the electric field in the region in question.

According to another embodiment of the invention, in which the AlN layer is lightly doped with acceptors instead, positive holes will in a corresponding way be provided at said interface as free charge carriers for smoothing out the electrical field in the region in question. In this case the band-off-set between the valence bands of AlN and SiC is utilised.

Further advantages and preferred features of the invention will appear from the following description and the other dependent claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

With reference to the appended drawings, below follows a specific description of preferred embodiments of the invention cited as examples.

In the drawings:

Fig 1 is a schematic view of a semiconductor diode of SiC being passivated in accordance with the invention,

Fig 2 is an enlarged view of a portion of the device according to Fig 1 in which the electric field is high in a blocking state of the device,

Fig 3 is a further enlarged view of an interface part of the portion shown in Fig 2 with an illustration of the extension of the valence and conduction bands in the SiC-layer and in the passivation sub-layer closest to the SiC-layer when this is made of said second material, and what happens when said second material is lightly doped with donors, and

Fig 4 and 5 are views similar to Fig 3 showing the arrangement of passivation sub-layers in devices according to the second and third embodiment of the invention, respectively.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

Fig 1 illustrates by a way of a non-limitative example of a device to which the invention may be applied, a semiconductor diode with three semiconductor layers of SiC, namely a first highly doped layer 1 of P-type, a second lightly doped layer 2 of N-type and a third highly doped layer 3 of N-type. The three layers are superimposed in the order mentioned. The device does also have an ohmic metal contact 4 arranged on the top of said first layer and forming the anode of the diode, and a second ohmic metal contact 5 arranged in contact with said third semiconductor layer and forming the cathode of the diode. The device is encapsulated and the edges 19 of the device are passivated by a passivation layer 6 covering the entire device with exception of the two contacts 4 and 5. The device may be produced by known growing and etching techniques. In a conventional way, the device will be conducting when a positive voltage is applied to the metal contact 4 in contact with the layer of P-type and blocking when a negative voltage is applied to that contact with respect to the potential of the second contact 5. In the blocking state of the device the electric field will be concentrated to the PN-junction 7 between said first and second layers, and the requirements of the passivation will be highest in that region so as to make it possible for the device to withstand as high voltages as possible without any breakdown.

Fig 2 shows how the passivation layer may comprise two superimposed sub-layers 8 and 9 of which that closest to the semiconductor edge is made of a monocrystalline material, in the present embodiment of AlN. AlN has already been grown with a high quality on SiC. The AlN-layer may also have some minor concentrations of one or several other Group 3B-nitrides or SiC. The crystalline layer 8 with AlN as major component may be grown on the SiC layers 1, 2, 3 in such a way that the interface 10 between the sub-layer 8 and the semiconductor layers will be substantially without any disorder and by that have a very low trap density. AlN has a very high breakdown field and may withstand very high fields without the occurrence of any damages thereon, so that in this case first of all a comparatively thin layer of AlN is applied on the semiconductor edge surfaces so as to take up a considerable part of the electric field, and another sub-layer of a material which may not withstand such high electric fields without any damage thereof may be arranged on top of the AlN-layer 8 to take up the residual of the electric field. This layer 9 may be done much thicker than the AlN-layer and will be of any suitable insulating material, such as for example an organic material, such as a polymide or any amorphous insulating layer. Thus, the layer 9 will be there for taking up a part of the electric field and prevent breakdowns from occurring, but it is primarily there for reducing the electric field at the external surface thereof to such an extent that surrounding equipment or devices will not be influenced thereby.

Fig 3 illustrates what is happening when the sub-layer 8 in Fig 2 is lightly doped with donors. Due to the off-set of the conduction band levels $E_C$ between aluminium nitride and silicon carbide the donated electrons 11 of the sub-layer 8 will energetically fall down to the conduction band of the SiC next to said interface 10. Accordingly, free charge carriers in the form of electrons are in this way provided at said interface. This means, that the interface will act as a semi-insulating layer in that a weak leakage current will flow along said interface when a voltage is applied in the blocking direction of the device. This means that the electrical field will be smoothed out by extending the surface depletion layer in the direction of the arrow 12 in Fig 1. Accordingly, this means that the device may withstand higher blocking voltages before breakdown occurs. However, it is important to dope the layer 8 to a very low extent, because leakage currents are principally not desired and should therefore be kept within low limits.

The corresponding phenomena may be achieved by doping the AlN-layer 8 with acceptors and using the band off-set between AlN and SiC with respect to the energy levels $E_V$ of the valence bands and obtaining positive holes as free charge carriers at the interface 10.

Fig 4 shows an embodiment according to the invention with a passivation layer comprising three superimposed sub-layers 13, 14 and 15. The sub-layer 13 applied on the semiconductor layer 2 is made of a crystalline, semi-insulating material, i.e. of a material having a high resistivity, but which allow a weak leakage current to flow therein in the blocking state of the device so as to smooth out the electrical field in the same way as described above with reference to Fig 3. Thanks to the crystalline property of the material of the sub-layer 13 the trapping density at the interface 10 will be low and by that the stability at the interface high. The sub-layer 14 arranged on top of the semi-insulating layer 13 is made of said second material, i.e. crystalline AlN or a crystalline alloy having AlN as a major component. This sub-layer is intended to take up a large part of the electrical field. Finally, the sub-layer 15 corresponds to the sub-layer 9 in the embodiment according to Fig 2.

Fig 5 shows a further embodiment of the invention in which the passivation layer comprises three superimposed sub-layers 16, 17, 18 of which the sub-layer 16 applied on the semiconductor layer 2 is made of said second material and has the same purpose as the layer 8 of Fig 2 but is undoped. The sub-layer 17 arranged thereon is made of a semi-insulating material, which does not necessarily have to be crystalline, and this layer allows a weak leakage current to flow therein in the blocking state of the device so as to smooth out the electric field in the region in which it is high. The external sub-layer 18 corresponds to the sub-layer 15 of Fig 4 and the sub-layer 9 of Fig 2.

The invention is of course not in any way restricted to the preferred embodiments described above, but many possibilities to modifications thereof will be apparent to a man with ordinary skill in the art.

As mentioned in the introduction the invention is applicable to all types of semiconductor devices which require passivation, also unipolar semiconductor devices, where the electric field is high close to the source and high breakdown fields must be sustained there.

The proportions of the different layers shown in the figures do not have anything to do with reality, but are only chosen for illustration reasons and can be totally different. Although the passivation layer is shown to be much thinner than the SiC-layer, these layers may have approximately the same thickness or the SiC-layer may even be thinner than the passivation layer. It would also be possible to grow the second material directly onto the SiC semiconductor layer that thick that no other layer has to be applied thereon for taking up any part of the electric field, but in practice a rubber coating or the like will nevertheless probably always be applied outside the layer of the second material. The choice of the thicknesses of the different layers will in practice depend on the conditions under which the device in question is intended to operate and the procedures of production of said layers (degree of complication, production time etc.).

The second material may consist of an alloy having AlN as major component and one or a combination of Group 3B-nitrides and SiC as the other component or components, since these different components have a complete miscibility. However, AlN has to be the major component, since the ability thereof to withstand high electric fields is superior and it has a better lattice-match to SiC, which is of importance when the second material is arranged next to the SiC-layer of the device.

It has turned out to be very advantageous to use $Al_xB_{(1-x)}N$ as said second material, since the content of B in AlN will increase the bandgap and the breakdown voltage of the material. Furthermore, the B-content will make the material more resistent to oxidation. Very important is also that the lattice match can be improved, and a theoretical perfect lattice match may be achieved at 4% incoroporation of B. Thanks of the better lattice match it will be possible to grow thicker layers. The boron content may advantageously be about 4% at the interface to the SiC-layer for obtaining a perfect lattice match and then increase in the direction away therefrom for increasing the oxidation resistance of the passivation layer.

It will of course be possible to cover different surfaces of the device by different passivation layers and adapt the nature of the passivation layer to the conditions prevailing in the different regions of the device. It is also within the scope of the invention to leave areas of the device without any passivation layer according to the invention.

All definitions concerning the materials of the different device layers do of course also include inevitable impurities as well as intentional doping when SiC is concerned.

The definition layer is to be interpreted broadly and comprise all types of volume extensions and shapes.

The word crystalline means a good periodicity of the lattice in the three dimensions over greater regions, i.e. typically polycrystalline structures are excluded.

## Claims

1. A semiconductor device comprising at least one semiconductor layer (1-3) of SiC and a layer (6) applied on at least a portion of an edge surface (19) of said SiC-layer so as to passivate this edge surface portion,
**characterized** in that at least the portion (8, 13, 16) of said passivation layer closest to said edge surface portion of the SiC-layer is made of a first crystalline material, and that the passivation layer comprises a portion (8, 14, 16) made of a second material having crystalline AlN as only component or as a major component of a crystalline alloy constituting said second material.

2. A device according to claim 1,
**characterized** in that said first material is substantially lattice-matched to SiC and has substantially the same coefficient of thermal expansion as SiC.

3. A device according to claim 1 or 2,
**characterized** in that said second material is constituted by said alloy and the other component or components than AlN thereof is one or a combination of Group 3B-nitrides and SiC.

4. A device according to claim 1 or 2,
**characterized** in that said second material has crystalline AlN as only component.

5. A device according to any of claims 1-4,
**characterized** in that said first crystalline material is said second material.

6. A device according to claims 3 and 5,
**characterized** in that said second material is $Al_xB_{(1-x)}N$.

7. A device according to claim 6,
**characterized** in that x is 0,92-0,98, preferably around 0,96.

8. A device according to claim 7,
characterized in that the B-content in said second material is around 4% at the interface to the SiC-layer and increases gradually in the direction away therefrom.

9. A device according to any of claims 1-8, in which said passivation layer (6) is applied at least in a region of the device where the electric field is high in a blocking state of the device,
characterized in that said passivation layer comprises at least two superimposed sub-layers of which one (14, 16) is made of said second material and another (13, 17) is made of a semi-insulating material allowing a weak leakage current to flow therein in said blocking state of the device for smoothing out the electric field in said region.

10. A device according to claim 9,
characterized in that the sub-layer applied on the SiC-layer (1-3) is the one (13) made of a semi-insulating material, and that the sub-layer (14) made of said second material is arranged on the top of that semi-insulating material layer.

11. A device according to claim 9,
characterized in that the sub-layer (16) made of said second material is applied on the SiC-layer (1-3), and that the layer (17) made of the semi-insulating material is arranged on the top of said second material layer.

12. A device according to claim 5, in which said passivation layer (6) is applied at least in a region of the device where the electric field is high in a blocking state of the device,
characterized in that said second material is lightly N-doped to provide electrons as free charge carriers at the interface between the SiC-layer (1-3) and the layer (8) of the second material so as to make a weak current flow at said interface in said blocking state of the device for smoothing out the electric field in said region.

13. A device according to claim 5, in which said passivation layer is applied at least in a region of the device where the electric field is high in a blocking state of the device,
characterized in that said second material is lightly P-doped to provide positive holes as free charge carriers at the interface between the SiC-layer (1-3) and the layer of the second material so as to make a weak current flow at said interface in said blocking state of the device for smoothing out the electric field in said region.

14. A device according to any of the claims 1-13, which comprises at least two adjacent semiconductor layers (1, 2) of SiC of which a first is N-doped and a second is P-doped,
characterized in that said passivation layer portion of said first material is applied on the edge surface (19) of the SiC-layer of the PN-junction between the two SiC-layers for passivation of the edge surfaces on both sides thereof.

15. A device according to any of claims 1-14,
characterized in that said passivation layer (16) comprises at least two superimposed sub-layers of which one (8, 14, 16) is made of said second material and another, external sub-layer (9, 15, 18) is made of another material being insulating.

16. A device according to claim 15,
characterized in that said external sub-layer (9, 15, 18) is made essentially thicker than said layer (8, 14, 16) of said second material.

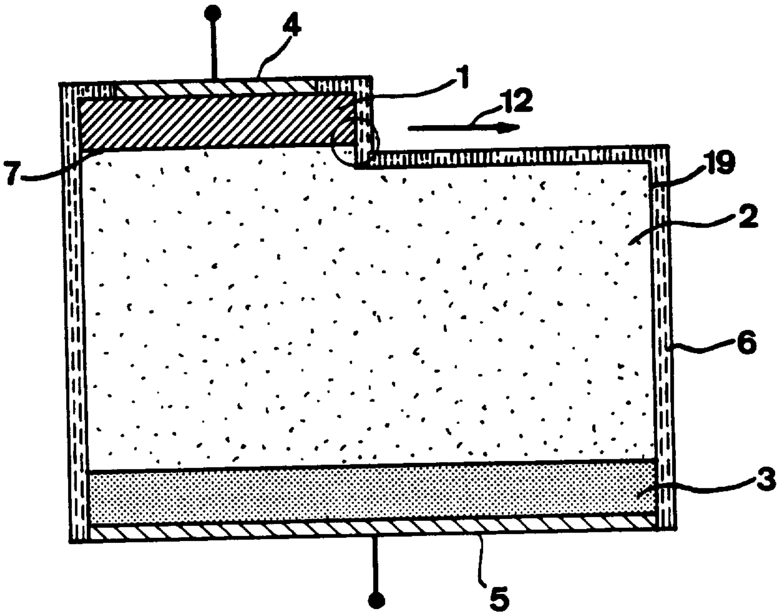


Fig 1

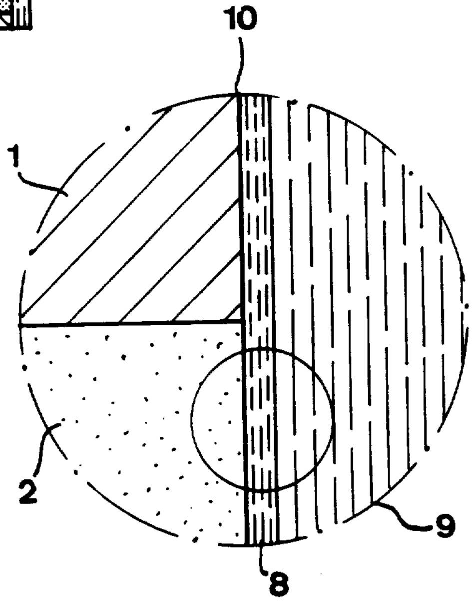
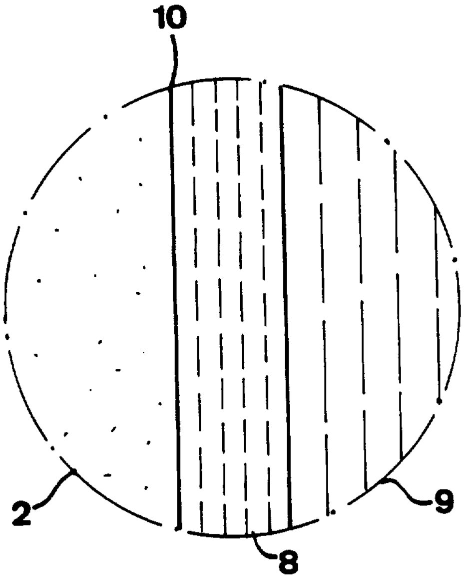


Fig 2



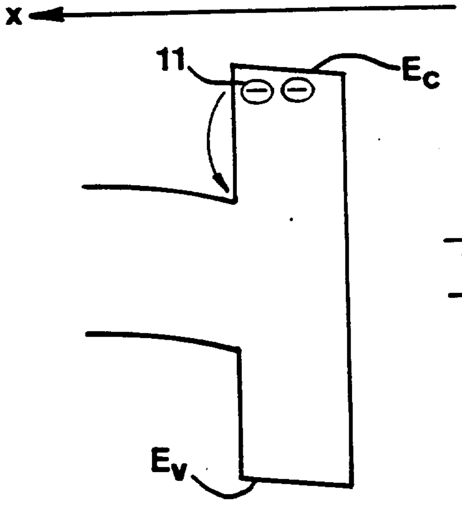


Fig 3

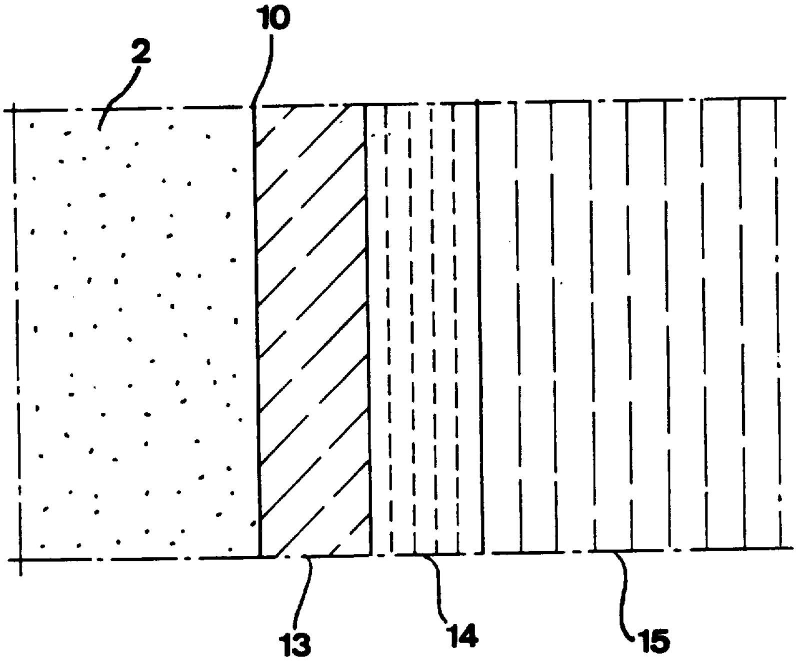


Fig 4

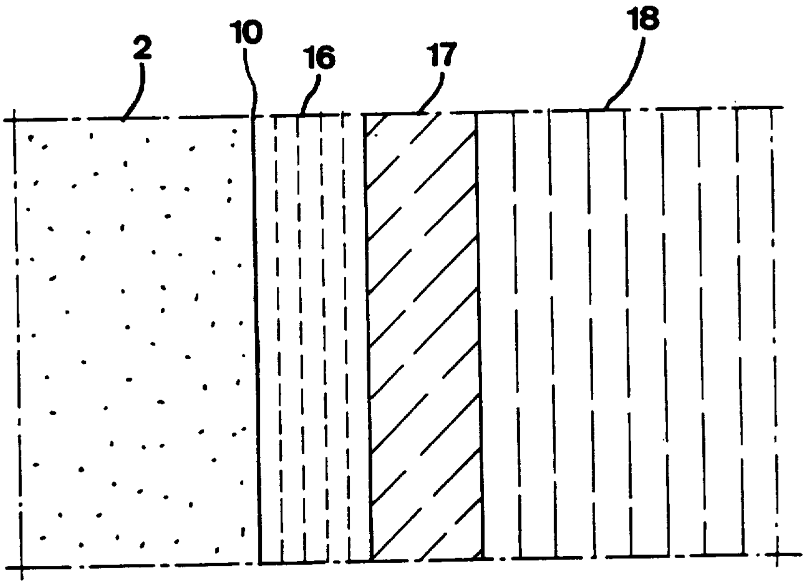


Fig 5

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 95/01596

## A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 23/29, H01L 29/12
According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DIALOG: 2, 350, 351, 434

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
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☒ Further documents are listed in the continuation of Box C.  ☒ See patent family annex.

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| Date of the actual completion of the international search<br>11 June 1996 | Date of mailing of the international search report<br>12-06-96 |
| Name and mailing address of the ISA/<br>Swedish Patent Office<br>Box 5055, S-102 42 STOCKHOLM<br>Facsimile No. +46 8 666 02 86 | Authorized officer<br>Pär Moritz<br>Telephone No. +46 8 782 25 00 |

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