United States Patent [19]

Parks

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[45] **Jan. 9, 1973**

[54] **METHOD OF MAKING A BATCH FABRICATED MAGNETIC MEMORY**

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[73] Assignee: **The Bunker-Ramo Corporation,** Oak Brook, Ill.

[22] Filed: **Aug. 23, 1971**

[21] Appl. No.: **176,411**

Related U.S. Application Data

[62] Division of Ser. No. 864,616, Oct. 8, 1969, Pat. No. 3,623,037.

[52] **U.S. Cl.**.....**29/604,** 29/625

[51] **Int. Cl.**.....**H01f 7/06**

[58] **Field of Search**...29/604, 625; 340/174 PW, 174 TF, 340/174 S, 174 VA

[56] **References Cited**

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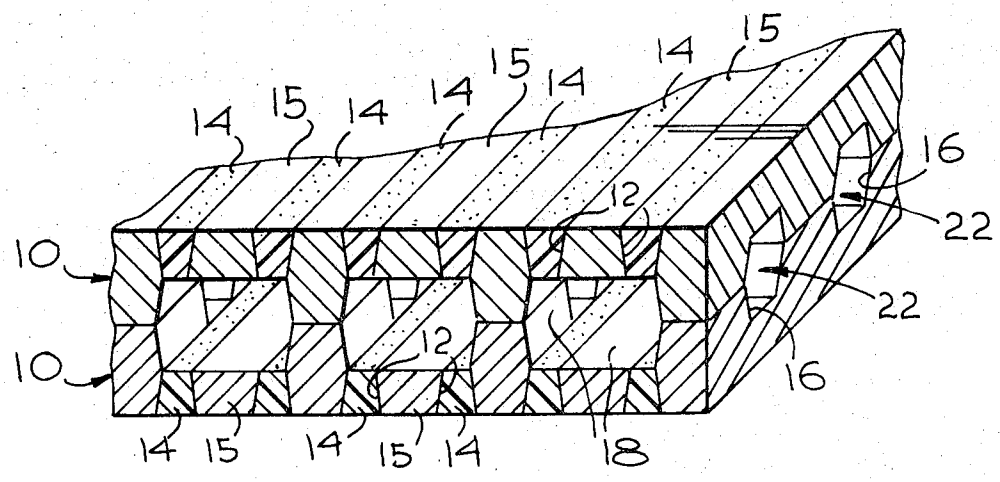
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Primary Examiner—Charles W. Lanham
Assistant Examiner—Carl E. Hall
Attorney—Frederick M. Arbuckle

[57] **ABSTRACT**

A magnetic wire memory construction comprising a plurality of stacked memory planes, each memory plane being formed from two like-formed self-supporting and rigid metal sheets in opposed relation. The sheets have channels formed therein using precision batch fabricated metal sculpturing techniques, with certain of the channels being filled with insulative material. The dimensions and locations of the channels are chosen so that precisely located memory wire receiving tunnels and corresponding insulated drive line strips perpendicular thereto are formed when the sheets are placed together in opposed relation. Memory wire elements are inserted into the tunnels which protect and shield the elements and maintain them accurately positioned with respect to one another and to the drive line strips so as to permit achieving a memory of increased density and speed of operation.

9 Claims, 11 Drawing Figures



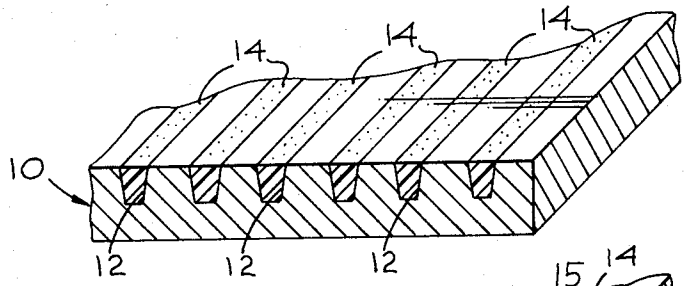


Fig. 1

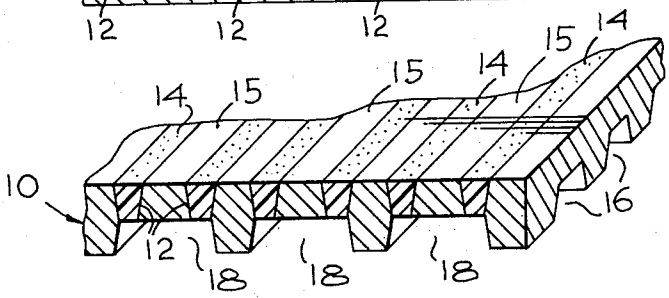


Fig. 2

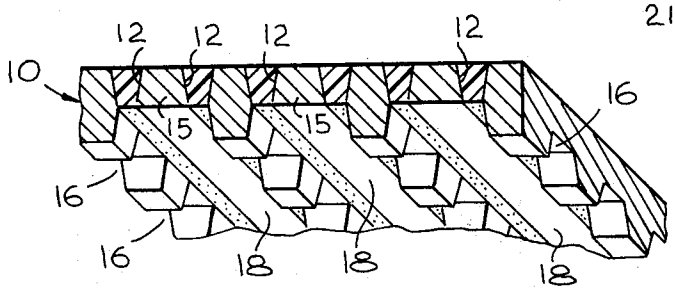


Fig. 3

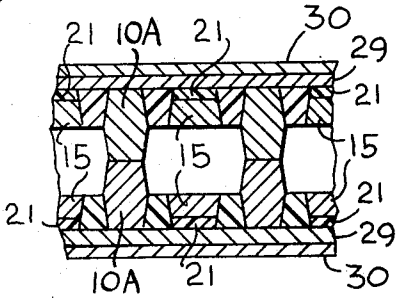


Fig. 5A

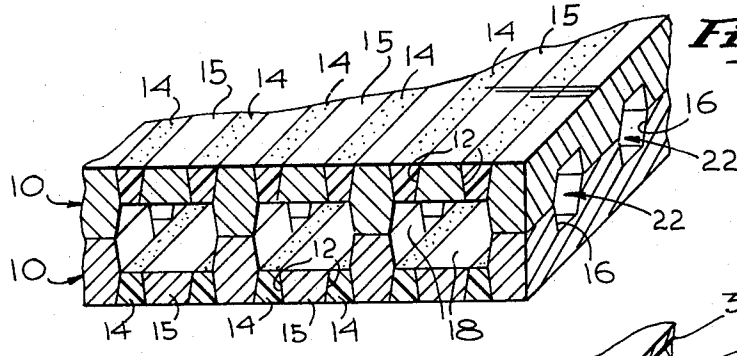


Fig. 4

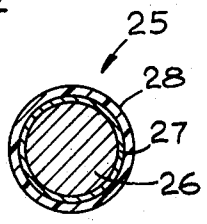


Fig. 6

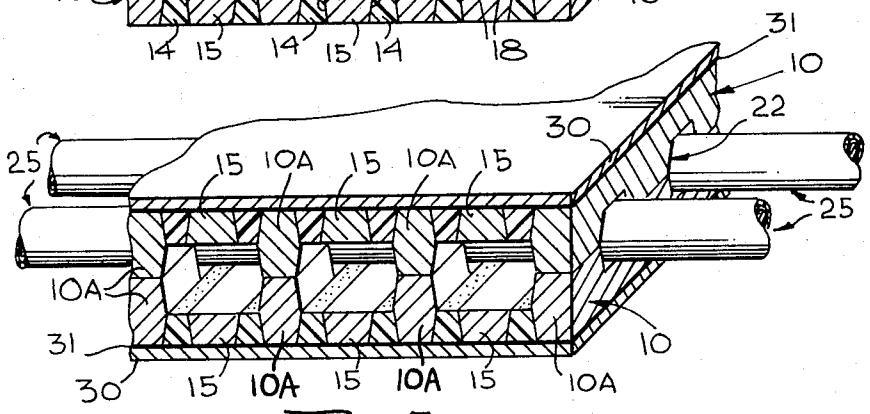


Fig. 5

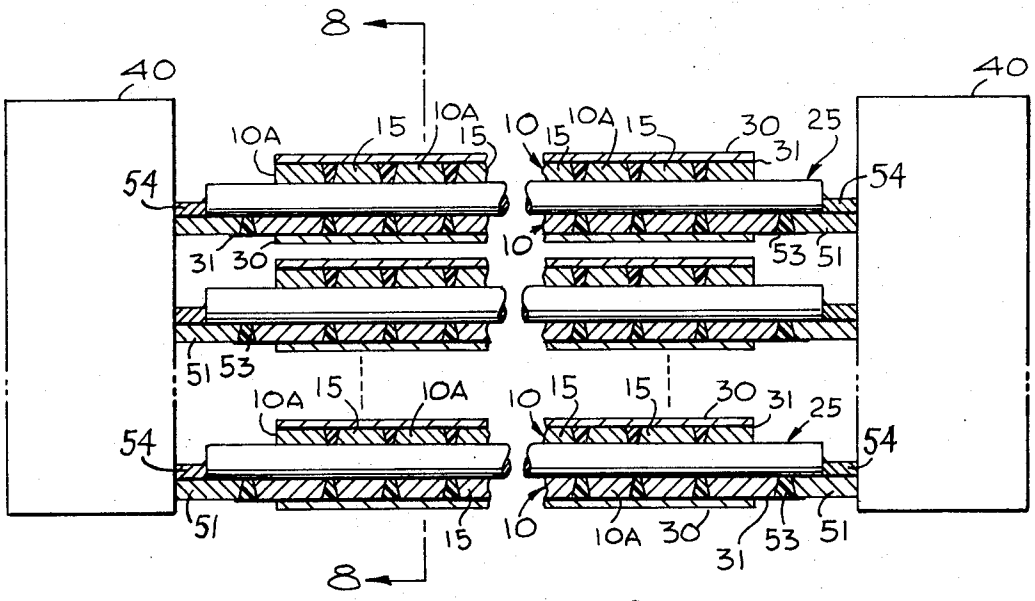

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Fig. 7

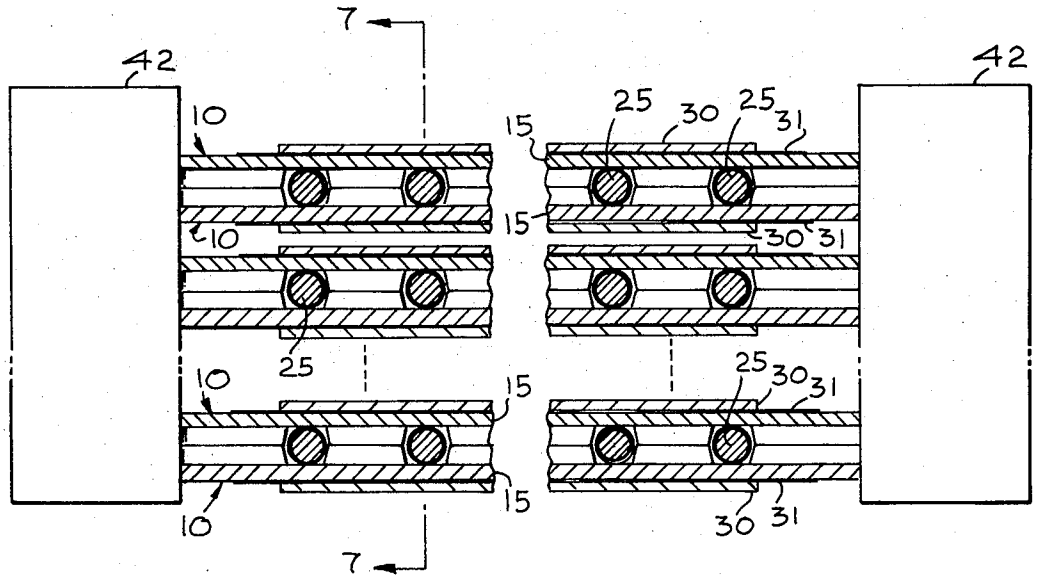

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Fig. 8

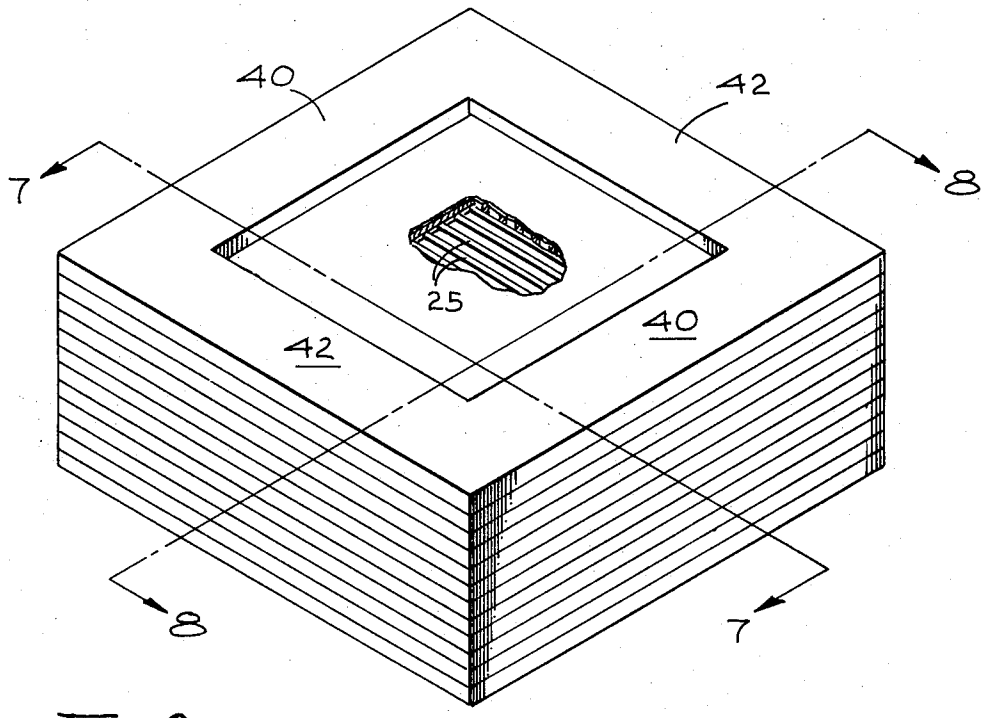


Fig. 9

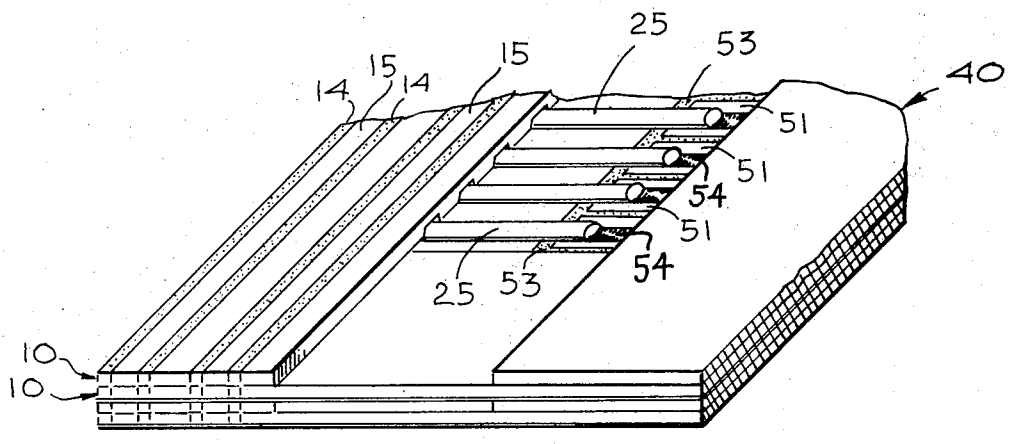


Fig. 10

METHOD OF MAKING A BATCH FABRICATED MAGNETIC MEMORY

This is a division of application Ser. No. 864,616, filed Oct. 8, 1969 now U.S. Pat. No. 3,623,037, issued Nov. 23, 1971.

BACKGROUND OF THE INVENTION

The present invention relates generally to a magnetic memory and to a method of construction thereof. More particularly, the invention relates to a magnetic memory of the type employing wire-like memory elements.

It is well recognized that the construction of a magnetic wire memory presents significant problems which can result in increased fabrication costs and/or degraded memory performance. Such problems involve, for example, memory wire insertion, drive and sense line interconnection requirements, cross-talk, excessive heating, lack of uniformity, noise cancellation, etc.

SUMMARY OF THE PRESENT INVENTION

The present invention is directed to a magnetic wire memory construction and fabrication method therefor which makes possible the provision of an improved magnetic wire memory which significantly reduces the problems heretofore associated with such memories.

Briefly, a basic feature of the present invention resides in the use of precision batch fabricated metal sculpturing techniques on metal sheets for forming memory planes having tunnels and insulated conductive drive line strips at predetermined locations whereby, after stacking of the planes, a modular magnetic wire memory structure is obtained in which the magnetic wire elements are uniformly and symmetrically retained with respect to each other and to the memory drive lines with an accuracy and shielding significantly greater than would be possible using other known types of memory constructions. As a result, noise cancellation can be achieved to a much higher degree than was heretofore possible so as to permit achieving a significantly greater packing density as well as an increased speed of operation. Also, the use of sculptured metal sheets provides the memory with a much greater heat dissipation capability than would otherwise be possible.

The specific nature of the invention as well as other features, objects, advantages and uses thereof will become apparent from the following description of an exemplary embodiment and method in accordance with the invention taken in conjunction with the accompanying drawings in which:

FIGS. 1–4 are fragmentary cross-sectional and pictorial views illustrating stages in the fabrication of a memory plane in accordance with the invention;

FIG. 5 is a fragmentary cross-sectional and pictorial view of a memory plane in accordance with the invention;

FIG. 5A is a fragmentary cross-sectional view of a modified form of the structure of FIG. 5;

FIG. 6 is a cross-sectional view illustrating the structure of an exemplary plated wire memory element which may be employed in the memory of the invention;

FIGS. 7 and 8 are cross-sectional, partially schematic views illustrating how a plurality of the memory planes of FIG. 5 may be stacked and peripherally interconnected to form a multi-plane three-dimensional memory;

FIG. 9 is an overall pictorial view illustrating an exemplary arrangement of the memory of FIGS. 7 and 8; and

FIG. 10 is a fragmentary pictorial view illustrating how peripheral interconnections may typically be provided to the memory elements.

It is to be understood that like numerals designate like elements throughout the figures of the drawing. It is also to be understood that various thicknesses and sizes shown in the drawings are exaggerated for the sake of clarity.

Referring initially to FIG. 1, a rigid self-supporting conductive metal plate or sheet 10 which may, for example, be beryllium copper has a first plurality of spaced parallel channels 12 chemically etched in one surface thereof. The channels 12 are filled with dielectric material 14 which is ground flush with the surface.

As will be understood from FIGS. 2 and 3, the other surface of the sheet 10 is chemically etched to form second and third pluralities of spaced parallel channels 16 and 18 respectively perpendicular and parallel to the channels 12. The channels 18 are also located opposite respective channels 12 and have a width and depth with respect thereto so as to form spaced conductive strips 15 insulated from one another and from the sheet 10, and supported by the dielectric material 14. It is to be understood that well known precision chemical etching techniques, such as photolithograph, may be employed for etching the channels 12, 16, and 18.

Two identical sheets 10 etched as shown in FIGS. 2 and 3 are then accurately fused together in opposed relation to provide the resulting memory plane structure illustrated in FIG. 4. It will be noted that the opposed channels 16 combine to form tunnels 22 into which memory wire elements 25 are inserted as illustrated in FIG. 5. These tunnels 22 serve to hold and protect the memory wire elements 25 and to keep them accurately positioned with respect to the conductive strips 15. It is to be understood that suitable tunnels could also be provided with channels 16 provided in only one of the sheets 10.

Still referring to FIG. 5, it will be seen that the conductive strips 15 perpendicularly cross the wire elements 25 on opposite sides thereof so as to permit their use as drive lines. It will also be seen that each memory element 25 is completely surrounded by contacting metal portions of the sheets 10, and that the drive line strips 15 alternate with contacting metal portions 10A of the sheets 10, thereby providing good shielding for each memory element 25 as well as for each opposed pair of drive lines 15. If even greater shielding is desired, a construction as illustrated in FIG. 5A could be provided in which the drive line strips 15 are recessed from the outer surfaces and the recesses 21 filled with dielectric material ground flush with the outer surfaces. An adjacent contacting conductive layer 29 is then provided over the surface such as by plating or by the provision of a metal sheet fused thereto to complete the conductive encirclement of each pair of opposed drive lines 15.

As illustrated in FIGS. 5 and 6, a high permeability magnetic layer 30 of, for example, conetic or permalloy may also be provided on one or both of the outer sides of each plane in order to reduce memory cell disturbance by the earth's magnetic field. An insulation layer 31 is additionally provided in the embodiment of FIG. 5 to prevent the magnetic layer 30 from shorting the insulated strips 15.

FIG. 6 illustrates an exemplary type of memory element which may be employed for each of the memory elements 25 in FIG. 5. Typically, the memory element 25 illustrated in FIG. 6 comprises a beryllium copper inner wire 26 having, for example, a diameter of 0.005 inch and on which is plated an essentially single domain thin film 27 of magnetic material such as permalloy having a thickness of, for example, 10,000 Angstroms. The plating is done in a circumferential magnetic field produced by current flowing in the inner wire 26 so that the resulting film 27 is magnetically anisotropic, displaying remanent magnetism in the circumferential direction (commonly referred to as the "easy" direction), but not in the longitudinal direction (commonly referred to as the "hard" direction). A final insulative coating 28 of, for example, 0.0001 inch of a thermoplastic material is applied over the magnetic film 27, such as by dipping, so as to prevent shorting of the drive line conductive strips 15 when the memory wire elements 25 are inserted in the tunnels 22 as shown in FIG. 5.

FIGS. 7–9 illustrate how a plurality of the memory planes of FIG. 5 may be stacked and peripherally interconnected to form a multi-plane three-dimensional memory. FIG. 7 is a cross-section taken longitudinally through the center of a wire memory element 25 and perpendicular to the drive line strips 15, while FIG. 8 is a cross-section taken longitudinally through the center of a drive line strip 15 and perpendicular to the wire memory elements 25, as indicated by the line 8—8 in FIG. 7, the line 7—7 in FIG. 8, and the lines 7—7 and 8—8 in FIG. 9.

The peripheral sections 40 and 42 in FIGS. 7–9 contain circuitry which provides appropriate interconnections for the inner conductors 26 of the memory wire elements 25 and the drive line strips 15. These peripheral sections 40 and 42 may also advantageously contain the sensing, selecting and driving circuitry required for the memory. The circuitry in the sections 40 and 42 is preferably provided using the coaxial packaging techniques disclosed in the commonly assigned U.S. Pat. No. 3,351,816 and in the commonly assigned copending patent applications Ser. No. 613,652, filed Feb. 2, 1967, and Ser. No. 819,888, filed Apr. 28, 1969. As illustrated in FIG. 9, the resulting memory will then comprise a stack of wafers containing memory wire elements and drive lines as well as the peripheral sensing, driving, selecting, and interconnecting circuitry therefor.

It will be seen in FIGS. 7 and 10 that the lower sheet 10 of each memory plane extends into the peripheral sections 40 in order to feed thereto the memory wire connecting strips 51 to which are soldered the ends of the inner conductors of the memory elements 25. The solder is indicated by the numeral 154. Insulative material 53 is provided to insulate the connecting strips 51 from each other and from the sheet 10. Also, as shown in FIG. 8, both of the sheets 10 extend into the peripheral sections 42 in order to feed the drive line strips 15 thereto. Thus, the memory sheets 10 may conveniently be incorporated with the circuitry of the peripheral wafers to provide the resulting structure shown in FIG. 9.

It will be understood that a memory constructed as described herein may be operated in various known types of operating modes in either a destructive or nondestructive manner. One skilled in the art will readily be able to provide the required driving, sensing, selecting, and interconnecting circuitry for this purpose. It will also be understood that, in accordance with well known noise cancellation techniques, certain of the wires 25 may be provided without a magnetic film 27 (FIG. 6) thereon so that they may serve as "dummies" to provide for noise cancellation.

Although the invention has been described in connection with a particular exemplary embodiment, it is to be understood that the construction, arrangement, fabrication and/or use of the invention is subject to considerable variations and/or modifications without departing from the scope of the invention as defined in the appended claims.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. In a method of making a magnetic memory,
providing first and second self-supporting conductive planar members,
forming electrically insulated conductors in a common plane of each planar member spaced from a surface thereof and also forming in said surface of at least one planar member a plurality of spaced channels extending in a direction so as to cross said conductors,
disposing said planar members in opposed relation to one another with the conductors of one planar member opposite and parallel to respective conductors of the other planar member and so that the channels form tunnels crossed by conductors on opposite sides thereof, and
inserting wire-like memory elements into said tunnels.

2. In a method of making a magnetic memory,
providing first and second self-supporting conductive planar members,
forming dielectric-filled spaced parallel channels in one surface of each planar member and a plurality of spaced parallel memory element channels in the other surface of at least one planar member extending in a direction so as to cross said dielectric-filled channels,
forming a plurality of isolating channels in said other surface of each planar member parallel to said dielectric-filled channels and having a location, width, and depth relative thereto so as to electrically isolate spaced parallel conductive portions of each planar member to thereby form a plurality of spaced, electrically isolated conductors parallel to said dielectric-filled channels and located in a common plane perpendicularly spaced from said other surface, and
disposing said planar members in opposed relation to one another with the conductors and the memory element channels of each planar member opposite

and parallel to respective conductors of the other planar member and so that the memory element channels form memory element receiving tunnels crossed by conductors on opposite sides thereof.

3. The invention in accordance with claim 2, wherein said method includes the additional step of inserting wire-like memory elements into said tunnels.

4. The invention in accordance with claim 3, wherein said channels are formed using precision chemical etching techniques.

5. The invention in accordance with claim 3, wherein each isolating channel is formed opposite a respective conductor if its planar member with a width extending at least beyond the nearest side of each of the dielectric-filled channels forming the conductor and with a depth extending to the conductor.

6. The invention in accordance with claim 3, wherein said method includes the additional steps of recessing the conductors of each planar member from said one surface thereof, filling said recesses with dielectric material, and providing a conductive layer adjacent and in electrical contact with the surface of each planar member containing said recesses so as to provide conductive encirclement of each pair of opposed conductors.

7. The invention in accordance with claim 3, wherein said method includes the additional step of providing a magnetic layer adjacent at least one of the surfaces of said planar members containing said dielectric-filled channels.

8. The invention in accordance with claim 3, wherein said method includes the additional step of stacking a plurality of opposed pairs of planar members to form a three-dimensional memory.

9. The invention in accordance with claim 3, wherein each wire-like memory element has a conductive inner wire and a magnetic thin film thereon, and wherein said method includes forming insulated connecting conductors in one of said planar members and electrically connecting said connecting conductors to respective conductive inner wires of said memory elements.

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