June 18, 1963 SVEN ERIK WAHLSTRÖM 3,094,689

MAGNETIC CORE MEMORY CIRCUIT

Filed June 20, 1960

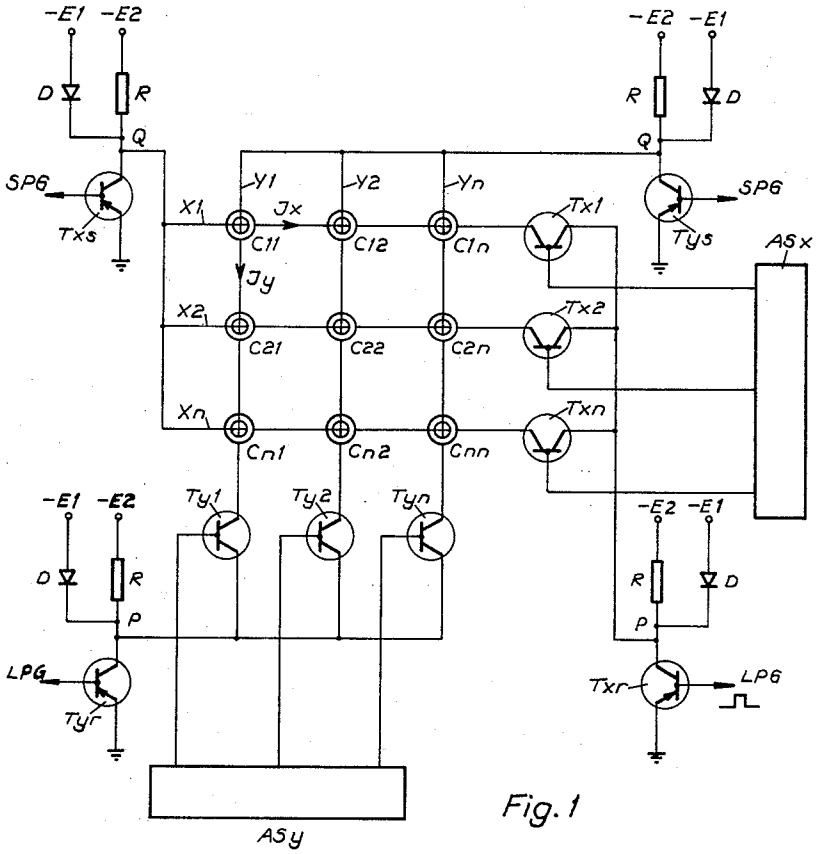

Fig. 1

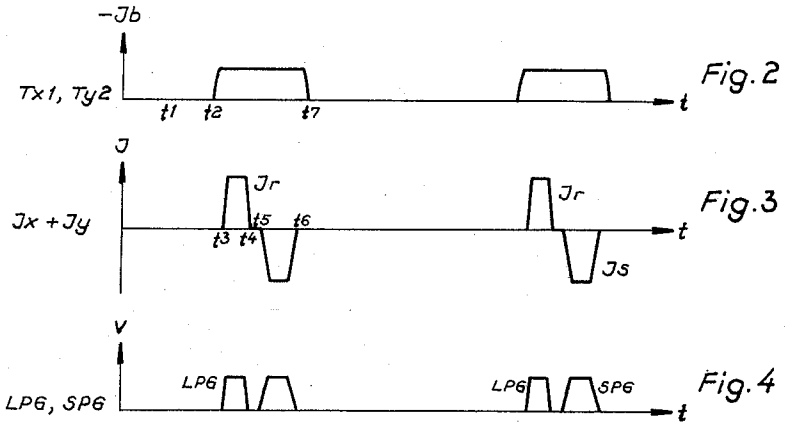

Fig. 2

Fig. 3

Fig. 4

INVENTOR
SVEN ERIK WAHLSTRÖM
By Hamerand Nydick
ATTORNEYS

United States Patent Office 3,094,689 Patented June 18, 1963

3,094,689

MAGNETIC CORE MEMORY CIRCUIT

Sven Erik Wahlström, Enskede, Sweden, assignor to Aktiebolaget Atvidabergs Industrier, Atvidaberg, Sweden, a joint-stock company of Sweden

Filed June 20, 1960, Ser. No. 37,318
Claims priority, application Sweden July 10, 1959
2 Claims. (Cl. 340—174)

The present invention relates to a magnetic core memory circuit, particularly a magnetic core memory where one or more memory cores are selected and magnetized with the aid of transistor switches.

In the magnetic core memories manufactured hitherto, the selection and magnetization of the desired cores in order to write or read information in the core is generally performed by means of electron tube circuits. There are several reasons why transistors with their longer life time and lower power consumption are not used more extensively to drive core memories, at least not greater memories where the reading and writing pulses are very fast.

One reason is that the impedance of a drive winding, which can pass through several thousand cores is very non-linear and moreover is depending on the number of cores to be switched. If the rise time of the drive pulses is very short and the winding is passing some thousand cores the electromotive force induced in the drive winding may reach some twenty or thirty volts. In order to maintain a constant current in the drive winding and thus a well defined switching time in spite of the non-linear impedance it is necessary that the drive winding is fed by a constant current source. This problem has generally been solved in such a manner that the driver stage generates a well defined voltage pulse and feeds the drive winding through a series resistor which is so great that the influence of the drive winding on the current will become negligible. When using transistors instead of electron tubes in the drive circuits the transistors will take up a very high voltage when they are non-conducting. As high speed transistors which withstand high voltages when cut off are not readily available today, it has been necessary to reduce the demand for a constant current during the whole drive pulse.

One possibility for transistorizing a magnetic core memory at least partly is to select the desired winding, for example an X-winding with the aid of transistor switches individual to the different windings and then to feed all the windings of this class (for example the X-windings) of the memory matrix with drive pulses from a constant current source containing electron tubes. The transistor switch of the selected winding is made conducting before the drive pulse appears, and thus the voltage across the switches of the non-selected windings is reduced to electromotive force induced in the selected winding.

Disregarding that electron tubes are unsuitable in transistor circuits, the last mentioned circuit has some drawbacks, particularly in core memories of the kind where the drive pulse is built up of a read pulse having a certain polarity, immediately followed by a write pulse having the opposite polarity. The transistor switches of the non-selected windings then must have such a base bias that the collector-base diode cannot be made conducting when the collector during one half of the drive pulse (for example the positive pulse if the transistor is a pnp-transistor) is acting as an emitter.

Thus it is necessary to select such a transistor that the collector-base diode can withstand twice the induced E.M.F.

These drawbacks can be avoided with a circuit according to the invention with core memories comprising a

plurality of core groups where each group of cores is provided with at least one common winding and a normally closed gate in series with the winding, said gate being controlled by a first control circuit (for example an address register). The invention is characterized therein that all windings and the pertaining gates are connected in parallel between two constant current sources which are normally short circuited to a common point through electronic switches, one of which is arranged to be opened when the cores are to be set into one magnetic state while the other switch is arranged to be opened when the cores are to be set into the opposite state, whereby a constant current is caused to flow in the desired direction from one constant current source through the gate and the common winding of the selected core group.

The invention shall be more fully described in connection to the enclosed drawings wherein—

FIG. 1 shows a schematic diagram of a core memory according to the invention and

FIGS. 2, 3 and 4 show pulse diagrams.

In FIG. 1, C11, C12 . . . C_{nn} designate a number of ring shaped memory cores having a rectangular hysteresis loop, said cores being arranged in a matrix array. The cores are provided on one hand with windings X1, X2, X*n* each common to all cores of a row and on the other hand with windings Y1, Y2, Y*n* each common to the cores of a column. The windings are preferably a single wire threaded through the cores. The memory operates according to the coincidence principle i.e. both one X- and one Y-winding must carry cooperating currents if a core should change the state. T*x*1, T*x*2, T*xn* and T*y*1, T*y*2, T*yn* designate transistor gates for the X- and Y-windings respectively, said gates being utilized for selecting a certain core in the memory. The transistors are normally cut off but they can be made conducting by applying a suitable voltage to the base, for example from an address register AS*x* and AS*y* respectively. All the X-windings X1, X2, X*n* are connected in parallel between a read pulse drive circuit and a write pulse drive circuit. Each drive circuit comprises a constant current source containing a voltage source —E2 having a comparatively high negative voltage connected in series with a resistor R having a value which is high compared with the impedance of the X windings and a normally conducting transistor T*xr* and T*xs* respectively. The collectors of said transistors are connected to the point P and Q respectively where the resistor R is connected to the parallel connected X windings. The emitters of the transistors T*xr* and T*xy* are grounded. The base electrode of the transistor T*xr* is connected to a readpulse generator LPG while the base of the transistor T*xs* is connected to a write pulse generator SPG. The waveform of the positive pulses generated by said pulse generators is shown in FIG. 4. In order to protect the transistors against surge voltages a diode D is connected between each point P and Q respectively and a negative voltage source —E1 the voltage of which is somewhat higher than the highest possible voltage which can be induced in the windings.

The Y-windings are in the same manner connected between two drive circuits of the same kind as the drive circuits of the Y-windings and thus they are not described in greater detail. The transistors included in the drive circuits of the Y-windings are designated T*yr* and T*ys*, respectively.

The operation of the circuit will be described in the following with reference to the pulse diagrams of FIGS. 2–4. At the time *t*1 all the transistors T*x*1–T*xn* and T*y*1–T*yn* are non-conducting while the transistors T*xr*, T*xs*, T*yr* and T*ys* are conducting. All the points P and Q thus have zero potential and no current can flow through the X- and Y-windings. At the time *t*2 a certain core,

for example C21 is selected by the address registers ASx and ASy causing the transistors Tx2 and Ty1 to be made conducting by reducing the base potential so much that a base current having the wave form shown in FIG. 2 is beginning to flow. At the time *t*3 when a sufficient amount of charge carriers have been injected in the base regions of the transistors Tx2 and Ty1, the read pulse generator LPG is generating a read pulse having the waveform shown in FIG. 4, said pulse being applied to the base of the transistors T*xr* and T*yr*. Said transistors which are of a type having a short rise and decay time, are cut off causing the short circuit between the points P and ground to be interrupted. Now currents will flow on one hand from ground through the transistor T*xs*, the winding X2, the transistor Tx2 and the resistor R to the voltage —E2, and on the other hand from ground through the transistor T*ys*, the winding Y1, the transistor Ty1 and the resistor R to the voltage —E2. The sum I*r* of said currents has the waveform shown in FIG. 3 with comparatively steep edges. If the core C21 is set into the magnetic state representing a binary "one," it is zero set and a voltage pulse is induced in a read out winding (not shown). At the time *t*4 immediately after the end of the read pulse when the transistors T*xr* and T*yr* are again made conducting and the currents through the windings X2 and Y1 cease, a write pulse is generated during the time *t*5–*t*6 by the write pulse generator SPG, causing the transistors T*xs* and T*ys* to be cut off so that currents having the reverse direction are obtained through the windings Y1 and X2 and set the core into the "one"-state. At the time *t*7 when the write pulse has ceased the transistors Tx2 and Ty1 are again made non-conducting. After a moment a new read and write pulse appears and information can be read out and be written at an arbitrary location in the memory.

Owing to the fact that one of the transistors T*xr* or T*xs* and T*yr* or T*ys*, respectively, and one of the transistors Tx1–T*xn* and Ty1–T*yn*, respectively, is always conducting the potential of the points P and Q can never exceed the voltage induced in a selected winding, and thus the required voltage rate of the transistors is moderate. As the emitter or collector voltage of the transistors Tx1–T*xn*, Ty1–T*yn* never exceeds ground potential they only need a small positive bias to be kept non-conducting, and thus the drive circuits of the address registers can be made very simple.

The windings which have not been selected by the address registers are connected to ground through the drive transistors T*xs* and T*ys* respectively. Thus error signals owing to capacitive coupling between the read out winding (not shown) and the unselected windings can be avoided in the read out winding.

The transistors Tx1–T*xn* and Ty1–T*yn* conduct currents in both directions and they should preferably be bilateral as is indicated in the circuit diagram. As such

transistors up to now have been expensive and not readily available it may be necessary to use standard unilateral transistors.

If the transistor type used has a considerably lower rated emitter-base than collector-base back voltage the collector electrode is preferably connected to the points P of the drive circuits. Owing to the steeper edges of the read pulses the voltage induced in a selected winding will namely become higher during reading than during writing.

If the rated back voltages are of the same magnitude it is however suitable to connect the emitter electrodes of the transistors Tx1–T*xn* and Ty1–T*yn* to the points P particularly if the current amplification B of the transistor is small in the inverted circuit i.e. when the collector is acting as emitter.

If the emitter is connected to the point P the current through the winding is composed of the base current and the current flowing to the point P during the reading phase. During the writing phase, however the current through the winding is almost equal to the current to the point Q. In this manner the base current which shall be delivered by the address register may be lower than if the collector is connected to the point P.

Of course the invention is not limited to the shown embodiment but it can be modified in many ways.

I claim:

1. A magnetic core memory circuit comprising a plurality of groups of magnetic cores forming a matrix, each core of which has a rectangular hysteresis loop, each group of cores in said array is connected to at least one common winding, normally closed gate circuit means connected in series with each of said windings for selecting a core, control means connected to said gate means for controlling said gate means, said plurality of windings connected to said cores and said gate circuit means connected thereto are connected in parallel between two constant current sources each of which is normally short-circuited to a common potential by means of transistor switching means, one transistor means of which is cut off when setting the cores into one magnetic state while another transistor means is cut off when setting the cores into a reverse state, a constant current flowing from one current source to the other through a winding of a core selected by said control means, and non-selected windings being connected to said common potential.

2. A circuit as claimed in claim 1 characterized therein that the control means are provided to open and close the gate of a selected core group only at the times when both switches are conducting.

References Cited in the file of this patent

UNITED STATES PATENTS

2,917,727	Reach	Dec. 15, 1959
2,939,119	Einsele	May 31, 1960
3,054,988	Edwards	Sept. 18, 1962