Disclosed is a technique for providing a stable current driver for active matrix light emitting displays, in particular, active matrix organic light emitting diode (AMOLED) displays. The techniques include a driving method to generate a gate-source voltage independent of the threshold voltage of the drive thin film transistor (TFT) and OLED voltage, by using a local current reference.
Locally Referenced Voltage Programmed Pixel for AMOLED Displays

ABSTRACT

Disclosed is a technique for providing a stable current driver for active matrix light emitting displays, in particular, active matrix organic light emitting diode (AMOLED) displays. The techniques include a driving method to generate a gate-source voltage independent of the threshold voltage of the drive thin film transistor (TFT) and OLED voltage, by using a local current reference.
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FIELD OF THE INVENTION

The present invention generally relates to a light emitting device displays, and particularly, to a driving technique for AMOLED, and to enhance the brightness stability of the OLED by using circuit compensation.

SUMMARY OF INVENTION

This invention provides a simple and highly stable voltage-programmed pixel circuit, suitable for use in AMOLEDs. Since its driving scheme is very simple, the cost of external driver extremely decreases. This driving scheme is suitable particularly for large area display and TVs due to its fast settling time as well as small area mobile phone and PDA displays.

Advantages

The pixel circuit provides a stable current independent of the threshold voltage shift of the drive TFT and OLED degradation under prolonged display operation, to efficiently improve the display operating lifetime. Moreover, because of the driving scheme simplicity, we expect lower cost for external driver.
DETAILED DESCRIPTION OF THE INVENTION

The present invention involves a technique for driving a column of pixels to provide stable OLED operation.

FIG. 1 (a-b) shows a pixel circuit along with its control signals. This method is valid with complementary device (p-type transistor) as well. The pixel circuit comprises three transistors $T_1$, $T_2$ and $T_3$, a storage capacitor $C_1$ and an organic light-emitting diode (OLED) $O_{10}$. The pixel circuit is connected to a select line ($SEL[n]$), two signal lines ($VDATA_1$ and $VDATA_2$), a negative voltage line ($SEL[n+1]$), a positive voltage line ($VDD$).

Transistors $T_1$, $T_2$ and $T_3$ can be amorphous silicon, nano/micro crystalline silicon, poly silicon, organic thin-film transistors (TFT), or transistors in standard CMOS technology. The source terminal of driving transistor $T_1$ is connected to the anode electrode of the OLED $O_{10}$. The drain terminal of $T_1$ is connected to $VDD$, and the gate terminal of $T_1$ is connected to $VDATA_2$ through $T_2$. The storage capacitor is connected between the source and gate of $T_1$.

Transistor $T_2$ is a switch. The gate terminal of $T_2$ is connected to the select line ($SEL[n]$). The drain terminal of $T_2$ is connected to $VDATA_2$, and the source terminal is connected to the gate terminal of $T_1$.

Transistor $T_3$ is the programmer transistor. The gate terminal of $T_3$ is connected to $VDATA_1$. The source terminal of $T_3$ is connected to $SEL[n+1]$, and the drain terminal is connected to the anode terminal of the OLED $O_{10}$. The cathode electrode of the OLED $O_{10}$ is connected to the common ground.

The operation of presented pixel in FIG 1 (b) consists of two operating cycles: programming cycle and driving cycle.

With reference to the waveform shown on FIG. 1 (b) we describe the following operating cycles.

1. The first operating cycle: $SEL[n]$ is high and $SEL[n+1]$ has a negative voltage (VSS). $VDATA_2$ goes to a bias voltage (VB), and $VDATA_1$ has the programming voltage (VP) resulting in the voltage of node B as:
$$V_{mode\_H} = VB - (VP - VSS) - VT1 + VT3$$

where VT1 and VT3 are the threshold voltage of T1 and T3, respectively.

The second operating cycle: SEL[n] is low, and SEL[n+1] is high (because of the next row programming cycle). The VGS of T1 is given by

$$VGS = (VP - VSS) + VT1 - VT3.$$  

Since T3 is on for just small fraction of time, its VT shift is negligible. Therefore, the current of T1 during the operating cycle is independent of the shift in its threshold voltage.

FIG. 2 shows an array structure with pixel 20, 21 of FIG. 1 (a).

The array consists of pixels 20, 21 which are arranged in rows and columns. VDATA1 and VDATA2 are shared between the common column pixels while SEL and VDD are shared between common row pixels in an array structure. In order to save the area and increase the aperture ratio, VDD is shared between two consecutive rows.

FIG. 3 (a-b) shows a pixel circuit along with its control signals. This method is valid with complementary device (p-type transistor) as well.

The pixel circuit comprises three transistors T1, T2 and T3, a storage capacitor C1 and an organic light-emitting diode (OLED) 30. The pixel circuit is connected to a select line (SEL[n]), a signal line (VDATA), a negative voltage line (SEL[n+1]), a positive voltage line (VDD).

Transistors T1, T2 and T3 can be amorphous silicon, nano/micro crystalline silicon, poly silicon, organic thin-film transistors (TFT), or transistors in standard CMOS technology. The source terminal of driving transistor T1 is connected to the anode electrode of the OLED 30. The drain terminal of T1 is connected to VDD, and the gate terminal of T1 is connected to VDD through T2. The storage capacitor is connected between the source and gate of T1.

Transistor T2 is a switch. The gate terminal of T2 is connected to the select line (SEL[n]). The drain terminal of T2 is connected to VDD, and the source terminal is connected to the gate terminal of T1.
Transistor T3 is the programmer transistor. The gate terminal of T3 is connected to VDATA1. The source terminal of T3 is connected to SEL[n+1], and the drain terminal is connected to the anode terminal of the OLED 30. The cathode electrode of the OLED 30 is connected to the common ground.

The operation of presented pixel in FIG 3 (b) consists of two operating cycles: programming cycle and driving cycle.

With reference to the waveform shown on FIG. 3 (b) we describe the following operating cycles.

The first operating cycle: SEL[n] is high and SEL[n+1] has a negative voltage (VSS). VDATA goes to a programming voltage (VP), and VDD has the bias voltage (VB) resulting in the voltage of node B as:

\[ V_{node-B} = V_B - (V_P - V_S) - VT_1 + VT_3 \]

where VT1 and VT3 are the threshold voltage of T1 and T3, respectively.

The second operating cycle: SEL[n] is low, and SEL[n+1] is high (because of the next row programming cycle). The VGS of T1 is given by

\[ V_{GS} = (V_P - V_S) + VT_1 - VT_3 \]

Since T3 is on for just small fraction of time, its VT shift is negligible. Therefore, the current of T1 during the operating cycle is independent of the shift in its threshold voltage.

FIG. 4 shows an array structure with pixel 40, 41 of FIG. 1 (a).

The array consists of pixels 40, 41 which are arranged in rows and columns. VDATA is shared between the common column pixels while SEL and VDD are shared between common row pixels in an array structure. In order to save the area and increase the aperture ratio, VDD is shared between two consecutive rows.

FIG. 5 (a-b) shows a pixel circuit along with its control signals. This method is valid with complementary device (p-type transistor) as well.

The pixel circuit comprises three transistors T1, T2, T3 and T4, two storage capacitors 51, 52 and an organic light-emitting diode (OLED) 50. The pixel circuit is connected to a
select line (SEL[n]), two signal lines (VDATA1 and VDATA2), a negative voltage line (SEL[n+1]), a positive voltage line (VDD).

Transistors T1, T2, T3 and T4 can be amorphous silicon, nano/micro crystalline silicon, poly silicon, organic thin-film transistors (TFT), or transistors in standard CMOS technology.

The source terminal of driving transistor T1 is connected to the anode electrode of the OLED 50. The drain terminal of T1 is connected to VDD, and the gate terminal of T1 is connected to VDATA2 through T2. The storage capacitor is connected between the source and gate of T1.

Transistor T2 is a switch. The gate terminal of T2 is connected to the select line (SEL[n]). The drain terminal of T2 is connected to VDATA2, and the source terminal is connected to the gate terminal of T1.

The source terminal of programmer transistor T3 is connected SEL[n+1]. The drain terminal of T3 is connected to the source of T1, and the gate terminal of T3 is connected to VDATA1 through T4.

Transistor T4 is a switch transistor. The gate terminal of T3 is connected to SEL[n]. The source terminal of T3 is connected to VDATA1, and the drain terminal is connected to the gate terminal of T1.

The operation of presented pixel in FIG 5 (b) consists of two operating cycles: programming cycle and driving cycle.

With reference to the waveform shown on FIG. 5 (b) we describe the following operating cycles.

The first operating cycle: SEL[n] is high and SEL[n+1] has a negative voltage (VSS). VDATA1 goes to a programming voltage (VP), and VDATA2 has the bias voltage (VB) resulting in the voltage of node B as:

\[ V_{node-B} = VB - (VP - VSS) - VT1 + VT3 \]

where VT1 and VT3 are the threshold voltage of T1 and T3, respectively. The VGS of T1 is given by

\[ VGS = (VP - VSS) + VT1 - VT3 \].

The second operating cycle: SEL[n] goes to an intermediate voltage in which T2 is off and T4 is on. VDATA1 goes to zero, so T3 turns off.
The Third operating cycle; SEL[n] is low, and SEL[n+1] is high (because of the next row programming cycle). Since T3 is on for just a small fraction of time, its VT shift is negligible. Therefore, the current of T1 during the operating cycle is independent of the shift in its threshold voltage.

The same array structure as FIG. 2 can be used for this pixel as well.

FIG. 6 (a-b) shows a pixel circuit along with its control signals. This method is valid with complementary device (p-type transistor) as well.

The pixel circuit comprises three transistors T1, T2, T3 and T4, two storage capacitors 61, 62 and an organic light-emitting diode (OLED) 60. The pixel circuit is connected to a select line (SEL[n]), a signal line (VDATA), a negative voltage line (SEL[n+1]), a positive voltage line (VDD).

Transistors T1, T2, T3 and T4 can be amorphous silicon, nano/micro crystalline silicon, poly silicon, organic thin-film transistors (TFT), or transistors in standard CMOS technology.

The source terminal of driving transistor T1 is connected to the anode electrode of the OLED 60. The drain terminal of T1 is connected to VDD, and the gate terminal of T1 is connected to VDATA2 through T2. The storage capacitor is connected between the source and gate of T1.

Transistor T2 is a switch. The gate terminal of T2 is connected to the select line (SEL[n]). The drain terminal of T2 is connected to VDD, and the source terminal is connected to the gate terminal of T1.

The source terminal of programmer transistor T3 is connected SEL[n+1]. The drain terminal of T3 is connected to the source of T1, and the gate terminal of T3 is connected to VDATA through T4.

Transistor T4 is a switch transistor. The gate terminal of T3 is connected to SEL[n]. The source terminal of T3 is connected to VDATA, and the drain terminal is connected to the gate terminal of T1.

The operation of presented pixel in FIG 6 (b) consists of two operating cycles: programming cycle and driving cycle.
With reference to the waveform shown on FIG. 6 (b) we describe the following operating cycles.

The first operating cycle: SEL[n] is high and SEL[n+1] has a negative voltage (VSS). VDATA goes to a programming voltage (VP), and VDD has the bias voltage (VB) resulting in the voltage of node B as:

\[ V_{node-B} = VB - (VP - VSS) - VT1 + VT3 \]

where VT1 and VT2 are the threshold voltage of T1 and T3, respectively. The VGS of T1 is given by

\[ VGS = (VP - VSS) + VT1 - VT3. \]

The second operating cycle: SEL[n] goes to an intermediate voltage in which T2 is off and T4 is on. VDATA goes to zero, so T3 turns off.

The third operating cycle: SEL[n] is low, and SEL[n+1] is high (because of the next row programming cycle). Since T3 is on for just a small fraction of time, its VT shift is negligible. Therefore, the current of T1 during the operating cycle is independent of the shift in its threshold voltage.

The same array structure as FIG. 4 can be used for this pixel as well.

FIG. 7 shows the simulation result for the circuit and waveform shown in the FIG. 1 (a) and (b). The result shows that the change in the OLED current due 2-volt VT-shift in T1 is less than 4%.
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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 (a-c) is a circuit diagram of an embodiment of a pixel circuit and its corresponding waveforms.
FIG. 2 is an array structure of the pixel presented in FIG 1.
FIG. 3 (a-b) is a circuit diagram of an embodiment of a pixel circuit and its corresponding waveform.
FIG. 4 is an array structure of the pixel presented in FIG 3.
FIG. 5 (a-b) is a circuit diagram of an embodiment of a pixel circuit and its corresponding waveform.
FIG. 6 (a-b) is a circuit diagram of an embodiment of a pixel circuit and its corresponding waveform.
FIG. 7 shows the current stability of the pixel after a 2-vlot VT shift in drive TFT.
FIG. 1
FIG. 3
FIG. 4

- SEL[j]
- VDD[j/2]
- SEL[j+1]
- VDD[j/2+1]
- SEL[j+2]
- SEL[j+3]
- VDATA1[i]
- VDATA2[i]
- VDATA1[i+1]
- VDATA2[i+1]
FIG. 5

(a) Schematic diagram of a circuit with components labeled T1, T2, T3, T4, VDD, VDATA1, VDATA2, SEL[n], SEL[n+1], and OLED.

(b) Timing diagram showing SEL, VDATA2, VDATA1, and their respective programming cycles (1), (2), and (3), followed by a driving cycle.
FIG. 6
FIG. 7