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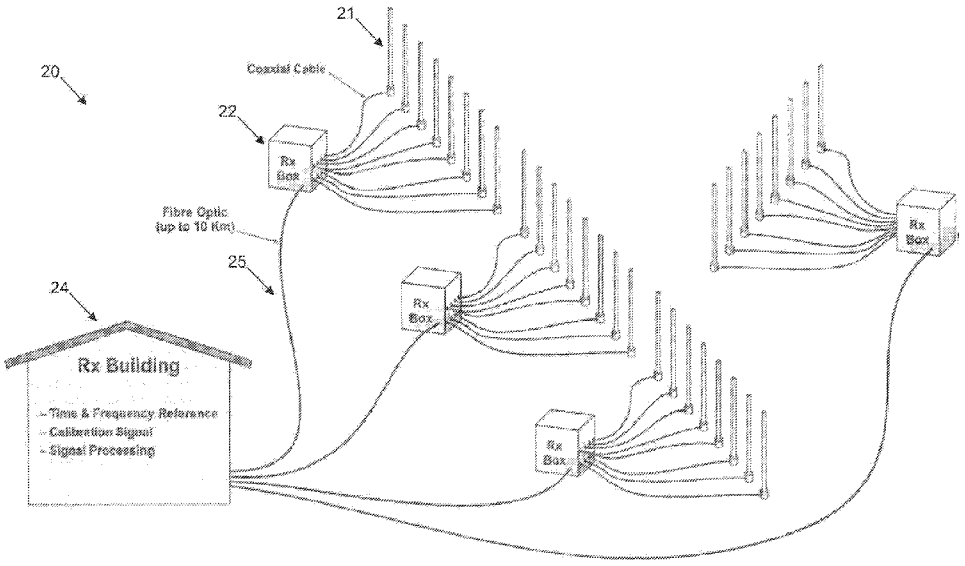

Fig. 2

(57) Abstract: A method of determining the optical delay of an optical waveguide, the method including the steps of: transmitting a first periodic modulated optical signal along the optical waveguide with a first modulation frequency; determining a phase inverted copy of the periodic modulated signal; simultaneously transmitting the phase inverted copy of the periodic modulated signal along the optical waveguide; processing the output of the optical waveguide to determine a beat frequency between the transmitted signals; and utilising the beat frequency to determine a distance measure from a transmitter to a receiver end of the optical waveguide.

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Accurate Timing Distribution System and Method

FIELD OF THE INVENTION

[0001] The present invention provides for systems and methods for the accurate tracking of timing and distances of signals communicated over geographically distributed locations.

BACKGROUND OF THE INVENTION

[0002] Any discussion of the background art throughout the specification should in no way be considered as an admission that such art is widely known or forms part of common general knowledge in the field.

[0003] Often there is a need for the communication of high volumes of sensed information from a series of geographically disparate located sensors to a central location.

[0004] Examples of systems requiring high volume data transfers and accurate relative timing of the sensor include synthetic aperture telescope projects such as the square kilometre array (SKA) telescope where multiple receivers are separately geographically located and their signals combined to provide for a higher resolution signal.

[0005] Further, such systems are often operated in a beamforming mode which requires extremely accurate timing and distance information to be conveyed from a series of sensors to a central control. Other sensor networks also have such requirements, such as for example, complex long range radar systems.

[0006] There is therefore a general need to provide for accurate timing control of such arrangements. Additionally, there is a general need for an effective receiver capable of handling optical and electrical signals and their interfacing.

SUMMARY OF THE INVENTION

[0007] It is an object of the invention, in its preferred form to provide for an accurate timing control between a centrally located control unit and a series of sensors.

[0008] In accordance with a first aspect of the present invention, there is provided a method of determining the optical delay of an optical waveguide, the method including the steps of: (a) transmitting a first periodic modulated optical signal along the optical waveguide with a first modulation frequency; (b) determining a phase inverted copy of the periodic modulated signal; (c) simultaneously transmitting the phase inverted copy of the periodic modulated signal along the optical waveguide; (d) processing the output of the optical waveguide to determine a beat frequency between the transmitted signals; and (e)

utilising the beat frequency to determine a distance measure from a transmitter to a receiver end of the optical waveguide.

[0009] In some embodiments there is also the step of determining the propagation delay across the optical waveguide from the beat frequency. The optical waveguide can comprise an optical fibre connecting a geographically separated receiver and transmitter. The first periodic modulated optical signal can comprise a sinusoidal or clocked waveform.

[0010] In accordance with a further aspect of the present invention, there is provided a method of determining a distance of transmission of an optical signal over an optical waveguide link, the method including the steps of: (a) transmitting a correlated forward and return modulated optical signal over the optical waveguide link; (b) determining a beat frequency of the interference of the two signals; and (c) utilising the beat frequency to determine a corresponding distance measurement of the transmitted signal.

[0011] The forward and return modulating optical signals are preferably inverted copies of one another.

[0012] In accordance with a further aspect of the present invention, there is provided a signal receiver for receiving a series of antenna input signals from a series of antennas, the receiver including: a receiver optical control unit, receiving optical timing signals, including optical clocking signal, optical time interval signals and optical control signals; the receiver optical control unit: converting the optical clocking signal into a corresponding electrical sampling signal for antenna signal sampling; converting the optical time interval signal into a corresponding electrical time interval signal for controlling the sampling time period; converting the optical control signals into corresponding electrical control signals including a calibration signal, providing sampling delay information for sampling of the antenna signals; at least one signal sampling unit for sampling and filtering the antenna input signal, and converting them to a corresponding digital optical signal, the signal sampling unit utilising: an antenna input signal for sampling an antenna signal; the electrical time interval signal for controlling the sampling frequency; the calibration signal for controlling a sampling delay for delaying the output of the sampled antenna signal; the signal sampling unit sampling the antenna signal and outputting an optical data sampled signal and the sampling frequency.

[0013] The optical clocking signal can be also utilised to develop a receive optical control unit clocking signal. The electrical time interval signal preferably can include a 1 period per second timing signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

[0015] Fig. 1 illustrates schematically a general arrangement of a series of sensors and corresponding control unit;

[0016] Fig. 2 illustrates one form of sensing array having multiple antenna arrays interconnected to receivers and an overall control unit;

[0017] Fig. 3 illustrates one form of signal processing train used in an embodiment;

[0018] Fig. 4 illustrates the overall split receiver architecture;

[0019] Fig. 5 illustrates the 100MHz signal conditioning circuit;

[0020] Fig. 6 illustrates the 1PPS modulation circuit;

[0021] Fig. 7 illustrates a timing diagram of the modulation of the 1PPS signal;

[0022] Fig. 8 illustrates a timing diagram of the modulation of the 1PPS signal at startup;

[0023] Fig. 9 illustrates the external interfaces of the TOCU;

[0024] Fig. 10 illustrates a photo of a TOCU prototype front panel;

[0025] Fig. 11 illustrates a photo of a TOCU back panel;

[0026] Fig. 12 schematically illustrates the TOCU block diagram;

[0027] Fig. 13 schematically illustrates the control/status PWA;

[0028] Fig. 14 schematically illustrates the operation of the bidirectional transceivers;

[0029] Fig. 15 schematically illustrates a block diagram of the SYNC PWA;

[0030] Fig. 16 illustrates a clocking diagram of the 1PPS timing;

[0031] Fig. 17 schematically illustrates a block diagram of the reference PWA;

[0032] Fig. 18 schematically illustrates the digital dual mixer time difference circuit;

[0033] Fig. 19 schematically illustrates the fibre calibration timing diagram;

[0034] Fig. 20 schematically illustrates the LDE display PWA block diagram;

[0035] Fig. 21 schematically illustrates the ROCU fibre length calculation;

[0036] Fig. 22 schematically illustrates the ROCU external interfaces;

[0037] Fig. 23 schematically illustrates the ROCU;

[0038] Fig. 24 schematically illustrates the Control/Status PWA;

[0039] Fig. 25 schematically illustrates the calibration PWA;

[0040] Fig. 26 schematically illustrates the reference PWA;

[0041] Fig. 27 schematically illustrates tje LED Display PWA;

[0042] Fig. 28 schematically illustrates the split stand alone DRxIV;

[0043] Fig. 29 schematically illustrates the split eight way system DVxiV;

[0044] Fig. 30 schematically illustrates the split front end DRxIV structure;

[0045] Fig. 31 schematically illustrates the split standalone backend DRxIV structure;

[0046] Fig. 32 schematically illustrates the split eight way system backend DRxIV structure;

[0047] Fig. 33 schematically illustrates the AFE;

[0048] Fig. 34 schematically illustrates the ADC;

[0049] Fig. 35 schematically illustrates the Narrowband DDC;

[0050] Fig. 36 schematically illustrates the Wideband DDC;

[0051] Fig. 37 schematically illustrates the ALC;

[0052] Fig. 38 schematically illustrates the FLC;

[0053] Fig. 39 schematically illustrates the split DRxIV control and status unit;

[0054] Fig. 40 schematically illustrates the split DRxIV daisy chaining.

DETAILED DESCRIPTION

[0055] The preferred embodiments provide for a system and method which allows extremely accurate timing information to be communicated between a control unit location and a series of geographically dispersed sensors in a sensor network.

[0056] Such an arrangement is illustrated 1 in Fig. 1, wherein a series of Sensors e.g. 2-4 communicate with a central control unit 5 over a communications link 6, which in this case is assumed to be optical. Each of the sensors e.g. 2 involves a high speed sensing operation. This involves sensing the environment, normally in an analog manner, converting the sensed signal to a digital signal having a known relative time measure. Each of the sensors e.g. 2 can be separately geographically located in a dispersed manner. The control unit 5 needs to accurately combine the signals from the sensors in a time relative manner to an accurate level of measurement.

[0057] The arrangement 1 of Fig. 1 is generic and will have specific design requirements depending on needs and application requirements. For example, when applied to an antenna array sensing system, the layout may be similar to that shown in Fig. 2, whereby a large number of receivers e.g. 21 having a predetermined topology are interconnected to a receiver box or bunker 22 by means of coaxial cable. Here

they are collated and converted into an optical form. The signals in each receiver box can be concentrated and further dispatched to a receiver building 24 for further signal processing.

[0058] The receiver building 24 is responsible for distribution of accurate time and frequency reference signals to the receivers 22 so as to facilitate their accurate positioning near each antenna array. Ideally, the number of RF Boxes 22 is readily expandable.

[0059] Turning now to Fig. 3, there is illustrated one form of signal processing train arrangement for the sampling and dispatch of signals in such an arrangement. Each antenna element e.g. 21 feeds an Rx Box 30 via a short coaxial cable 31. The received signal undergoes amplification 32, filtering 33, analog to digital conversion 34, data speed down conversion 35 (if necessary), before optical conversion 36 for transmission 37 across output optical fibre 25. The data is sent to the Receiver building (24 of Fig. 2) for backend signal processing. One signal processing train can be provided for each antenna, with multiple sensors connected to a single Receiver.

[0060] Inside each Rx Box is also a receiver optical control unit (ROCU) 42 providing receiver control, which provides timing information across all the receivers, including outputs comprising a 100MHz reference 44, a 1 pulse per second (1PPS) synchronisation signal 45 and calibration signals 46. The calibration signal is used to calibrate the array and receiver system.

[0061] The optical fiber transmission 25 provides the necessary timing signals to the ROCU module 40 and returns the sensed data 37.

[0062] The 100MHz frequency reference to each RF Box is ideally spectrally pure with low phase noise. Hence the receiver is able to use the reference as if it was the source. As described hereinafter, each of the 100MHz signals 44 is further phased locked to a reference. The 1PPS signal provides each RF box with a known time signal which allows for corrections within the receiver signal processing.

[0063] Turning now to Fig. 4, there is illustrated one form of structural arrangement of timing signals between the receiving and transmitting systems. In this arrangement, timing signals, including the 1PPS signal and 100Mhz signals, are generated by a timing system 51. They are optically converted and replicated by FRD unit 54 before being sent to split receiver back end units e.g. 55, timing optical control units 56.

[0064] A fiber distribution network 57 in turn distributes the signals to a series of shelters e.g. 52 where they are used to provide timing information for the ROCU units and the reception and conversion of signals e.g. 59. The sampling units 59 are otherwise referred to as Digital Receiver MkIV Split Receivers (sDRxIV), and will be described hereinafter.

[0065] The TOCU 56 acts to provide overall calibration and receives as inputs the 1PPS and 100MHz signals 60,62, and conditions these signals for transmission over fibre distribution system 57. The TOCU

also calibrates the length of fibre used to transmit the signals to each ROCU 58, which is located within each receiver shelter 52. In one arrangement, the single TOCU 56 drives 16 shelters 52. The TOCU distribution unit, reconstitutes the 100MHz and 1PPS signals into a format for use by the receivers and provide a phase coherent calibration signal to calibrate the receivers.

[0066] The timing system 51 produces a 1PPS output 64 which can be derived from a GPS signal monitor 68 producing 1 period per second. The 100MHz signal 68 is also produced from a Wenzel phase lock oscillator 70 to thereby produces a 100MHz reference signal 68 for distribution.

100MHz signal 60, 68

[0067] The 100MHz reference signal is forwarded to the TOCU 56 via FRD 54. The FRD outputs the 100MHz signal as a clock signal also to each of the 16 RxBE units e.g. 55.

[0068] As will be further described hereinafter, the TOCU 56 converts the input signals to optical equivalents. Fig. 5 shows the operational aspects of this conversion 70. The TOCU, squares 72 the input signal 71 and converts the signal to an optical signal via fiber transceiver 73 for transmission as a fibre output 74.

1PPS Signal 52

[0069] Fig. 6 illustrates the derivation and transmission of the 1PPS signal for transmission. The 1PPS signal can be derived from the GPS unit output either via a LVDS signal 81 or a single edge TTL signal 82, derived from the GPS unit. The source can be selectable via a mechanical switch 83. The 1PPS signal must first be modulated for fibre transmission by FPGA 84 as it generally is not suitable for transmission in a raw form. The FPGA 84, again reformats the signal for optical transmission, before it is converted to an optical signal by fiber transceiver 85 which can be on the TOCU.

[0070] Turning now to Fig. 7, there is illustrated a clocking diagram 90 for the 1PPS signal generation. A suitable modulation of the 1PPS signal 92 can be achieved by XORing the signal with a 50MHz clock 91. Whilst the 1PPS signal 92 is low, the 50MHz clock passes through the XOR gate in phase with the clock 91. Just prior to a 1PPS transition, the 50MHz clock is gated off 93. This causes the modulated 1PPS signal to stay low 95 until the 1PPS signal transitions to a high 96, at which time the modulated 1PPS also transitions to high 97. This high is then held until the 50MHz clock is gated back on 98. The gating of the 50MHz for a high transition is controlled by a high counter 99. When the counter reaches 49,999,996, it triggers the 50MHz to gate off. Two clock cycles after the 1PPS transition, the high counter is reset and the 50MHz clock is gated back on. As the 1PPS is now high, the modulated 1PPS 101 is 180 degrees out of phase with the 50MHz clock.

[0071] The trailing edge 102 of the 1PPS can be detected in a similar manner to the leading edge. Just prior to the 1PPS going low, the 50MHz clock can be gated off 103. This causes the modulated 1PPS to

stay high 104 until the 1PPS signal transitions to a low 102. This causes the modulated 1PPS also to transition to low 106. The gating of the 50MHz signal for the low transition is controlled by a low counter 100. When the counter reaches 49,999,996, it triggers the 50MHz to gate off 103. Two clock cycles after the 1PPS transition, the low counter is reset 108 and the 50MHz clock is gated back on 109. Because the 1PPS is now low, the modulated 1PPS 101 is now in phase with the 50MHz clock. In this manner, the low to high and the high to low transitions on the output fibre are related to only the input 1PPS, not the 50 or 100MHz clocks.

1PPS Initial Power Up

[0072] Turning now to Fig. 8, on power up or after a reset, the state of the 1PPS needs to be synchronised and established. The high and low counters are used 99, 100. The 50MHz clock 115 is passed through during a 1PPS transition e.g. 111, 112. When the transition is detected the high and low counters 99, 100, are reset and start their clock counts two clock cycles after the transition. During initial setup the modulated 1PPS 113 is in an unknown state.

[0073] Returning to Fig. 4, it is assumed that the TOCU control unit 54 is generally located in a first equipment room or Rx Building (24 of Fig. 2), and each of the ROCU units 58 are located within a corresponding receiver box or bunker 52.

[0074] A series of 16 distribution units e.g. 67, can be provided with each being located in a bunker or box environment for temperature stability. Interconnection is provided by an optical trunk e.g. 57, with one trunk for each optical interconnection.

[0075] On the Rx building side, the overall timing signals are provided by the TOCU 56. As noted previously, the TOCU 56 produces 1PPS output which is derived from a GPS signal monitor 68 producing a 1 period per second output signal 64. The 100MHz signal 68 is also produced via Wenzel phase lock oscillator 70 to thereby produces a 100MHz reference signal 52.

[0076] The output from master FRD 54 is also used to produce a clocking signal for the receipt of information by RxBE units 55. The TOCU 54 also provides for fibre calibration and include calibration loop output/inputs, 100MHz outputs and 1PPS signals 128 in an optical format.

[0077] Each of the optical trunk lines e.g. 61 are interconnected to a fibre patch panel 57 for distribution of optical signals, with the other receiving end also having a fiber distribution patch panel e.g. 67.

Timing Optical Control Unit 56

[0078] The Timing Optical Control (TOCU) is used to distribute timing, frequency reference and control signals to DRxIV front ends via a Receiver Optical Control Unit (ROCU). The TOCU must be

connected to a ROCU in order for the timing, frequency reference and control signals to be decoded into a format recognisable by the Digital Receiver MkIV Split Receiver (sDRxIV) system.

[0079] The TOCU generates and distributes reference timing signals for the DRxIV system. It accepts a 100MHz reference frequency input and distributes the reference frequency output over a fibre interface 16 ways. The TOCU also accepts a 1PPS input and distributes the 1PPS output over a fibre interface 16 ways. The TOCU provides a fibre control interface to the ROCU to allow control of the DRxIV front end.

[0080] The TOCU provides the capability to measure each connected fibre's propagation delay in conjunction with a ROCU to an accuracy better than 100pS. This measurement allows for timing adjustment of the DRxIV enabling delay adjustments across multiple geographically separated receivers. Communications/control with the TOCU is via 100Mbs Ethernet.

Hardware External Interface Requirements:

[0081] Fig. 9 illustrates the TOCU External Interfaces. The inputs can include:

[0082] E01 Reference Clock Input: The TOCU can have one 100MHz reference clock input.

[0083] E02 1PPS Input: The TOCU can have a LVDS 1PPS input. The TOCU can have a TTL 1PPS input.

[0084] E04 Power: The TOCU can operate from 110/240VAC.

[0085] E05 Network: The TOCU can have a network interface. The network interface can use the TCP/IP protocol. The network interface can be capable of connecting to a 10/100BaseT Ethernet Link.

[0086] E07 Reference Clock Return: The TOCU can provide sixteen (16) Reference Clock return inputs. The Reference Clock return inputs can be a single mode fibre interface

[0087] The Reference Clock inputs can use SFP LC connectors. The Reference Return inputs are shared on the same SFP transceiver and single fibre as the Reference Clock Outputs (E06)

[0088] E09 1PPS Return: The TOCU can provide sixteen (16) 1PPS return inputs. The 1PPS return inputs can be a single mode fibre interface. The 1PPS outputs can use SFP LC connectors. The 1PPS Return inputs are shared on the same SFP transceiver and single fibre as the 1PPS outputs (E08)

[0089] E11 ROCU Control Return: The TOCU can provide sixteen (16) control outputs. The ROCU Control Return can be single mode fibre interface. The ROCU Control Return can use SFP LC connectors. The ROCU Control Return inputs are shared on the same SFP transceiver and single fibre as the ROCU Control Outputs (E10)

Outputs

[0090] E06 Reference Clock Output: The TOCU can provide sixteen (16) Reference Clock outputs. The Reference Clock output can be single mode fibre interface. The Reference Clock outputs can use SFP LC connectors.

[0091] E08 1PPS Output: The TOCU can provide sixteen (16) 1PPS outputs. The 1PPS output can be single mode fibre interface. The 1PPS outputs can use SFP LC connectors.

[0092] E10 ROCU Control Output: The TOCU can provide sixteen (16) control outputs. The control output can be single mode fibre interface. The control outputs can use SFP LC connectors.

[0093] E10 Human Machine Interface (HMI): The TOCU can provide an external indication of status for internal supply voltages. The TOCU can provide external indication of the presence of the 100MHz input signal. The TOCU can provide external indication of the 1PPS input signal. The TOCU can provide external indication of control activity.

Hardware Capability Requirements

[0094] Reference Clock: The TOCU operates with a reference clock input of 100 MHz

[0095] 1PPS: The TOCU 1PPS timing input can be capable of accepting a 1 PPS signal with a pulse width of 20uS +/- 1uS. The TOCU 1PPS outputs can be time aligned to within 10nS to each other. .

[0096] Control: The TOCU control can also be via Ethernet. The TOCU can send status of the 1PPS signal and the reference clock to the network when a status request command is received. The TOCU can be capable of passing a ROCU command to the addressed ROCU when received.

Abbreviations

Abbreviation	Expansion
1PPS	1 Pulse Per Second
HFS	High Frequency Systems
HMI	Human Machine interface
HRS	Hardware Requirement Specification
ICD	Interface Control Document
LC	Lucent Connector
LVDS	Low Voltage Differential Signalling
ROCU	Receiver Optical Control
sDRxIV	Digital Receiver MkIV Split Receiver
SFP	Small Form factor Pluggable

SMA	Sub Miniature version A
TCP/IP	Transmission Control Protocol/Internet Protocol
TOCU	Timing Optical Control
TTL	Transistor Transistor Logic
UM	User Manual
VSWR	Voltage Standing Wave Ratio

1. TOCU Description

[0097] Use of a TOCU in conjunction with ROCUs is not restricted to a DRx IV split system, a monolithic DRx IV system can be connected to the ROCUs, however data sent from the receivers will require a separate controlled connection.

[0098] The TOCU generates and distributes reference timing signals for the Digital Receiver MkIV Split Receiver (sDRxIV) system. It accepts a 100MHz reference frequency input and distributes the reference frequency output over a fibre interface, 16 ways. The TOCU also accepts a 1PPS input and distributes the 1PPS output over a fibre interface, 16 ways. The TOCU finally provides a fibre control interface to allow control of downstream equipment. The fibre control interface is distributed 16 ways and each control line is individually addressable. Each TOCU fibre interface connects to a corresponding ROCU which in turn interfaces into connected sDRxIV equipment. Up to 16 ROCUs can be connected to a single TOCU. Communications/control with the TOCU is via 100Mbs Ethernet.

[0099] The TOCU is primarily used in Digital Receiver split systems where the A/D and analog front end is detached from the receivers' backend processor by fibre cable. The TOCU distributes up to sixteen sets of Reference Frequency, 1PPS and Control signals. These signals must be connected to a corresponding ROCU which in turn is connected to Drx IV split front ends.

[00100] The TOCU requires a reference clock of 100 MHz (+6 to +14dBm) and a 1PPS signal in LVDS or TTL standard. Network interface into the TOCU is via 100BaseT Ethernet.

1.1. Rear Panel Connections

[00101] Table 2 summarises the connections to the TOCU.

Table 1 – Hardware Interface Connections

Name	Description	Direction	Connector Type
X1-X16	100MHz[1]	Input/Output	LC
X17-X32	SYNC[1]	Input/Output	LC
X18-X48	CONTROL and STATUS[1]	Input/Output	LC

X49	SYNC IN TTL	Input	SMA
X50	JTAG	Input/Output	Mini IO 12 way
X51	100MHz IN	Input	SMA
X52	SYNC IN LVDS	Input	RJ45
X53	NETWORK	Input/Output	RJ45
	POWER	Input	IEC 3 Pin

[00102] Single mode Bi-Directional (BiDi) Fibre transceivers are used for all fibre communications and signal transport.

1.2. Status Indicators: The front panel includes several status indicators.

[00103] The TOCU is controlled via a network connection. Control of the TOCU is usually embedded in the Host's system software that is supplied with the higher level system. However for maintenance purposes, Simple Interface Control (SIC) software package can be used for controlling the TOCU outside of its' application environment.

[00104] Fig. 10 illustrates the front panel of a TOCU. Fig. 11 illustrates a rear panel of the TOCU.

[00105] Fig. 12 details the block diagram of the TOCU. The TOCU contains the following main components:

[00106] Control/Status PWA – Provides network control of the TOCU, sends control messages and receives status messages to/from the connected ROCUs.

[00107] Sync PWA – Modulates the sync signal (1PPS) and sends to the connected ROCUs.

[00108] Reference PWA – Sends the reference clock (100MHz) to the connected ROCUs.

[00109] Front Panel PWA – Provides status indications for the TOCU.

Control/Status PWA

[00110] The Control/Status PWA provides the following functionality:

[00111] Provides the network interface to the TOCU.

[00112] Monitors the presence of the reference clock.

[00113] Controls and monitors the Reference PWA.

[00114] Monitors the presence of the Sync signal.

[00115] Controls and monitors the Sync PWA.

[00116] Provides status indications via the front panel LEDs.

[00117] Monitors and controls the cooling fan speed.

[00118] Stores the unit's configuration in non-volatile memory.

[00119] Fig. 13 shows the block diagram of the Control/Status PWA.

1.2.1. Network

[00120] The Control/Status PWA includes an RJ-45 connector (X18) to connect the TOCU to a network. X18 is part of a Lantronix XPort device which doubles as a network to serial converter. The incoming network stream is converted to a serial stream which connects to the Altera Cyclone V FPGA. The serial stream is configured for 115kBps. The XPort device is used to receive commands and to transmit status messages to the host's controlling software. The XPort device is compatible with the TCP/IP protocol over a 10/100BaseTX Ethernet connection.

JTAG

[00121] The Control/Status PWA provides access to a Mini IO connector (X21). X21 is the JTAG interface to allow firmware uploads to the Control/Status PWA.

Control and Status

[00122] Control commands are passed over the fibre Tx/Rx to each Connected ROCU. Control signals can be destined for either the ROCU or a connected DRx. Where control of the DRx is required the command is sent to the ROCU controlling the receiver. The ROCU then forwards the command onto the applicable receiver. Status is reported back from each ROCU. Only the ROCU status is received. DRx status is usually returned through the data fibre of the receiver.

Fibre Tx/Rx

[00123] The Fibre Tx/Rx use Bi Directional (BiDi) SFP modules. There are sixteen (16) SFPs per TOCU, giving a capability of connecting up to sixteen ROCUs. Dependent upon requirements, not all SFPs are required. For example if only connection to eight (8) ROCUs is needed then only eight control status SFPs need be fitted. SFPs should always be populated from the lowest position up. The SFP modules can be removed and installed whilst the TOCU is powered.

BiDi Transceivers

[00124] Most optical transceivers utilise two fibres to transmit data between network components. One fibre is dedicated to receiving data, and the other is dedicated to *transmitting* data. A BiDi transceiver reduces the need for two fibres down to one. BiDi transceivers are fitted with Wavelength Division Multiplexing (WDM) couplers which combine and separate data travelling over a single fiber based on the light's wavelength. BiDi transceivers must be deployed in matched pairs, with their WDM couplers tuned to match the wavelength of the transmitter and receiver. An example BiDi transceiver is shown in Fig. 14.

1.2.2. Reference Clock

[00125] The Control/Status PWA receives a reference clock of 100MHz as a LVDS signal from the Reference PWA. The 100MHz input is fed into a clock select circuit. This circuit is used to detect the reference coming from the Reference PWA. If the reference clock is not present the circuit selects the

internal 100MHz xtal. With this configuration the Control/Status PWA will have a clock available to the FPGA irrespective of the state of the reference clock. This will allow communications to be maintained with the TOCU. However, the 100MHz from the xtal is not fed to the other PWAs. In this situation the TOCU will still be able to respond to commands, but not execute SYNC or Reference PWA commands, and will also broadcast a status message alerting that the reference clock is missing. All control and status reporting for the Reference PWA is handled by the Control/Status PWA.

Sync (1PPS)

[00126] The Control/Status PWA receives a 1PPS sync signal from the SYNC PWA. This signal is monitored by the FPGA. If the sync signal is missing the TOCU will broadcast a status message alerting that the sync signal is missing.

LED Control

[00127] By monitoring of the other PWAs the Control/Status PWA updates the Front Panel PWA LEDs to reflect the status of the TOCU. Table 3 provides a brief description of the function of each LED.

SYNC PWA

[00128] The SYNC PWA provides the following functionality: Modulates and distributes 1PPS over a fibre interface to connected ROCUs. Provides a reference 1PPS signal to measure time delay over the 1PPS fibre connections to the ROCUs. Selects 1PPS input standard (TTL or LDVS).

[00129] Fig. 15 shows the block diagram of the SYNC PWA.

1PPS Select

[00130] A 1 PPS time epoch is connected to the TOCU from the Site Timing Reference. The interface signal standard can be either LVDS or TTL. The signal standard is selectable by programming the TOCU.

1PPS Modulation

[00131] The 1 PPS time signal is modulated at 50MHz. This is necessary as the optical transceivers do not have the frequency response to pass a 1Hz signal. Fig. 16 describes the 1PPS modulation.

[00132] The 1PPS signal level is switched at a rate of 50MHz. A high counter counts the 50MHz high transitions and is aligned with the high transition of the 1PPS signal. When a count of 49,996 is reached the 50MHz is gated off and the 1PPS high transition is passed through. The 50MHz is then ungated two clock cycles later but out of phase and the high counter is reset.

[00133] A low counter counts the 50MHz high transitions but is aligned with the negative transition of the 1PPS signal. When a count of 49,996 is reached the 50MHz is gated off and the 1PPS low transition is passed through. The 50MHz is then ungated two clock cycles later, back in phase and the low counter is reset.

[00134] This method of modulation provides a definitive point of when the 1PPS transitions occur and is not subject to any variable timing delays through the SYNC PWA FPGA.

Reference/Returned 1PPS

[00135] The modulated 1PPS signal is fed back into the SYNC PWA FPGA. This signal is used as a reference by the TOCU to determine the time delay to the connected ROCUs via the 1PPS fibre connections. The time delay is calculated by comparing the time difference between the reference 1PPS and the returned 1PPS. The returned 1PPS is looped back through the ROCU and is measured internally by the SYNC PWA FPGA, to an accuracy of 2.5nS.

[00136] Within the FPGA a 200MHz clock is used to toggle period two (2) period counters: Counter 1 is toggled on the Low to High transition of the 200MHz clock. Counter 2 is toggled on the High to Low transition of the 200MHz clock

[00137] Both counters are triggered/reset by the TOCU Transmit 1PPS signal transitioning from Low to High. At completion of the count, both counter values are averaged together to give the propagation delay of the fibre in 2.5ns increments.

[00138] Fig. 7 previously discussed the 1PPS signal transmission arrangement, with Fig. 16 showing the 1PPS timing diagram.

JTAG

[00139] X23 is the JTAG interface to allow firmware uploads to the Sync PWA. It forms part of a JTAG chain and is connected to the Control/Status PWA. X20 is provided to allow connection and firmware programming to the Reference PWA through the same chain.

Fibre Tx/Rx

[00140] The Sync PWA fibre Tx/Rx use BiDi SFP modules. There are sixteen (16) SFPs per TOCU, giving a capability of connecting up to sixteen ROCUs. Dependent upon requirements, not all SFPs are required. For example if only connection to eight (8) ROCUs is needed then only eight control status SFPs need be fitted.

1.3. Reference (100MHz) PWA

[00141] The Reference PWA provides the following functionality: Distributes 100MHz over a fibre interface to connected ROCUs. Provides a reference 100MHz signal to measure time delay over the 100MHz fibre connections to the ROCUs.

[00142] Fig. 17 shows the block diagram of the Reference PWA.

100MHz

[00143] A 100MHz signal is connected to the TOCU from the Site Timing Reference. The interface signal standard is a sinewave between +6 to +14dBm with an output impedance of 50 ohms and is

connected via a female SMA connector. The 100MHz signal is level converted into an LVDS and LVPECL. The LVDS signal is fed to the FPGA and to a 20 way LVDS fanout buffer. Sixteen (16) are connected to the BiDi fibre transceivers for distribution to the ROCUs. Two (2) are returned to the FPGA and used as a reference. The last two (2) are distributed to the Ctrl/Status and SYNC PWA.

Reference/Returned 100MHz

[00144] The 100MHz signal is fed back into the Reference PWA FPGA. This signal is used as a reference by the TOCU to determine the phase delay of the transmitted 100MHz signal to the returned 100MHz signal from the ROCUs via the 100MHz fibre connections. Because the 1PPS fibre has had its propagation delay determined to within 2.5nS, it is assumed that the propagation delay difference between the 1PPS and Reference PWA is less than 1 reference signal wavelength. The phase delay of the 100MHz fibre cable is calculated by comparing the time difference between the reference 100MHz and the returned 100MHz. This is done using a Digital Dual Mixer Time Difference (DDMTD) circuit. The returned 100MHz is looped back through the ROCU. This is used as part of the TOCU/ROCU calibration.

Digital Dual Mixer Time Difference

[00145] A fractional Phase Locked Loop (PLL) is tuned to generate a low frequency beat signal when mixed with the transmitted and returned 100MHz signals. In the TOCU, the PLL is tuned to 99.995MHz, giving a beat frequency of 5kHz. **Fig. 18** illustrates the Mixer circuit, with **Fig. 19** showing an example corresponding timing diagram. The output of each flip flop produces a beat signal that is related to the phase of its' 100MHz input. The time difference between the leading edge of the beat signals can be used to calculate the phase difference. The time difference tbeat and hence the phase difference between the transmit and returned signals is given by: Dt = fbeat /ft x tbeat . As an example: tbeat = 10uS, ft = 100MHz, fbeat = 5kHz; Dt $= 5e^{3}/100e^{6} \times 10e^{-6}$; $= 500e^{-12}$ seconds, for a two way path (500pS).

Fibre Tx/Rx

[00146] The Reference PWA fibre Tx/Rx use BiDi SFP modules. There are sixteen (16) SFPs per TOCU, giving a capability of connecting up to sixteen ROCUs. Dependent upon requirements, not all SFPs are required. For example, if only connection to eight (8) ROCUs is needed then only eight control status SFPs need be fitted. SFPs should always be populated from the lowest position up. The SFP modules can be removed and installed whilst the TOCU is powered.

Display PWA

[00147] The Display PWA provides a visual indication of the presence of power supply voltages, the presence of a Sync and Reference (100MHz) signal. A status LED indicates if there is an issue with the TOCU and the activity between each TOCU/ROCU connection. Fig. 20 shows the block diagram of the Display PWA.

1.4. Calibration

[00148] As part of the overall calibration scheme for the TOCU and the ROCU, the skew across all reference (100MHz) fibre outputs needs to be known. The skew is stored in the TOCU registers 0x6030 through to 0x603F and is referenced to fibre O/P 1 (X1). A reference calibration should be carried out whenever a reference PWA SFP is replaced.

[00149] Fibre connections between a TOCU and multiple ROCUs can be of any length between 5m and 3km. However, the fibre connections between the 100MHz and 1PPS on any single ROCU should be the same electrical (optical) length within 0.5m. Fig. 21 illustrates an arranged interconnection.

[00150] Abbreviations

Abbreviation	Expansion
1PPS	1 Pulse Per Second
BiDi	Bi Directional
DDMTD	Digital Dual Mixer Time Difference
HFS	High Frequency Systems
HMI	Human Machine interface
HRS	Hardware Requirement Specification
ICD	Interface Control Document
LC	Lucent Connector
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signalling
Mbs	Megabits per second
MHz	Megahertz
PLL	Phase Lock Loop
PWA	Printed Wired Assembly
ROCU	Receiver Optical Control
sDRxIV	Digital Receiver MkIV Split Receiver
SFP	Small Form factor Pluggable
SIC	Simple Interface Control
SMA	Sub Miniature version A
TCP/IP	Transmission Control Protocol/Internet Protocol
TOCU	Timing Optical Control

TTL	Transistor Transistor Logic
UM	User Manual
VSWR	Voltage Standing Wave Ratio
WDM	Wavelength Division Multiplexing

2. Receiver Optical Control Unit 42

[00151] The Receiver Optical Control (ROCU) will be used to distribute timing, frequency reference and control signals to the BAE Systems Digital Receiver MkVI Split Receiver (sDRxIV) system. The ROCU will provide calibrated signals to connected receivers to allow for calibration and diagnostics across the connected receivers.

[00152] The ROCU must be connected to a Timing Optical Control Unit (TOCU) over a fibre interface in order for the timing, frequency reference and control signals to be decoded into a recognisable format. An Ethernet interface is provided for maintenance only.

[00153] The ROCU will also be used in conjunction with the TOCU to measure the connecting fibre lengths. When applied across multiple ROCUs it can be used to calibrate timing differences between ROCUs.

[00154] Fig. 22 illustrates the external interfaces of the ROCU.

General Description

[00155] The ROCU receives reference timing signals form the Timing Optical Control Unit (TOCU) and distributes these signals to the sDRxIV system. The ROCU accepts a 100MHz reference frequency via a fibre interface and redistributes the 100MHz 16 ways to the receiver front ends. The ROCU also accepts a 1PPS input via a fibre interface and redistributes the 1PPS 16 ways to the receiver front ends. The ROCU also provides a fibre control interface from the TOCU and converts to a serial interface to each receiver front end. Each serial interface control line is individually addressable. The ROCU also provides a calibration output to each receiver to permit calibration and diagnostics of the receivers.

[00156] The ROCU provides the capability to measure each connected fibre's propagation delay in conjunction with a TOCU to an accuracy of 100pS. This measurement allows for timing adjustment of the sDRxIV enabling delay adjustments across multiple geographically separated receivers.

[00157] Communications/control with the ROCU is via the fibre control interface from a TOCU. A 100Mbs Ethernet interface is provided for local maintenance activities. Power is supplied via a DRx MkIII/IV power supply unit.

2.1. Required States and Modes

[00158] The ROCU calibration input ports shall have two states, selected or not selected. When the ROCU calibration input is selected, it can be utilised by the ROCU calibration output ports via a level adjustment mechanism. When it is not selected, it is terminated in 50 ohms.

[00159] The ROCU calibration output ports have two operating states, active and inactive. The ROCU calibration output port's active state occurs when an output port is selected and is able to transmit a diagnostic or calibration signal from the selected ROCU calibration input port or internal DDS via a level adjustment mechanism. When the ROCU calibration output port is inactive, the output port is terminated with 50 ohms. The ROCU calibration output port's default state, when either powered or unpowered, is inactive.

2.2. Hardware External Interface Requirements

Inputs

E01 RF Input

[00160] The ROCU shall have a four (4) RF inputs. Two RF inputs are external connection; two RF inputs are wired internal connections Each RF input shall be selectable independent of the state of the other RF input. Each RF input shall be deselect-able independent of the state of the other RF input. Each selected RF input shall be in parallel with the other selected RF input. Selecting more than one RF input is only for specialised use. Under normal operating conditions, the controlling software is responsible for only selecting one ROCU RF input at a time. The External RF inputs shall have a VSWR less than 1.3:1 at its nominal input impedance of 50 Ohms, measured at 30MHz with none or one RF input selected.

E02 Network

[00161] The ROCU shall have a network interface. The network interface shall use the TCP/IP protocol. The network interface shall be capable of connecting to a 10/100BaseT Ethernet Link. This interface is used for maintenance only and is not used during normal operation. It is not active when a fibre connection is present.

E03 Human Machine Interface (HMI)

[00162] The ROCU shall provide an external indication of status for external supply voltages. The ROCU shall provide external indication of the presence of the 100MHz input signal. The ROCU shall provide external indication of the state of the selected RF input signals. The ROCU shall provide external indication of the 1PPS input signal.

E07 Serial Control Input

[00163] The ROCU shall have sixteen (16) Serial Control inputs. The each Serial Control input is shared on the same RJ45 as the Serial Control outputs (E06)

E09 Reference Clock Input

[00164] The ROCU shall have one reference clock input. The Reference Clock input shall be a single mode fibre connection. The Reference Clock input shall use a SFP LC fibre connector. The Reference Clock input shall use a single receive and transmit fibre connection. The Reference Return input is shared on the same SFP transceiver and single fibre.

E11 1PPS Input

[00165] The ROCU shall have one 1PPS input. The 1PPS input shall be a single mode fibre connection. The 1PPS input shall use a SFP LC fibre connector. The 1PPS input shall use a single receive and transmit fibre connection. The 1PPS Input is shared on the same SFP transceiver and single fibre.

E13 Fibre Control Input

[00166] The ROCU shall have one control input. The Control Input shall be a single mode fibre connection. The Control Input shall use a SFP LC fibre connector. The Control Input shall use a single receive and transmit fibre connection. The Fibre Control Input is shared on the same SFP transceiver and single fibre.

Outputs

E06 Serial Control Output

The ROCU shall provide sixteen (16) serial control outputs.

E08 Reference Clock Output

[00167] The ROCU shall provide sixteen (16) Reference Clock outputs. The Reference Clock output shall be at a level between +5 dBm and +8 dBm (nominally 6 dBm). The Reference shall have a VSWR less than 1.3:1 at its nominal input impedance of 50 Ohms, @ 100 MHz. The Reference Clock outputs shall use SMA female connectors.

E10 1PPS Output

[00168] The ROCU shall provide sixteen (16) LVDS compatible 1PPS outputs. All LVDS outputs shall be within +/-2 ns of each other.

E12 Fibre Control Output

[00169] The ROCU shall have one control output. The Control Output shall be a single mode fibre connection. The Control Output shall use a SFP LC fibre connector. The Control Output shall use a single receive and transmit fibre connection.

E14 Calibration RF Output

[00170] The ROCU shall provide sixteen (16) calibration outputs.

Hardware Capability Requirements

Calibration RF

[00171] The RF gain of the ROCU calibration system shall be -13dB +/-1.5dB when a 30MHz signal is selected on I/P 1 port and no internal attenuation is selected. The ROCU shall accept a CW RF input

signal no greater than 13dBm. The ROCU shall accept a Noise RF input signal no greater than 13dBm (-67dBm/Hz, 100MHz BW). The Calibration RF outputs shall have a minimum SNR of 100dB for an output level of -10dBm +/-1.5dB, no internal attenuators selected while using a 10MHz input signal. Each Calibration RF output shall be able to be set to active (selected) without affecting the state of any other ROCU RF output (short pulse switching transients excluded). Each Calibration RF output shall be able to be set to non-active (terminated) without affecting the state of any other ROCU Calibration RF output (short pulse switching transients excluded). The active Calibration RF outputs shall have a port to port amplitude delta less than 0.25dB at 20MHz. The active Calibration RF outputs shall have a port to port phase variation less than 1.5 degrees at 30MHz. The Calibration RF outputs shall have a port to port isolation greater than 100dB at 10MHz when in an inactive state. The active calibration RF outputs shall be capable of being attenuated in 0.25dB +/- 0.1dB steps up to a maximum of 71.75dB +/-1.5dB.

2.2.1. 1PPS

[00172] The ROCU shall be capable of generating a 1 PPS signal with a pulse width of 20uS +/- 5nS. The delay of the input 1 PPS signal shall be capable of being changed in increments of 10ps +/- 5ps to a maximum of 10nS.

2.2.2. Control

[00173] The ROCU shall send status of the 1PPS signal and the reference clock to the TOCU when a status request command is received. The ROCU shall store the ROCU gain calibration information into it's default flash location in an atomic operation when the correct 16-bit password is provided.

2.2.3. Serial Control

[00174] The ROCU shall provide serial control of the connected sDRxIV frontends.

2.2.4. ROCU Amplitude Calibration

[00175] The ROCU shall provide registers for sixteen (16) non-volatile programmable 16-bit words to store ROCU amplitude correction values for the calibration ports. The amplitude correction values shall be measured at 20.01MHz with no attenuation selected. The amplitude correction data shall be capable of being read from the amplitude correction registers. The amplitude correction data shall be capable of being written to the amplitude correction registers.

2.2.5. ROCU Phase Calibration

[00176] The ROCU shall provide three (3) sets of sixteen (16) non-volatile programmable 16-bit registers to store the ROCU phase correction values for the calibration ports. The phase correction values shall be measured at 10.01, 20.01 and 30.01MHz with no attenuation selected The phase correction data shall be capable of being read from the phase correction registers. The phase correction data shall be capable of being written to the phase correction registers.

3. Abbreviations

Abbreviation	Expansion
1PPS	1 Pulse Per Second
HFS	High Frequency Systems
HMI	Human Machine interface
HRS	Hardware Requirement Specification
ICD	Interface Control Document
LC	Lucent Connector
LVDS	Low Voltage Differential Signalling
Mbs	Megabits per second
MHz	Megahertz
ROCU	Receiver Optical Control
sDRxIV	Digital Receiver MkIV Split Receiver
SFP	Small Form factor Pluggable
SMA	Sub Miniature version A
TCP/IP	Transmission Control Protocol/Internet Protocol
TOCU	Timing Optical Control
TTL	Transistor Transistor Logic
UM	User Manual
VSWR	Voltage Standing Wave Ratio

[00177] The ROCU receives reference timing signals from the Timing Optical Control Unit (TOCU) and distributes these signals to Digital Receiver MkIV Split Receiver system. It accepts a 100MHz reference frequency via a fibre interface and redistributes the 100MHz; 16 ways to the split receivers. The ROCU also accepts a 1PPS input via a fibre interface and redistributes the 1PPS 16 ways to the split receivers. The ROCU also receives via a fibre interface, control from the TOCU and provides a serial interface to the split receiver system. The serial interface is distributed 16 ways and each control line is individually addressable. The ROCU also provides a RF calibration output to each receiver to permit calibration and diagnostics of the split receivers.

[00178] Communications/control with the ROCU is via the fibre control interface from a TOCU. A 100Mbs Ethernet interface is provided for local maintenance activities only. Power is supplied via a DRx MkIII/IV power supply unit.

[00179] The ROCU is used only in Digital Receiver split systems where the A/D and analog front end is detached from the receivers' backend processor by fibre cable. The ROCU distributes up to sixteen sets of Reference Frequency, 1PPS and Control signals.

[00180] The ROCU requires a TOCU to be connected and be passing valid Reference (100MHz), Sync (1PPS) and Control signals. Network interface to the ROCU is over the control fibre from the TOCU. A local control network interface is provided via a 100BaseT Ethernet connection.

[00181] Rear Panel Connections: Table 2 summarises the connections to the ROCU. Further information regarding these connections can be found in below.

Table 2 – Hardware Interface Connections

Name	Description	Direction
X22	100MHz IN[1]	Input/Output
X76	SYNC IN[1] TTL	Input/Output
X77	CONTROL and STATUS[1]	Input/Output
X78	JTAG	Input/Output
X4-X21	100MHz	Output
X23-X38	CALIBRATION	Output
X40	NOISE IN	Input
X39	I/P 1	Input
X58-X75	SYNC	Output
X42-X57	CONTROL and STATUS	Output
X79	NETWORK	Input/Output
X41	NOISE POWER	Output
X1-X2	POWER (2off)	Input

[00182] Single mode Bi-Directional (BiDi) Fibre transceivers used for all fibre communications and signal transport.

[00183] Status Indicators: The front panel includes several status indicators. The purpose of each indicator is given in the Table 3 below:

Table 3 – Status Indicators

Indicator	Colour	Description
Sync	Green	1PPS present
	Red	Clock not present or incorrect input selected

CLK	Green	Reference Clock present at correct level
	Red	Reference Clock not present or not at correct level
Status	Green	TOCU operating within selected parameters
	Red	Error condition detected. Status should be queried for fault
Noise	Green	Noise input Selected
	Not Illuminated	Noise input not selected
Aux	Green	External input selected
	Not Illuminated	External input not selected
Cal	Green	Internal calibration signal selected
	Not Illuminated	Internal calibration signal not selected
12 V	Green	Presence of 12V
5 V	Green	Presence of 5V
3.3 V	Green	Presence of 3.3V
Din	Flashing Green	Communications from the connected TOCU is being received
	Not Illuminated	No communications with connected TOCU or No TOCU connected
Dout	Flashing Green	Communications to the connected TOCU is being transmitted
	Not Illuminated	No communications with connected TOCU or No TOCU connected

Software Control

[00184] The ROCU is controlled via the Control/Status fibre connection. Control of the ROCU is usually embedded in the Host's system software that is supplied with the higher level system. However for maintenance purposes, control can be via the Ethernet port (X79) on the rear of the ROCU. A simple Interface Control (SIC) software package can be used for controlling the ROCU outside of its' application environment.

Main Components

[00185] Fig. 23 illustrates a block diagram of the ROCU. The ROCU contains the following main components:

[00186] Control/Sync PWA – Provides network control of the ROCU, sends control messages and receives status messages to/from the connected TOCU. Forwards control messages to the connected DRxIV front ends (FE). Receives the modulated 1PPS from the TOCU, demodulates and sends to connected DRxIV FEs.

[00187] Calibration PWA – Selects and/or generates the calibration signals and sends to the connected DRxIV FEs.

[00188] Reference PWA – Receives the reference clock (100MHz) from the connected TOCU and distributes to the Ctrl/Sync and Cal PWAs, and connected DRxIV FEs.

[00189] Front Panel PWA – Provides status indications for the ROCU.

Control/Status PWA

[00190] Fig 24 shows the block diagram of the Control/Sync PWA. The Control/Sync PWA provides the following functionality: Provides the network interface to the ROCU. Monitors the presence of the reference clock. Controls and monitors the Reference PWA. Demodulates and provides the Sync signal. Controls and monitors the Cal PWA. Provides status indications via the front panel LEDs. Monitors and controls the cooling fan speed. It stores the unit's configuration in non-volatile memory.

Network

[00191] The Control/Sync PWA network connection is through a fibre connection (X7) from the TOCU. All control commands and status requests are ported through this connection. The fibre transceiver is BiDirectional over a single fibre. All configuration, control and status messages pass over this connection between the TOCU and the ROCU. Configuration and control messages for all connected DRXIV FEs also pass over this connection.

[00192] DRxIV FE Control: All control commands destined for the DRxIV FEs are passed through the ROCU FPGA and forwarded to the DRxIV FEs over their own dedicated connection. Each DRxIV is individually addressable. Communications with each DRxIV is over a 3V3 serial interface.

[00193] Local Control: The Control/Sync PWA also includes an RJ-45 connector (X18) for an Ethernet connection to allow local control. This is for maintenance use only connection and is automatically disabled when an active control fibre is connected to X7. It is part of a Lantronix XPort device which doubles as a network to serial converter. The incoming network stream is converted to a serial stream which connects to the Altera Cyclone V FPGA. The serial stream is configured for 230kBps. The XPort device is used to receive commands and to transmit status messages to the host's maintenance software. The XPort device is compatible with the TCP/IP protocol over a 10/100BaseTX Ethernet connection.

JTAG

[00194] The Control/Sync PWA provides access to a Mini IO connector (X9). X9 is the JTAG interface to allow firmware uploads to the Control/Sync PWA. An internal JTAG chain is provided to allow firmware programming of the Cal PWA and Reference PWA via a JTAG chain connector (X20).

Fibre Tx/Rx

[00195] The Fibre Tx/Rx use Bi Directional (BiDi) SFP modules. There are two (2) SFPs per Control/Sync PWA. Table 4 details the uplink and downlink wavelengths used by the TOCU.

Table 4 - BiDi Wavelengths

Direction	Uplink (Tx)	Downlink (Rx)

Wavelength (nm)	1310	1490

Reference Clock

[00196] The Control/Sync PWA receives a reference clock of 100MHz as a LVDS signal from the Reference PWA. The 100MHz input is fed into a clock select circuit. This circuit is used to detect the 100MHz coming from the Reference PWA. If the reference clock is not present the circuit selects an internal 100MHz xtal. With this configuration the Control/Sync PWA will have a clock available to the FPGA irrespective of the state of the reference clock. This will allow communications to be maintained with the ROCU. However, the 100MHz from the xtal is not fed to the other PWAs. In this situation the ROCU will still be able to respond to commands, but not execute Cal or Reference PWA commands, and will also broadcast a status message alerting that the reference clock is missing. When no reference clock is available, the ROCU will not be able to supply a reference clock or 1PPS to the connected DRxIV FEs.

Sync (1PPS)

[00197] The Control/Sync PWA receives a modulated 1PPS sync signal from the TOCU. This signal is demodulated and then delayed. The delay is applied to allow adjustment over the 1PPS and 100MHz edge transitions alignment within the connected DRxIV FEs. Connection to the DRxIV FEs is LVDS standard and is via a RJ45 connector. All connected DRxIV FE 1PPS cables should to be the same electrical length to allow for calibration of the receive system.

[00198] The modulated 1PPS is also sent to the Cal (X10) and Reference PWAs (X22). If the sync signal is missing the TOCU will broadcast a status message alerting that the sync signal is missing. When no sync signal is available, the ROCU will not be able to supply a1PPS to the connected DRxIV FEs.

LED Control

[00199] By monitoring of the other PWAs the Control/Status PWA updates the Front Panel PWA LEDs to reflect the status of the ROCU.

Calibration PWA

[00200] Fig. 25 illustrates the Calibration PWA. The Calibration PWA provides the following functionality: Selects between four (4) test signal inputs (2 internal, 2 external). Provides +12V switched and TTL control for an external noise source. Provides a user definable calibration signal for calibrating the connected DRxIV FEs. Distributes the cal/test signal out to the connected DRxIV FEs. Monitors the phase of the Reference PWA's 100MHz output with the 100MHz input phase. Fig. 25 shows the block diagram of the Calibration PWA.

Test Signals

[00201] The Calibration PWA can select between four (4) test sources, 2 internal and 2 external. Cal RF, internal, generates a user controlled signal for calibration, 10MHz, internal, generated on the

Reference PWA, used for diagnostics, I/P 1, external, external signal generator can be connected on this port,

[00202] The selected test signal is attenuated via a programmable attenuator. The attenuator has a maximum attenuation of 31.75dB in 0.25dB steps. The output of the attenuator is passed through a fixed gain (15dB) amplifier. Two switchable 20dB attenuators are then used to further attenuate the test signal, if required, making the total attenuation available 71.75dB.

[00203] The test signal is then split through a series of splitters seventeen (17) ways, sixteen (16) off which are available as outputs on the back panel of the ROCU. The seventeenth output is fed to a log amp and the power is measured. The output amplitude is required as part of the receiver calibration.

[00204] All connected signals are fed into a 3dB PAD and any unselected signals are terminated into 50 ohms. The overall gain with no attenuation selected is -13dB +/-1.5dB. The maximum output signal level of the Calibration PWA is 0dBm +/- 1.5dB.

Cal RF

[00205] The Cal RF signal is generated internally by an AD9783 500MSPS DAC. The output of the DAC is tightly controlled so that the frequency, amplitude and starting phase can be determined. This allows the ability to not only calibrate the connected DRxIV FEs but also calibrate across ROCUs (array).

10MHz

[00206] The 10MHz signal is generated internally by the Reference PWA.

External I/P 1

[00207] The I/P 1 signal can be generated by attaching a signal generator or waveform generator to X17. The maximum I/P level allowed into the Calibration PWA is +13dBm.

External Noise

[00208] The noise signal can be generated by attaching a noise generator to X18. The maximum total I/P power allowed is +13dBm.

100MHz Phase Monitoring

[00209] The phase of the 100MHz output is calculated by comparing the time difference between the input 100MHz and the output 100MHz. This is done to ensure that the Phase Locked Loop (PLL) of the Reference PWA has not moved after a power reset or some other event. A Digital Dual Mixer Time Difference (DDMTD) circuit is incorporated to monitor the phase.

Digital Dual Mixer Time Difference

[00210] A fractional Phase Locked Loop (PLL) is tuned to generate a low frequency beat signal when mixed with the input and output 100MHz signals. The PLL as as previously described with reference to Fig. 18.

JTAG

[00211] X27 is the JTAG interface to allow firmware uploads to the Calibration PWA. It forms part of a JTAG chain and is connected to the Control/Sync PWA. X23 is provided to allow connection and firmware programming to the Reference PWA through the same chain.

Reference PWA

[00212] Fig. 26 shows the block diagram of the Reference PWA. The Reference PWA provides the following functionality: Receives 100MHz over a fibre interface from the connected TOCU. Distributes the 100MHz to the other PWAs in the ROCU. Uses the received 100MHz to discipline a NEL clean up oscillator. Distributes a clean 100MHz signal to the connected DRxIV FEs. Monitors the output level of the clean 100MHz signal.

100MHz

[00213] A 100MHz signal is received from the TOCU and is distributed to the Control/Sync and Calibration PWAs and to the on board FPGA. This signal is used as the main FPGA clock for all ROCU PWAs. The received 100MHz signal is also converted to a single ended CMOS signal for use by the clean-up oscillator's PLL.

Fibre Tx/Rx

[00214] The Reference PWA fibre Tx/Rx uses a BiDi SFP module.

Display PWA

[00215] The Display PWA provides a visual indication of the presence of power supply voltages, the presence of a Sync and Reference (100MHz) signal. A status LED indicates if there is an issue with the TOCU and the activity between each TOCU/ROCU connection. The Display PWA also provides a visual indication of which test signal has been selected. Fig. 27 shows the block diagram of the Display PWA.

[00216] The Display PWA contains three LEDs for displaying the status of the PSU voltages. The voltage indicators only illuminate when the ROCU is connected to a powered DRXIV PSU. The LCD display provides the following LED indications: Reference clock present, 1PPS present, TOCU Status, and Data traffic in and out per ROCU connection. 'Cal', 'Noise' or 'Aux' signal enabled. The Din and Dout indicators provide an indication that communications is active between the TOCU and the connected ROCUs. If and indicator does not flash the either no ROCU is connected or there is no communications occurring between the TOCU and ROCU.

Digital receivers

[00217] The system includes a Digital Receiver for the receipt of antenna signals. The receiver is hereinafter denoted the DRxIV. The DRxIV is a modular digital receiver designed to provide analogue signal conditioning and digital down conversion for HF radar and general applications.

[00218] The DRxIV has a modular design and is available in a range of topologies including a monolithic topology for a traditional receiver in a box solution and multiple split topologies for placing the analogue frontend of the receiver at the antenna and the digital backend of the receiver at some remote location connected by an optical link. This split receiver structure is as used in this embodiment. The split topologies are suitable for a receiver per element phased array system employing digital beamforming.

DRxIV Specifications

[00219] The specifications for the DRxIV are divided into the following five sub sections: Analogue Front End (AFE) Specifications. Analogue to Digital Conversion (ADC) Specifications. Digital Down Conversion (DDC) Specifications. Interface Specifications. Operational Specifications.

AFE General Specifications

[00220] Where a specification is frequency dependant, unless otherwise stated, the specification is verified at 14.401 MHz and designed for the operational frequency range.

Label	Description	MIN	TYP	MAX	Units
F	Operational frequency (Note 1)	7.5	-	35	MHz
F_RIP	AFE bypass ripple in operational frequency (Note 1)	-	-	2.5	dB
NF	Noise figure with 0 dB attenuation (Note 2)	-	8	10	dB
G	Analogue gain with 0 dB attenuation (Note 2)	39.5	40	40.5	dBm
O3IP	Output third order intercept point	50	-	-	dBm
Pmax	Input maximum power with 0 dB attenuation	-	-	6	dBm
RF_Zin	RF port input impedance	-	50	-	Ω
RF_VSWR	RF port voltage standing wave ratio	-	-	1.35:1	-
CAL_Zin	Calibration port input impedance	-	50	-	Ω
CAL_VSWR	Calibration port voltage standing wave ratio	-	-	1.2:1	-
CAL_ISO	Calibration port relay isolation (Note 3)	55	-	-	dB
CAL_CPL	Calibration port coupling isolation (Note 3)	-	29.7	-	dB
ATT	Variable attenuation range (Note 4)	-	62	-	dB
ΔATT	Variable attenuation incremental resolution (Note 4)	-	0.25	-	dB

Label	Description	MIN	TYP	MAX	Units
$\Delta\varphi$	Phase coherency between separate AFE's (Note 5)	-	5	-	degrees
$\varphi(t)$	Phase noise at 1Hz offset (Note 5)	100	-	-	dB
HPF	Number of controllable high pass preselection filters (Note 1)	-	3	-	-
LPF	Number of controllable low pass preselection filters (Note 1)	-	3	-	-

Table 5: AFE General Specifications

[00221] The Operational frequency filters are fixed. Total ripple over the operational frequency is will all preselection filters in bypass. It is derived by finding the maximum value and subtracting the minimum value in the pass band. The calibration input port is reverse coupled to the RF input with 20dB of isolation and 0.3 dB of insertion loss via a fixed 10 dB attenuator. The RF input can be switched via a controllable relay to a 50 Ω load with > 55 dB of isolation.

[00222] Variable attenuation is switched with a resolution of 1dB for automatic and firmware level control. However, 0.25dB resolution is available with manual control. Attenuation resolution has ± 0.2dB + 2% tolerance. During manufacture the attenuation actual measured 1 dB switched values are stored in an on board EEPROM and are available from the receiver control interface. Phase coherency is by design. Phase noise is measured using the DRxIV ADC and DDC and is indicative of the total receiver phase noise including the AFE.

3.1.1. AFE Filters Specifications

[00223] All AFE filter specifications are customisable on request. The values here are the default only. All high pass filters are specified at the maximum cut off frequency and may be up to 400 kHz lower. All low pass filters are specified at the minimum cut off frequency and may be up to 400 kHz higher. That is, passbands have a 400 kHz tolerance for extension at either end.

[00224] All selectable HPF and LPF can be bypassed by programmable control. The actual insertion loss for each preselection filter and bypass is 0.2 and this this is factored into the gain specification.

Label	Description	MIN	TYP	MAX	Units
HPF0_1dB	Fixed input high pass filter 1dB corner point	-	-	8	MHz
HPF0_ATT	Fixed input high pass filter stop band at 3 MHz	50	-	-	dB
HPF0_R	Fixed input high pass filter passband ripple	-	-	1	dB

Label	Description	MIN	TYP	MAX	Units
HPF0_R100	Fixed input high pass filter passband ripple in 100 kHz	-	-	0.01	dB
LPF0_1dB	Fixed input low pass filter 1dB corner point	35	-	-	MHz
LPF0_ATT	Fixed input low pass filter stop band at 41.5 MHz	50	-	-	dB
LPF0_R	Fixed input low pass filter passband ripple	-	-	1	dB
LPF0_R100	Fixed input low pass filter passband ripple in 100 kHz	-	-	0.01	dB
HPF1_1dB	Selectable high pass filter 1 1dB corner point	-	-	11.4	MHz
HPF1_ATT	Selectable high pass filter 1 stop band at 8.4 MHz	50	-	-	dB
HPF1_R	Selectable high pass filter 1 passband ripple	-	-	1	dB
HPF1_R100	Selectable high pass filter 1 passband ripple in 100 kHz	-	-	0.01	dB
HPF2_1dB	Selectable high pass filter 2 1dB corner point	-	-	15.8	MHz
HPF2_ATT	Selectable high pass filter 2 stop band at 12 MHz	50	-	-	dB
HPF2_R	Selectable high pass filter 2 passband ripple	-	-	1	dB
HPF2_R100	Selectable high pass filter 2 passband ripple in 100 kHz	-	-	0.01	dB
HPF3_1dB	Selectable high pass filter 3 1dB corner point	-	-	23.0	MHz
HPF3_ATT	Selectable high pass filter 3 stop band at 17.3 MHz	50	-	-	dB
HPF3_R	Selectable high pass filter 3 passband ripple	-	-	1	dB
HPF3_R100	Selectable high pass filter 3 passband ripple in 100 kHz	-	-	0.01	dB
LPF1_1dB	Selectable low pass filter 1 1dB corner point	11.9	-	-	MHz
LPF1_ATT	Selectable low pass filter 1 stop band at 16.3 MHz	50	-	-	dB
LPF1_R	Selectable low pass filter 1 passband ripple	-	-	1	dB
LPF1_R100	Selectable low pass filter 1 passband ripple in 100 kHz	-	-	0.01	dB

Label	Description	MIN	TYP	MAX	Units
LPF2_1dB	Selectable low pass filter 2 1dB corner point	17.0	-	-	MHz
LPF2_ATT	Selectable low pass filter 2 stop band at 23.5 MHz	50	-	-	dB
LPF2_R	Selectable low pass filter 2 passband ripple	-	-	1	dB
LPF2_R100	Selectable low pass filter 2 passband ripple in 100 kHz	-	-	0.01	dB
LPF3_1dB	Selectable low pass filter 3 1dB corner point	24.3	-	-	MHz
LPF3_ATT	Selectable low pass filter 3 stop band at 33 MHz	50	-	-	dB
LPF3_R	Selectable low pass filter 3 passband ripple	-	-	1	dB
LPF3_R100	Selectable low pass filter 3 passband ripple	-	-	0.01	dB

Table 6: AFE Filters Specifications

[00225] Ripple is the maximum value minus the minimum value between the specified cut off frequency and the maximum operational frequency for a high pass filter and the minimum operational frequency for a low pass filter. For the 100 kHz specification it is for any 100 kHz bin within the band described.

3.2. Analogue to Digital Converter Specifications

[00226] The ADC specifications cover both the ADC performance and the anti-aliasing filter at the input to the ADC. The low pass anti-alias filter is specified at the minimum cut off frequency and may be up to 400 kHz higher. That is, pass band has a 400 kHz tolerance for extension.

[00227] Where a specification is frequency dependant, unless otherwise stated, the specification is verified at 14.401 MHz and designed for the operational frequency range. Where applicable ADC performance specifications assume the input clock is at the maximum level.

No.	Label	Description	MIN	TYP	MAX	Units
2.1.1	Fs	ADC sample rate	-	100	-	MHz
2.1.2	ADC_RES	ADC resolution	-	16	-	bits
2.1.3	ADC_DR	ADC dynamic range	157	-	-	dB
2.1.4	ADC_OL	ADC overload point	-	13.27	-	dB
2.1.5	ADC_SFDR	ADC spurious free dynamic range	105	-	-	dB

No.	Label	Description	MIN	TYP	MAX	Units
2.1.6	CLK_Zin	ADC clock input impedance	-	50	-	Ω
2.1.7	CLK_VSWR	ADC clock input voltage standing wave ratio	-	-	2:1	-
2.1.8	CLK_MAX	ADC clock input power	-8	-	6	dBm
2.1.9	AAF_1dB	Anti-Alias high 1 dB corner point	44.5	-	-	MHz
2.1.10	AAF_ATT	Anti-Alias low stop band attenuation at 57 MHz	47	-	-	dB
2.1.11	AAF_R100	Anti-Alias passband ripple	-	-	1	dB
2.1.12	AAF_R100	Anti-Alias passband ripple in 100 kHz	-	-	0.01	dB

[00228] Table 7: ADC Specifications

[00229] The ADC requires a low phase noise reference clock. Input frequency must be 100 MHz, correct firmware operation is not guaranteed for other input frequencies. For convenience; ADC noise floor, ADC_FLOOR > ADC_OL – ADC_DR > -143.73 dB/Hz. ADC Noise **Figure** above thermal, ADC_NF = 174 + ADC_FLOOR = 30.27 dB. ADC_SFDR from second harmonic and higher. The minimum input clock for a split eight way system backend is 1 dBm, to accommodate the eight way clock splitter.

[00230] Ripple is the maximum value minus the minimum value between the specified cut off frequency and the minimum operation frequency. For the 100 kHz specification it is for any 100 kHz bin within the band described.

Digital Down Converter Specifications

[00231] The DDC specifications are split into general specifications, narrowband specifications, wideband specifications and synchronisation specifications.

DDC General Specifications

No.	Label	Description	MIN	TYP	MAX	Units
3.1.1	NNB	Number of narrowband channels	-	10	-	-
3.1.2	NWB	Number of wideband channels	-	1	-	-
3.1.3	NADC	Number or raw ADC channels	-	1	-	-
3.1.4	DDC_IPR	All channels independently programmable, all registers	-	YES	-	-

No.	Label	Description	MIN	TYP	MAX	Units
3.1.5	DDC_CUR	All channels can operate concurrently (Notes 1, 2)	-	YES	-	-
3.1.6	DDC_SYN	All channels sync to a common trigger source (Note 3)	-	YES	-	-

Table 8: DDC General Specifications

[00232] All narrowband and wideband channels can operate concurrently outputting at the highest rate of 10 * 2.54 MB/s + 50 MB/s = 75.4 MB/s on the 117 MB/s Gigabit link. The ADC channel alone can saturate the link at 200 MB/s but can run concurrently provided the link capacity is not exceeded, by collecting a specific number of samples with an inter dwell. Each DDC has an individual separate Numerically Controlled Oscillator (NCO). All channels can be independently delayed with respect to the common sync source.

DC Narrowband Specifications

No.	Label	Description	MIN	TYP	MAX	Units
3.2.1	NB_SR	Narrowband minimum selectable sample rate	10	-	316.46	kS/s
3.2.2	NB_BW	Narrowband minimum usable bandwidth	7.74	-	244	kHz
3.2.3	NB_ATT	Narrowband FIR stop band attenuation	195	-	-	dB
3.2.4	NB_FIRR	Narrowband FIR processing resolution	-	32	-	bits
3.2.5	NB_IQR	Narrowband output I and Q resolution	-	32	-	bits
3.2.6	NB_NCOR	Narrowband NCO resolution	-	64	-	bits
3.2.7	NB_FR	Narrowband tune frequency resolution	5.5	-	-	pHz
3.2.8	NB_PR	Narrowband start phase resolution	0.4e-18	-	-	radians
3.2.9	NB_SW	Narrowband sweep rate	0.542	-	4.9e12	Hz/s
3.2.10	NB_SWR	Narrowband NCO sweep resolution	-	64	-	bits
3.2.11	NB_SWerr	Narrowband sweep error	-	-	100	mHz

Table 9: DDC Narrowband Specifications

[00233] The selectable sample rate is defined by a programmable decimation. Usable bandwidth is 0.774 * NB_SR. ADC_DR 157 dB. Firmware level control (FLC) requires a further 32 dB from FIR. NB_ATT > ADC_DR + 32 dB = 189 dB. NB_FIRR and NB_IQR provide 194 dB > 189 dB. NB_FR = Fs / 2NB_NCOR and NB_SR = 2π / 2NB_NCOR. The sweep rate is programmable by a 64 bit register

which sets the value of an extra accumulator in the NCO. By entering values above 263 into this register the NCO will alias and sweep down. See ICD for more. Sweep error is specified at the maximum operational bandwidth of F_max – F_min = 27 MHz, with a sweep rate of 100 kHz/s.

3.2.1. DDC Wideband Specifications

No.	Label	Description	MIN	TYP	MAX	Units
3.3.1	WB_SR	Wideband minimum selectable sample rate	316.46	-	12500	kS/s
3.3.2	WB_BW	Wideband minimum usable bandwidth	250	-	10000	kHz
3.3.3	WB_ATT	Wideband FIR stop band attenuation	100	-	-	dB
3.3.4	WB_FIRR	Wideband FIR processing resolution	-	33	-	bits
3.3.5	WB_IQR	Wideband output I and Q resolution	-	16	-	bits
3.3.6	WB_NCOR	Wideband NCO resolution	-	64	-	bits
3.2.7	WB_FR	Wideband tune frequency resolution	5.5	-	-	pHz
3.2.8	WB_PR	Wideband start phase resolution	0.4e-18	-	-	radians
3.2.9	WB_SW	Wideband minimum rate	0.542	-	4.9e12	Hz/s
3.3.10	WB_SWR	Wideband NCO sweep resolution	-	64	-	bits
3.3.11	WB_SWerr	Wideband sweep error	-	-	100	mHz

Table 10: DDC Wideband Specifications

[00234] The selectable sample rate is defined by a programmable decimation. Usable bandwidth is 0.8 * WB_SR. WB_ATT limits out of band spur suppression, but not in band dynamic range which can process the full ADC_DR, as afforded by WB_FIRR. WB_IQR limit does not impact processing gain.

DDC Synchronization Specifications

No.	Label	Description	MIN	TYP	MAX	Units
3.4.1	SYNC_DTR	DDC synchronisation delay time resolution (Note 1)	-	10	-	ns
3.4.2	SYNC_DTM	DDC synchronisation programmable delay time maximum (Note 2)	-	-	> 1	year
3.4.4	SYNC_CTM	DDC synchronisation programmable cycle time maximum (Note 2)	-	-	> 1	year
3.4.3	SYNC_CTR	DDC synchronisation programmable cycle time resolution (Note 1)	-	10	-	ns

No.	Label	Description	MIN	TYP	MAX	Units
3.4.5	SYNC_DW	DDC synchronisation dwell counter (Note 3)	-	YES	-	-
3.4.6	SYNC_SP	DDC synchronisation sample counter (Note 3)	-	YES	-	-
3.4.7	SYNC_SN	DDC number of sync (Note 4)	-	1	-	-

Table 11: DDC Synchronisation Specifications

[00235] **NOTE 1:** Each DDC is independently programmable with a delay start from a common synchronisation source and a repetitive cycle start. The delay and cycle counters are 64 bit and increment at the ADC sample rate allowing alignment to a specific ADC sample.

[00236] NOTE 2: The delay and cycle counters being 64 bit incrementing at 10 ns will wrap after an effectively infinite period (>5800 years).

[00237] NOTE 3: Synchronisation can be independently programmed for each DDC to cycle (dwell) once a given number of samples are collected, and to stop cycling after a given number of dwells.

[00238] NOTE 4: In a split topology there is one sync source input at the backend, and another at the front end. The frontend sync source is sample aligned on the optical link. Either source can be used however the front end should be used if synchronous level control is required. In a monolithic topology only one sync source, at the receiver, is available.

Interface Specifications

[00239] The DRxIV full set of controllable features and interfacing details can be found in the ICD. The following describes the communications ports physical specifications.

No.	Label	Description	MAX	TYP	MIN	Units
4.1.1	ETH_PHY	Ethernet physical layer interface	-	IEEE 802.3	-	-
4.1.2	ETH_P1	Protocol for sample collection, status and control	-	TCP/IP	-	-
4.1.3	ETH_P2	Protocol for enumeration and soft reset	-	UDP/IP	-	-
4.1.4	ETH_P3	Protocol for ping	-	ARP/ICMP	-	-
4.1.5	SER_PHY	Split topology frontend serial interface protocol.	-	UART	-	-
4.1.6	SER_VCC	Serial (UART and External IO) signal voltage level	-	3.3	-	V

No.	Label	Description	MAX	TYP	MIN	Units
4.1.7	SER_BAUD	UART baud rate	-	115200	-	baud
4.1.8	SER_BITS	UART data bits	-	8	-	bits
4.1.9	SER_PAR	UART serial parity	-	None	-	-
4.1.10	SER_STOP	UART stop bits	-	1	-	bits
4.1.11	SER_FLOW	UART flow control	-	None	-	-
4.1.12	OF_SPEED	Split topology optical link speed	-	3.125	-	Gb/s
4.1.13	OF_PMA	Split topology optical link physical media attachment	-	SFP+	-	-
4.1.14	OF_DIR	Split topology optical link uni or bi directional (Note 1)	-	YES	-	-
4.1.15	OF_DAISY	Split topology supports daisy chaining (Note 2)	-	YES	-	-

Table 12: Control Interface Specifications

[00240] NOTE 1: By default the split topology receiver uses unidirectional link to pass raw ADC samples, synchronisation and status from the frontend to the backend. It is intended that the frontend be controlled via the UART interface in this mode. If a backend to frontend optical link is used in a split topology, once the fibre is physically connected the backend SFP+ the Tx path must be manually enabled at the backend on power up.

[00241] NOTE 2: Daisy chaining allows a single frontend data stream to be input to one backend and then be looped back out of the backend and input into another backed, thereby providing an extension of the number of DDCs available limited only by the number of backbend's. This provides a mechanism for a full spectral processing if required.

Operational Specifications

[00242] The following specifications provide additional hardware information.

No.	Label	Description	MIN	TYP	MAX	Units
5.1.1	DDR_SIZE	DDR2 memory on board the backend (Note 1)	-	2048		MB
5.1.2	DDR_AV	DDR2 memory available (Note 1)	-	1792		MB
5.1.3	POW_M	Monolithic receiver power (Note 2)	-	-	40	W
5.1.4	POW_FE	Split frontend power (Note 2)	-	-	20	W

No.	Label	Description	MIN	TYP	MAX	Units
5.1.5	POW_BE	Split standalone backend power (Note 2)	-	-	20	W
5.1.6	POW_8BE	Split 8 way backend system power (Note 2)	-	-	200	W
5.1.7	OT	Minimum operating temperature (Note 3)	-10	-	60	Degrees C
5.1.8	ST	Minimum storage temperature (Note 3)	-40	-	100	Degrees C
5.1.9	WET_min	Minimum operational relative humidity (Note 3)	0	-	95	%
5.1.10	SIZE_M	Size of a monolithic receiver (Note 4)	-	0.5		RU
5.1.11	SIZE_FE	Size of a split frontend (Note 4)	-	0.5		RU
5.1.12	SIZE_BE	Size of a split standalone backend (Note 4)	-	0.5		RU
5.1.13	SIZE_8BE	Size of split eight way backend system (Note 4)	-	4		RU

Table 13: Operational Specifications

[00243] NOTE 1: 2 GB of memory is physically attached to the board. By default all of it is being used by firmware for a TCP/IP buffer to prevent sample loss in the event of heavy network back pressure. (See ICD, unlike TCP/IP between computers with disk storage the DRxIV must provide real time samples, and if the host is unavailable for transfer the buffer will eventually roll over). However only 256 MB is required by the TCP/IP buffer for normal network traffic loads and on request firmware variants are available that use this memory for ADC sample delay buffering. At 200MB/s ADC sample rate, 1792 MB provides 8.96 s of delay.

[00244] NOTE 2: See the section on topologies, not all components are needed for all systems.

4. Physical Description

Topologies Models and Options

[00245] The DRxIV is available in a number of different topologies and models and with different options. With respect to topologies the DRxIV is available in either a monolithic topology or a split topology. When in a split topology the DRxIV is available as either a standalone split model or an eight way system split model. Whilst the embodiment utilise a split topology, the single monolithic topology is also described for illustrative purpose. Finally the DRxIV can be manufactured with custom analogue signal conditioning with respect to controllable preselection and fixed input bandpass filtering as required.

4.1.1. Split Topology

[00246] In the split topology, the DRxIV is provided with the digital backend in one form factor and the analogue signal conditioning and analogue to digital conversion in another form factor separated by an optical link, as depicted in **Fig. 28 and Fig. 29**.

[00247] When in a split topology the DRxIV can be set to run in a unidirectional mode or bidirectional mode. This is depicted in **Fig. 28 and Fig. 29** by the dashed line for the backend Tx to frontend Rx optical link.

4.1.1.1. Unidirectional Mode

[00248] In unidirectional mode only the frontend Tx to backend Rx optical fibre needs to be connected. This is the default mode for the receiver on power up. In this mode the frontend must be controlled via a separate Universal Asynchronous Receive and Transmit (UART) interface.

4.1.1.2. Bidirectional Mode

[00249] In Bidirectional Mode both the frontend Tx and backend Rx and the backend Tx and frontend Rx optical fibres must be connected. On power up the receiver must be manually controlled to be put in this mode. In this mode both the frontend and backend can be controlled by the backend Ethernet interface, additionally the frontend can still be controlled via the UART interface.

4.1.2. Stand Alone Model

[00250] The DRxIV in spit topology is available in a standalone model. This model of split DRxIV has a half RU frontend and a half RU backend, as depicted in **Fig. 28**.

4.1.3. Eight Way System Model

[00251] The DRxIV in split topology is available in an eight way system model. This model of split DRxIV has eight individual half RU frontends and one 4 RU backend containing eight backend modules. The eight backend modules behave as eight individual standalone backend receivers. The 4 RU backend chassis contains a common power supply and clock splitter for the eight modules. The split eight way system is depicted in **Fig. 29**.

4.1.4. Internal Oscillator Option

[00252] The DRxIV monolithic, split frontend, split backend and split backend eight way system can be provided with an internal oscillator for development purposes, so that an external oscillator is not required. If the monolithic or split frontend is provided with an internal oscillator then the Auxiliary Daughter Board (AUD) option is not available. If the internal oscillator option is used the clock input becomes a clock output from the oscillator.

4.1.5. Auxiliary Daughter Board Option

[00253] The DRxIV monolithic and split frontend can be provided with an AUD for additional analogue signal conditioning, which can be plumbed at the front of the RF chain prior to the DRxIV analogue signal conditioning. A number of control lines are available for custom control of the auxiliary daughter board.

Boards and Structure

[00254] Depending on the levels of integration, the DRxIV can include a number of individual Printed Circuit Boards (PCB's). These PCB's provide the main functionality for the DRxIV and include:

[00255] Back End Receiver (BER) board

[00256] Analogue to Digital Converter (ADC) board

[00257] Analogue Front End (AFE) board

[00258] Parallel to Optical (P2O) board

[00259] Optical to Parallel (O2P) board

[00260] Auxiliary Daughter (AUD) board (optional)

[00261] Back Front Panel (BFP) board

[00262] Front Front Panel (FFP) board

[00263] Chassis Front Panel (CFP) board

[00264] Standalone DC Distribution (SDC) board

[00265] Chassis DC Distribution (CDC) board

[00266] Fig. 30 illustrates the arrangement of boards on the split front end DRxIV structure for front end A/D conversion, sampling and transmission.

[00267] Fig. 31 illustrates the split standalone backend DRxIV structure, with Fig. 32 illustrating the split eight way system backend DRxIV structure used to provide multiple backend processing.

[00268] The PCB revision and component build variant for each of these boards, with exception of the SDF and CDF boards, is available from the on board EEPROM's on the BER board, P2O board and O2P board.

4.1.5.1. BER Board

[00269] The BER board is in a monolithic receiver or the backend of a split receiver. It takes ADC digital samples as inputs and provides the main receiver operations of baseband mixing, decimation and FIR filtering. The BER also contains an on board EEPROM for storing system information and provides 786 bytes of user definable storage.

4.1.5.2. ADC Board

[00270] The ADC board connects to the BER board in a monolithic receiver and the P2O board in a split receiver. It provides the ADC functionality, clock conditioning and an input RF anti-aliasing filter.

4.1.5.3. AFE Board

[00271] The AFE board exists in the frontend of a split receiver. It connects RF to the ADC board. The AFE board has an antenna RF input that passes through a first stage bandpass filter, a multistage amplifier chain, three selectable high pass filters, three selectable low pass filters and two variable attenuators.

[00272] With respect to the attenuators attenuator B is located closer to the ADC input and should be used first. Attenuator A is located closer to the RF input and should be used last as it adds directly to the noise figure of the receiver. Additionally, the AFE has a calibration input which is reverse coupled into the RF input with a 29.7 dB insertion loss. If required, the RF input can be relay switch to a 50 ohm load providing 55 dB of isolation to calibration input.

4.1.5.4. P2O Board

[00273] The P2O board exists only in the frontend of a split receiver. The main function of the P2O board is to encode the ADC samples from the ADC board and to transmit them on the 3.125Gb/s optical link to the backend synchronised with a frontend 1PPS sync pulse.

[00274] Additionally, the P2O board provides a UART interface a 1 PPS sync pulse interface, fan control and multiplexes register status data onto the frontend to backend optical link and receives and decodes register control data from the backend to frontend optical link.

[00275] The P2O board provides AFE control and front panel LED control for a split receiver. The P2O also contains an on board EEPROM for storing system information and provides 786 bytes of user definable storage.

4.1.5.5. O2P Board

[00276] The O2P board exists in the backend of a split receiver. The main function of the O2P board is to decode ADC samples from the frontend and provided samples to the BER board in such a way that it emulates an interface to the ADC board.

[00277] Additionally, the O2P board encodes register control data for the backend to frontend optical link and register status data from the frontend to backend optical link. It also provides the bidirectional / unidirectional control and the daisy chaining function. The O2P also contains an on board EEPROM for storing system information and provides 786 bytes of user definable storage.

4.1.5.6. BFP Board

[00278] There are two types of BFP boards. The first type is provided with a split standalone backend. This type has an LCD screen containing receiver information and a number of LEDs. The other type is provided with the split eight way system and provides LED indicators regarding receiver operation and the optical link status for each of the eight receiver modules and an LED indication of the power rails.

4.1.5.7. FFP Board

[00279] The FFP board is provided with the split frontend and provides LED indicators for the power rails and receiver operations.

4.1.5.8. SDC and CDC Boards

[00280] Provide DC power filtering and distribution as well as fan drive.

[00281] Fig. 30 to Fig. 32 show how these boards are arranged in a split frontend, a split standalone backend and an eight way system.

4.2. Interfacing

[00282] The following section describes the physical connections to the DRxIV, the connection descriptions and a description of the front panel and LED's.

4.2.1. External Connections

[00283] The following Tables 10 to 14 describe the connectors to the DRxIV for the various topologies and models.

4.2.1.1. Split Frontend Connections

Name	Description	Direction	Type
X01	RF Input	I	SMA 50 ohm
X02	DC Power Input	I	Lemo 2B 12 Pin
X03	UART Interface	I / O	DB9
X04	JTAG Interface	I/O	AVX 9257 12 Way
X05	100 MHz Clock	I / (O if optional OSC)	SMA 50 ohm
X06	1 PPS Sync Pulse	I	RJ 45
X07	Optical Interface SFP+	I / O	SC
X08	RF Calibration	I	SMA 50 ohm

Table 14 : Split Frontend Connections

4.2.1.2. Split Standalone Backend Connections

Name	Description	Direction	Type
X01	Optical Interface SFP+	I / O	SC
X02	DC Power Input	I	Lemo 2B 12 Pin
X03	External Interface	I	DB9

X04	JTAG Interface	I/O	AVX 9257 12 Way
X05	100 MHz Clock	I / (O if optional OSC)	SMA 50 ohm
X06	1 PPS Sync Pulse	I	RJ 45
X07	Ethernet Interface	I / O	RJ 45
X08	RF Calibration	I	SMA 50 ohm

Table 15 : Split Standalone Backend Connections

4.2.1.3. Split Eight Way System Backend Rx Module Connections

Name	Description	Direction	Type
X01	JTAG Interface	I/O	AVX 9257 12 Way
X02	Optical Interface SFP+	I / O	SC
X03	1 PPS Sync Pulse	I	RJ 45
X04	Ethernet Interface	I / O	RJ 45

Table 16 : Split Eight Way System Backend Rx Module Connections

4.2.1.4. Split Eight Way System Backend Power and Clock Module Connections

Name	Description	Direction	Type
X01	100 MHz Clock	I / (O if optional OSC)	SMA 50 ohm
X02	AC Power Input	I	IEC

Table 17 : Split Eight Way System Backend Rx Module Connections

4.2.1.5. External Interface

[00284] The External interface provides a programmable mechanism by which the DRxIV can be used to detect signals from and provide signals to external equipment. Each pin is programmable as either an input or output and can be read or written to.

4.2.1.6. UART Interface

For the split front end the external interface is used for the UART interface. JTAG Interface

The JTAG interface is used for programming firmware and on chip debugging of FPGA's.

4.2.1.7. 100 MHz Clock

The DRxIV requires a 50 ohm low phase noise input clock.

4.2.1.8. Ethernet Interface

The Ethernet interface uses a standard 802.11 Gigabit cable.

4.2.1.9. Optical Interface

[00285] The optical interface uses by default a standard SFP+ optical transceiver with a 1310nm wavelength capable of 3.125 Gb/s over 10 km. The transceiver is accessible for the frontend and standalone backend. For the eight way system backend the top cover must be removed to access the transceivers.

[00286] Alternate SFP+ transceivers can be used if required. If SFP transceivers are used the SFP+ diagnostics EEPROM values will not be available.

4.2.1.10. Calibration Input

[00287] The calibration input is to the AFE board uses 50 ohm SMA connector.

4.2.1.11. Split Standalone Backend Front Panel

[00288] The split standalone backend front panel has an LCD screen and six LED indicators. The LCD screen provides the receiver MAC and serial number and the state of the Ethernet connection when the receiver is not enumerated. Once enumerated the LCD with show the channel set up and state of the attenuators and preselection filters.

Split Backend Reset Button

[00289] The reset button on the rear of a standalone backend or a module from the eight way system receiver will cause all firmware in the BER board FPGA to be dropped and the firmware to be reloaded from an on board configuration device, essentially mimicking a power cycle to the BER board, without actually powering down the other hardware. As the BER board does its start-up initialisation it will make no change to the O2P board, which will retain its programmed optical configuration. Neither will this reset have any effect on the frontend.

Split Frontend Reset Button

[00290] The reset button on the rear of a frontend will cause all firmware in the P2O board FPGA to be dropped and the firmware to be reloaded from an on board configuration device, essentially mimicking a power cycle to the P2O board, without actually powering down the other hardware. As the P2O board does its start-up initialisation it will overwrite all settings in the AFE board to their default state. A frontend reset will have no effect on the backend.

5. Functional Description

[00291] The primary functions of the DRxIV include: The analogue signal conditioning of the HF RF input; Analogue to digital conversion of the conditioned signal; The digital mixing, decimation and filtering of the digital samples and the output of the resultant I and Q values. Sample synchronisation.

[00292] The additional functions provided by the DRxIV include: Level control with Firmware Level Control FLC and Automatic Level Control ALC. Split system optical bi directional and uni directional

control and status and optical daisy chaining. EEPROM stored scale factors, attenuation calibration values, and user data storage. ADC max hold reporting. Fan and temperature control.

5.1. Analogue Signal Conditioning

[00293] Fig. 33 shows a block diagram of one form of the DRxIV AFE. The first stage is the input bandpass filter. This is followed by variable attenuator A and an input low noise amplifier. There are three individually selectable high pass filters and three individually selectable low pass filters separated by another low noise amplifier. Each filter bank can be bypassed. Note that the switching is by solid state RF switches and not relays. Finally, there is variable attenuator B and a high linearity amplifier. With respect to the attenuators, variable attenuator B, closest to the output should be used first as attenuator A, closest to the input adds directly to the noise figure.

[00294] The attenuators can be controllable in 1 dB steps using individual registers for backwards compatibility however there are an additional two registers for controlling the attenuators with a 0.25 dB resolution. Also, the EEPROM on the AFE contains the actual recorded calibrated attenuation values each 1 dB step.

5.2. Analogue to Digital Conversion

[00295] **Fig. 34** provides a block diagram of the DRxIV ADC. The RF signal from the AFE is first low pass filtered by the anti-alias filter then converted to digital samples which are output to the BER board.

5.3. Digital Down Conversion

[00296] The DRxIV has 10 narrowband channels, one wideband channel and one raw ADC channel. The raw ADC channel can be sample synchronised in the same way as the narrowband and wideband channels, but provides no signal processing and raw ADC samples are output.

5.3.1. Narrowband Digital Down Conversion

[00297] The DRxIV has ten narrowband channels which can be independently tuned and synchronised. The narrowband channels have a variable decimation between of between 316 and 10000 and a usable bandwidth of 77.4%.

[00298] Fig. 35 shows a block diagram of the narrowband Digital Down Converter (DDC). The ADC samples are digitally mixed with a synthesised 64 bit local oscillator and decimated using a Cascade Integrator Comb (CIC) filter. The samples are digitally scaled to accommodate for the variable CIC gain with decimation to maintain a flat response.

[00299] Following the CIC filter are two Finite Impulse Response (FIR) filters. The FIR filters have default tap coefficients, however the FIR filters in each narrowband channel can be individually programmed with custom FIR tap coefficients.

[00300] If using custom tap coefficients note that the group delay must be altered to accommodate the change. Also the custom tap coefficients are volatile.

5.3.2. Wideband Digital Down Conversion

[00301] The DRxIV has one wideband channel which can be independently synchronised. The wideband channel has a decimation of between 8 and 316 and a usable bandwidth of 80%.

[00302] Fig. 36 shows a block diagram of the wideband DDC. Unlike the narrowband channels it does not support custom tap coefficients and has only one FIR filter.

5.4. Sample Synchronisation

[00303] The DRxIV accepts as an input an LVDS 1PPS synchronisation pulse. For a split receiver there are two inputs one at the frontend and one at the backend. The frontend 1PPS is placed on the frontend to backend optical link synchronised with the ADC sample for which it occurred at the frontend. The DDC channels require the backend or frontend 1PPS be manually selected for synchronisation. While a split DRxIV does support a backend synchronisation 1 PPS being used it is not recommend as it there is no synchronisation for the level control, FLC and ALC algorithms.

[00304] With respect to sample synchronisation for the ALC and FLC algorithms, the synchronisation 1PPS is not selectable, as the level control algorithms exist either in the frontend for a split receiver and only one 1PPS is available.

5.5. Level Control

[00305] The DRxIV provides two different automatic level control methods. A legacy traditional Automatic Level Control (ALC) and a Firmware Level Control (FLC).

[00306] As there is only once set of attenuators and so only one of the automatic level control methods can be used at a time. If one method is enabled while the other is already enabled, the already enabled method is automatically disabled.

[00307] In addition to the provided automatic level control methods, the DRxIV can be used with manual level control and the analogue signal condition section of this document.

[00308] ALC and FLC block diagrams are in Fig. 37 and Fig. 38 for comparison.

5.5.1. Automatic Level Control

[00309] ALC is the traditional legacy method of level control, provided for backwards compatibility. The ALC uses the full 64 dB of attenuation in 1 dB increments. ALC can be programmed to start at any time with respect to the 1PPS and to reoccur with a periodic cycle time.

[00310] The ALC algorithm takes multiple measurements of input ADC power and adjusts the attenuation to maintain a given headroom below ADC overload.

[00311] If an ALC cycle is run while collecting samples, the collection will be corrupted as the attenuation will be switched during the sample gather. Since gathers may be asynchronous to a predefined ALC cycle time an asynchronous ALC inhibit is provided to prevent attenuation switching should it be required. If an ALC is inhibited there will be no ALC until the next cycle time or manual enable.

5.5.2. Firmware Level Control FLC

[00312] FLC is a method of level control that can be operated while gathering samples with almost no sample impact during attenuation switching. Essentially the ADC samples are digitally scaled in firmware in at a precise time with respect to the attenuation switching so that the output IQ level is indicative of true input power, with the AFE gain taken into account.

[00313] Owing to the alignment between the switch and the scale, the speed of the switch, the fact that the DDC averages all impacted ADC samples into one down converted sample and that much of the impact is outside of the passband of the DDC FIR, the attenuation change is almost undetectable in a high purity test environment. Furthermore, in a noisy external environment the attenuation change is undetectable and beneath the background noise.

[00314] The effect of operating with FLC is that the output IQ is scaled to the input power of the receiver before the AFE and represents true input power. The IQ output being 32 bits has a dynamic range of 194dB. The ADC dynamic range is approximately 158 dB and the FLC attenuation variation is 32 dB so the total range required of the IQ is 190.

[00315] FLC does not increase the ADC sensitivity of the receiver and the total ADC dynamic range moves within the range afforded by the IQ output. However, it does allow the receiver to be operated for long continuous periods in a shifting external HF environment with asynchronous interferes with a very low ADC overload headroom. The FLC headroom is programmable and by default it is 10 dB, however FLC can be run for long periods with a headroom as low as 2 dB.

[00316] In order to synchronise the impact of FLC over a receiver per element system, headroom measurement and necessary attenuation switching occurs aligned with the 1PPS. Furthermore, the attenuation switch occurs in only 1dB steps either up or down.

[00317] In order to provide better scale factors for FLC the 1dB attenuation steps for the AFE are calibrated. In a split receiver topology, it is important that after a backend reset (or re-enumeration) that the frontend calibration values be manually read or that the automatic ‘tell’ time be set to a low enough value that the values are automatically updated.

[00318] The FLC only uses the attenuator B 32 dB of variation. While FLC is in operation the front attenuator A can be manually controlled, to deafen the DRxIV in high external noise environments. If this

option is used, the effect of the attenuation is not digitally scaled in FLC and must be manually accommodated for. Also, the effect of the attenuator A adds directly to the receiver noise figure.

5.6. Split System Optical Link

[00319] The split DRxIV optical link has a number of features not apparent in an ordinary packet based optical link. The DRxIV optical link uses a protocol that operates differently in each direction. The optical link can be operated in a unidirectional or bidirectional mode, or can be used to daisy chain one frontend to multiple backend's. Owing to the modular design of the split system there are some reset implications regarding the use of the optical link. In addition to the optical control registers there are a number of optical status registers for diagnosing optical faults.

5.6.1. Frontend to Backend Optical Link

[00320] The frontend to backend optical link is the main link required for operation. The frontend to backend is not packet based but is a stream of ADC samples with sample aligned meta data for 1 PPS and FLC synchronisation as well as sample synchronisation and a multiplexed frontend register status addresses and data.

[00321] There are two status bits for the frontend to backend optical link. One to indicate that the optical fibre from frontend to backend is physically attached, and a second to indicate that sample synchronisation has occurred. These are on the front panel LED indicators, in the Ethernet application layer packet headers and available from register reads. Additionally, if either the link or synchronisation is lost, an alarm containing the register read values will be output on the Ethernet interface once every 500 ms until the matter is resolved. By default, the split DRxIV operates in a unidirectional from frontend to backend mode only.

5.6.2. Backend to Frontend Optical Link

[00322] The backend to frontend optical link when enabled provides the function of sending register control address and data from the backend to the frontend allowing the split receiver to be controlled entirely from the backend Ethernet interface.

5.6.3. Uni Directional / Bi Directional Control and Status

[00323] The split DRxIV has an Ethernet interface at the backend and a UART interface at the frontend. Register writes at either end go onto a common control bus, and register reads from either end go onto a common status bus.

[00324] As shown in Fig. 39, the control bus at the backend bus is encoded and put onto the backend to frontend optical link, and the status bus at the frontend is encoded and multiplexed onto the frontend to backend optical link along with the samples and other metadata.

[00325] In this way when operated in bi directional mode the whole receiver can be controlled from the backend Ethernet interface, however the frontend can still be controlled from the UART interface and frontend register status reads are available at both the backend Ethernet interface and the frontend UART interface.

[00326] When operated in uni directional mode the backend Ethernet interface is used to control the backend and UART interface must be used to control the frontend. In either case register status reads at the frontend are available at both ends.

5.6.4. Tell Registers

[00327] There are some register values that are are needed at the backend for proper operation, such as the attenuation calibration values for correct FLC scaling and the FLC status as well as hardware variants for convenience and values required for the LCD screen in a split standalone model.

[00328] These register values are automatically put onto the status bus once a second and transmitted to the backend and are known as Tell Registers.

[00329] The Tell time is set to 1 second by default because if the backend is reset it needs to be updated with the values from the frontend on next enumeration. The constant data on the status bus can be suppressed by setting the tell time to a maximum of 11 minutes. Changing the tell time will cause a tell to occur immediately on write. As care must be taken to ensure the backend is updated on re enumeration, if the tell is to be suppressed it can be done so by writing the largest possible time to the tell register once on enumeration.

5.6.5. Optical Daisy Chaining

[00330] Fig. 40 depicts optical daisy chaining. A single frontend can be used to feed samples to multiple backend's, by putting each backend into a daisy chain mode. If being used for daisy chaining and the frontend is to be controlled in a bi directional manner it is the last backend in the chain that is used to control the frontend. While any number of standalone or eight way chassis modules can be included in the chain, if just one eight way chassis is used such that all modules are linked by daisy chaining then there are in total 80 narrowband channels available to collect samples across the spectrum.

5.6.6. Split System Reset Considerations

[00331] For a monolithic DRxIV a receiver TCP disconnect or BER receiver board UDP reset (or push button reset) will put the BER board into a reset state and the AFE board will be overwritten with default power up values, as described in the section on reset buttons. For a split receiver these things will only reset the BER board. The O2P board and frontend will be unaffected, so as to preserve the programmed optical settings for direction and daisy chaining. Therefore, it is important to manually overwrite the AFE values to their required default state on re enumeration of the DRxIV.

5.7. EEPROM Chain

[00332] The Split DRxIV has four EEPROM's one on the BER board, one on the O2P board, one on the P2O board and a final one on the AFE board.

5.7.1. AFE EEPROM

[00333] The AFE EEPROM operates independently and differently from the three EEPROM's on the digital boards. The AFE EEPROM contains the following information: AFE Gain; AFE Attenuation Calibration Values; AFE Hardware Variant and AUD Hardware Variant.

[00334] The content of the AFE EEPROM is designed to be local to that particular board, and the AUD board to which it is connected. In this way the entire analogue chain from a split frontend chain be moved to a new form factor and can retain its configuration.

5.7.2. Digital Boards EEPROM's

[00335] Each of the three EEPROMs on the digital boards is 1024 bytes in size and is byte addressable. The top 256 bytes in each EEPROM are reserved for factory set system information. The lower 768 bytes are available to user definable data. The location of system information with the EEPROM chain of the three digital boards is intended to follow the form factor containing the hardware for which the information is intended. Each EEPROM can be independently written to with any user definable data, and with respect to the BER user definable data this is output with the enumeration request packet.

5.7.2.1. Split Receiver BER board EEPROM System Information

[00336] For the split DRxIV the BER board contains all system information pertaining to the backend apart from what is contained in the AFE EEPROM and the O2P hardware variant. As the ADC board is in the frontend for a split receiver this information is no carried in the BER board EEPROM, however the ADC board information are in 'Tell Registers' and are available at the backend of a split receiver after the first Tell update. This includes: Ethernet MAC Number; System Hardware Variant; BER Hardware Variant; BFP Hardware Variant; ADC Channel Digital Scale Factor; Wideband Channel Digital Scale Factor; and Narrowband Channel Digital Scale Factor

5.7.2.2. Split Receiver O2P board EEPROM System Information

[00337] The only system information contained in the O2P EEPROM is the O2P board hardware variant.

5.7.2.3. Split Receiver P2O board EEPROM System Information

[00338] The P2O board EEPROM contains all frontend system information that is not contained in the AFE. This includes: Frontend Serial Number; ADC Hardware Variant; ADC Board Analogue Scale Factor; P2O Hardware Variant and FFP Hardware Variant.

5.7.3. EEPROM's Programming

[00339] On reset all values from all EEPROMs are read and stored in internal volatile RAM and registers. When updated over the Ethernet or UART interface using the respective register addresses only the volatile values are updated. With the exception of the AFE EEPROM, to write to the EEPROM system information all hardware variants are updated across all digital board EEPROM's on batch, all scale factors are updated across all digital board EEPROM's on batch and all identification MAC and frontend serial information is updated across all digital board's on batch. If in bi directional optical mode this provides transparent programming across all digital boards. If in uni directional optical mode due respect must be paid to where the EEPROM values are stored. All AFE EEPROM writes are done on batch separately, including analogue boards hardware variants however optical uni / bi directional mode must still be observed.

6. Abbreviations

Abbreviation	Expansion
ADC	Analogue to Digital Converter
AUD	Auxiliary Daughter Board
DDC	Digital Down Converter
IDC	Interface Control Document
LED	Light Emitting Diode
NB	Narrowband
RU	Rack Unit
UART	Universal Asynchronous Receive and Transmit
WB	Wideband

Interpretation

[00340] Reference throughout this specification to "one embodiment", "some embodiments" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment", "in some embodiments" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments.

[00341] As used herein, unless otherwise specified the use of the ordinal adjectives "first", "second", "third", etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

[00342] In the claims below and the description herein, any one of the terms comprising, comprised of or which comprises is an open term that means including at least the elements/features that follow, but not excluding others. Thus, the term comprising, when used in the claims, should not be interpreted as being limitative to the means or elements or steps listed thereafter. For example, the scope of the expression a device comprising A and B should not be limited to devices consisting only of elements A and B. Any one of the terms including or which includes or that includes as used herein is also an open term that also means including at least the elements/features that follow the term, but not excluding others. Thus, including is synonymous with and means comprising.

[00343] As used herein, the term “exemplary” is used in the sense of providing examples, as opposed to indicating quality. That is, an “exemplary embodiment” is an embodiment provided as an example, as opposed to necessarily being an embodiment of exemplary quality.

[00344] It should be appreciated that in the above description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the Detailed Description are hereby expressly incorporated into this Detailed Description, with each claim standing on its own as a separate embodiment of this invention.

[00345] Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the invention, and form different embodiments, as would be understood by those skilled in the art. For example, in the following claims, any of the claimed embodiments can be used in any combination.

[00346] Furthermore, some of the embodiments are described herein as a method or combination of elements of a method that can be implemented by a processor of a computer system or by other means of carrying out the function. Thus, a processor with the necessary instructions for carrying out such a method or element of a method forms a means for carrying out the method or element of a method. Furthermore,

an element described herein of an apparatus embodiment is an example of a means for carrying out the function performed by the element for the purpose of carrying out the invention.

[00347] In the description provided herein, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

[00348] Similarly, it is to be noticed that the term coupled, when used in the claims, should not be interpreted as being limited to direct connections only. The terms "coupled" and "connected," along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Thus, the scope of the expression a device A coupled to a device B should not be limited to devices or systems wherein an output of device A is directly connected to an input of device B. It means that there exists a path between an output of A and an input of B which may be a path including other devices or means. "Coupled" may mean that two or more elements are either in direct physical or electrical contact, or that two or more elements are not in direct contact with each other but yet still co-operate or interact with each other.

[00349] Thus, while there has been described what are believed to be the preferred embodiments of the invention, those skilled in the art will recognize that other and further modifications may be made thereto without departing from the spirit of the invention, and it is intended to claim all such changes and modifications as falling within the scope of the invention. For example, any formulas given above are merely representative of procedures that may be used. Functionality may be added or deleted from the block diagrams and operations may be interchanged among functional blocks. Steps may be added or deleted to methods described within the scope of the present invention.

CLAIMS:

1. A method of determining the optical delay of an optical waveguide, the method including the steps of:

(a) transmitting a first periodic modulated optical signal along the optical waveguide with a first modulation frequency;

(b) determining a phase inverted copy of the periodic modulated signal;

(c) simultaneously transmitting the phase inverted copy of the periodic modulated signal along the optical waveguide;

(d) processing the output of the optical waveguide to determine a beat frequency between the transmitted signals; and

(e) utilising the beat frequency to determine a distance measure from a transmitter to a receiver end of the optical waveguide.

2. A method as claimed in claim 1 further comprising determining the propagation delay across the optical waveguide from the beat frequency.

3. A method as claimed in claim 1 wherein the optical waveguide comprises an optical fibre connecting a geographically separated receiver and transmitter.

4. A method as claimed in any previous claim wherein said first periodic modulated optical signal comprises a sinusoidal or clocked waveform.

5. A method of determining a distance of transmission of an optical signal over an optical waveguide link, the method including the steps of:

(a) transmitting a correlated forward and return modulated optical signal over the optical waveguide link;

(b) determining a beat frequency of the interference of the two signals; and

(c) utilising the beat frequency to determine a corresponding distance measurement of the transmitted signal.

6. A method as claimed in claim 5 wherein said forward and return signals comprise either a sinusoidal or binary clock signal.

7. A method as claimed in claim 6 wherein said forward and return modulating optical signals are inverted copies of one another.

8. A signal receiver for receiving a series of antenna input signals from a series of antennas, the receiver including:

a receiver optical control unit, receiving optical timing signals, including optical clocking signal, optical time interval signals and optical control signals; the receiver optical control unit:

converting the optical clocking signal into a corresponding electrical sampling signal for antenna signal sampling;

converting the optical time interval signal into a corresponding electrical time interval signal for controlling the sampling time period;

converting said optical control signals into corresponding electrical control signals including a calibration signal, providing sampling delay information for sampling of the antenna signals;

at least one signal sampling unit for sampling and filtering the antenna input signal, and converting them to a corresponding digital optical signal, the signal sampling unit utilising:

an antenna input signal for sampling an antenna signal;

the electrical time interval signal for controlling the sampling frequency;

the calibration signal for controlling a sampling delay for delaying the output of the sampled antenna signal;

the signal sampling unit sampling the antenna signal and outputting an optical data sampled signal and the sampling frequency.

9. A signal receiver as claimed in claim 8 wherein the optical clocking signal is also utilised to develop a receive optical control unit clocking signal.

10. A signal receiver as claimed in claim 8 wherein said electrical time interval signal includes a 1 period per second timing signal.

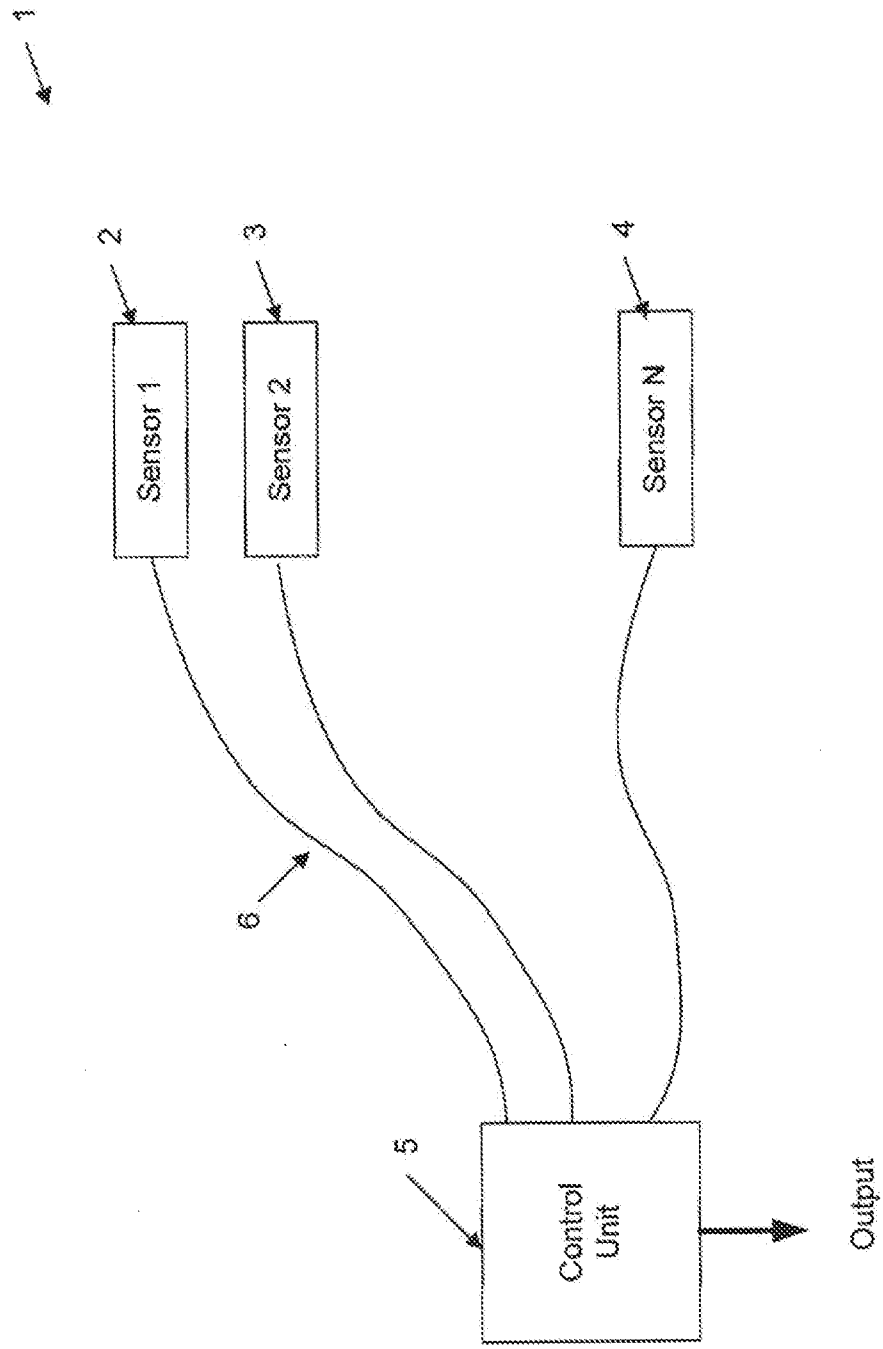


Fig. 1

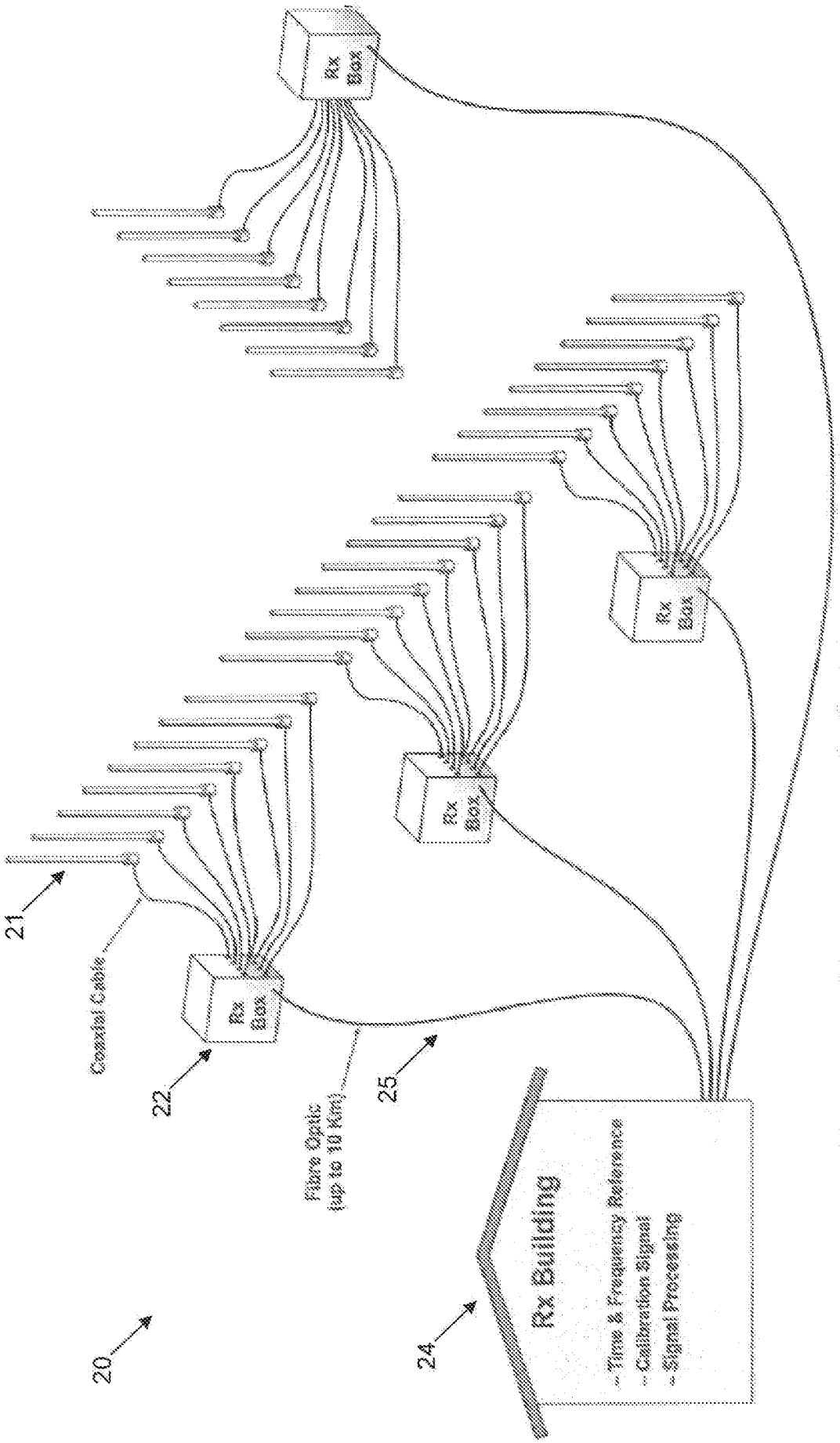

Rx Box
Rx Box
Rx Box
Rx Box
21
Coaxial Cable
22
Fibre Optic (up to 10 Km)
25
Rx Building
- Time & Frequency Reference
- Calibration Signal
- Signal Processing
24
20

Fig. 2

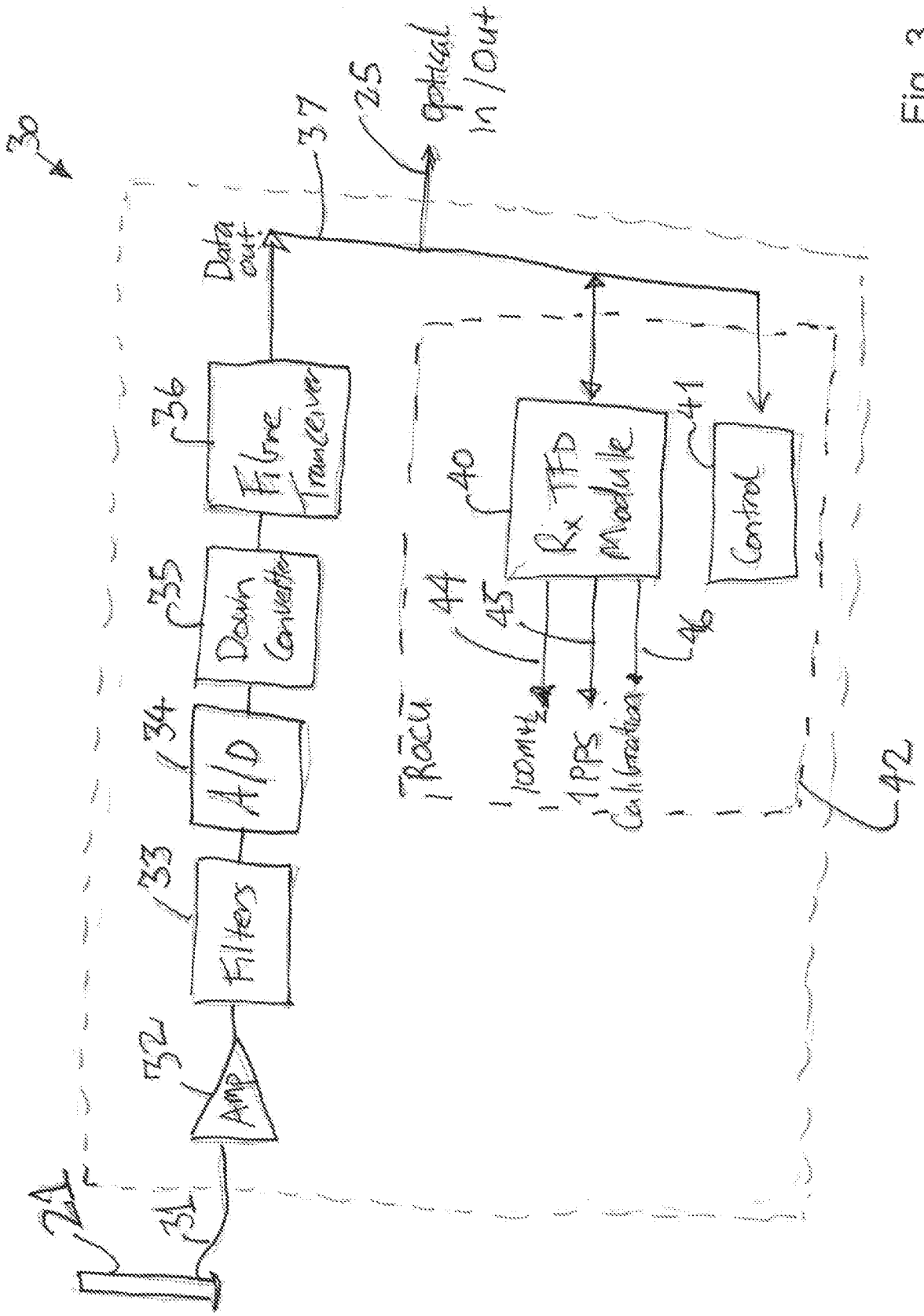
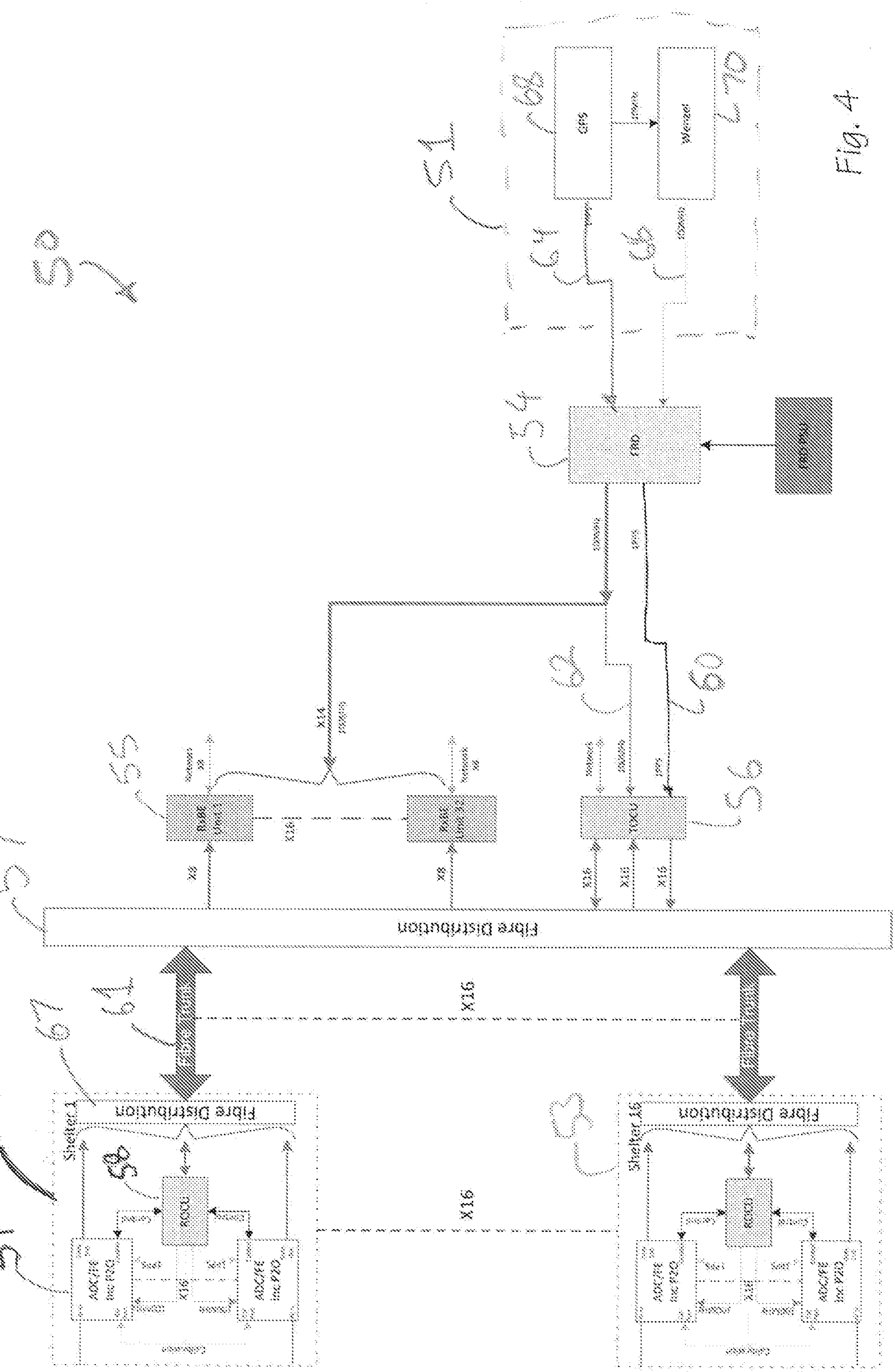

30
37
25
optical in/out
Data out
36
Fibre Transceiver
35
Down Converter
34
A/D
33
Filters
32
AMP
24
31
RACU
40
Rx TFD Module
41
Control
44
45
46
42
10MHz
1PPS
Calibration

Fig. 3


Fibre Distribution
Fibre Distribution
Fibre Distribution
Shelter 1
Shelter 16
X16
X16
50
51
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58
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62
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66
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68
70

Fig. 4

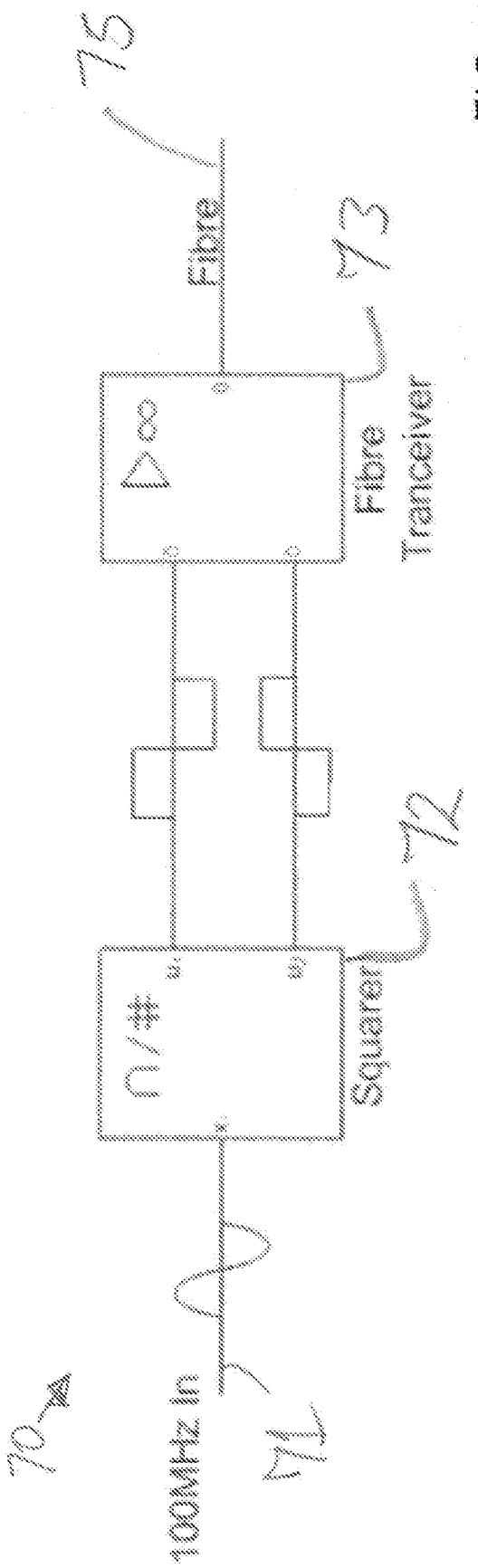

70
100MHz In
71
n/#
Squarer
72
Fibre Tranceiver
73
Fibre
75

FIG. 5

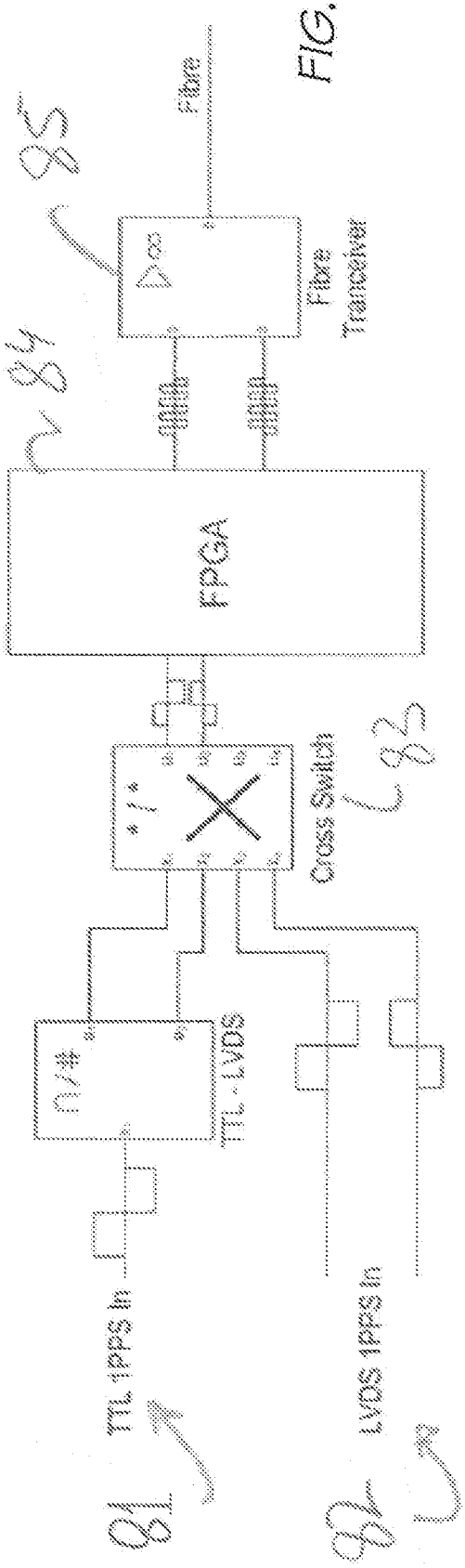

81
TTL 1PPS In
LVDS 1PPS In
91
n/#
TTL - LVDS
Cross Switch
82
FPGA
84
Fibre Tranceiver
85
Fibre

FIG. 6

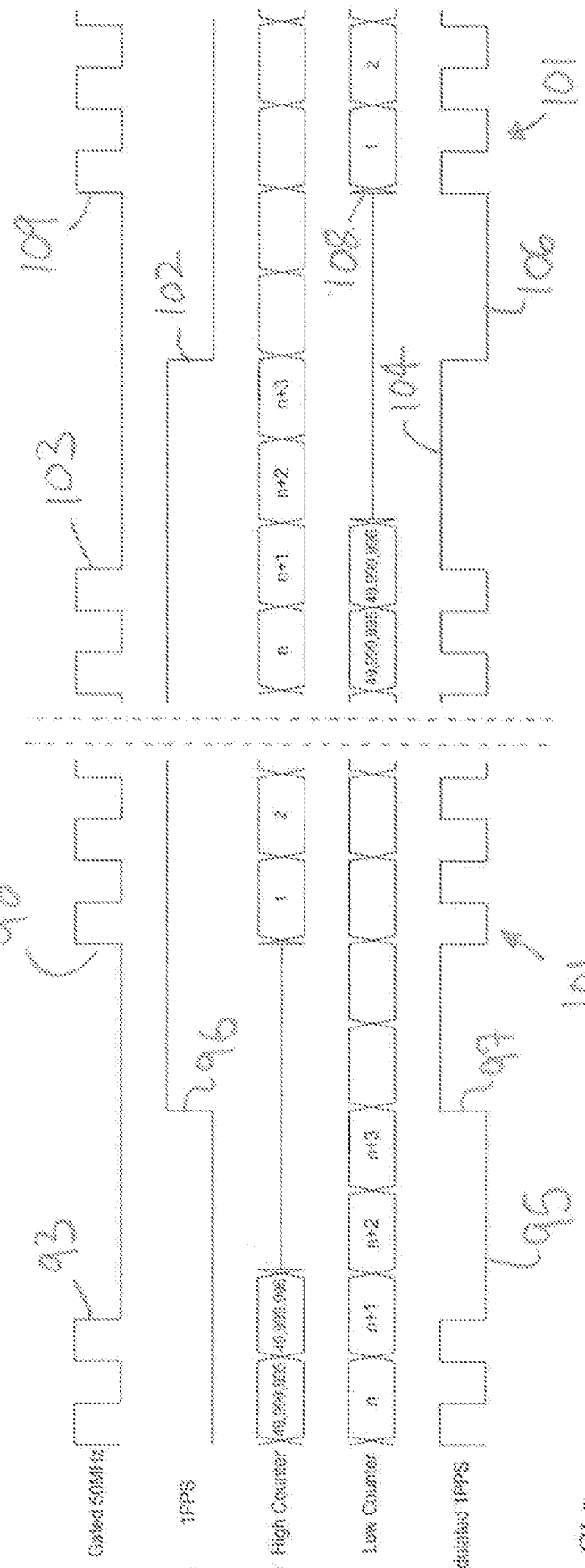

Gated 50MHz
1PPS
High Counter
Low Counter
Modulated 1PPS
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
n
n+1
n+2
n+3
1
2

FIG. 7

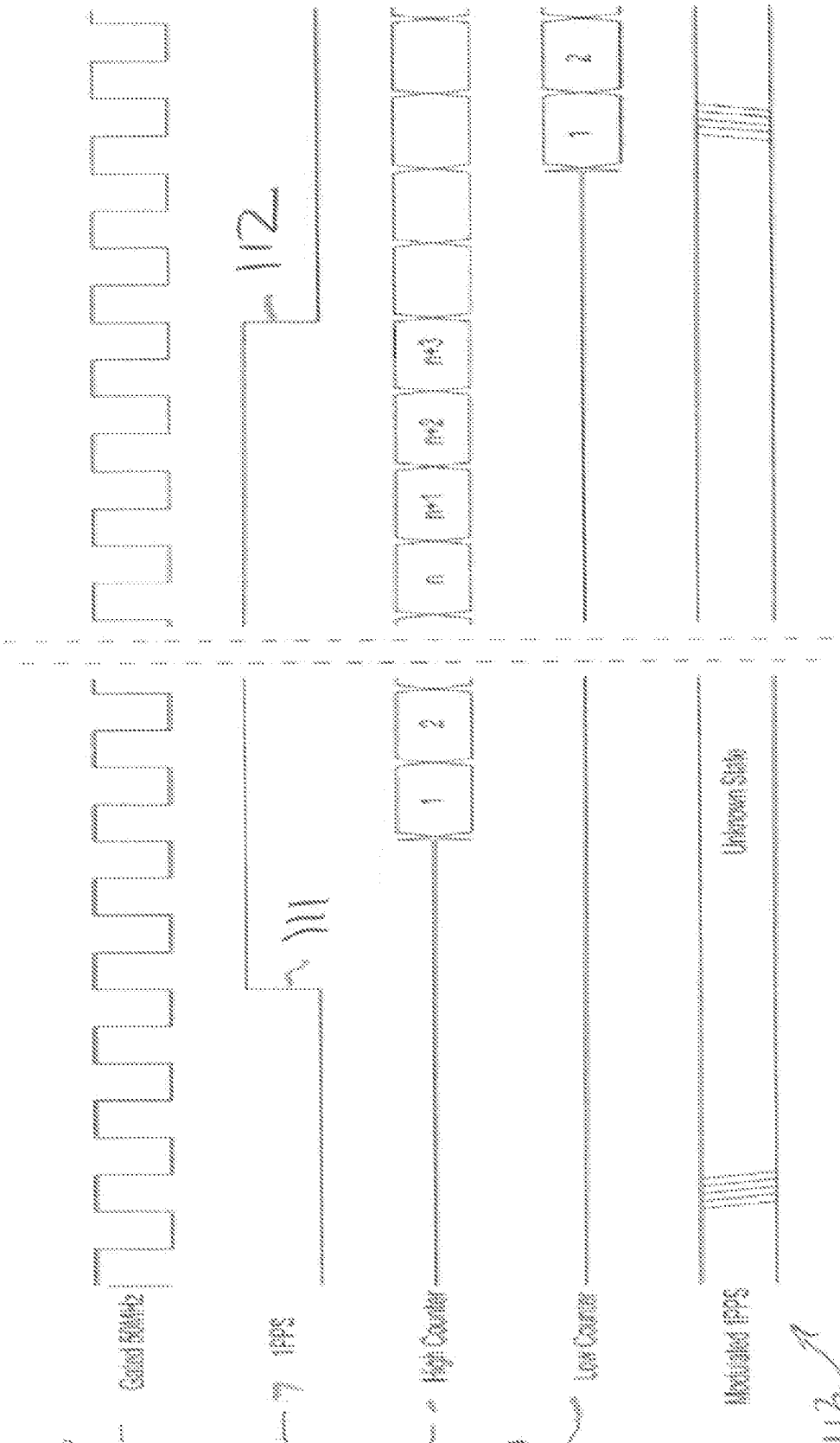

116
Gated 80MHz
114
PPS
112
111
99
High Quality
100
Low Quality
Unknown State
Monitored PPS
110

FIG. 8

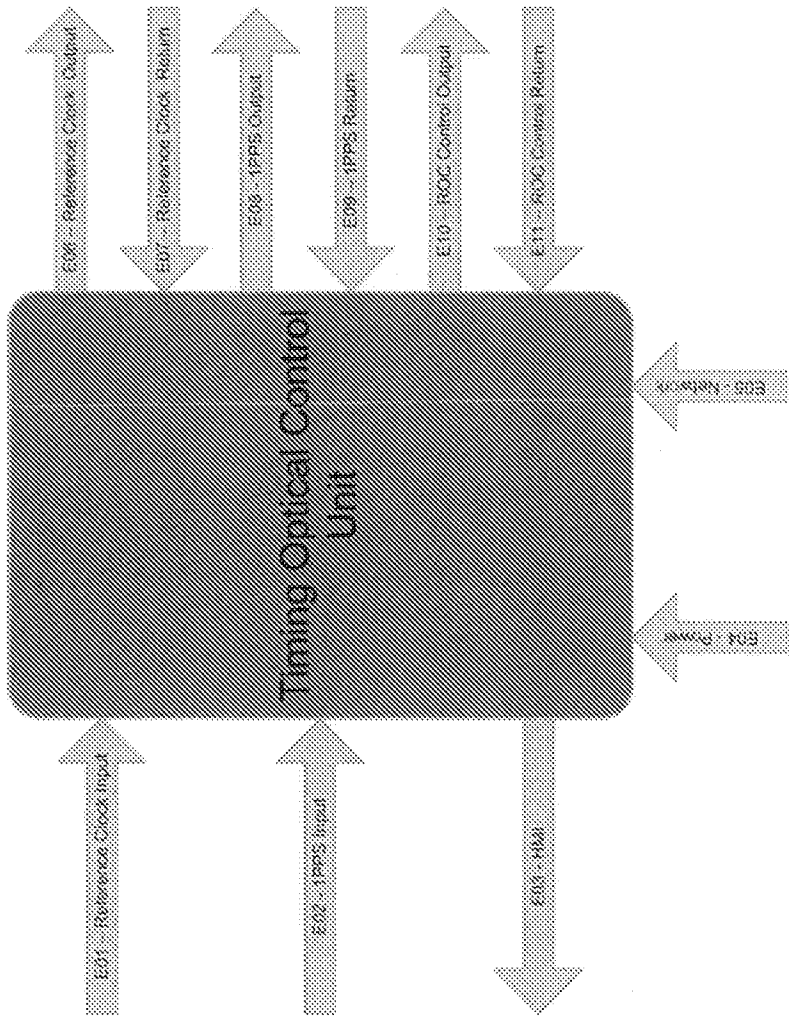

Timing Optical Control Unit
E06 - Reference Clock Output
E07 - Reference Clock Return
E08 - 1PPS Output
E09 - 1PPS Return
E10 - ROC Control Output
E11 - ROC Control Return
E01 - Reference Clock Input
E02 - 1PPS Input
E05 - HMI

FIG. 9

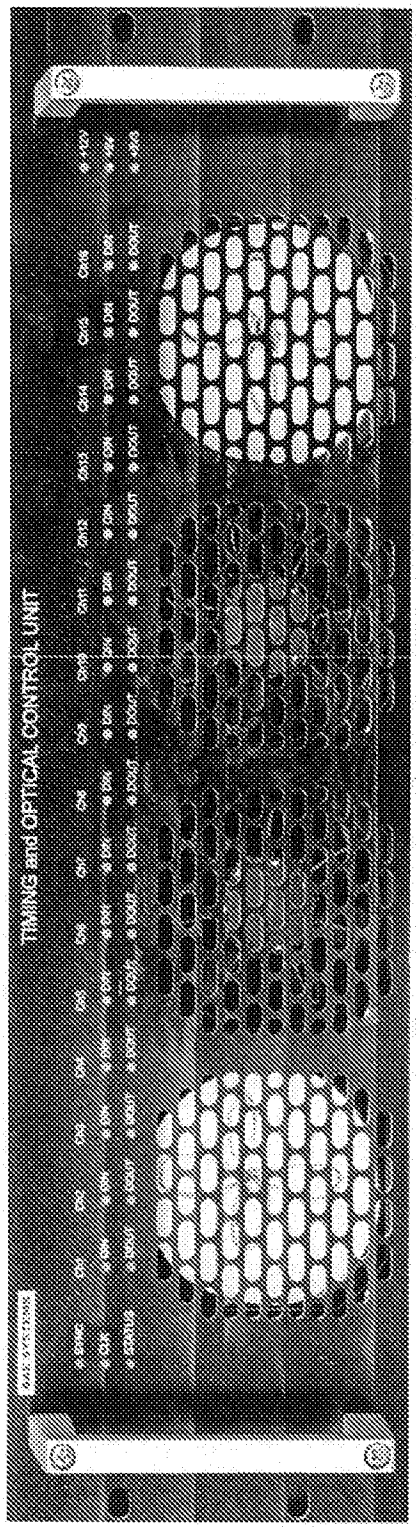


FIG. 10 Timing Optical Control Unit front panel

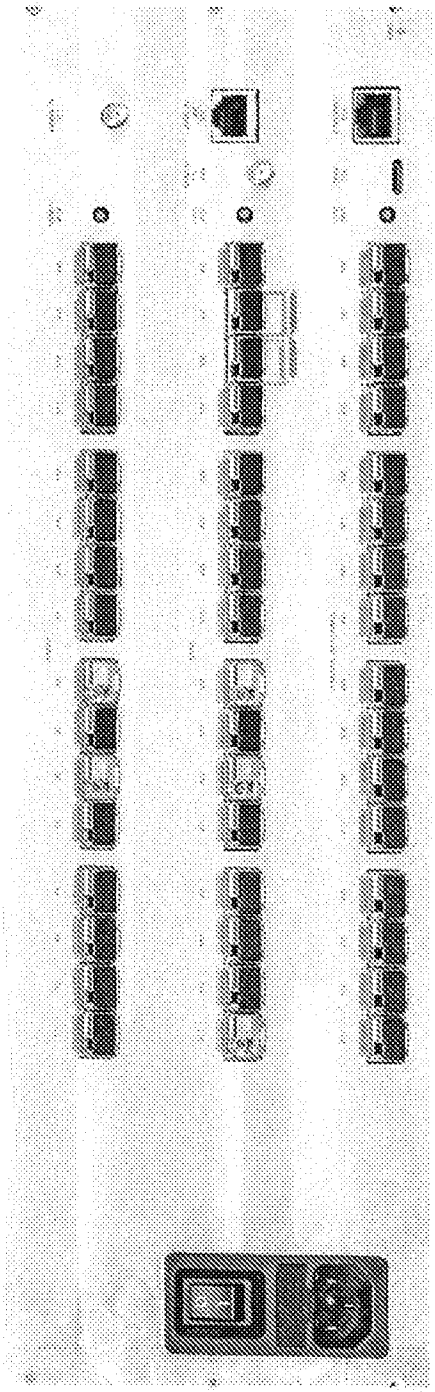
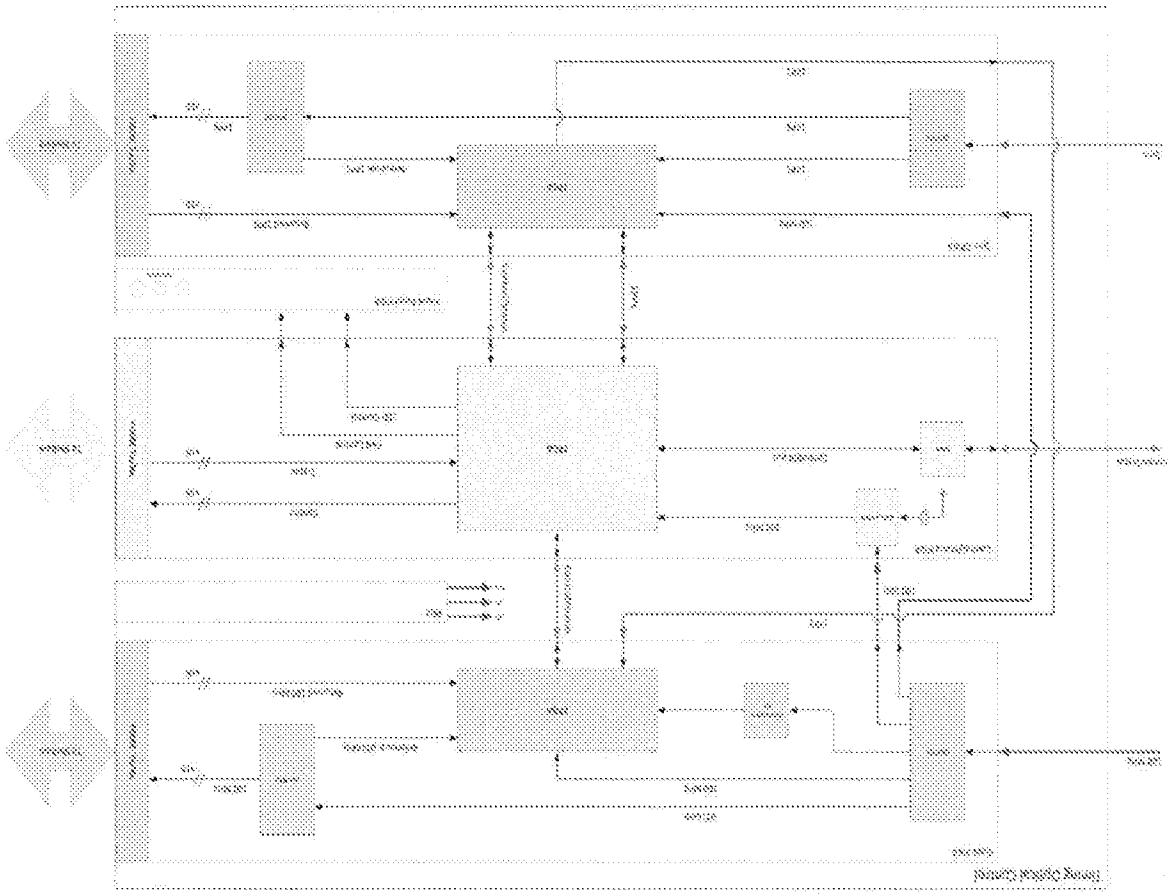


FIG. 11 TOC Rear Panel



TOC Block Diagram

FIG. 12

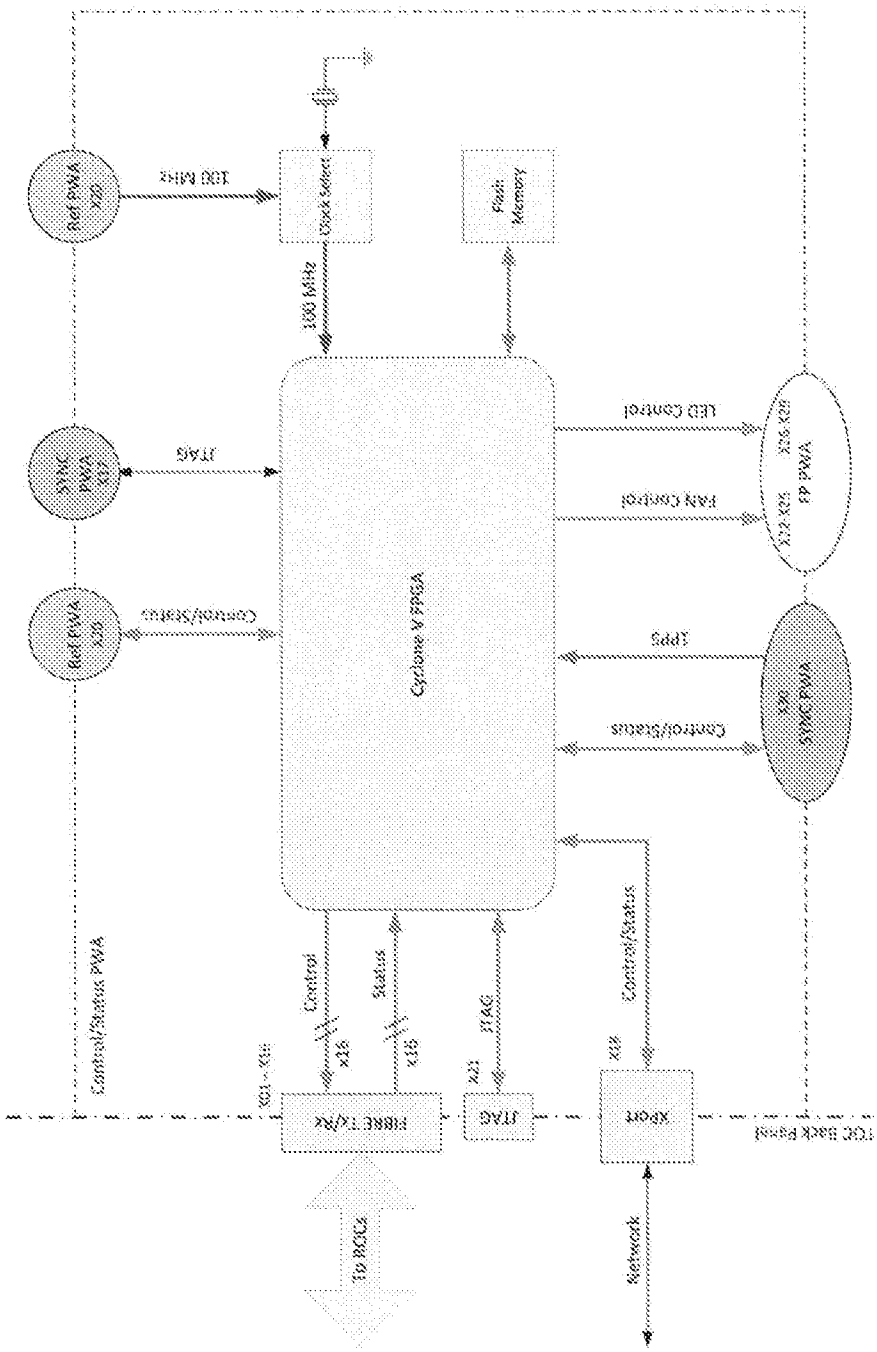

Ref PWA
X9
10M MHz
Clock Select
100 MHz
Flash Memory
JTAG
Control/Status
Ref PWA
X8
Cyclone V FPGA
LED Control
Fan Control
FP PWA
X24-X25
X26-X28
1PPS
Control/Status
SYNC PWA
X9
Control/Status PWA
Control
Status
JTAG
X16
X16
X21
X8
X01 - X08
Control/Status
FIBRE TX/RX
JTAG
Xport
TGC Back Panel
To RGCs
Network

FIG. 13

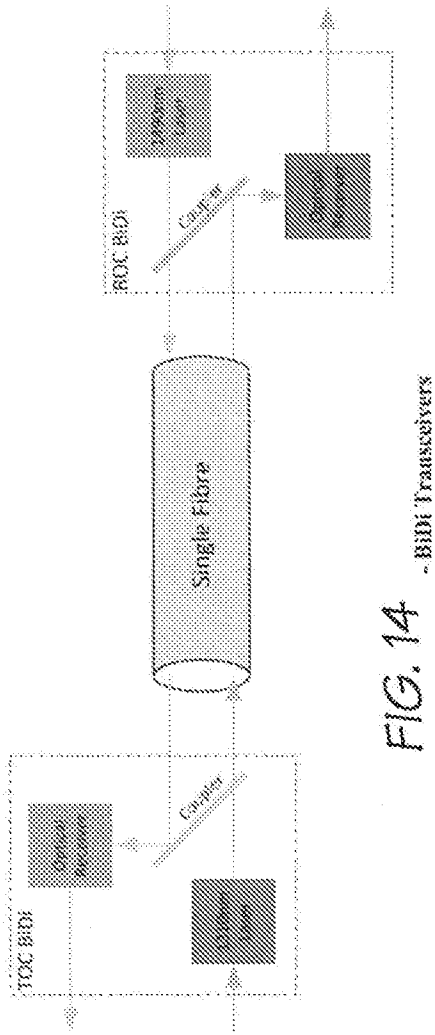


FIG. 14 - BiDi Transceivers

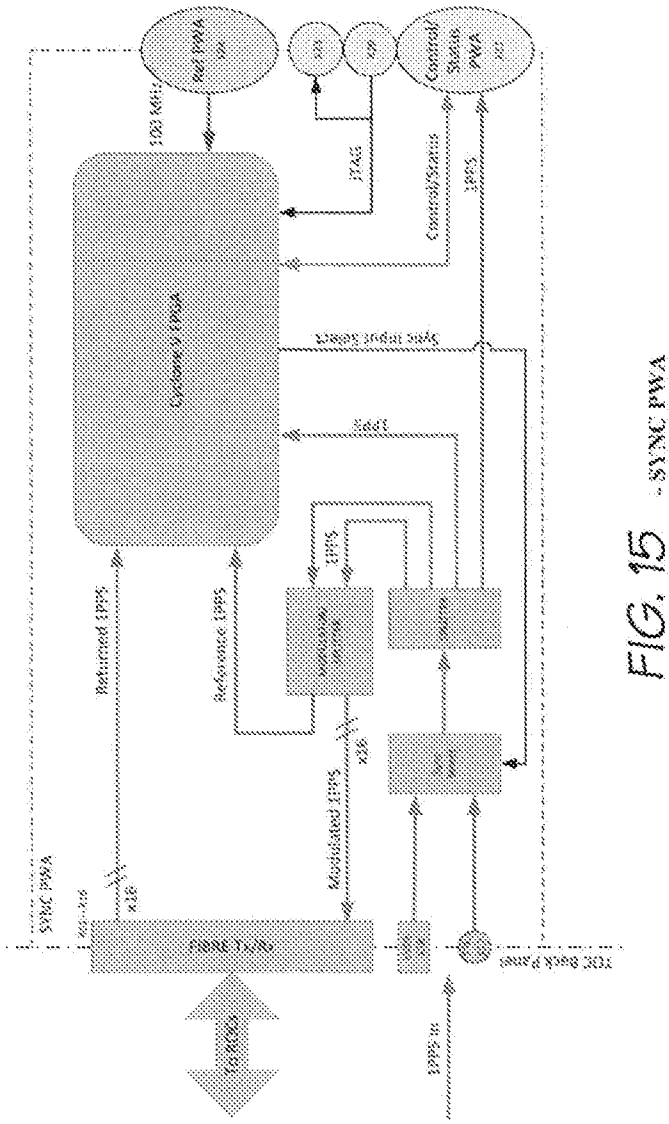


FIG. 15 - SYNC PWA

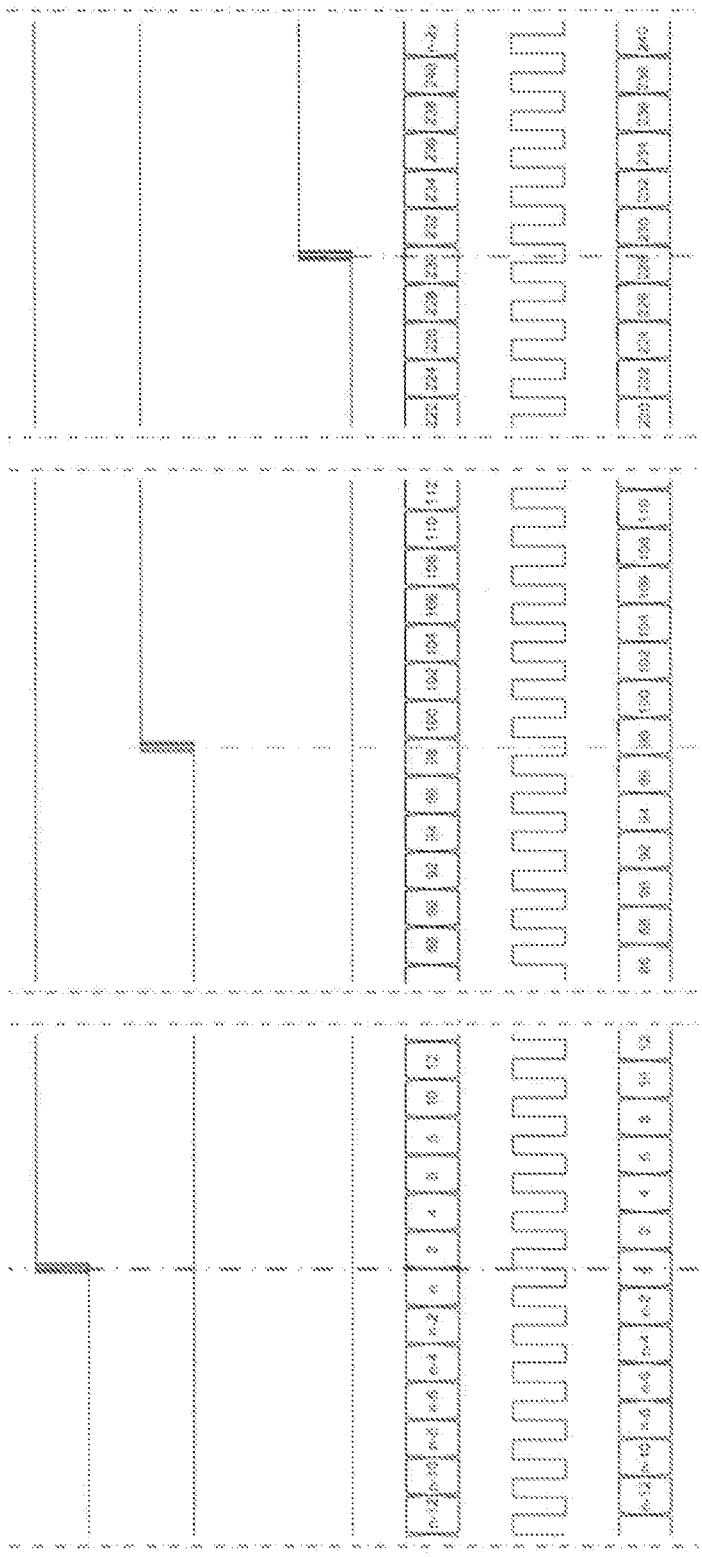

TOC Transmit 1PPS
Receive ROC 1 1PPS
Receive ROC N 1PPS
High Edge Counter
200MHz Clock
Low Edge Counter
- 1PPS Timing Diagram

FIG. 16

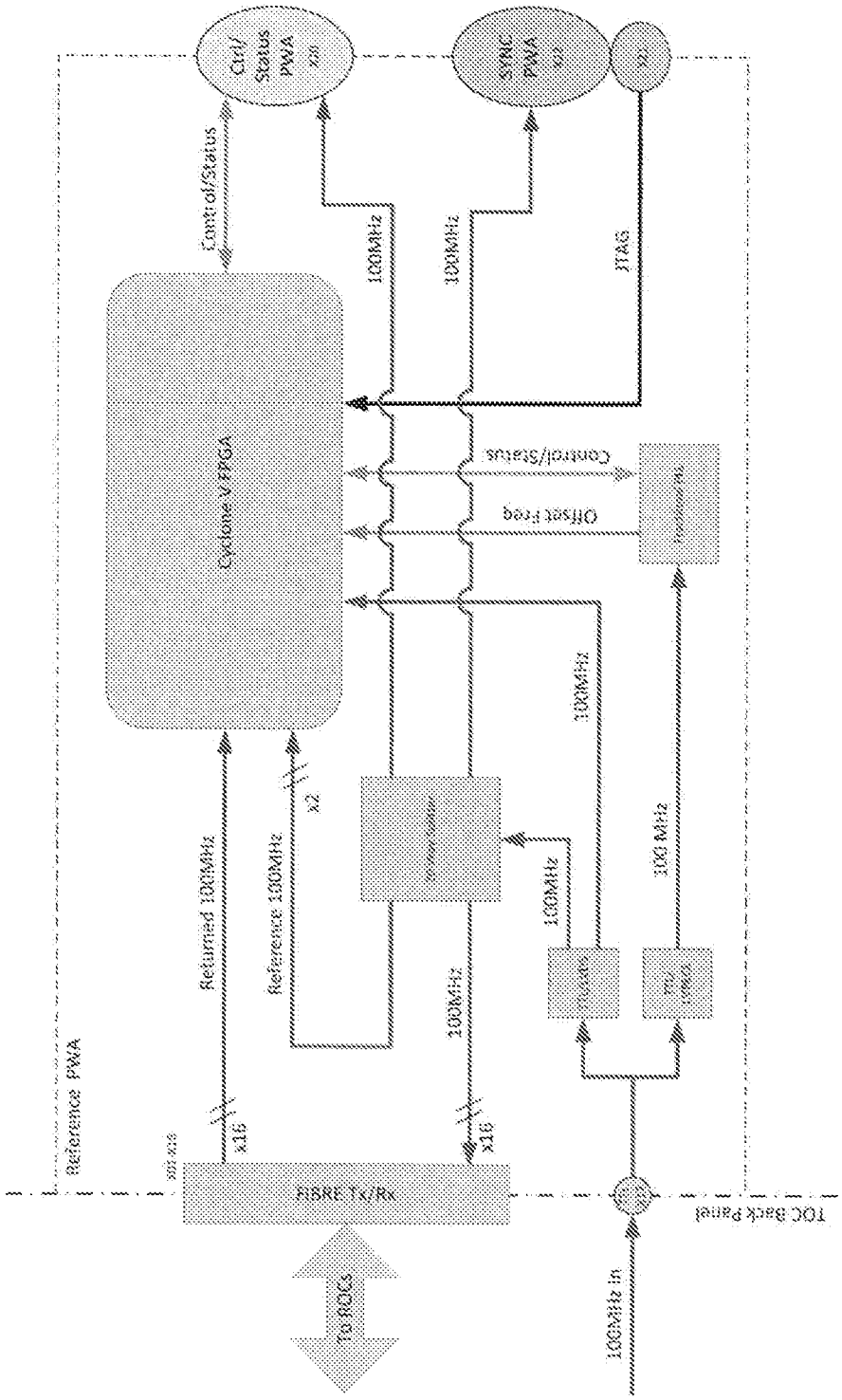


FIG. 17 - Reference PWA

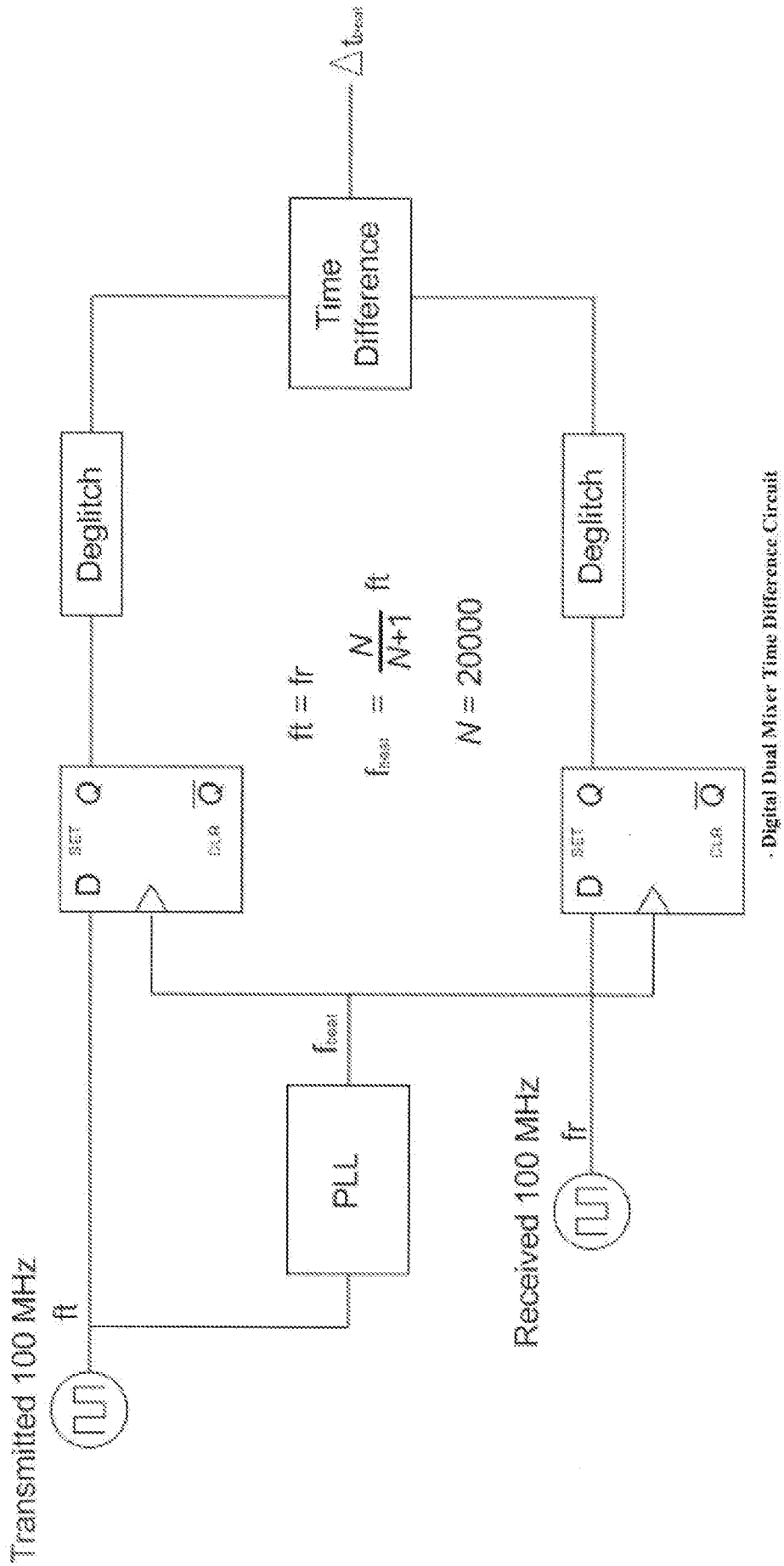


FIG. 18

. Digital Dual Mixer Time Difference Circuit

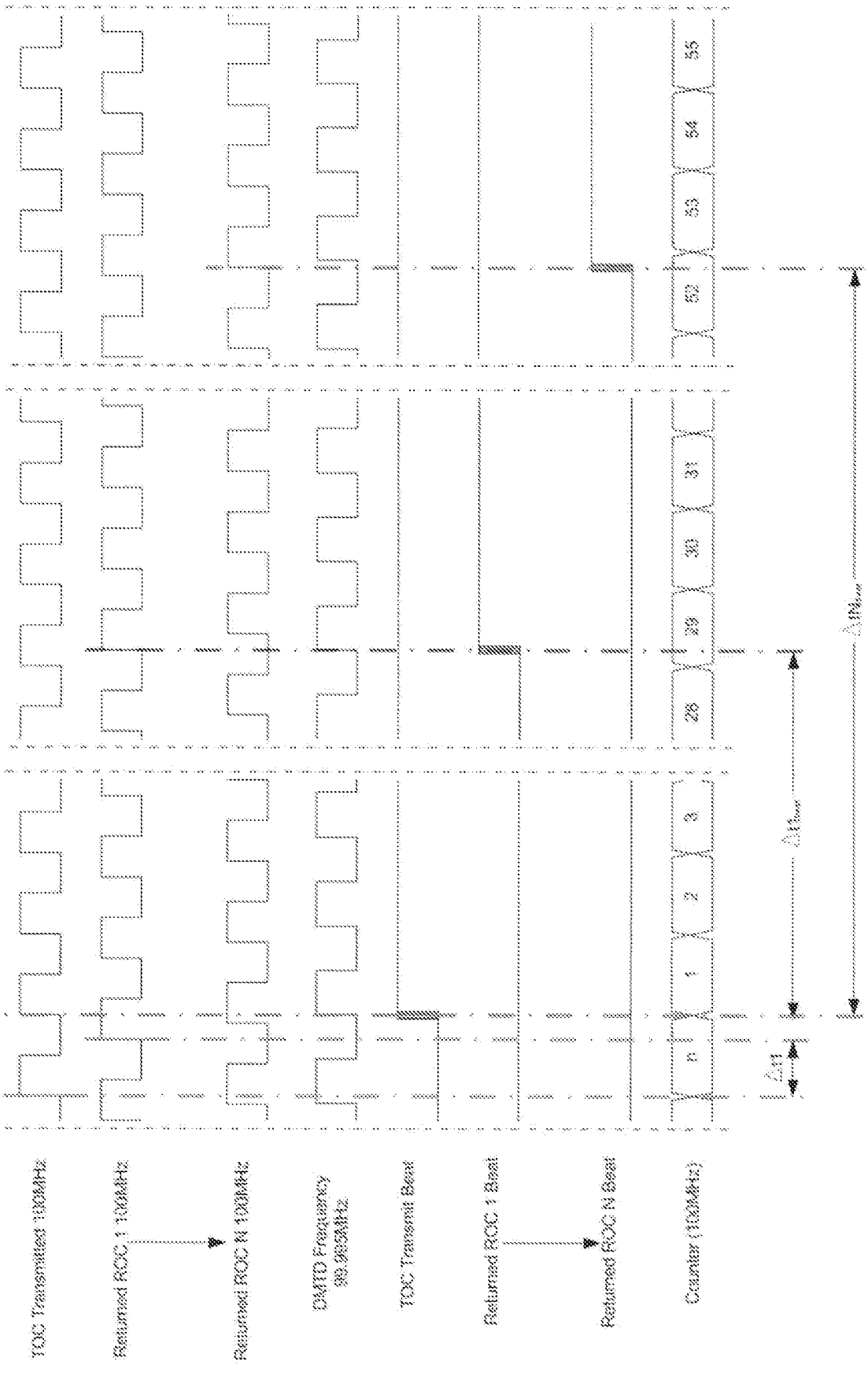


FIG. 19 - 100MHz Fibre Calibration Timing Diagram

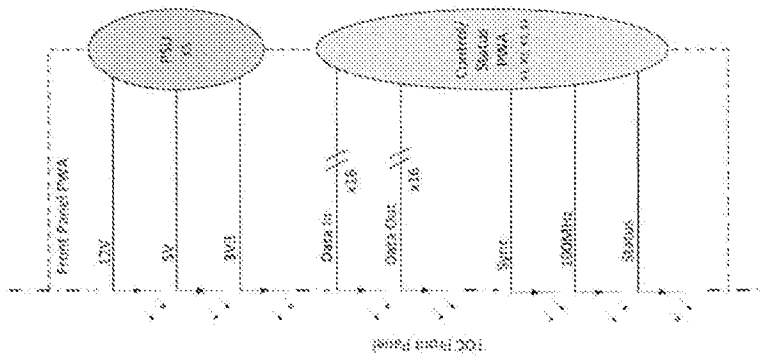


FIG. 20 – LED Display PWA Block Diagram

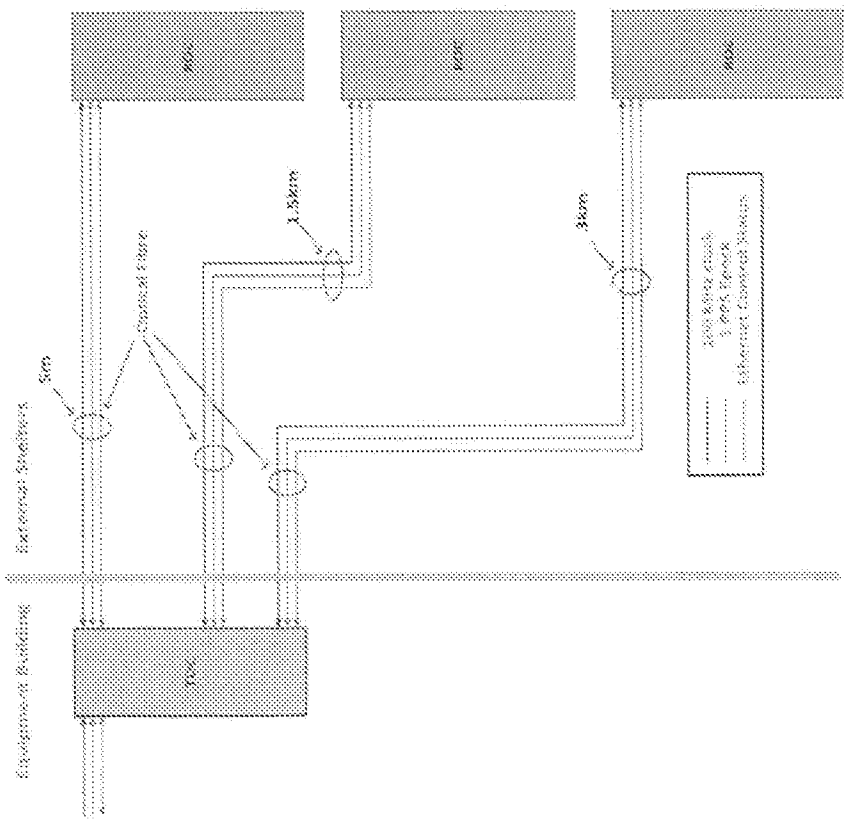

TOC/ROC Fibre Lengths
5m
1.5km
3km
Ethernet Fibre
External Structure
Equipment Building

FIG. 21

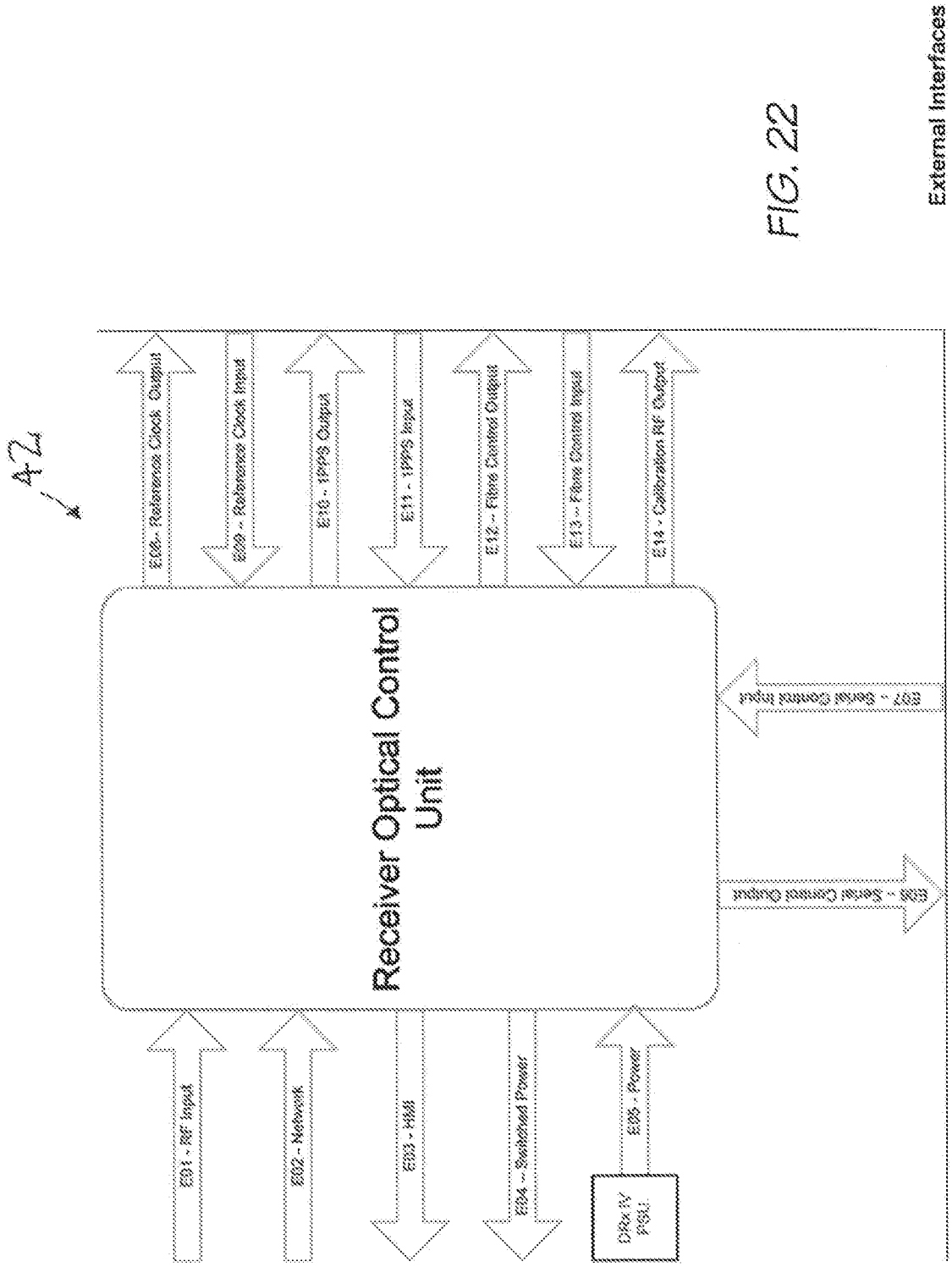
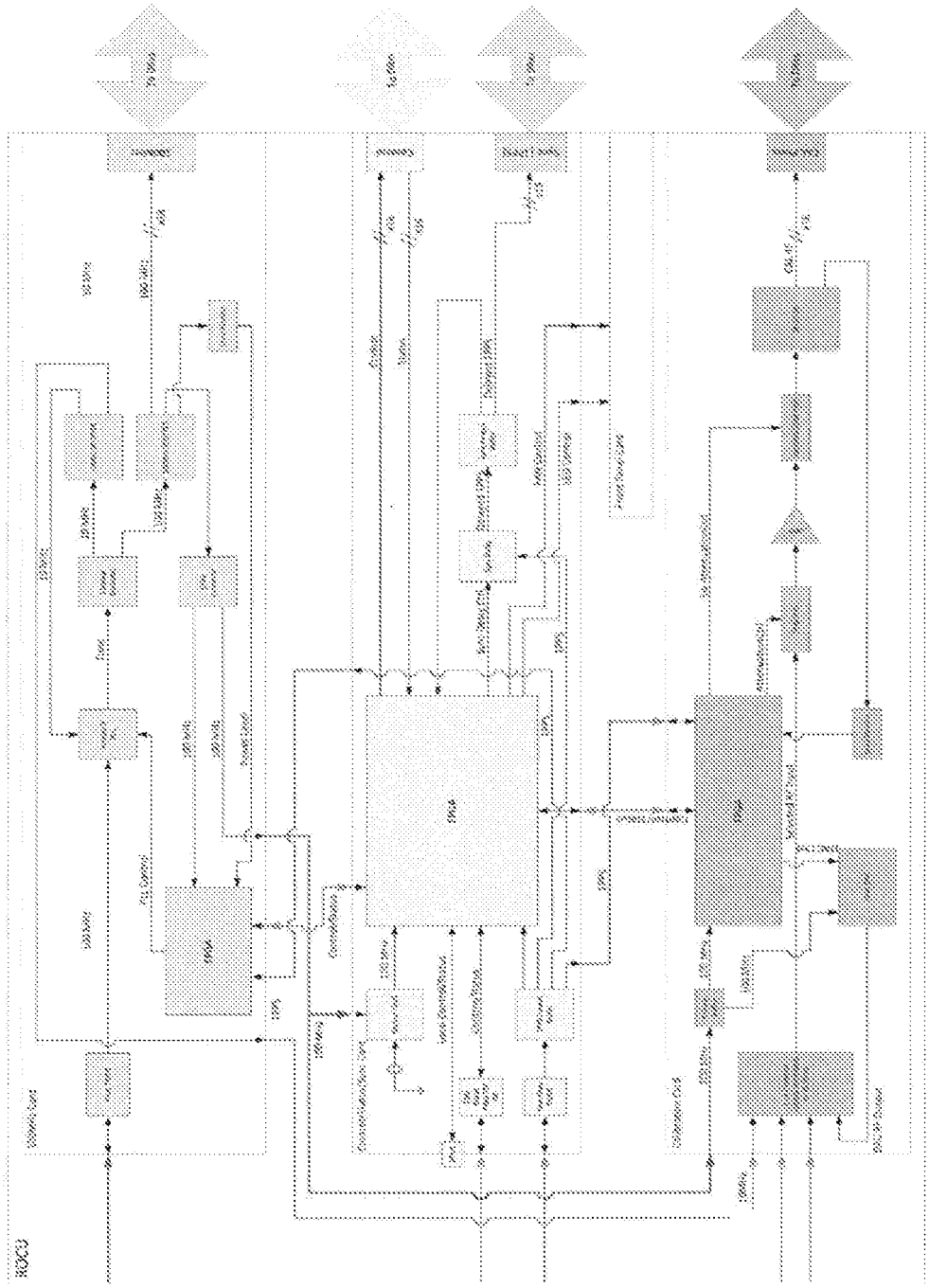

42
Receiver Optical Control Unit
E01 - RF Input
E02 - Network
E03 - HMI
E04 – Switched Power
E05 - Power
E06 - Reference Clock Output
E09 – Reference Clock Input
E10 - 1PPS Output
E11 - 1PPS Input
E12 – Fibre Control Output
E13 – Fibre Control Input
E14 - Calibration RF Output
E07 - Serial Control Input
E08 - Serial Control Output
External Interfaces

FIG. 22



ROCU Block Diagram

FIG. 23

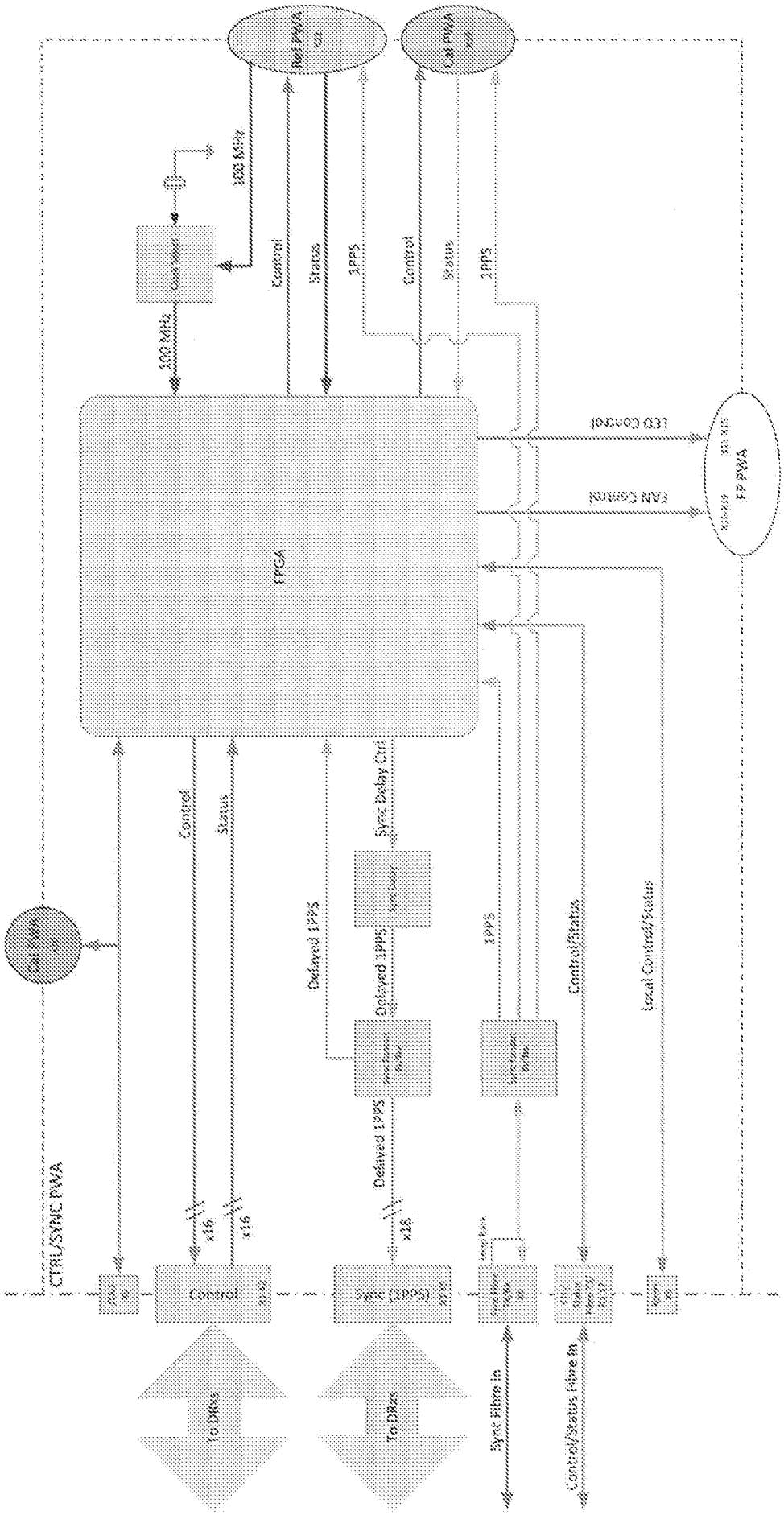

Ref PWA
Cal PWA
100 MHz
Control
Status
1PPS
FPGA
LED Control
FAN Control
FP PWA
Sync Delay Ctrl
Delayed 1PPS
Local Control/Status
CTRL/SYNC PWA
x16
x18
Sync (1PPS)
To DRxs
Sync Fibre In
Control/Status Fibre In
Control/Status PWA

FIG. 24

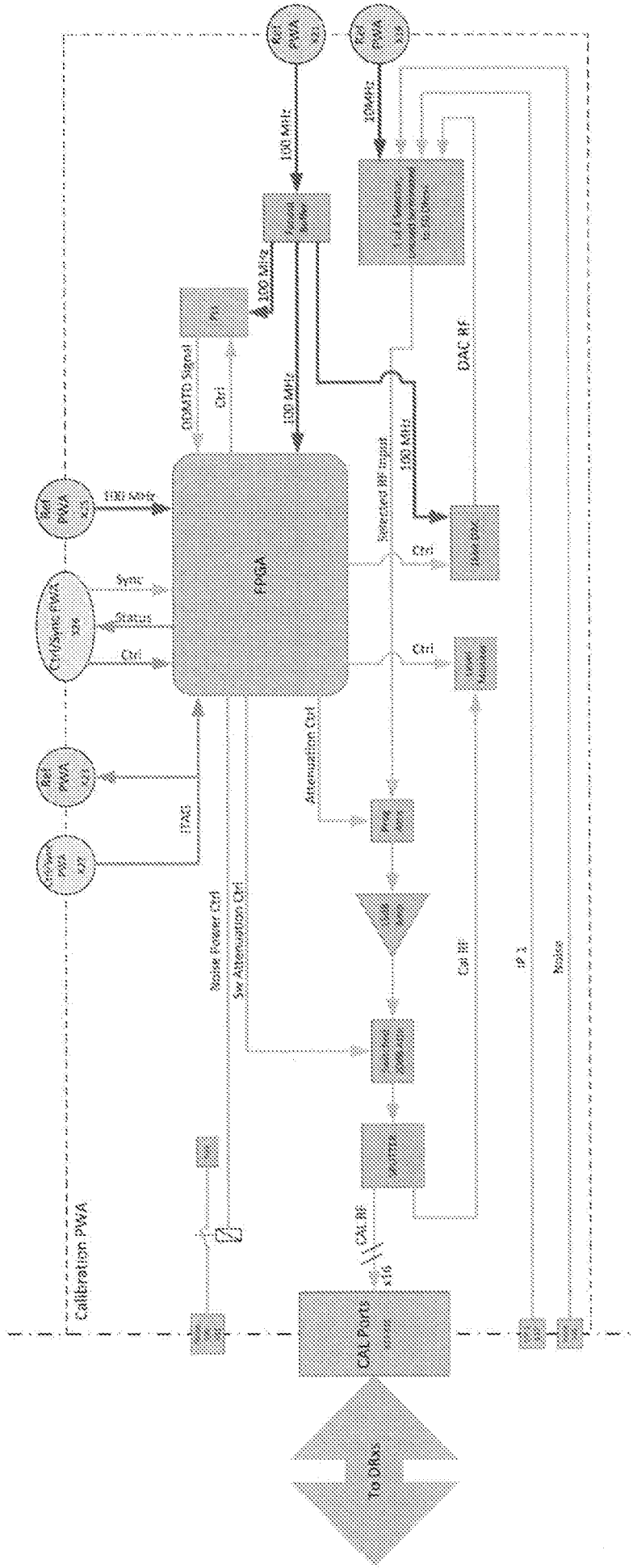

Ref PWA
100 MHz
10MHz
100 MHz
100 MHz
DAC RF
100 MHz
DDMTD Signal
Ctrl
Ctrl
Ctrl
Ctrl
Sync
Status
Ctrl
FPGA
Attenuation Ctrl
Ref PWA
Ref PWA
Ref PWA
Noise Power Ctrl
Sw Attenuation Ctrl
Cal RF
IF 1
Noise
CAL RF
x16
CAL Ports
To DMs
Calibration PWA

FIG. 25

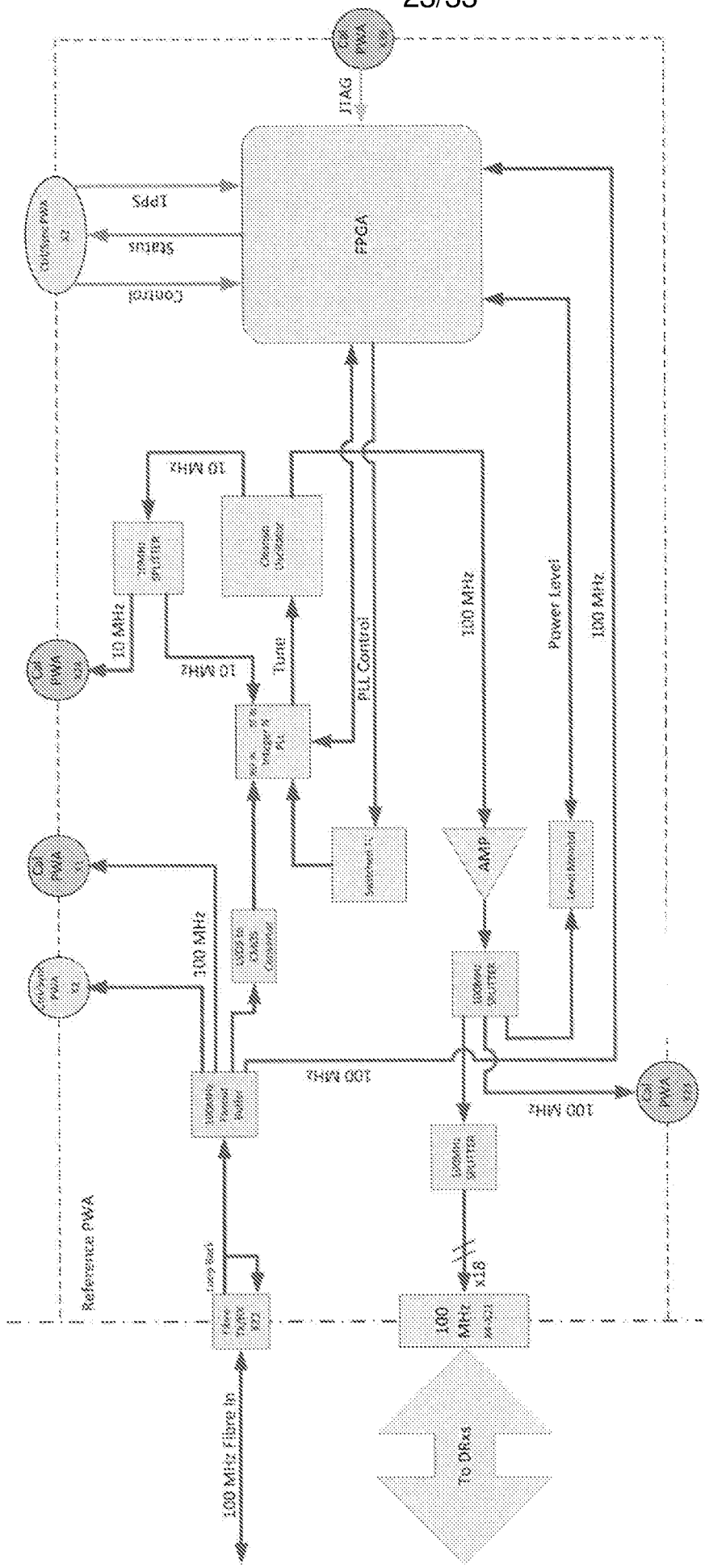


FIG. 26 Reference PWA

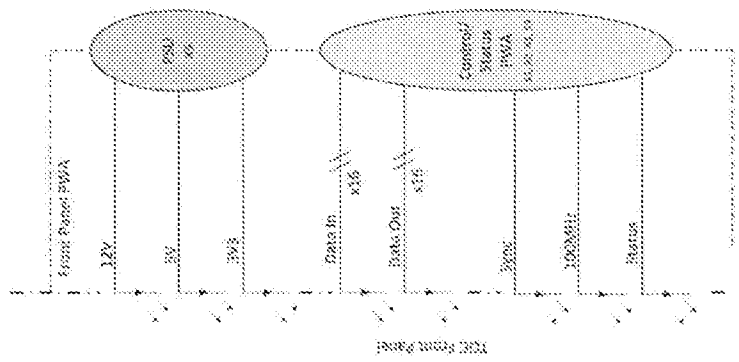


FIG. 27 – LED Display PWA Block Diagram

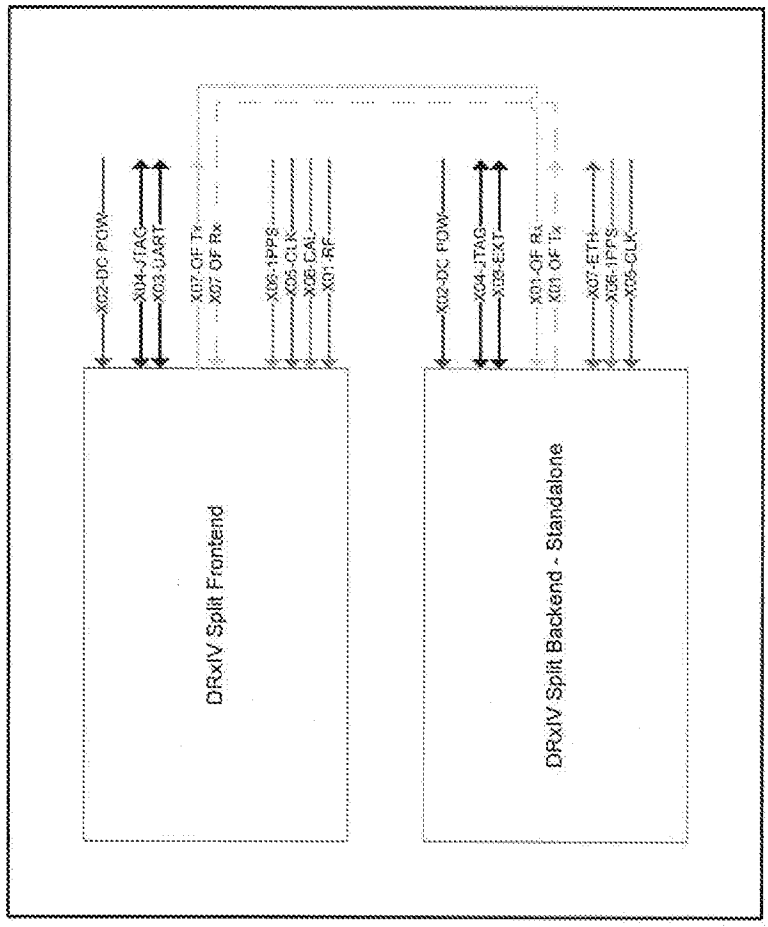


FIG. 28 Split Standalone DRxIV

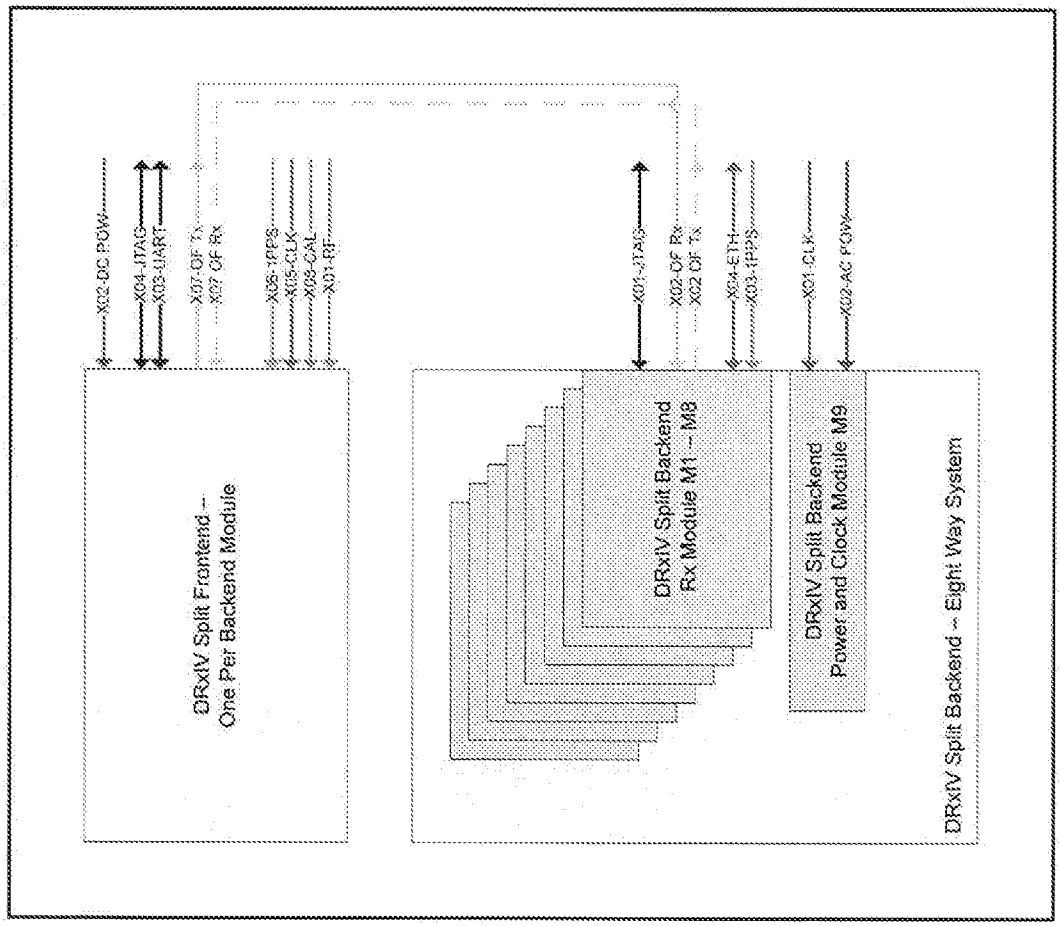


FIG. 29 : Split Eight Way System DRxIV

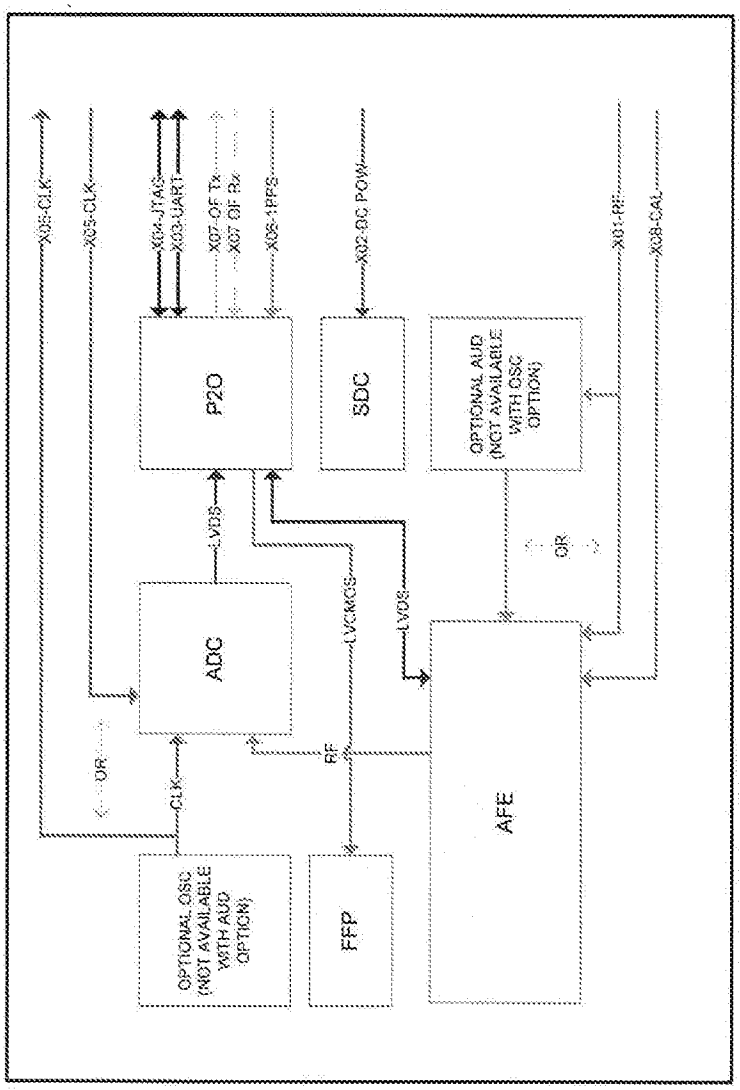
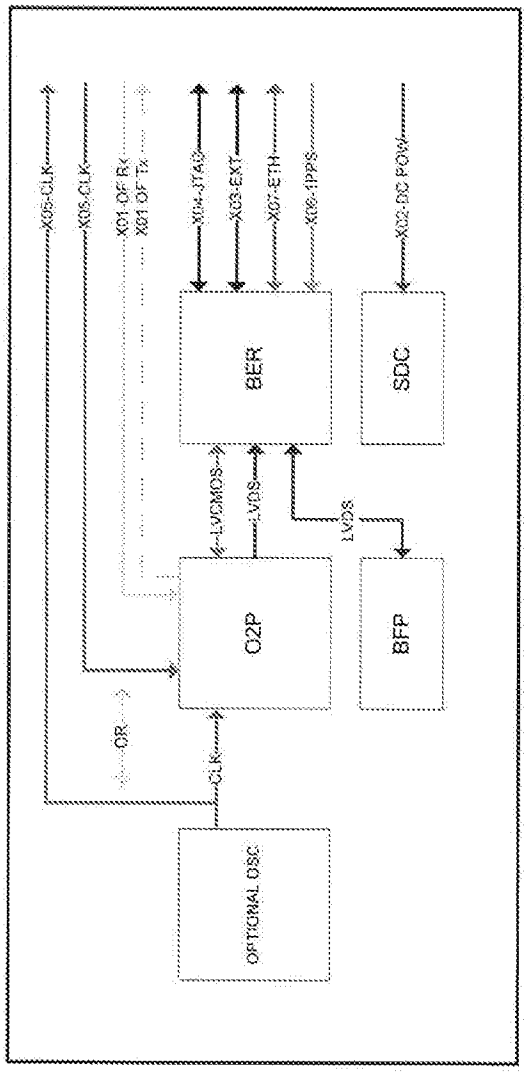


FIG. 30 : Split Frontend DRxIV Structure



Split Standalone Backend DRxIV Structure

Fig. 31

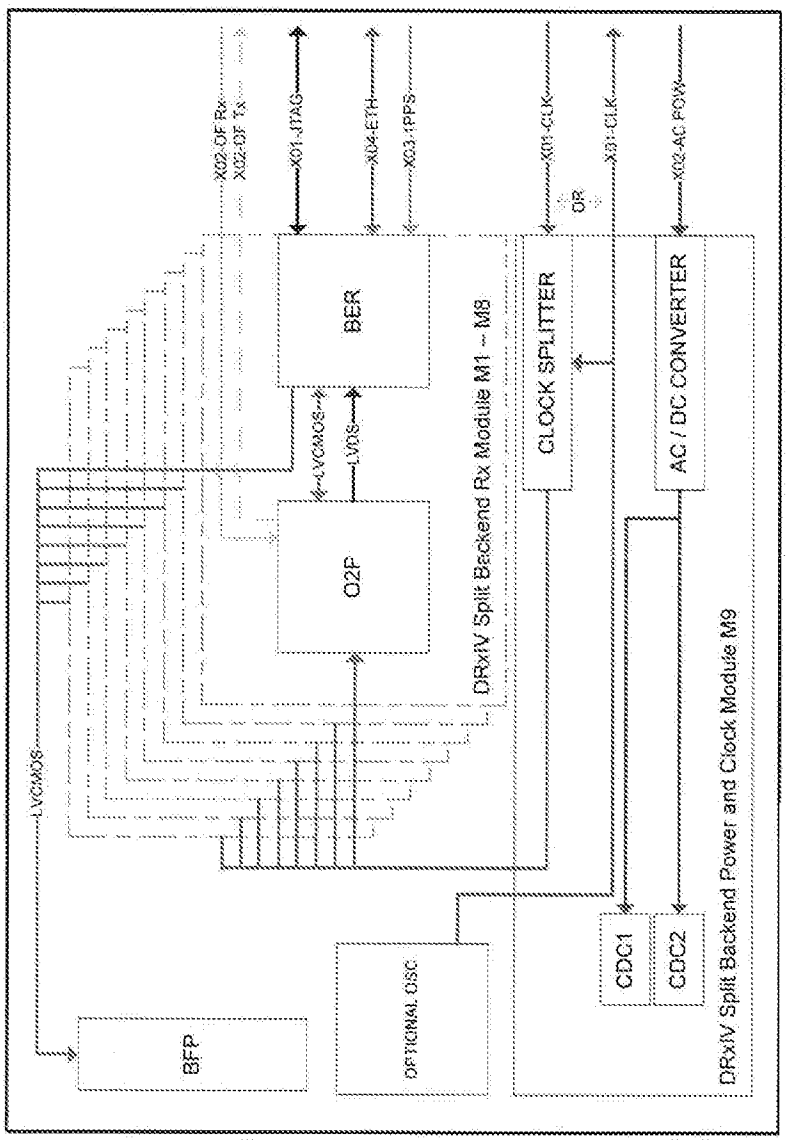
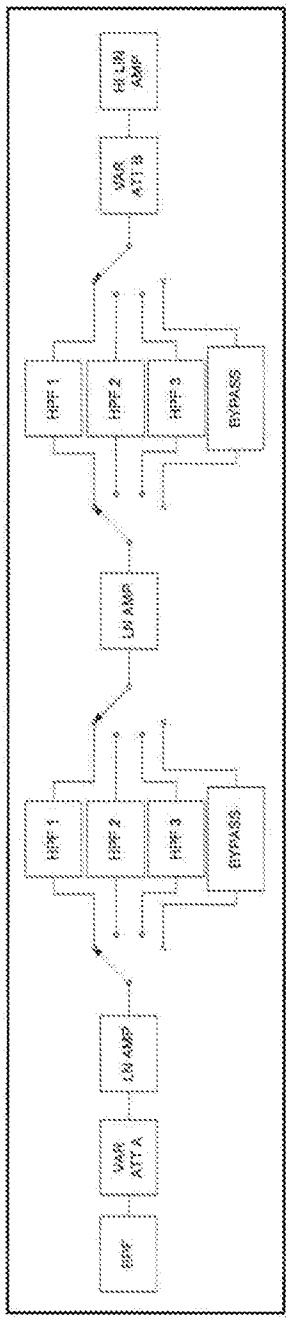
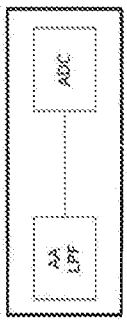


Fig. 32 Split Eight Way System Backend DRxIV Structure



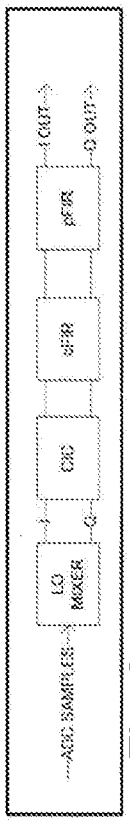
DRxIV AFE Block Diagram

Fig. 33



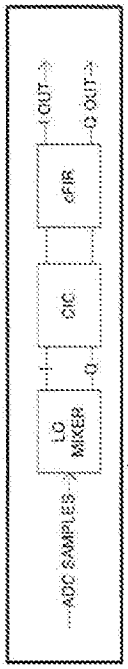
DRxIV ADC Block Diagram

Fig. 34



DRxIV Narrowband DDC Block Diagram

Fig. 35



DRxIV Wideband DDC Block Diagram

Fig. 36

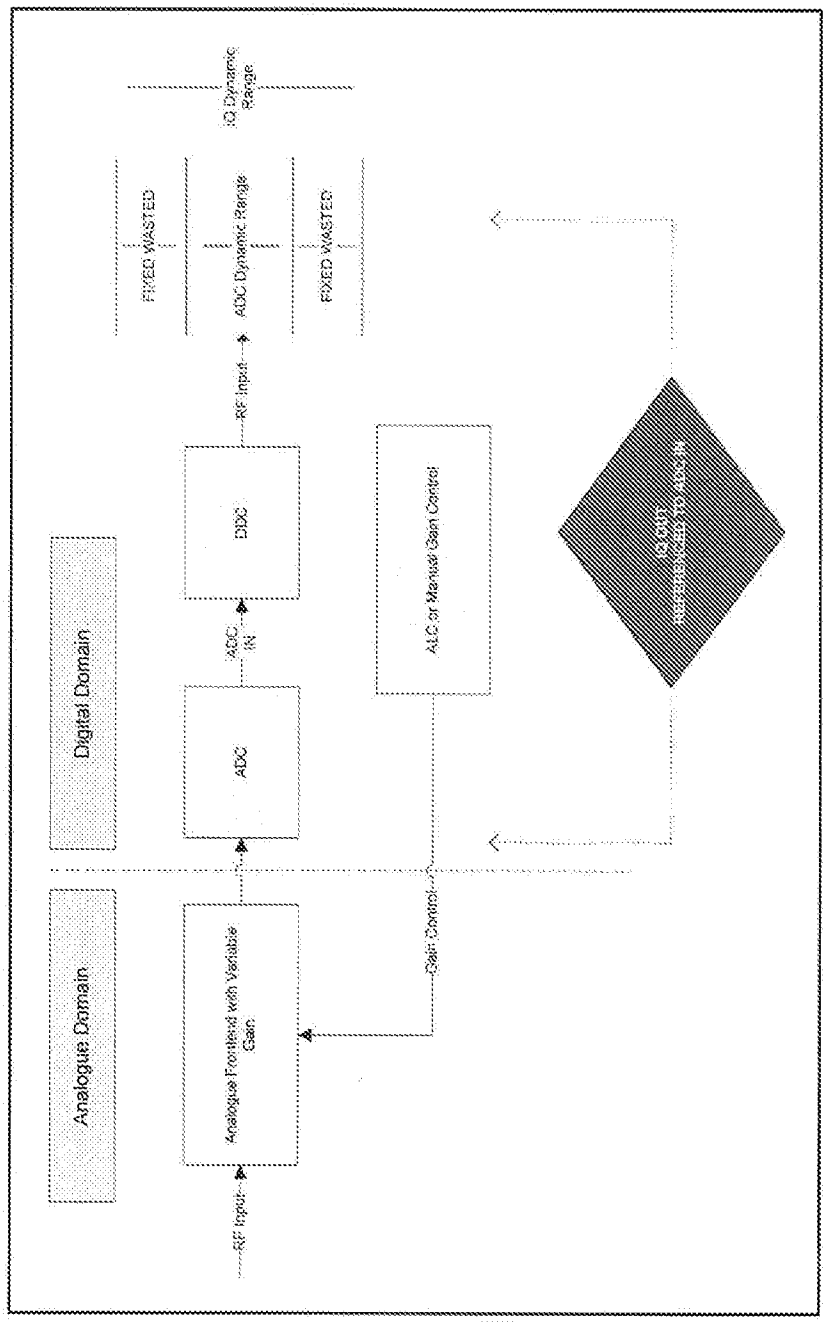
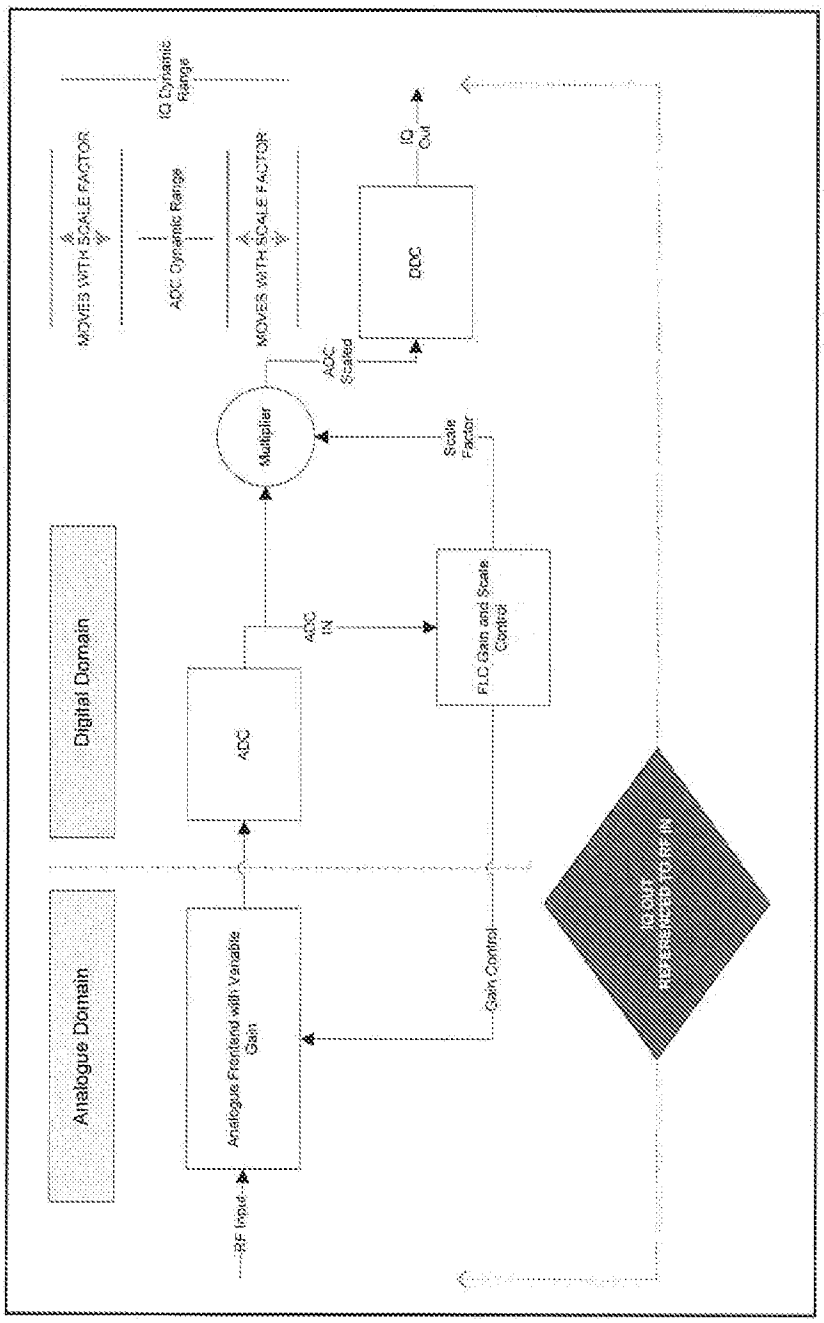

Analogue Domain
Digital Domain
RF Input
Analogue Frontend with Variable Gain
ADC
ADC IN
DDC
RF Input
FIXED WASTED
ADC Dynamic Range
FIXED WASTED
IQ Dynamic Range
Gain Control
ALC or Manual Gain Control
IQ DATA
DRxIV ALC Block Diagram

Fig. 37



DRxIV FLC Block Diagram

Fig. 38

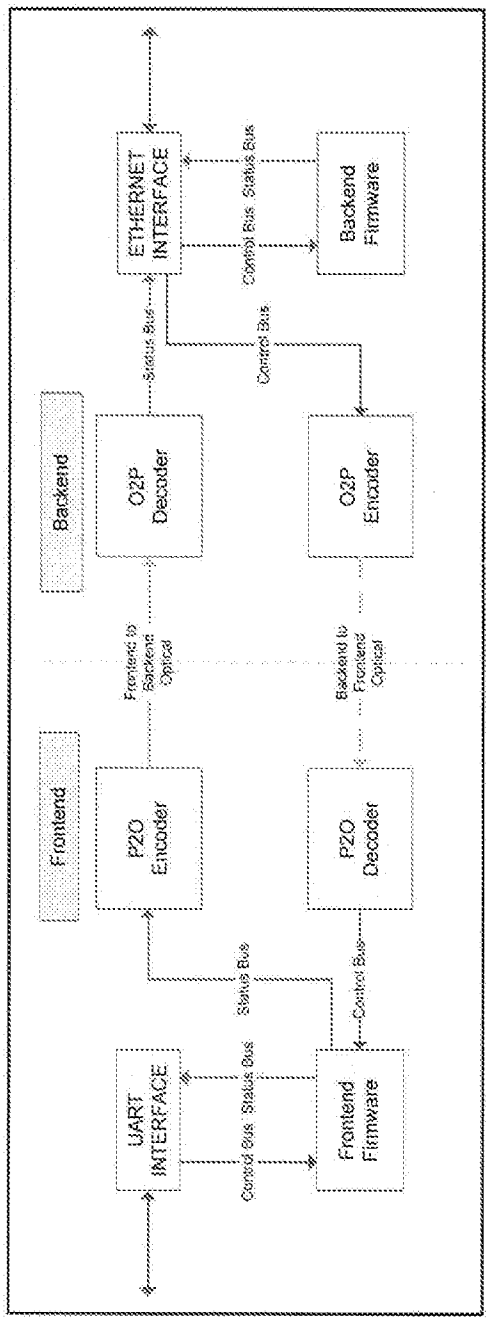


Fig. 39 : Split DRxIV Control and Status

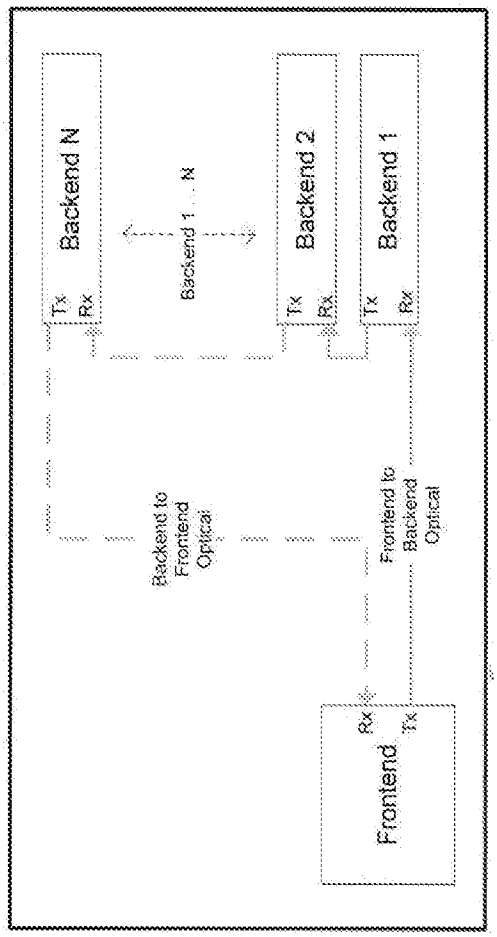


Fig. 40 : Split DRxIV Daisy Chaining

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2019/050726

A. CLASSIFICATION OF SUBJECT MATTER

H04B 10/61 (2013.01) H04L 7/00 (2006.01) G01B 11/02 (2006.01) G01S 17/46 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Google, Google Patents, Google Scholar: distance detection using beat frequency in optical fibers, beat frequency optical network timing synchronisation, optical beat frequency determine distance, antenna optical timing synchronize clock, and other similar terms

EPOQUE (PATENW): IPC/CPCs: G01B9/02007, G01B9/02003, G01B9/02, H04B10/61, G01S17/46, G01B11/02, Keywords: OPTICAL, DELAY, FIBERS, DETERMINE, BEAT, REQUENCY, HOMODYNE, INVERSE, PHASE, CLOCK, SIGNAL, MODULATE, DISTANCE, TRANSMISSION and other similar terms

Espacenet and **IP Australia Internal Databases**: Inventor: Averay Robert; Applicant: BAE Systems; CPC: H04B10/60, G01B9/02, G01S17/32

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 September 2019	20 September 2019

Name and mailing address of the ISA/AU	**Authorised officer**
AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA Email address: pct@ipaustralia.gov.au	David Carberry AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No. +61 (0)2 6225 6191

INTERNATIONAL SEARCH REPORT C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		International application No. **PCT/AU2019/050726**
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/0051146 A1 (JENSEN et al.) 03 March 2011 Figs 2-3, [0005], [0028], [0030]-[0034]	1-4
X	Berkovic G. *et al.*, "Optical methods for distance and displacement measurements", Advances in Optics and Photonics **4**, 441–471 (2012) doi:10.1364/AOP.4.000441 Whole document, especially Section 2.7	5-7
X	US 5781297 A (CASTORE) 14 July 1998 Abstract, Col 2 L62 – Col 3 L32	5-7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU2019/050726

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
the subject matter listed in Rule 39 on which, under Article 17(2)(a)(i), an international search is not required to be carried out, including

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See Supplemental Box for Details

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-7

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Supplemental Box

Continuation of: **Box III**

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

This Authority has found that there are different inventions based on the following features that separate the claims into distinct groups:

- Group 1: Claims 1-7 are directed to a method for determining the distance of transmission for an optical waveguide. The features of transmitting a modulated optical signal along a waveguide, determining a beat frequency, and using the beat frequency to determine a distance are specific to this group of claims.

- Group 2: Claims 8-10 are directed to a signal receiver. The features of a receiver optical control unit which receives optical timing signals, and a signal sampling unit for filtering the antenna input signal are specific to this group of claims.

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

When there is no special technical feature common to all the claimed inventions there is no unity of invention.

In the above groups of claims, the identified features may have the potential to make a contribution over the prior art but are not common to all the claimed inventions and therefore cannot provide the required technical relationship. Therefore there is no special technical feature common to all the claimed inventions and the requirements for unity of invention are consequently not satisfied *a priori*.

INTERNATIONAL SEARCH REPORT Information on patent family members	International application No. **PCT/AU2019/050726**

This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document/s Cited in Search Report		**Patent Family Member/s**	
Publication Number	**Publication Date**	**Publication Number**	**Publication Date**
US 2011/0051146 A1	03 March 2011	US 2011051146 A1	03 Mar 2011
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End of Annex

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.