



(12) **United States Design Patent**
Motohashi et al.

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(54) **SEMICONDUCTOR MODULE**

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(**) Term: **14 Years**

(21) Appl. No.: **29/491,549**

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(57) **CLAIM**

The ornamental design for a semiconductor module, as shown and described.

(30) **Foreign Application Priority Data**

Feb. 19, 2014 (JP) D2014-003350

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/110, 182; 257/678, 684, 690, 691;
361/713, 679.01, 728, 736, 772, 773,
361/774, 775, 760, 761, 783, 820; 174/250,
174/253; 438/15, 25, 26, 51, 54, 55, 63, 64,
438/65, 106
See application file for complete search history.

DESCRIPTION

FIG. 1 is a front view of a semiconductor module showing our new design;
FIG. 2 is a rear view of the semiconductor module of FIG. 1;
FIG. 3 is a left side view of the semiconductor module of FIG. 1;
FIG. 4 is a right side view of the semiconductor module of FIG. 1;
FIG. 5 is a top view of the semiconductor module of FIG. 1;
FIG. 6 is a bottom view of the semiconductor module of FIG. 1; and,
FIG. 7 is a top, front and right side perspective view of the semiconductor module of FIG. 1.

The broken lines shown in the drawings represent portions of the semiconductor module that form no part of the claimed design.

The ornamental design of the present disclosure is a semiconductor module on which power semiconductor elements and the like may be mounted. A plurality of pin-shaped terminals projects from the top surface. Each end in a longitudinal direction includes a mounting hole. Each corner includes a positioning boss.

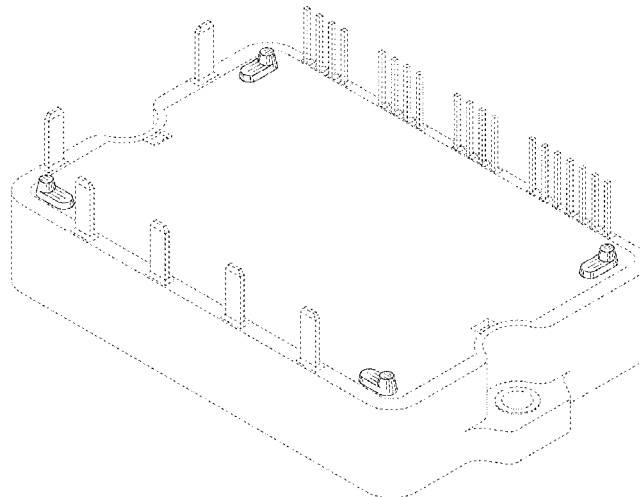
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1 Claim, 7 Drawing Sheets



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Fig. 1

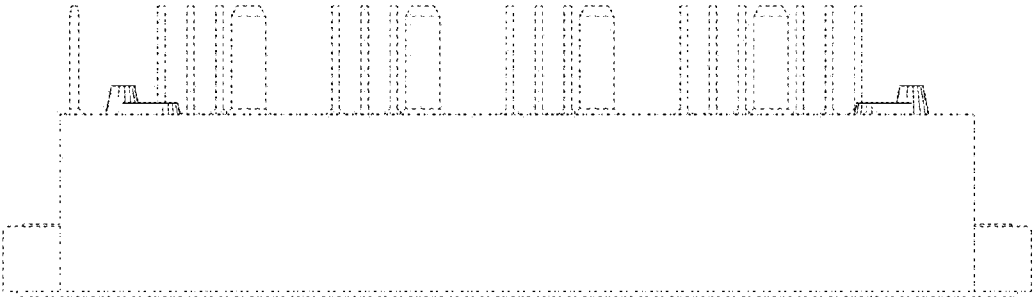


Fig.2

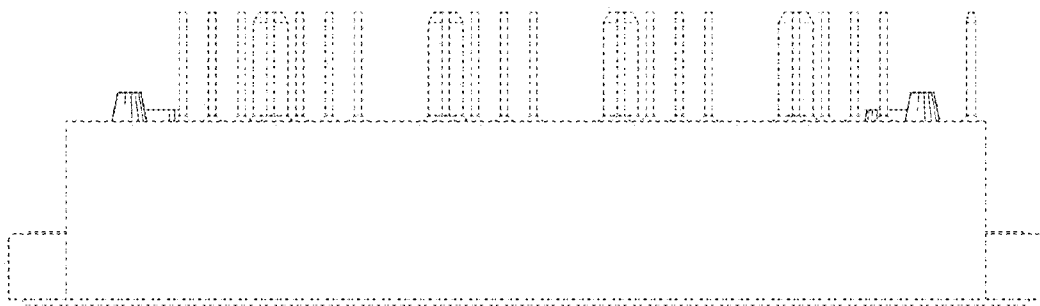


Fig. 3

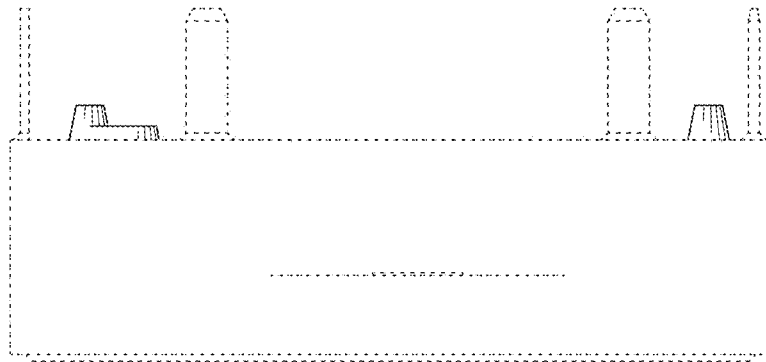


Fig. 4



Fig.5

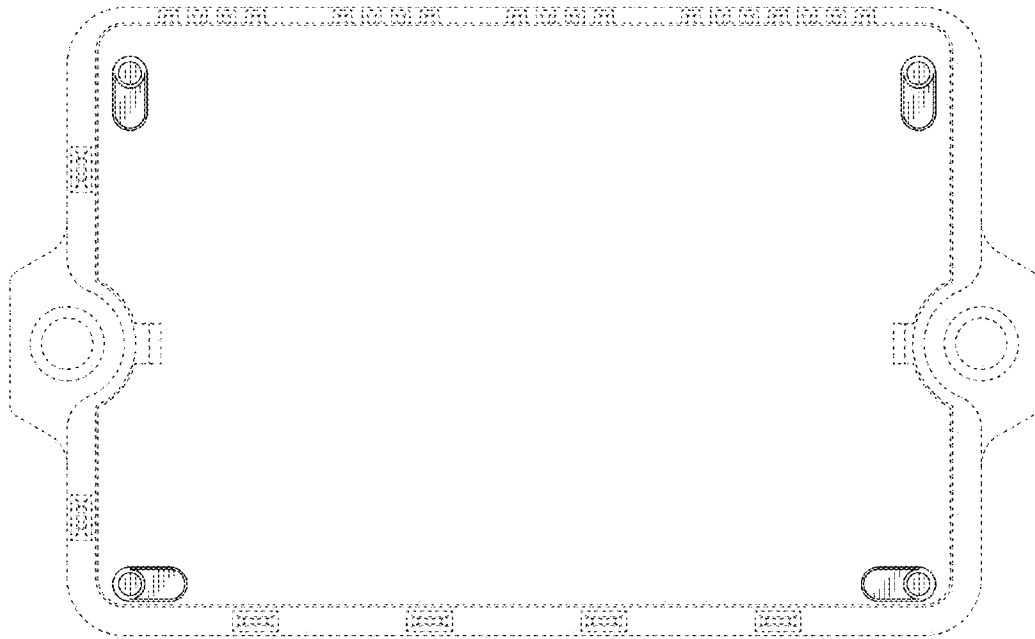


Fig.6



Fig.7

