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# (54) **Title**: PHOTOVOLTAIC MODULE AND METHOD OF MANUFACTURING A PHOTOVOLTAIC MODULE HAVING MULTIPLE SEMICONDUCTOR LAYER STACKS

(57) **Abstract**: A method of manufacturing a photovoltaic module is provided. The method includes providing an electrically insulating substrate and a lower electrode, depositing a lower stack of silicon layers above the lower electrode, and depositing an upper stack of silicon layers above the lower stack. The lower and upper stacks include N-I-P junctions. The lower stack has an energy band gap of at least 1.60 eV while the upper stack has an energy band gap of at least 1.80 eV. The method also includes providing an upper electrode above the upper stack. The lower and upper stacks convert incident light into an electric potential between the upper and lower electrodes with the lower and upper stacks converting different portions of the light into the electric potential based on wavelengths of the light.

# PHOTOVOLTAIC MODULE AND METHOD OF MANUFACTURING A PHOTOVOLTAIC MODULE HAVING MULTIPLE SEMICONDUCTOR LAYER STACKS

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a nonprovisional patent application of, and claims priority benefit from, co-pending U.S. Provisional Patent Application Serial No. 61/185,770, entitled "Photovoltaic Devices Having Tandem Semiconductor Layer Stacks" (the "'770 Application"), and filed on June 10, 2009; co-pending U.S. Provisional Patent Application Serial No. 61/221,816, entitled "Photovoltaic Devices Having Multiple Semiconductor Layer Stacks" (the "'816 Application"), and filed on June 30, 2009; and co-pending U.S. Provisional Patent Application Serial No. 61/230,790, entitled "Photovoltaic Devices Having Multiple Semiconductor Layer Stacks" (the "'790 Application"), and filed on August 3, 2009. The entire disclosure of the '770, '816, and '790 Applications are incorporated by reference herein in their entirety.

## BACKGROUND OF THE INVENTION

[0002] The subject matter described herein relates to photovoltaic devices. Some known photovoltaic devices include thin film solar modules having active portions of thin films of silicon. Light that is incident onto the modules passes into the active silicon films. If the light is absorbed by the silicon films, the light may generate electrons and holes in the silicon. The electrons and holes are used to create an electric potential and/or an electric current that may be drawn from the modules and applied to an external electric load.

[0003] Photons in the light excite electrons in the silicon films and cause the electrons to separate from atoms in the silicon films. In order for the photons to excite the electrons and cause the electrons to separate from the atoms in the films, the photons must have an energy that exceeds the energy band gap in the silicon films. The energy of the photons is related to the wavelengths of light that is incident on the films. Therefore, light is absorbed by the silicon films based on the energy band gap of the films and the wavelengths of the light.

[0004] Some known photovoltaic devices include tandem layer stacks that include two or more sets of silicon films deposited on top of one another and between a lower electrode and an upper electrode. The different sets of films may have different energy band gaps. Providing different sets of films with different band gaps may increase the efficiency of the devices as more wavelengths of incident light can be absorbed by the devices. For example, a first set of films may have a greater energy band gap than a second set of films. Some of the light having wavelengths associated with an energy that exceeds the energy band gap of the first set of films is absorbed by the first set of films to create electron-hole pairs. Some of the light having wavelengths associated with energy that does not exceed the energy band gap of the first set of films passes through the first set of films without creating electron-hole pairs. At least a portion of this light that passes through the first set of films may be absorbed by the second set of films if the second set of films has a lower energy band gap.

[0005] In order to provide different sets of films with different energy band gaps, the silicon films may be alloyed with germanium to change the band gap of the films. But, alloying the films with germanium tends to reduce the deposition rate that can be used in manufacturing. Furthermore, silicon films alloyed with germanium tend to be more prone to light-induced degradation than those with no germanium. Additionally, germane, the source gas used to deposit silicon-germanium alloy, is costly and hazardous.

[0006] As an alternative to alloying silicon films with germanium, the energy band gap of silicon films in a photovoltaic device may be reduced by depositing the silicon films as microcrystalline silicon films instead of amorphous silicon films. Amorphous silicon films typically have larger energy band gaps than silicon films that are deposited in a microcrystalline state. Some known photovoltaic devices include semiconductor layer stacks having amorphous silicon films stacked in series with a microcrystalline silicon films. In such devices, the amorphous silicon films are deposited in a relatively small thickness to reduce carrier transport-related losses in the junction. For example, the amorphous silicon films may be deposited with a small thickness to reduce the amount of electrons and holes that are excited from silicon atoms by incident light and recombine with other silicon atoms or other electrons and holes before reaching the top or bottom electrodes. The electrons and holes that do not reach the electrodes do not contribute to the voltage or current created by the photovoltaic device. But, as the thickness of the amorphous silicon junction is reduced, less light is absorbed by the amorphous silicon junction and the flow of photocurrent in the silicon films is reduced. As a result, the efficiency of the photovoltaic device in converting incident light into electric current can be limited by the amorphous silicon junction in the device stack.

[0007] In some photovoltaic devices having relatively thin amorphous silicon films, the surface area of photovoltaic cells in the device that have the active amorphous silicon films may be increased relative to inactive areas of the cells. The active areas include the silicon films that convert incident light into electricity while non-active or inactive areas include portions of the cells where the silicon film is not present or that do not convert incident light into electricity. The electrical power generated by photovoltaic devices may be increased by increasing the active areas of the photovoltaic cells in the device relative to the inactive areas in the device. For example, increasing the width of the cells in a monolithically-integrated thin film photovoltaic module having active amorphous silicon films increases the fraction or percentage of active photovoltaic material in the module that is exposed to sunlight. As the fraction of active photovoltaic material increases, the total photocurrent generated by the device may increase.

[0008] Increasing the width of the cells also increases the size or area of light-transmissive electrodes of the device. The light-transmissive electrodes are the electrodes that conduct electrons or holes created in the cells to create the voltage or current of the device. As the size or area of the light-transmissive electrodes increases, the electrical resistance (R) of the light-transmissive electrodes also increases. The electric current (I) that passes through the light-transmissive electrodes also may increase. As the current passing through the light-transmissive electrodes and the resistance of the light-transmissive electrodes increase, energy losses, such as $I^2R$ losses, in the photovoltaic device increase. As the energy losses increase, the photovoltaic device becomes less efficient and less power is generated by the device. Therefore, in monolithically-integrated thin film photovoltaic devices, there exists a trade-off between the fraction of active photovoltaic material in the devices and the energy losses incurred in the transparent conducting electrodes of the devices.

[0009] A need exists for photovoltaic devices having increased efficiency in converting incident light into electric current and/or with decreased energy losses.

## BRIEF DESCRIPTION OF THE INVENTION

[0010] In one embodiment, a method of manufacturing a photovoltaic module is provided. The method includes providing an electrically insulating substrate and a lower electrode, depositing a lower stack of silicon layers above the lower electrode, and depositing an upper stack of silicon layers above the lower stack. The lower and upper stacks include N-I-P junctions. The lower stack has an energy band gap of at least 1.60 eV while the upper stack has an energy band gap of at least 1.80 eV. The method also includes providing an upper electrode above the upper stack. The lower and upper stacks convert incident light into an electric potential between the upper and lower electrodes with the lower and upper stacks converting different portions of the light into the electric potential based on wavelengths of the light.

[0011] In another embodiment, a monolithically-integrated photovoltaic module is provided. The module includes an electrically insulating substrate, a lower electrode above the substrate, a lower stack of silicon layers above the lower electrode, an upper stack of silicon layers above the lower stack, and an upper electrode above the upper stack. The lower stack has an energy band gap of at least 1.60 eV while the upper stack has an energy band gap of at least 1.80 eV. The energy band gap of the upper stack is greater than the energy band gap of the lower stack such that the lower and upper stacks convert different portions of incident light into an electric potential between the upper and lower electrodes based on wavelengths of the light.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figure 1 is a schematic view of a substrate configuration photovoltaic cell in accordance with one embodiment.

[0013] Figure 2 schematically illustrates structures in a template layer shown in Figure 1 in accordance with one embodiment.

[0014] Figure 3 schematically illustrates structures in the template layer shown in Figure 1 in accordance with another embodiment.

[0015] Figure 4 schematically illustrates structures in the template layer shown in Figure 1 in accordance with another embodiment.

[0016] Figure 5 is a schematic diagram of a substrate configuration photovoltaic device 500 in accordance with one embodiment.

[0017] Figure 6 is a flowchart of a process for manufacturing a substrate configuration photovoltaic device in accordance with one embodiment.

[0018] The foregoing summary, as well as the following detailed description of certain embodiments of the presently described technology, will be better understood when read in conjunction with the appended drawings. For the purpose of illustrating the presently described technology, certain embodiments are shown in the drawings. It should be understood, however, that the presently described technology is not limited to the arrangements and instrumentality shown in the attached drawings. Moreover, it should be understood that the components in the drawings are not to scale and the relative sizes of one component to another should not be construed or interpreted to require such relative sizes.

## DETAILED DESCRIPTION OF THE INVENTION

[0019] Figure 1 is a schematic view of a substrate configuration photovoltaic cell 100 in accordance with one embodiment. The cell 100 includes a substrate 102 and a light transmissive cover layer 104 with two semiconductor junction stacks, or layer stacks, 106, 108 disposed between the substrate 102 and cover layer 104. In one embodiment, the semiconductor junction stacks 106, 108 include N-I-P layer stacks of silicon. The cell 100 is a substrate-configuration photovoltaic cell. For example, light that is incident on the cell 100 on the cover layer 104 opposite the substrate 102 is converted into an electric potential by the cell 100. The light passes through the cover layer 104 and additional layers and components of the cell 100 to upper and middle layer stacks 106, 108. The light is absorbed by the upper and middle layer stacks 106, 108.

[0020] Photons in the light excite electrons and cause the electrons to separate from atoms in the layer stacks 106, 108. Complementary positive charges, or holes, are created when the electrons separate from the atoms. The layer stacks 106, 108 have different energy band gaps that absorb different portions of the spectrum of wavelengths in the light. The electrons drift or diffuse through the layer stacks 106, 108 and are collected at one of upper and lower electrodes 112, 114, or electrodes 112, 114. The holes drift or diffuse through the upper and lower electrodes 112, 114 and are collected at the other of the upper and lower electrodes 112, 114. The collection of the electrons and holes at the upper and lower electrodes 112, 114 generates an electric potential difference in the cell 100. The voltage difference in the cell 100 may be added to the potential difference that is generated in additional cells (not shown). As described below, the potential difference generated in a plurality of cells 100 serially coupled with one another may be added together to increase the total potential difference generated by the cells 100. Electric current is generated by the flow of electrons and holes between neighboring cells 100. The current may be drawn from the cells 100 and applied to an external electric load.

[0021] The components and layers of the cell 100 are schematically illustrated in Figure 1, and the shape, orientation and relative sizes of the components and layers that are shown in Figure 1 are not intended to be limiting. The substrate 102 is located at the bottom of the cell 100, or on the side of the cell 100 that is opposite the side that receives incident light that is converted into electricity. The substrate 102 provides mechanical support to the other layers and components of the cell 100. The substrate 102 includes, or is formed from, a dielectric material, such as a non-conductive material. The substrate 102 may be formed from a dielectric having a relatively low softening point, such as one or more dielectric materials having a softening point below about 750 degrees Celsius. By way of example only, the substrate 102 may be formed from soda-lime float glass, low iron float glass or a glass that includes at least 10 percent by weight of sodium oxide ($Na_2O$). In another example, the substrate may be formed from another type of glass, such as float glass or borosilicate glass. Alternatively, the substrate 102 is formed from a ceramic, such as silicon nitride ($Si_3N_4$) or aluminum oxide (alumina, or $Al_2O_3$). In another embodiment, the substrate 102 is formed from a conductive material, such as a metal. By way of example only, the substrate 102 may be formed from stainless steel, aluminum, or titanium.

[0022] The substrate 102 has a thickness that is sufficient to mechanically support the remaining layers of the cell 100 while providing mechanical and thermal stability to the cell 100 during manufacturing and handling of the cell 100. The substrate 102 is at least approximately 0.7 to 5.0 millimeters thick in one embodiment. By way of example only, the substrate 102 may be an approximately 2 millimeter thick layer of float glass. Alternatively, the substrate 102 may be an approximately 1.1 millimeter thick layer of borosilicate glass. In another embodiment, the substrate 102 may be an approximately 3.3 millimeter thick layer of low iron or standard float glass.

[0023] A textured template layer 116 may be deposited above the substrate 102. Alternatively, the template layer 116 is not included in the cell 100. The template layer 116 is a layer having a controlled and predetermined three dimensional texture that imparts the texture onto one or more of the layers and components in the cell 100 that are deposited onto or above the template layer 116. In one embodiment, the texture template layer 116 may be deposited and formed in accordance with one of the embodiments described in co-pending U.S. Nonprovisional Patent Application Serial No. 12/762,880, entitled "Photovoltaic Cells And Methods To Enhance Light Trapping In Thin Film Silicon," and filed April 19, 2010 ("'880 Application"). The entire disclosure of the '880 Application is incorporated by reference herein in its entirety. With respect to the '880 Application, the texture of the template layer 116 may be determined by the shape and dimensions of one or more structures 200, 300, 400 (shown in Figures 2 through 4) of the template layer 116. The template layer 116 is deposited above the substrate 102. For example, the template layer 116 may directly deposited onto the substrate 102.

[0024] Figure 2 schematically illustrates peak structures 200 in the template layer 116 in accordance with one embodiment. The peak structures 200 are created in the template layer 116 to impart a predetermined texture in layers above the template layer 116. The structures 200 are referred to as peak structures 200 as the structures 200 appear as sharp peaks along an upper surface 202 of the template layer 116. The peak structures 200 are defined by one or more parameters, including a peak height (Hpk) 204, a pitch 206, a transitional shape 208, and a base width (Wb) 210. As shown in Figure 2, the peak structures 200 are formed as shapes that decrease in width as the distance from the substrate 102 increases. For example, the peak structures 200 decrease in size from bases 212 located at or near the substrate 102 to several peaks 214. The peak structures 200 are represented as triangles in the two dimensional view of Figure 2, but alternatively may have a pyramidal or conical shape in three dimensions.

[0025] The peak height (Hpk) 204 represents the average or median distance of the peaks 214 from the transitional shapes 208 between the peak structures 200. For example, the template layer 116 may be deposited as an approximately flat layer up to the bases 212 of the peaks 214, or to the area of the transitional shape 208. The template layer 116 may continue to be deposited in order to form the peaks 214. The distance between the bases 212 or transitional shape 208 to the peaks 214 may be the peak height (Hpk) 204.

[0026] The pitch 206 represents the average or median distance between the peaks 214 of the peak structures 200. The pitch 206 may be approximately the same in two or more directions. For example, the pitch 206 may be the same in two perpendicular directions that extend parallel to the substrate 102. In another embodiment, the pitch 206 may differ along different directions. Alternatively, the pitch 206 may represent the average or median distance between other similar points on adjacent peak structures 200. The transitional shape 208 is the general shape of the upper surface 202 of the template layer 116 between the peak structures 200. As shown in the illustrated embodiment, the transitional shape 208 can take the form of a flat “facet.” Alternatively, the flat facet shape may be a cone or pyramid when viewed in three dimensions. The base width (Wb) 210 is the average or median distance across the peak structures 200 at an interface between the peak structures 200 and the base 212 of the template layer 116. The base width (Wb) 210 may be approximately the same in two or more directions. For example, the base width (Wb) 210 may be the same in two perpendicular directions that extend parallel to the substrate 102. Alternatively, the base width (Wb) 210 may differ along different directions.

[0027] Figure 3 illustrates valley structures 300 of the template layer 116 in accordance with one embodiment. The shapes of the valley structures 300 differ from the shapes of the peak structures 200 shown in Figure 2 but may be defined by the one or more of the parameters described above in connection with Figure 2. For example, the valley structures 300 may be defined by a peak height (Hpk) 302, a pitch 304, a transitional shape 306, and a base width (Wb) 308. The valley structures 300 are formed as recesses or cavities that extend into the template layer 116 from an upper surface 310 of the valley structures 300. The valley structures 300 are shown as having a parabolic shape in the two dimensional view of Figure 3, but may have conical, pyramidal, or paraboloid shapes in three dimensions. In operation, the valley structures 300 may vary slightly from the shape of an ideal parabola.

[0028] In general, the valley structures 300 include cavities that extend down into the template layer 116 from the upper surface 310 and toward the substrate 102. The valley structures 300 extend down to low points 312, or nadirs, of the template layer 116 that are located between the transition shapes 306. The peak height (Hpk) 302 represents the average or median distance between the upper surface 310 and the low points 312. The pitch 304 represents the average or median distance between the same or common points of the valley structures 300. For example, the pitch 304 may be the distance between the midpoints of the transition shapes 306 that extend between the valley structures 300. The pitch 304 may be approximately the same in two or more directions. For example, the pitch 304 may be the same in two perpendicular directions that extend parallel to the substrate 102. In another embodiment, the pitch 304 may differ along different directions. Alternatively, the pitch 304 may represent the distance between the low points 312 of the valley structures 300. Alternatively, the pitch 304 may represent the average or median distance between other similar points on adjacent valley structures 300.

[0029] The transitional shape 306 is the general shape of the upper surface 310 between the valley structures 300. As shown in the illustrated embodiment, the transitional shape 306 can take the form of a flat "facet." Alternatively, the flat facet shape may be a cone or pyramid when viewed in three dimensions. The base width (Wb) 308 represents the average or median distance between the low points 312 of adjacent valley structures 300. Alternatively, the base width (Wb) 308 may represent the distance between the midpoints of the transition shapes 306. The base width (Wb) 308 may be approximately the same in two or more directions. For example, the base width (Wb) 308 may be the same in two perpendicular directions that extend parallel to the substrate 102. Alternatively, the base width (Wb) 308 may differ along different directions.

[0030] Figure 4 illustrates rounded structures 400 of the template layer 116 in accordance with one embodiment. The shapes of the rounded structures 400 differ from the shapes of the peak structures 200 shown in Figure 2 and the valley structures 300 shown in Figure 3, but may be defined by the one or more of the parameters described above in connection with Figures 2 and 3. For example, the rounded structures 400 may be defined by a peak height (Hpk) 402, a pitch 404, a transitional shape 406, and a base width (Wb) 408. The rounded structures 400 are formed as protrusions of an upper surface 414 of the template layer 114 that extend upward from a base film 410 of the template layer 114. The rounded structures 400 may have an approximately parabolic or rounded shape. In operation, the rounded structures 400 may vary slightly from the shape of an ideal parabola. While the rounded structures 400 are represented as parabolas in the two dimensional view of Figure 4, alternatively the rounded structures

400 may have the shape of a three dimensional paraboloid, pyramid, or cone that extends upward away from the substrate 102.

[0031] In general, the rounded structures 400 project upward from the base film 410 and away from the substrate 102 to rounded high points 412, or rounded apexes. The peak height (Hpk) 402 represents the average or median distance between the base film 410 and the high points 412. The pitch 404 represents the average or median distance between the same or common points of the rounded structures 400. For example, the pitch 404 may be the distance between the high points 412. The pitch 404 may be approximately the same in two or more directions. For example, the pitch 404 may be the same in two perpendicular directions that extend parallel to the substrate 102. Alternatively, the pitch 404 may differ along different directions. In another example, the pitch 404 may represent the distance between midpoints of the transition shapes 406 that extend between the rounded structures 400. Alternatively, the pitch 404 may represent the average or median distance between other similar points on adjacent rounded structures 400.

[0032] The transitional shape 406 is the general shape of the upper surface 414 between the rounded structures 400. As shown in the illustrated embodiment, the transitional shape 406 can take the form of a flat “facet.” Alternatively, the flat facet shape may be a cone or pyramid when viewed in three dimensions. The base width (Wb) 408 represents the average or median distance between the transition shapes 406 on opposite sides of a rounded structure 400. Alternatively, the base width (Wb) 408 may represent the distance between the midpoints of the transition shapes 406.

[0033] In accordance with one embodiment, the pitch 204, 302, 402 and/or base width (Wb) 210, 308, 408 of the structures 200, 300, 400 are approximately 400 nanometers to approximately 1500 nanometers. Alternatively, the pitch 204, 302, 402 of the structures 200, 300, 400 may be smaller than approximately 400 nanometers or larger than approximately 1500 nanometers. The average or median peak height (Hpk)

204, 302, 402 of the structures 200, 300, 400 may be approximately 25 to 80% of the pitch 206, 304, 404 for the corresponding structure 200, 300, 400. Alternatively, the average peak height (Hpk) 204, 302, 402 may be a different fraction of the pitch 206, 304, 404. The base width (Wb) 210, 308, 408 may be approximately the same as the pitch 206, 304, 404. In another embodiment, the base width (Wb) 210, 308, 408 may differ from the pitch 206, 304, 404. The base width (Wb) 210, 308, 408 may be approximately the same in two or more directions. For example, the base width (Wb) 210, 308, 408 may be the same in two perpendicular directions that extend parallel to the substrate 102. Alternatively, the base width (Wb) 210, 308, 408 may differ along different directions.

[0034] The parameters of the structures 200, 300, 400 in the template layer 116 may vary based on whether the PV cell 100 (shown in Figure 1) is a dual- or triple-junction cell 100 and/or on which of the semiconductor films or layers in the stacks 106, 108, 110 (shown in Figure 1) is the current-limiting layer. For example, the layer stacks 106, 108, 110 may include three or more stacks of N-I-P and/or P-I-N doped amorphous or doped microcrystalline silicon layers. One or more parameters described above may be based on which of the semiconductor layers in the N-I-P and/or P-I-N stacks is the current-limiting layer. For example, one or more of the layers in the N-I-P and/or P-I-N stacks may limit the amount of current that is generated by the PV cell 100 when light strikes the PV cell 100. One or more of the parameters of the structures 200, 300, 400 may be based on which of these layers is the current-limiting layer.

[0035] In one embodiment, if the PV cell 100 (shown in Figure 1) includes a microcrystalline silicon layer in one or more of the layer stacks 106, 108, 110 (shown in Figure 1) and the microcrystalline silicon layer is the current limiting layer of the layer stacks 106, 108, 110, the pitch 206, 304, 404 of the structures 200, 300, 400 in the template layer 116 below the microcrystalline silicon layer may be between approximately 500 and 1500 nanometers. The microcrystalline silicon layer has an energy band gap that corresponds to infrared light having wavelengths between approximately 500 and 1500 nanometers. For example, the structures 200, 300, 400 may reflect an increased amount of infrared light having wavelengths of between 500 and 1500 nanometers if the pitch 206, 404, 504 is approximately matched to the wavelengths. The transitional shape 208, 306, 406 of the structures 200, 300, 400 may be a flat facet and the base width (Wb) 210, 308, 408 may be 60% to 100% of the pitch 206, 304, 404. The peak height (Hpk) 204, 302, 402 may be between 25% to 75% of the pitch 206, 304, 404. For example, a ratio of the peak height (Hpk) 204, 302, 402 to the pitch 206, 304, 404 may provide scattering angles in the structures 200, 300, 400 that reflect more light back into the silicon layer stacks 106, 108, 110 relative to other ratios.

[0036] In another example, if the PV cell 100 (shown in Figure 1) includes one or more layer stacks 106, 108, 110 being formed of or including amorphous silicon, the range of pitches 206, 304, 404 for the template layer 116 may vary based on which of the layer stacks 106, 108, 110 (shown in Figure 1) is the current limiting stack. If the upper and/or middle layer stacks 106, 108 include microcrystalline N-I-P or P-I-N doped semiconductor layer stacks, the lower layer stack 110 includes an amorphous N-I-P or P-I-N doped semiconductor layer stack, and the upper and/or middle layer stack 106, 108 is the current limiting layer, then the pitch 206, 304, 504 may be between approximately 500 and 1500 nanometers. In contrast, if the lower silicon layer stack 108 is the current limiting layer, then the pitch 206, 304, 404 may be between approximately 350 and 1000 nanometers.

[0037] Returning to the discussion of the cell 100 shown in Figure 1, the template layer 116 may be formed in accordance with one or more of the embodiments described in the ‘880 Application. For example, the template layer 116 may be formed by depositing an amorphous silicon layer onto the substrate 102 followed by texturing the amorphous silicon using reactive ion etching through silicon dioxide spheres placed on the upper surface of the amorphous silicon. Alternatively, the template layer 116 may be formed by sputtering an aluminum and tantalum bilayer on the substrate 102 and then anodizing the template layer 116. In another embodiment, the template layer may be formed by depositing a film of textured fluorine-doped tin oxide ($SnO_2$:F) using atmospheric chemical vapor deposition. One or more of these films of the template layer 116 may be obtained from a vendor such as Asahi Glass Company or Pilkington Glass. In an alternative embodiment, the template layer 116 may be formed by applying an electrostatic charge to the substrate 102 and then placing the charged substrate 102 in an environment having oppositely charged particles. Electrostatic forces attract the charged particles to the substrate 102 to form the template layer 116. The particles are subsequently permanently attached to the substrate 102 by depositing an adhesive "glue" layer (not shown) onto the particles in a subsequent deposition step or by annealing the particles and substrate 102. Examples of particle materials include faceted ceramics and diamond like material particles such as silicon carbide, alumina, aluminum nitride, diamond, and CVD diamond.

[0038] The lower electrode 114 is deposited above the template layer 116. The lower electrode 114 is comprised of a conductive reflector layer 118 and a conductive buffer layer 120. The reflector layer 118 is deposited above the template layer 116. For example, the reflector layer 118 may be directly deposited onto the template layer 116. The reflector layer 118 has a textured upper surface 122 that is dictated by the template layer 116. For example, the reflector layer 118 may be deposited onto the template layer 116 such that the reflector layer 118 includes structures (not shown) that are similar in size and/or shape to the structures 200, 300, 400 (shown in Figures 2 through 4) of the template layer 116.

[0039] The reflector layer 118 may include, or be formed from, a reflective conductive material, such as silver. Alternatively, the reflector layer 118 may include, or be formed from, aluminum or an alloy that includes silver or aluminum. The reflector layer 118 is approximately 100 to 300 nanometers in thickness in one embodiment and may be deposited by sputtering the material(s) of the reflector layer 118 onto the template layer 116.

[0040] The reflector layer 118 provides a conductive layer and a reflective surface for reflecting light upward into the layer stacks 106, 108. For example, a portion of the light that is incident on the cover layer 104 and that passes through the layer stacks 106, 108 may not be absorbed by the layer stacks 106, 108. This portion of the light may reflect off of the reflector layer 118 back into the layer stacks 106, 108 such that the reflected light may be absorbed by the layer stacks 106, 108. The textured upper surface 122 of the reflector layer 118 increases the amount of light that is absorbed, or "trapped" via partial or full scattering of the light into the plane of the layer stacks 106, 108. The peak height (Hpk) 204, 302, 403, pitch 206, 304, 404, transitional shape 208, 306, 406, and/or base width (Wb) 210, 308, 408 (shown in Figures 2 through 4) may be varied to increase the amount of light that is trapped in the layer stacks 106, 108, 110 for a desired or predetermined range of wavelengths of incident light.

[0041] The buffer layer 120 is deposited above the reflector layer 118 and may be directly deposited onto the reflector layer 118. The buffer layer 120 provides an electric contact to the lower layer stack 108. For example, the buffer layer 120 may include, or be formed from, a transparent conductive oxide (TCO) material that is electrically coupled with the active silicon layers in the lower layer stack 108. In one embodiment, the buffer layer 120 includes aluminum doped zinc oxide, zinc oxide and/or indium tin oxide. The buffer layer 120 may be deposited in a thickness of approximately 50 to 500 nanometers, although a different thickness may be used.

[0042] In one embodiment, the buffer layer 120 provides a chemical buffer between the reflector layer 118 and the lower layer stack 108. For example, the buffer layer 120 may prevent chemical attack on the lower layer stack 108 by the reflector layer 118 during processing and manufacture of the cell 100. The buffer layer 120 impedes or prevents contamination of the silicon in the lower layer stack 108 and may reduce plasmon absorption losses in the lower layer stack 108.

[0043] The buffer layer 120 may provide an optical buffer between the reflector layer 118 and the lower layer stack 108. For example, the buffer layer 120 may be a light transmissive layer that is deposited in at thickness that increases the amount of light within a predetermined range of wavelengths that is reflected off of the reflector layer 118. The thickness of the buffer layer 120 may permit certain wavelengths of light to pass through the buffer layer 120, reflect off of the reflector layer 118, pass back through the buffer layer 120 and into the lower layer stack 108. By way of example only, the buffer layer 120 may be deposited at a thickness of approximately 75 to 80 nanometers.

[0044] The lower layer stack 108 is deposited above, or directly onto, the lower electrode 114. The lower layer stack 108 may be deposited at a thickness of approximately 100 to 600 nanometers, although the lower layer stack 108 may be deposited at other thicknesses. The lower layer stack 108 includes three sublayers 132, 134, 136 of silicon in one embodiment.

[0045] The sublayers 132, 134, 136 may be n-doped, intrinsic, and p-doped amorphous silicon (a-Si:H) films, respectively. For example, the sublayers 132, 134, 136 may form an amorphous N-I-P junction or layer stack. In one embodiment, the lower layer stack 108 is deposited as a junction stack of silicon layers without including, or in the absence of, germanium (Ge) in the sublayers 132, 134, 136. For example, the lower layer stack 108 may have 0.01% or less germanium content. The germanium content represents the amount of germanium in the lower layer stack 108 relative to the other materials in the lower layer stack 108. The sublayers 132, 134, 136 may be deposited using plasma enhanced chemical vapor deposition (PECVD) at relatively high deposition temperatures. For example, the sublayers 132, 134, 136 may be deposited at temperatures of approximately 200 to 350 degrees Celsius. In one embodiment, the two lower sublayers 132, 134 are deposited at temperatures of approximately 250 to 350 degrees Celsius while the top sublayer 136 is deposited at a temperature of approximately

200 degrees Celsius. For example, the top sublayer 136 may be deposited at a temperature between 150 and 250 degrees Celsius.

[0046] The deposition of the sublayers 132, 134, 136 at relatively high deposition temperatures may decrease the energy band gap of the lower layer stack 108 relative to amorphous silicon layers that are deposited at lower deposition temperatures. As the deposition temperature of amorphous silicon increases, the energy band gap of the silicon may decrease. For example, depositing the sublayers 132, 134, 136 as amorphous silicon layers at temperatures between approximately 200 and 350 degrees Celsius may cause the band gap of the lower layer stack 108 to be approximately 1.60 to 1.80 eV, such as at least 1.65 eV. Decreasing the band gap of the lower layer stack 108 may cause the sublayers 132, 134, 136 to absorb a larger subset of the spectrum of wavelengths in the incident light and may result in a greater electric current to be generated by a plurality of cells 100 electrically interconnected in a series.

[0047] Deposition of one or more of the sublayers 132, 134, 136 in the lower layer stack 108 at relatively high deposition temperatures may be verified by measuring the hydrogen content of the lower layer stack 108. In one embodiment, the final hydrogen content of one or more of the sublayers 132, 134, 136 is less than approximately 12 atomic percent if the sublayer(s) 132, 134, 136 were deposited at temperatures above approximately 250 degrees Celsius. In another embodiment, the final hydrogen content of one or more of the sublayers 132, 134, 136 is less than approximately 10 atomic percent if the sublayer(s) 132, 134, 136 were deposited at temperatures above approximately 250 degrees Celsius. In another embodiment, the final hydrogen content of one or more of the sublayers 132-136 is less than approximately 8 atomic percent if the sublayer(s) 132, 134, 136 were deposited at temperatures above approximately 250 degrees Celsius. The final hydrogen content in one or more of the sublayers 132-136 may be measured using Secondary Ion Mass Spectrometer ("SIMS"). A sample of one or more of the sublayers 132-136 is placed into the SIMS. The sample is then sputtered with an ion beam. The ion beam causes secondary ions to be ejected from the sample. The secondary ions are collected and analyzed using a mass spectrometer. The mass spectrometer then determines the molecular composition of the sample. The mass spectrometer can determine the atomic percentage of hydrogen in the sample. Alternatively, the final hydrogen concentration in one or more of the sublayers 132, 134, 136 may be measured using Fourier Transform Infrared spectroscopy ("FTIR"). In FTIR, a beam of infrared light is then sent through a sample of one or more of the sublayers 132, 134, 136. Different molecular structures and species in the sample may absorb the infrared light differently. Based on the relative concentrations of the different molecular species in the sample, a spectrum of the molecular species in the sample is obtained. The atomic percentage of hydrogen in the sample can be determined from this spectrum. Alternatively, several spectra are obtained and the atomic percentage of hydrogen in the sample is determined from the group of spectra.

[0048] As described below, the top sublayer 136 may be a p-doped silicon film. In one such embodiment where the top sublayer 136 is a p-doped film, the bottom and middle sublayers 132, 134 may be deposited at the relatively high deposition temperatures within the range of approximately 250 to 350 degrees Celsius while the top sublayer 136 is deposited at a relatively lower temperature within the range of approximately 150 to 200 degrees Celsius. The p-doped top sublayer 136 is deposited at the lower temperature to reduce the amount of interdiffusion between the p-doped top sublayer 136 and the intrinsic middle sublayer 134. Depositing the p-doped top sublayer 136 at a lower temperature may increase the band gap of the top sublayer 136 and/or makes the top sublayer 136 more transmissive of visible light.

[0049] The bottom sublayer 132 may be an amorphous layer of n-doped silicon. In one embodiment, the bottom sublayer 132 is deposited in a PECVD chamber with an operating frequency of approximately 13.56 MHz using a source gas combination of hydrogen ($H_2$), silane ($SiH_4$) and phosphine, or phosphorus trihydride ($PH_3$) at a vacuum pressure of approximately 1 to 3 torr and at an energy of approximately 200 to 400 Watts. The ratio of source gases used to deposit the bottom sublayer 132 may be approximately 4 to 12 parts hydrogen gas to approximately 1 part silane to approximately 0.007 parts phosphine.

[0050] The middle sublayer 134 may be an amorphous layer of intrinsic silicon. Alternatively, the middle sublayer 134 may be a polymorphous layer of intrinsic silicon. In one embodiment, the middle sublayer 134 is deposited in a PECVD chamber with an operating frequency of approximately 13.56 MHz using a source gas combination of hydrogen (H) and silane ($SiH_4$) at a vacuum pressure of approximately 1 to 3 torr and at an energy of approximately 100 to 400 Watts. The ratio of source gases used to deposit the middle sublayer 134 may be approximately 4 to 12 parts hydrogen gas to approximately 1 part silane.

[0051] In one embodiment, the top sublayer 136 is a protocrystalline layer of p-doped silicon. Alternatively, the top sublayer 136 may be an amorphous layer of p-doped silicon. In one embodiment, the top sublayer 136 is deposited at a temperature of approximately 200 degrees Celsius in a PECVD chamber with an operating frequency of approximately 13.56 MHz using a source gas combination of hydrogen (H), silane ($SiH_4$), and boron trifluoride ($BF_3$), TMB, or diborane ($B_2H_6$) at a vacuum pressure of approximately 1 to 2 torr and at an energy of approximately 200 to 400 Watts. The ratio of source gases used to deposit the top sublayer 136 may be approximately 100 to 2000 parts hydrogen gas to approximately 1 part silane to approximately 0.1 to 1 part dopant gas.

[0052] The three sublayers 132, 134, 136 may form an N-I-P junction or layer stack of active silicon layers. The lower layer stack 108 may have an energy band gap that differs from the energy band gap of the upper layer stack 106. The different energy band gaps of the lower and upper layer stacks 106, 108 may permit the lower and upper layer stacks 106, 108 to absorb different wavelengths of incident light and may increase the efficiency of the cell 100 in converting incident light into electric potential and/or current.

[0053] The upper layer stack 106 is deposited above the lower layer stack 108. For example, the upper layer stack 106 may be directly deposited onto the lower layer stack 108. In one embodiment, the upper layer stack 106 is deposited at a thickness of approximately 50 to 200 nanometers, although the upper layer stack 106 may be deposited at a different thickness. The upper layer stack 106 may include three sublayers 138, 140, 142 of silicon. In one embodiment, the sublayers 138, 140, 142 are n-doped, intrinsic, and p-doped amorphous silicon (a-Si:H) films that form an N-I-P junction or layer stack. The sublayers 138, 140, 142 may be deposited using plasma enhanced chemical vapor deposition (PECVD) at relatively low deposition temperatures. For example, the sublayers 138, 140, 142 may be deposited at a temperature of approximately 150 to 220 degrees Celsius.

[0054] The deposition of the sublayers 138, 140, 142 at relatively lower deposition temperatures may reduce interdiffusion of dopants between the sublayers 132, 134, 136 in the lower layer stack 108 and/or between the sublayers 138, 140, 142 in the upper layer stack 106. The diffusion of dopants in and between the sublayers 132, 134, 136, 138, 140, 142 increases as the temperature at which the sublayers 132, 134, 136, 138, 140, 142 are heated also increases. Using lower deposition temperatures may reduce the amount of dopant interdiffusion in the sublayers 132, 134, 136, 138, 140, 142. Use of lower deposition temperatures in a given sublayer 132, 134, 136, 138, 140, 142 may reduce hydrogen evolution from the underlying sublayers 132, 134, 136, 138, 140, 142 in the cell 100.

[0055] The deposition of the sublayers 138, 140, 142 at relatively lower deposition temperatures may increase the energy band gap of the upper layer stack 106 relative to amorphous silicon layers that are deposited at higher deposition temperatures. For example, depositing the sublayers 138, 140, 142 as amorphous silicon layers at temperatures between approximately 150 and 200 degrees Celsius may cause the band gap of the upper layer stack 106 to be approximately 1.80 to 2.00 eV. Increasing the band gap of the upper layer stack 106 may cause the upper layer stack 106 to absorb a smaller subset of the spectrum of wavelengths in the incident light, but may increase the electric potential difference generated in the cell 100.

[0056] The bottom sublayer 138 may be an amorphous layer of n-doped silicon. In one embodiment, the bottom sublayer 130 is deposited at a temperature between approximately 150 and 220 degrees Celsius in a PECVD chamber with an operating frequency of approximately 13.56 MHz using a source gas combination of hydrogen ($H_2$), silane ($SiH_4$) and phosphine, or phosphorus trihydride ($PH_3$) at a vacuum pressure of approximately 1 to 3 torr and at an energy of approximately 200 to 400 Watts. The ratio of source gases used to deposit the bottom sublayer 138 may be approximately 4 to 12 parts hydrogen gas to approximately 1 part silane to approximately 0.005 parts phosphine.

[0057] The middle sublayer 140 may be an amorphous layer of intrinsic silicon. Alternatively, the middle sublayer 140 may be a polymorphous layer of intrinsic silicon. In one embodiment, the middle sublayer 140 is deposited at a temperature between approximately 150 and 220 degrees Celsius in a PECVD chamber with an operating frequency of approximately 13.56 MHz using a source gas combination of hydrogen (H) and silane ($SiH_4$) at a vacuum pressure of approximately 1 to 3 torr and at an energy of approximately 200 to 400 Watts. The ratio of source gases used to deposit the middle sublayer 140 may be approximately 4 to 20 parts hydrogen gas to approximately 1 part silane.

[0058] In one embodiment, the top sublayer 142 is a protocrystalline layer of p-doped silicon. Alternatively, the top sublayer 142 may be an amorphous layer of p-doped silicon. In one embodiment, the top sublayer 142 is deposited at a temperature between approximately 150 and 200 degrees Celsius in a PECVD chamber with an operating frequency of approximately 13.56 MHz using a source gas combination of hydrogen (H), silane ($SiH_4$), and boron trifluoride ($BF_3$), TMB, or diborane ($B_2H_6$) at a vacuum pressure of approximately 1 to 2 torr and at an energy of approximately 2000 to

3000 Watts. The ratio of source gases used to deposit the top sublayer 142 may be approximately 100 to 200 parts hydrogen gas to approximately 1 part silane to approximately 0.1 to 1 part dopant gas.

[0059] As described above, the upper and lower layer stacks 106, 108 may have different energy band gaps to each absorb different subsets of a spectrum of incident light wavelengths. In one embodiment, the layer stacks 106, 108 may each absorb a different set of wavelengths of light, with two or more of the layer stacks 106, 108 absorbing at least partially overlapping spectra of the wavelengths of incident light. The upper layer stack 106 may have a larger energy band gap than the lower layer stack 108. The different energy band gaps in the cell 100 may enable the cell 100 to covert a significant portion of the incident light into electric current. For example, the lowest energy band gap of the lower layer stack 108 may enable the lower layer stack 108 to absorb the longest wavelengths of incident light while the largest energy band gap of the upper layer stack 106 may enable the upper layer stack 106 to absorb smaller wavelengths of incident light relative to the lower layer stack 108. For example, the upper layer stack 106 may absorb a range of wavelengths of visible incident light while providing the largest electric potential of the layer stacks 106, 108.

[0060] The energy band gaps of the layer stacks 106, 108 may be measured using ellipsometry. Alternatively, an external quantum efficiency (EQE) measurement may be used to obtain the energy band gaps of the layer stacks 106, 108. The EQE measurement is obtained by varying wavelengths of light that are incident upon a semiconductor layer or layer stack and measuring the efficiency of the layer or layer stack in converting incident photons into electrons that reach the external circuit. Based on the efficiencies of the layer stacks 106, 108 in converting incident light into electrons at different wavelengths, the energy band gaps of the layer stacks 106, 108 may be derived. For example, each of the layer stacks 106, 108 may be more efficient in converting incident light having an energy that is greater than the band gap of the particular layer stack 106, 108 than the particular layer stack 106, 108 is in converting light of a different energy.

[0061] The upper electrode 112 is deposited above the upper layer stack 106. For example, the upper electrode 112 may be directly deposited onto the upper layer stack 106. The upper electrode 112 includes, or is formed from, a conductive and light transmissive material. For example, the upper electrode 112 may be formed from a transparent conductive oxide. Examples of such materials include zinc oxide ($ZnO$), tin oxide ($SnO_2$), fluorine doped tin oxide ($SnO_2$:F), tin-doped indium oxide (ITO), titanium dioxide ($TiO_2$), and/or aluminum-doped zinc oxide (Al:ZnO). The upper electrode 112 can be deposited in a variety of thicknesses. In some embodiments, the upper electrode 112 is approximately 50 nanometers to 2 micrometers thick.

[0062] In one embodiment, the upper electrode 112 is formed from a 60 to 90 nanometer thick layer of ITO or Al:ZnO. The upper electrode 112 may function as both a conductive material and a light transmissive material with a thickness that creates an anti-reflection (AR) effect in the upper electrode 112 of the cell 100. For example, the upper electrode 112 may permit a relatively large percentage of one or more wavelengths of incident light to propagate through the upper electrode 112 while reflecting a relatively small percentage of the wavelength(s) of light to be reflected by the upper electrode 112 and away from the active layers of the cell 100. By way of example only, the upper electrode 112 may reflect approximately 5% or less of one or more of the desired wavelengths of incident light away from the layer stacks 106, 108. In another example, the upper electrode 112 may reflect approximately 3% or less of the desired wavelengths of incident light away from the layer stacks 106, 108. In another embodiment, the upper electrode 112 may reflect approximately 2% or less of the desired wavelengths of incident light away from the layer stacks 106, 108. In yet another example, the upper electrode 112 may reflect approximately 1% or less of the desired wavelengths of incident light away from the layer stacks 106, 108. The thickness of the upper electrode 112 may be adjusted to change the desired wavelengths of incident light that propagate through the upper electrode 112 and down into the layer stacks 106, 108. Although the sheet resistance of relatively thin upper electrodes 112 may be relatively high in one or more embodiments, such as approximately 20 to 50 ohms per square, the relatively high sheet resistance of the upper electrode 112 may be compensated for by decreasing a width of the upper electrodes 112 in each cell 100 of a photovoltaic module, as described below.

[0063] An adhesive layer 144 is deposited above the upper electrode 112. For example, the adhesive layer 144 may be deposited directly on the upper electrode 112. Alternatively, the adhesive layer 144 is not included in the cell 100. The adhesive layer 144 secures the cover layer 104 to the upper electrode 112. The adhesive layer 144 may prevent moisture ingress into the cell 100. The adhesive layer 144 may include a material such as a polyvinyl butyral ("PVB"), surlyn, or ethylene-vinyl acetate ("EVA") copolymer, for example.

[0064] The cover layer 104 is placed above the adhesive layer 144. Alternatively, the cover layer 104 is placed on the upper electrode 112. The cover layer 104 includes or is formed from a light transmissive material. In one embodiment, the cover layer 104 is a sheet of tempered glass. The use of tempered glass in the cover layer 104 may help to protect the cell 100 from physical damage. For example, a tempered glass cover layer 104 may help protect the cell 100 from hailstones and other environmental damage. In another embodiment, the cover layer 104 is a sheet of soda-lime glass, low-iron tempered glass, or low-iron annealed glass. The use of a highly transparent, low-iron glass cover layer 104 can improve the transmission of light to the layer stacks 106, 108. Optionally, an anti-reflective (AR) coating (not shown) may be provided on the top of the cover layer 104.

[0065] Figure 5 is a schematic diagram of a substrate configuration photovoltaic device 500 and a magnified view 502 of the device 500 according to one embodiment. The device 500 includes a plurality of photovoltaic cells 504 electrically coupled in series with one another. The cells 504 may be similar to the cells 100 (shown in Figure 1). For example, each of the cells 504 may have a tandem arrangement of the layer stacks 106, 108 (shown in Figure 1), that each absorb a different subset of the spectrum of wavelengths of light. In one embodiment, the spectrum of wavelengths of light that is absorbed by two or more of the layer stacks in the cells 504 may at least partially overlap one another. The schematic illustration of Figure 1 may be a cross-sectional view of the device 500 along line 1-1 in Figure 5. The device 500 may include many cells 504 electrically coupled with one another in series. By way of example only, the device 500 may have twenty-five, fifty, or one hundred or more cells 504 connected with one another in a series. Each of the outermost cells 504 also may be electrically connected with one of a plurality of leads 506, 508. The leads 506, 508 extend between opposite ends 510, 512 of the device 500. The leads 506, 508 are connected with an external electrical load 510. The electric current generated by the device 500 is applied to the external load 510.

[0066] As described above, each of the cells 504 includes several layers. For example, each cell 504 includes a substrate 512 that is similar to the substrate 102 (shown in Figure 1), a lower electrode 514 that is similar to the lower electrode 114 (shown in Figure 1), a multi-layer stack 516 of semiconductor materials, an upper electrode 518 that is similar to the upper electrode 112 (shown in Figure 1), an adhesive layer 520 that is similar to the adhesive layer 144 (shown in Figure 1) and a cover layer 522 that is similar to the cover layer 104 (shown in Figure 1). The multi-layer stack 516 may include upper, middle and lower junction stacks of active silicon layers that each absorb or trap a different subset of the spectrum of wavelengths of light that is incident on the device 500. For example, the multi-layer stack 516 may include an upper layer stack that is similar to the upper layer stack 106 (shown in Figure 1) and a lower layer stack that is similar to the lower layer stack 108 (shown in Figure 1). The device 500 is a substrate configuration device because light is incident on the cover layer 522 which is disposed opposite of the substrate 512.

[0067] The upper electrode 518 of one cell 504 is electrically coupled with the lower electrode 514 in a neighboring, or adjacent, cell 504. As described above, the collection of the electrons and holes at the upper and lower electrodes 518, 514 generates a voltage difference in each of the cells 504. The voltage difference in the cells 504 may be additive across multiple cells 504 in the device 500. The electrons and holes flow through the upper and lower electrodes 518, 514 in one cell 504 to the opposite electrode 518, 514 in a neighboring cell 504. For example, if the electrons in a first cell 504 flow to the lower electrode 514 in a when light strikes the tandem layer stack 516, then the electrons flow through the lower electrode 514 of the first cell 504 to the upper electrode 518 in a second cell 504 that is adjacent to the first cell 504. Similarly, if the holes flow to the upper electrode 518 in the first cell 504, then the holes flow from the upper electrode 518 in the first cell 504 to the lower electrode 514 in the second cell 504. Electric current and voltage is generated by the flow of electrons and holes through the upper and lower electrodes 518, 514. The current is applied to the external load 510.

[0068] The device 500 may be a monolithically integrated solar module similar to one or more of the embodiments described in co-pending U.S. Application Serial No. 12/569,510, filed September 29, 2009, and entitled “Monolithically-Integrated Solar Module” (“‘510 Application”). The entire disclosure of the ‘510 Application is incorporated by reference herein. For example, in order to create the shapes of the lower and upper electrodes 514, 518 and the tandem layer stack 516 in the device 500, the device 500 may be fabricated as a monolithically integrated module as described in the ‘510 Application. In one embodiment, portions of the lower electrode 514 are removed to create lower separation gaps 524. The portions of the lower electrode 514 may be removed using a patterning technique on the lower electrode 514. For example, a laser light that scribes the lower separation gaps 524 in the lower electrode 514 may be used to create the lower separation gaps 524. After removing portions of the lower electrode 514 to create the lower separation gaps 524, the remaining portions of the lower electrode 514 are arranged as linear strips extending in directions transverse to the plane of the magnified view 502.

[0069] The multi-layer stack 516 is deposited on the lower electrode 514 such that the multi-layer stack 516 fills in the volumes in the lower separation gaps 524. The multi-layer stack 516 is then exposed to a focused beam of energy, such as a laser beam, to remove portions of the multi-layer stack 516 and provide inter-layer gaps 526 in the multi-layer stack 516. The inter-layer gaps 526 separate the multi-layer stacks 516 of adjacent cells 504. After removing portions of the multi-layer stacks 516 to create the inter-layer gaps 526, the remaining portions of the multi-layer stacks 516 are arranged as linear strips extending in directions transverse to the plane of the magnified view 502.

[0070] The upper electrode 518 is deposited on the multi-layer stack 516 and on the lower electrode 514 in the inter-layer gaps 526. In one embodiment, the conversion efficiency of the device 500 may be increased by depositing a relatively thin upper electrode 518 with a thickness that is adjusted or tuned to provide an anti-reflection (AR) effect. For example, a thickness 538 of the upper electrode 518 may be adjusted to increase the amount of visible light that is transmitted through the upper electrode 518 and into the multi-layer stack 516. The amount of visible light that is transmitted through the upper electrode 518 may vary based on the wavelength of the incident light and the thickness of the upper electrode 518. One thickness of the upper electrode 518 may permit more light of one wavelength to propagate through the upper electrode 518 than light of other wavelengths. By way of example only, the upper electrode 518 may be deposited at a thickness of approximately 60 to 90 nanometers.

[0071] The AR effect provided by the upper electrode 518 may increase the total electrical power generated by the device 500 as more light may propagate through the upper electrode 518 to the multi-layer stack 516. The increased power output arising from the anti-reflection effect provided by the upper electrode 518 may be sufficient to overcome at least some, if not all, of the energy losses, such as the $I^2R$

losses, that occur in the upper electrode 518. For example, the increased amount of photocurrent that results from an increased amount of light passing through the upper electrode 518 may overcome or at least partially compensate for the $I^2R$ power loss associated with the relatively high sheet resistance of a thin upper electrode 518. Under conditions of relatively high output voltage and relatively low current density, the $I^2R$ losses in a thin upper electrode 518 may be sufficiently small that a width 540 of the cell 504 may be as large as approximately 0.6 to 1.2 centimeters even if the sheet resistance of the upper electrode 518 is greater than 10 ohms per square, such as a sheet resistance of at least approximately 15 to 30 ohms/square. Because the width 540 of the cell 504 can be controlled in the device 500, the $I^2R$ power loss in the upper electrode 518 may be reduced without the use of a conducting grid on top of a thin upper electrode 518.

[0072] Portions of the upper electrode 518 are removed to create upper separation gaps 528 in the upper electrode 518 and electrically separate the portions of the upper electrode 518 in adjacent cells 504 from each other. The upper separation gaps 528 may be created by exposing the upper electrode 518 to a focused beam of energy, such as a laser light. The focused beam of energy may locally increase a crystalline fraction of the multi-layer stack 516 proximate to the upper separation gaps 528. For example, the crystallinity of the multi-layer stack 516 in a vertical portion 530 that extends between the upper electrode 518 and the lower electrode 514 may be increased by exposure to the focused beam of energy. Additionally, the focused beam of energy may cause diffusion of dopants within the multi-layer stack 516. The vertical portion 530 of the multi-layer stack 516 is disposed between the upper and lower electrodes 518, 514 and below a left edge 534 of the upper electrode 518. As shown in Figure 5, each of the gaps 528 in the upper electrode 518 are bounded by the left edge 534 and an opposing right edge 536 of the upper electrodes 518 in adjacent cells 504.

[0073] The crystalline fraction of the multi-layer stack 516 and the vertical portion 530 may be determined by a variety of methods. For example, Raman spectroscopy can be used to obtain a comparison of the relative volume of noncrystalline material to crystalline material in the multi-layer stack 516 and the vertical portion 530. One or more of the multi-layer stack 516 and the vertical portion 530 sought to be examined can be exposed to monochromatic light from a laser, for example. Based on the chemical content and crystal structure of the multi-layer stack 516 and the vertical portion 530, the monochromatic light may be scattered. As the light is scattered, the frequency (and wavelength) of the light changes. For example, the frequency of the scattered light can shift. The frequency of the scattered light is measured and analyzed. Based on the intensity and/or shift in the frequency of the scattered light, the relative volumes of amorphous and crystalline material of the multi-layer stack 516 and the vertical portion 530 being examined can be determined. Based on these relative volumes, the crystalline fraction in the multi-layer stack 516 and the vertical portion 530 being examined may be measured. If several samples of the multi-layer stack 516 and the vertical portion 530 are examined, the crystalline fraction may be an average of the several measured crystalline fractions.

[0074] In another example, one or more TEM images can be obtained of the multi-layer stack 516 and the vertical portion 530 to determine the crystalline fraction of the multi-layer stack 516 and the vertical portion 530. One or more slices of the multi-layer stack 516 and the vertical portion 530 being examined are obtained. The percentage of surface area in each TEM image that represents crystalline material is measured for each TEM image. The percentages of crystalline material in the TEM images can then be averaged to determine the crystalline fraction in the multi-layer stack 516 and the vertical portion 530 being examined.

[0075] In one embodiment, the increased crystallinity and/or the diffusion of the vertical portion 530 relative to a remainder of the multi-layer stack 516 forms a built-in bypass diode 532 that vertically extends through the thickness of the multi-layer stack 516 in the view shown in Figure 5. For example, the crystalline fraction and/or interdiffusion of the multi-layer stack 516 in the vertical portion 530 may be greater than the crystalline fraction and/or interdiffusion in a remainder of the multi-layer stack 516. Through control of the energy and pulse duration of the focused beam of energy, the built-in bypass diode 532 can be formed through individual ones of the individual cells 504 without creating an electrical short in the individual cells 504. The built-in bypass diode 532 provides an electrical bypass through a cell 504 in the device 500 that may prevent damage to a particular cell 504, group of cells 504, and/or device 500 when the particular cell 504 is shaded from light. For example, without the built-in bypass diodes 532, a cell 504 that is shaded or no longer exposed to light while the other cells 504 continue to be exposed to light may become reversed biased by the electric potential generated by the exposed cells 504. The electric potential generated by the light-exposed cells 504 may be built up across the shaded cell 504 at the upper and lower electrodes 518, 514 of the shaded cell 504. As a result, the shaded cell 504 may increase in temperature and, if the shaded cell 504 significantly increases in temperature, the shaded cell 504 may become permanently damaged and/or incinerate. A shaded cell 504 that does not have a built-in bypass diode 532 also may prevent electric potential or current from being generated by the entire device 500. Consequently, shaded cells 504 that do not have built-in bypass diodes 532 may result in a significant amount of wasted or lost electric current from the device 500.

[0076] With the built-in bypass diodes 532, the electric potential generated by the cells 504 that are exposed to light may bypass a shaded cell 504 that has a bypass diode 532 through the bypass diodes 532 formed at the edges of the upper separation gaps 528 of the shaded cell 504. The increased crystallinity of the portion 530 of the multi-layer stack 516 and/or interdiffusion between the upper electrode 518 and the portion 530 in the multi-layer stack 516 provides a path for electric current to pass through when the shaded cell 504 is reverse biased. For example, the reverse bias across the shaded cell 504 may be dissipated through the bypass diodes 532 as the bypass diodes 532 have a lower electrical resistance characteristic under reverse bias than the bulk of the shaded cell 504.

[0077] The presence of a built-in bypass diode 532 in a cell 504 or device 500 may be determined by comparing the electrical output of the device 500 before and after shading an individual cell 504. For example, the device 500 may be illuminated and the electrical potential generated by the device 500 is measured. One or more cells 504 may be shaded from the light while the remaining cells 504 are illuminated. The device 500 may be short circuited by joining the leads 506, 508 together. The device 500 may then be exposed to light for a predetermined time period, such as one hour. Both the shaded cells 504 and the unshaded cells 504 are then once again illuminated and the electrical potential generated by the device 500 is measured. In one embodiment, if the electrical potential before and after the shading of the cells 504 is within approximately 100 millivolts of one another, then the device 500 includes built-in bypass diodes 532. Alternatively, if the electrical potential after the shading of the cells 504 is approximately 200 to 2500 millivolts lower than the electrical potential prior to the shading of the cells 504, then the device 500 may not include the built-in bypass diodes 532.

[0078] In another embodiment, the presence of a built-in bypass diode 532 for a particular cell 504 may be determined by electrically probing the cell 504. If the cell 504 demonstrates a reversible, non-permanent diode breakdown when the cell 504 is reverse biased without illumination, then the cell 504 includes the built-in bypass diode 532. For example, if the cell 504 demonstrates greater than approximately 10 milliamps per square centimeter of leakage current when a reverse bias of approximately -5 to -8 volts is applied across the upper and lower electrodes 514, 518 of the cell 504 without illumination, then the cell 504 includes the built-in bypass diode 532.

[0079] Figure 6 is a flowchart of a process 600 for manufacturing a substrate configuration photovoltaic device in accordance with one embodiment. At 602, a substrate is provided. For example, a substrate such as the substrate 102 (shown in Figure 1) may be provided. At 604, a template layer is deposited onto the substrate. For example, the template layer 116 (shown in Figure 1) may be deposited onto the substrate

102. Alternatively, flow of the process 600 may bypass 604 along a path 606 such that no template layer is included in the photovoltaic device. At 608, a lower electrode is deposited onto the template layer or the substrate. For example, the lower electrode 114 (shown in Figure 1) may be deposited onto the template layer 116 or the substrate 102.

[0080] At 610, portions of the lower electrode are removed to separate the lower electrode of each cell in the device from one another. As described above, portions of the lower electrode may be removed using a focused beam of energy, such as a laser beam. At 612, a lower junction stack is deposited. For example, a lower N-I-P stack of silicon layers such as the lower layer stack 108 (shown in Figure 1) may be deposited onto the lower electrode 114 (shown in Figure 1). At 614, an upper junction stack is provided. For example, an upper N-I-P stack of silicon layers such as the upper layer stack 106 (shown in Figure 1) may be deposited onto the lower layer stack 108. The lower and upper layer stacks form a multi-layer stack of the device, similar to the multi-layer stack 516 (shown in Figure 5) described above.

[0081] At 616, portions of the multi-layer stack are removed between adjacent cells in the device. For example, sections of the upper and lower layer stacks 106, 108 (shown in Figure 1) may be removed between adjacent cells 504 (shown in Figure 5), as described above. In one embodiment, removal of the multi-layer stack also includes removing portions of the intermediate reflector layer between adjacent cells in the device. At 618, an upper electrode is deposited above the upper layer stack. For example, the upper electrode 112 (shown in Figure 1) may be deposited above the upper layer stack 106. At 620, portions of the upper electrode are removed. For example, portions of the upper electrode 112 are removed to separate the upper electrodes 112 of adjacent cells 504 in the device 500 (shown in Figure 5) from one another. As described above, removal of portions of the upper electrode 112 may result in the formation of built-in bypass diodes in cells of the device.

[0082] At 622, conductive leads are electrically joined to the outermost cells in the device. For example, the leads 506, 508 (shown in Figure 5) may be electrically coupled with the outermost cells 504 (shown in Figure 5) in the device 500 (shown in Figure 5). At 624, an adhesive layer is deposited above the upper electrode. For example, the adhesive layer 144 (shown in Figure 1) may be deposited above the upper electrode 112 (shown in Figure 1). At 626, a cover layer is affixed to the adhesive layer. For example, the cover layer 104 (shown in Figure 1) may be joined to the underlying layers and components of the cell 100 (shown in Figure 1) by the adhesive layer 144. At 628, a junction box is mounted to the device. For example, a junction box that is configured to deliver electric potential and/or current from the device 500 to one or more connectors may be mounted to and electrically coupled with the device 500.

[0083] It is to be understood that the above description is intended to be illustrative, and not restrictive. For example, the above-described embodiments (and/or aspects thereof) may be used in combination with each other. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the subject matter disclosed herein without departing from its scope. Dimensions, types of materials, orientations of the various components, and the number and positions of the various components described herein are intended to define parameters of certain embodiments, and are by no means limiting and are merely exemplary embodiments. Many other embodiments and modifications within the spirit and scope of the claims will be apparent to those of skill in the art upon reviewing the above description. The scope of the subject matter described herein should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled. In the appended claims, the terms “including” and “in which” are used as the plain-English equivalents of the respective terms “comprising” and “wherein.” Moreover, in the following claims, the terms “first,” “second,” and “third,” etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

WHAT IS CLAIMED IS:

1. A method of manufacturing a photovoltaic module, the method comprising:

providing an electrically insulating substrate and a lower electrode;

depositing a lower stack of silicon layers above the lower electrode, the lower stack comprising an N-I-P junction having an energy band gap of at least 1.60 eV;

depositing an upper stack of silicon layers above the lower stack, the upper stack comprising an N-I-P junction having an energy band gap of at least 1.80 eV; and

providing an upper electrode above the upper stack, wherein the lower and upper stacks convert incident light into an electric potential between the upper and lower electrodes, each of the lower and upper stacks converting different portions of the light into the electric potential based on wavelengths of the light.

2. The method of claim 1, wherein the depositing the lower stack comprises depositing amorphous silicon layers without depositing germanium (Ge).

3. The method of claim 1, wherein a content of germanium in the lower stack is 0.01% or less.

4. The method of claim 1, wherein the depositing the lower stack includes depositing a bottom sublayer of amorphous n-doped silicon, a middle sublayer of amorphous intrinsic silicon, and a top sublayer of p-doped silicon, the top sublayer deposited at a lower temperature than the bottom and middle sublayers.

5. The method of claim 4, wherein the depositing the bottom, middle, and top sublayers comprises depositing the bottom and middle sublayers at a temperature

of at least 250 degrees Celsius and depositing the top sublayer at a temperature of 220 degrees Celsius or less.

6. The method of claim 1, wherein the depositing the upper stack comprises depositing the upper stack at a temperature that is less than the depositing of the lower stack.

7. The method of claim 1, wherein the depositing the upper stack comprises depositing a bottom sublayer of amorphous n-doped silicon, a middle sublayer of amorphous intrinsic silicon, and a top sublayer of p-doped silicon at a temperature that is 220 degrees Celsius or less.

8. The method of claim 1, further comprising removing portions of the upper electrode to electrically separate sections of the upper electrode in adjacent photovoltaic cells, wherein the removing operation forms a bypass diode extending through the lower and upper stacks from the lower electrode to the upper electrode in the photovoltaic cells.

9. The method of claim 8, wherein the removing operation increases a crystalline fraction of a portion of the lower and upper stacks to be greater than a remainder of the lower and upper stacks, the portion having the increased crystalline fraction forming the bypass diode.

10. The method of claim 8, further comprising conducting electric current between the upper and lower electrodes through the bypass diode when the photovoltaic cell having the bypass diode is reverse biased.

11. The method of claim 8, further comprising conducting electric current between the upper and lower electrodes through the bypass diode when the photovoltaic cell having the bypass diode is shaded from incident light and adjacent cells are exposed to the light.

12. A monolithically-integrated photovoltaic module comprising:

an electrically insulating substrate;

a lower electrode disposed above the substrate;

a lower stack of silicon layers disposed above the lower electrode and having an energy band gap of at least 1.60 eV;

an upper stack of silicon layers disposed above the lower stack and having an energy band gap of at least 1.80 eV; and

an upper electrode disposed above the upper stack, wherein the energy band gap of the upper stack is greater than the energy band gap of the lower stack such that the lower and upper stacks convert different portions of incident light into an electric potential between the upper and lower electrodes based on wavelengths of the light.

13. The photovoltaic cell of claim 12, wherein the lower stack comprises an amorphous silicon junction without germanium (Ge) disposed in the lower stack.

14. The photovoltaic cell of claim 12, wherein each of the lower and upper stacks comprise N-I-P junctions of amorphous silicon.

15. The photovoltaic cell of claim 12, wherein the lower stack comprises a bottom sublayer of N-doped silicon, a middle sublayer of intrinsic silicon, and a top sublayer of P-doped silicon, the top sublayer having a different energy band gap than the bottom and middle sublayers.

16. The photovoltaic cell of claim 12, wherein the lower stack comprises a bottom sublayer of N-doped silicon, a middle sublayer of intrinsic silicon, and a top sublayer of P-doped silicon, the top sublayer transmitting more of the light

through the top sublayer than each of the bottom and middle sublayers transmit the light through the respective bottom or middle sublayer.

17. The photovoltaic cell of claim 12, further comprising a bypass diode extending through the lower and upper stacks from the lower electrode to the upper electrode in the photovoltaic cells, the bypass diode including a portion of the lower and upper stacks having a crystalline fraction that is greater than a remainder of the lower and upper stacks.

18. The photovoltaic cell of claim 17, wherein the bypass diode conducts electric current between the upper and lower electrodes through the upper and lower stacks when the upper and lower electrodes are reverse biased.

19. The photovoltaic cell of claim 17, wherein the bypass diode conducts electric current between the upper and lower electrodes through the upper and lower stacks when the cell is shaded from the light and adjacent cells are exposed to the light.

20. The photovoltaic cell of claim 12, wherein the lower stack comprises a layer of silicon doped with trimethyl boron ($B(CH_3)_3$) and the upper stack comprises a layer of silicon doped with boron trifluoride ($BF_3$ ).

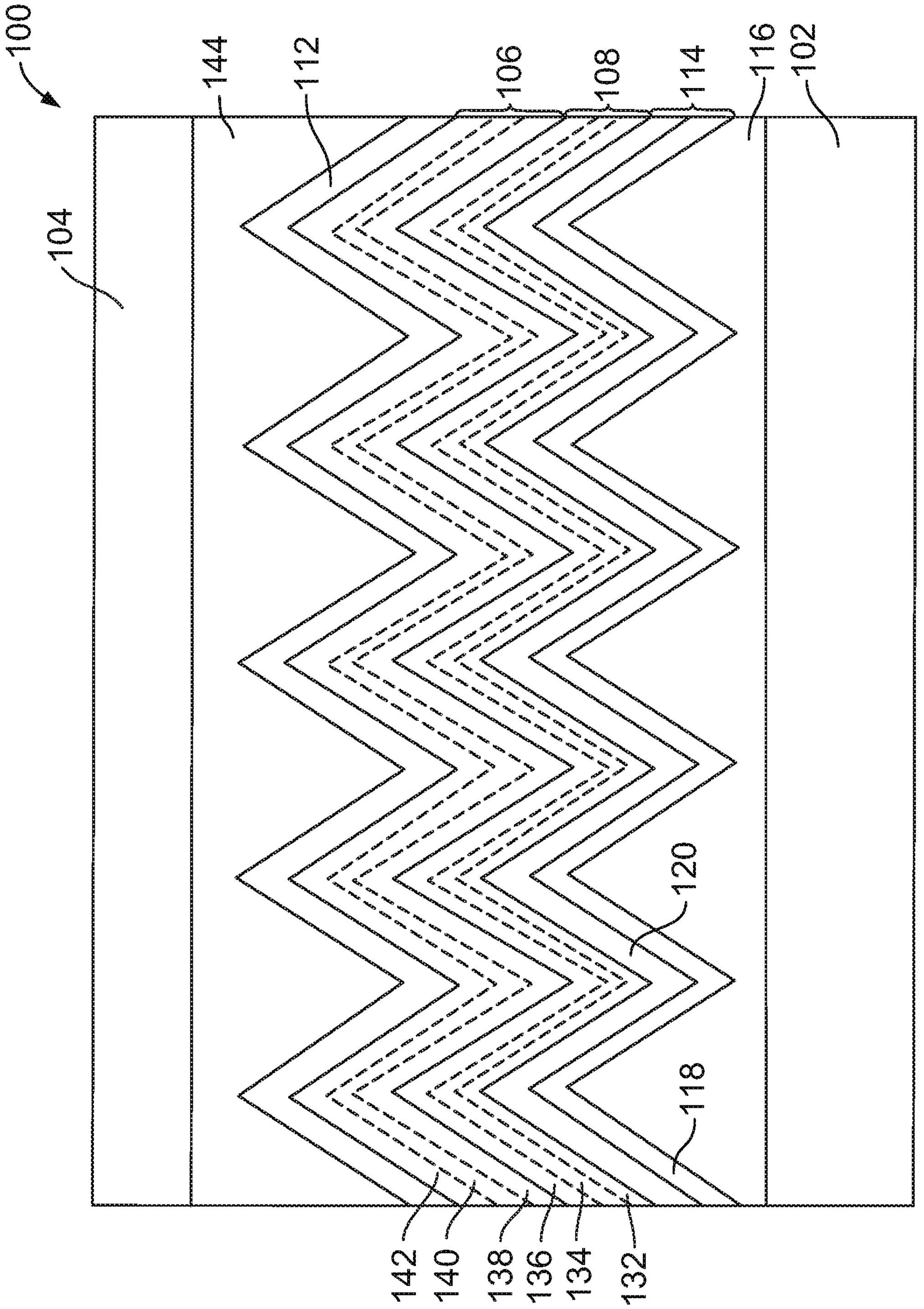
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FIG. 1

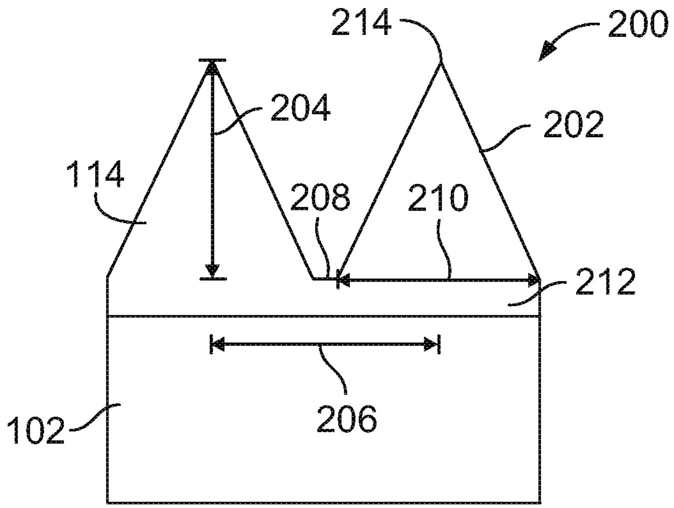

FIG. 2

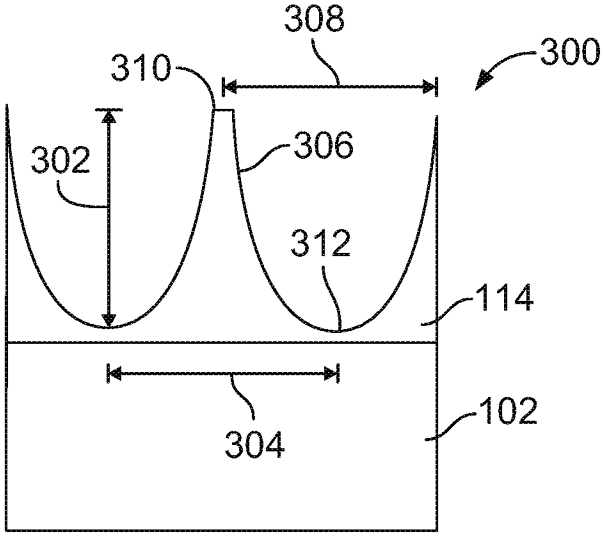

FIG. 3

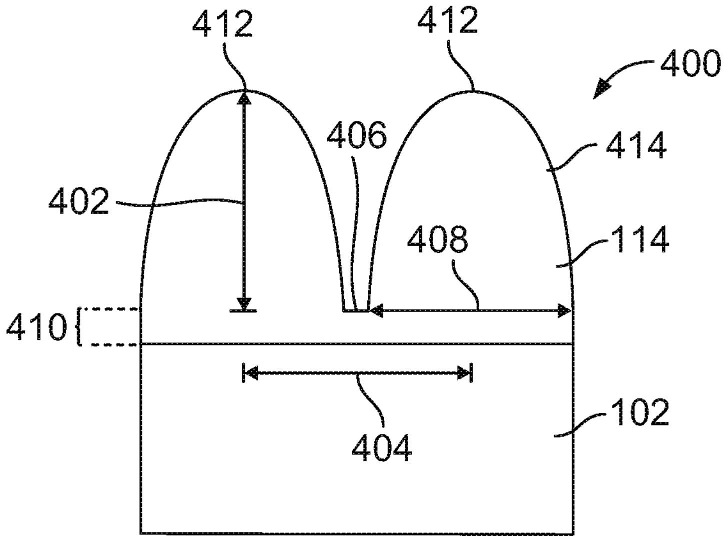

FIG. 4

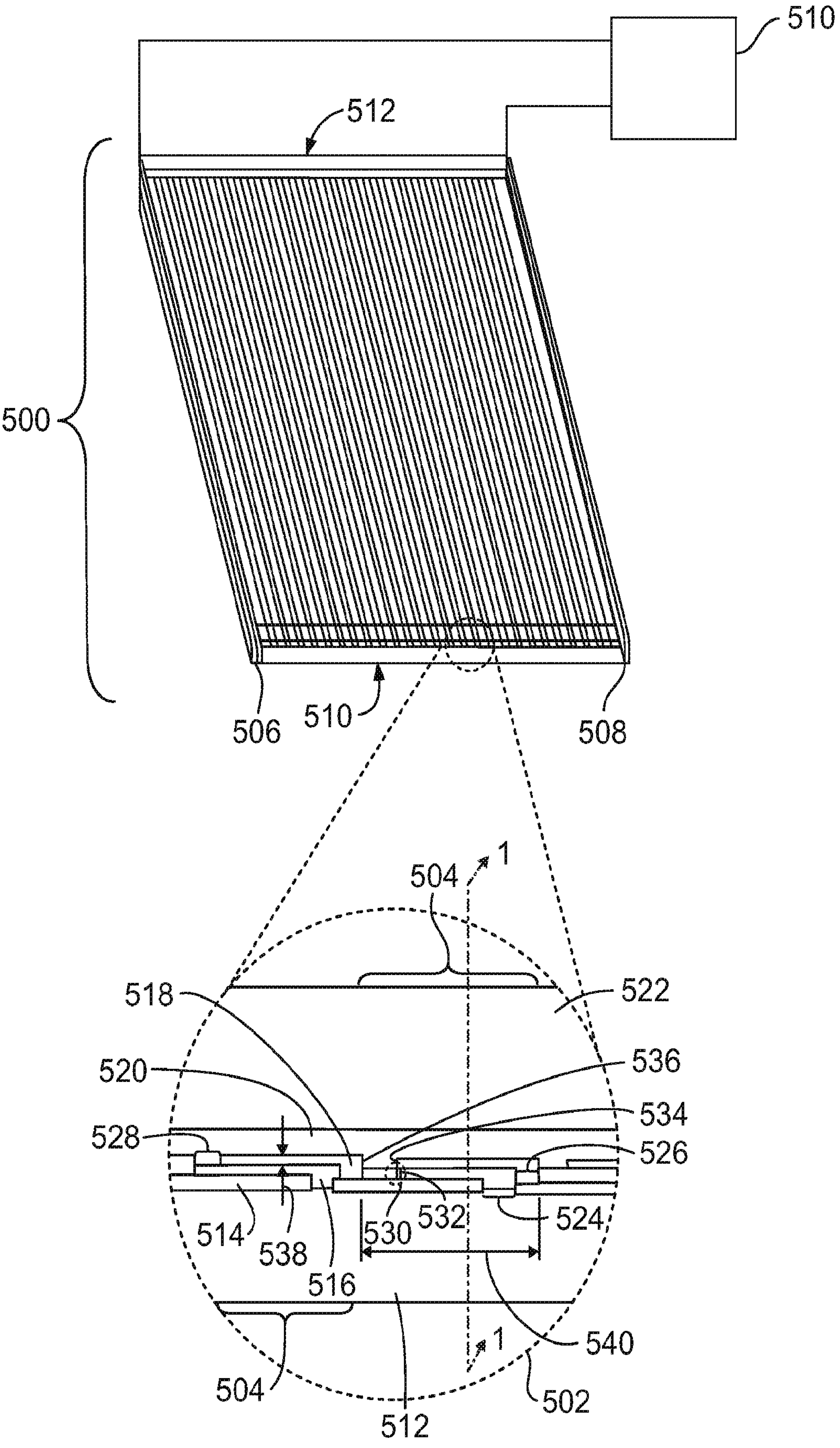
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FIG. 5

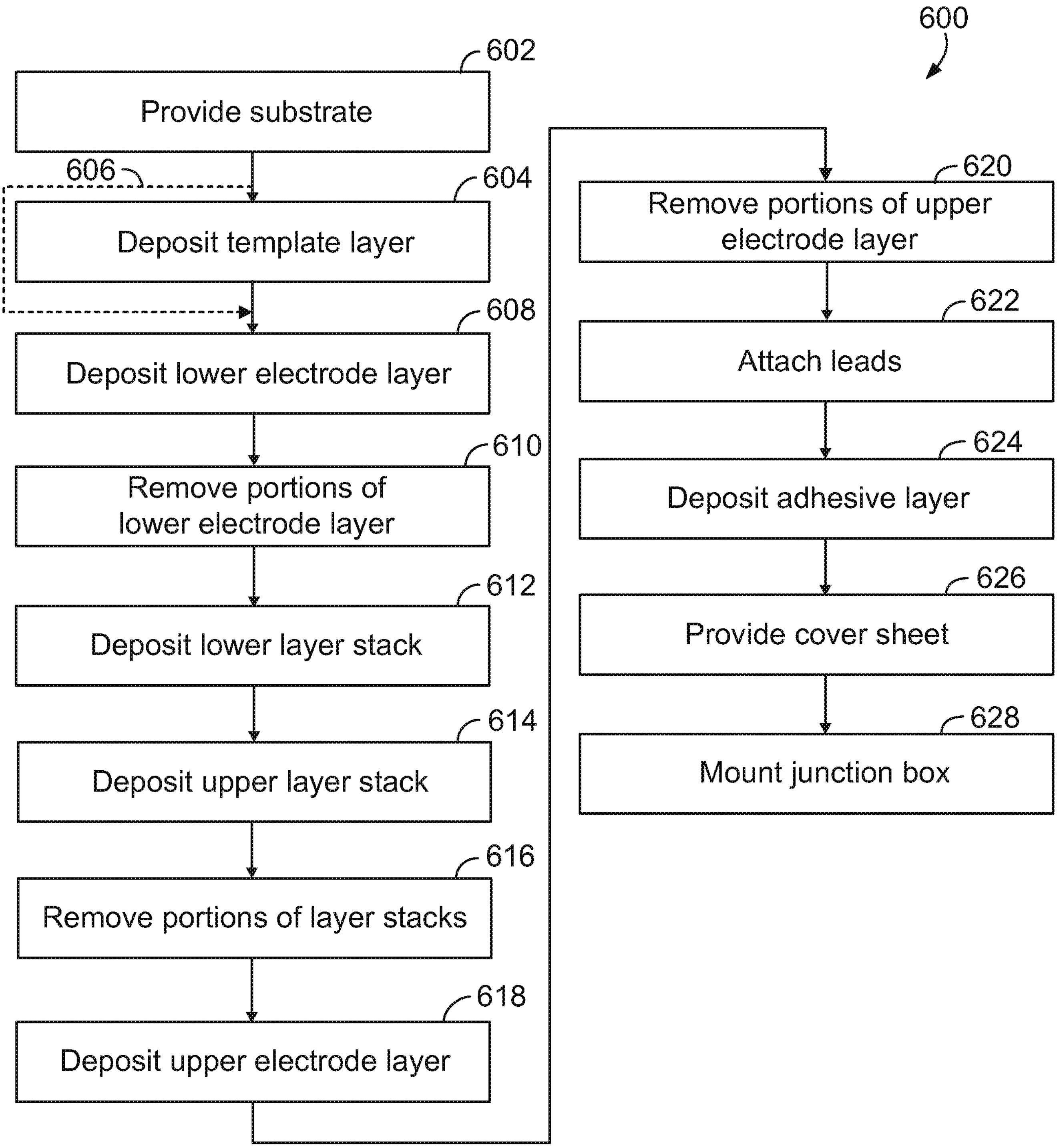
600
602
Provide substrate
606
604
Deposit template layer
608
Deposit lower electrode layer
610
Remove portions of lower electrode layer
612
Deposit lower layer stack
614
Deposit upper layer stack
616
Remove portions of layer stacks
618
Deposit upper electrode layer
620
Remove portions of upper electrode layer
622
Attach leads
624
Deposit adhesive layer
626
Provide cover sheet
628
Mount junction box

FIG. 6