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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Blvd., Santa Clara, CA 95054 (US).

(72) Inventors: **NGE, Chee Lim**; 16788 NW Arizona Drive, Beaverton, Oregon 97006 (US). **JAIN, Amit**; 4648 NW Moretti Terrace, Portland, Oregon 97229 (US). **DEVAL, Anant S.**; 12602 NW Waker Drive, Portland, Oregon 97229 (US). **ANGEL, Nimrod**; 1 Hod Street, 3508524 Haifa (IL). **PAILLET, Fabrice**; 1416 NW Benfield Dr., Portland, Oregon 97229 (US). **ZELIKSON, Michael**; Albert Schweitzer 67 Apt. 2, 34995 Haifa (IL). **RODRIGUEZ, Sergio Carlo**; 2499 NW 206th Avenue, Hillsboro, Oregon 97006 (US).

(74) Agent: **MUGHAL, Usman A.**; Green, Howard, & Mughal, LLP, 5 Centerpointe Dr., Suite 400, Lake Oswego, Oregon 97035 (US).

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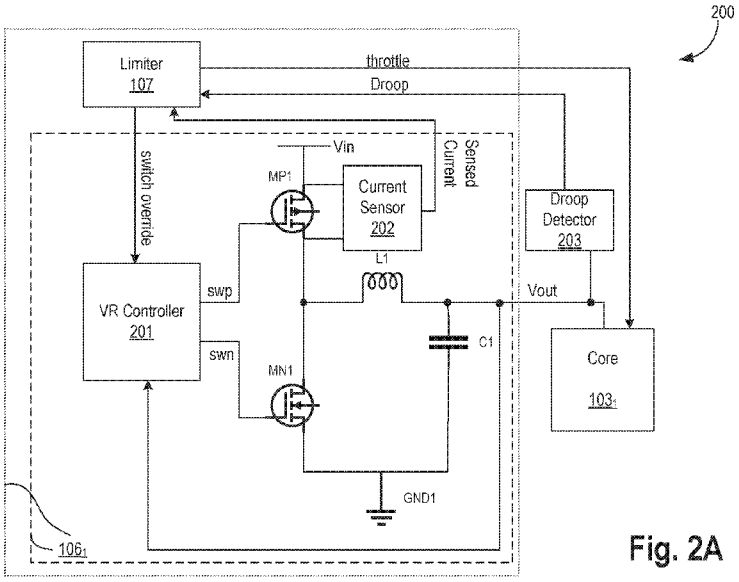


Fig. 2A

(57) Abstract: Described is an apparatus and method to prevent a processor from abruptly shutting down by proactive power management. The apparatus comprises a power supply rail to receive a current and a voltage from a power supply generator (e.g., a DC-DC converter, and low dropout regulator); a processor coupled to the power supply rail, wherein the processor is to operate with a current and a voltage provided by the power supply rail; and an interface to receive a request to throttle one or more performance parameters of the processor when a monitored current through the power supply rail or a monitored voltage on the power supply rail crosses a threshold current or a threshold voltage, respectively, wherein the threshold current is below a catastrophic threshold current of a voltage regulator, or wherein the threshold voltage is above a catastrophic threshold voltage of the processor.

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APPARATUS AND METHOD FOR PROACTIVE POWER MANAGEMENT

CLAIM OF PRIORITY

[0001] This Application claims priority to U.S. Patent Application No. 16/230,440, filed December 21, 2018, and titled "APPARATUS AND METHOD FOR PROACTIVE POWER MANAGEMENT," which is incorporated by reference in its entirety for all purposes.

BACKGROUND

[0002] Recently, process technology has hit the limit of Dennard scaling. To provide higher performance to a processor (e.g., a computer processing unit (CPU)), the power supply maximum current (IccMax) for the processor needs to also increase. Higher IccMax allows for faster execution speed at the cost of higher power consumption. However, currently customers desire to reduce the area of the printed circuit board (PCB) having the processor. This desire is in part to reduce size and weight of the PCB to provide mobility to the end users. Voltage regulators (VRs) are used to provide regulated power to the processor. Traditional VRs use large area to deliver higher IccMax, and hence performance, and this becomes a technical dilemma to resolve because providing higher performance while scaling down the size of the PCB is a challenge. In some applications, a processor may execute or run synthetic virus applications for an extended time which may reach 2X power consumption with respect to a real load limit. This may require the VR to supply higher than an application limited IccMax. Ideally, a VR is designed to supply IccMax to the processor to allow the processor to run real or normal applications instead of virus application(s). Designing a computer system that can allow a processor, manufactured in today's process technology, to run virus applications and real applications without causing catastrophic reliability failures is a challenge.

[0003] The background description provided herein is for the purpose of generally presenting the context of the disclosure. Unless otherwise indicated herein, the materials described in this section are not prior art to the claims in this application and are not admitted to be prior art by inclusion in this section.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various

embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0005] **Figs. 1A-B** illustrate a part of a computing system having a processor with an apparatus for proactive power management to avoid processor shutdown, in accordance with some embodiments.

[0006] **Fig. 2A** illustrates a high-level architecture of the apparatus with a current sensor across a high-side switch, and a voltage droop detector used to proactively manage power of a processor, in accordance with some embodiments.

[0007] **Fig. 2B** illustrates a high-level architecture of the apparatus with a current sensor across an inductor, and a voltage droop detector used to proactively manage power of a processor, in accordance with some embodiments.

[0008] **Fig. 3A** illustrates a high-level architecture of the apparatus with a current sensor across a high-side switch, a voltage droop detector, and a clamp used to proactively manage power of a processor, in accordance with some embodiments.

[0009] **Fig. 3B** illustrates a high-level architecture of the apparatus with a current sensor across an inductor, a voltage droop detector, and a clamp used to proactively manage power of a processor, in accordance with some embodiments.

[0010] **Fig. 4** illustrates an apparatus for generating control signals for proactively managing power of a processor, in accordance with some embodiments.

[0011] **Fig. 5** illustrates an apparatus for clamping a voltage on a power supply rail coupled to the processor, in accordance with some embodiments.

[0012] **Fig. 6** illustrates an apparatus to sense or measure current through the inductor, in accordance with some embodiments.

[0013] **Fig. 7** illustrates a timing diagram and trainset response of the apparatus without voltage clamp and with sufficiently large load capacitance, in accordance with some embodiments.

[0014] **Fig. 8** illustrates a timing diagram and transient response of the apparatus with a voltage clamp and with relatively small load capacitance, in accordance with some embodiments.

[0015] **Fig. 9** illustrates a computing system with apparatus to proactively manage power of a processor, in accordance with some embodiments.

DETAILED DESCRIPTION

[0016] Some embodiments describe an apparatus for combined fast coordination of various mechanisms in a voltage regulator (VR) and a processor operation for effective and proactive power management. While the embodiments are described with reference to a buck DC-DC converter, the embodiments are not limited to such. Other forms of voltage generating circuitries such as low dropout (LDO) regulators, boost DC-DC converters, and the like can also be used in the overall system to proactively manage power of the processor and/or the entire computing system.

[0017] In some embodiments, a VR goes into cycle-by-cycle current limit, and provides a signal to the processor that enacts throttling in response to certain performance metrics exceeding predetermine (or programmable) thresholds. For example, when the current through a high-side switch of a VR increases a threshold current level between two VR switching cycles (or another number of cycles), then a power control unit (PCU) or any other suitable logic may instruct the processor to throttle its operating frequency. In one such embodiment, a divider ratio of a PLL (phase locked loop) is adjusted to reduce the operating frequency of the clock used by the processor without having the PLL lose phase lock. As such, fast throttling in the processor is executed with minimal latency when VR goes into current limit at real application level.

[0018] In some cases, the voltage on the power supply rail providing power to the processor droops when the processor (or load) current exceeds the level expected for executing a real application on the processor. In some embodiments, the apparatus monitors the voltage droop and when the voltage drops below a certain threshold, the PCU or any other suitable power management circuity may send a signal to the processor to throttle its operating frequency to reduce the load before the complete droop occurs. In some embodiments, the occurrence of the voltage droop or current spike is estimated based on execution of the real application on the processor. For example, speculative execution of certain instructions or other instruction in a pipeline can provide an indication that a voltage droop may occur and so the processor may want to throttle its frequency to avoid a possible shutdown of the VR and hence the processing system.

[0019] These signals from the PCU or power management circuitries to the processor are not merely alarm(s), but part of a mechanism that allows the VR to be designed for a low current rating. In some embodiments, when a large droop occurs, the decoupling capacitance or alternatively a clamp circuit support the voltage on the power supply rail during the time the load exceeds the VR voltage/current peak limit. As such, the VR can be designed to

operate for real application power delivery while allowing short durations of processor peak power. Other technical effects will be evident from the various embodiments and figures.

[0020] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0021] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0022] The term “device” may generally refer to an apparatus according to the context of the usage of that term. For example, a device may refer to a stack of layers or structures, a single structure or layer, a connection of various structures having active and/or passive elements, etc. Generally, a device is a three-dimensional structure with a plane along the x-y direction and a height along the z direction of an x-y-z Cartesian coordinate system. The plane of the device may also be the plane of an apparatus which comprises the device.

[0023] Throughout the specification, and in the claims, the term "connected" means a direct connection, such as electrical, mechanical, or magnetic connection between the things that are connected, without any intermediary devices.

[0024] The term "coupled" means a direct or indirect connection, such as a direct electrical, mechanical, or magnetic connection between the things that are connected or an indirect connection, through one or more passive or active intermediary devices.

[0025] The term “adjacent” here generally refers to a position of a thing being next to (e.g., immediately next to or close to with one or more things between them) or adjoining another thing (e.g., abutting it).

[0026] The term "circuit" or “module” may refer to one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function.

[0027] The term "signal" may refer to at least one current signal, voltage signal, magnetic signal, or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0028] The term "scaling" generally refers to converting a design (schematic and layout) from one process technology to another process technology and subsequently being reduced in layout area. The term "scaling" generally also refers to downsizing layout and devices within the same technology node. The term "scaling" may also refer to adjusting (e.g., slowing down or speeding up – i.e. scaling down, or scaling up respectively) of a signal frequency relative to another parameter, for example, power supply level.

[0029] The terms "substantially," "close," "approximately," "near," and "about," generally refer to being within +/- 10% of a target value. For example, unless otherwise specified in the explicit context of their use, the terms "substantially equal," "about equal" and "approximately equal" mean that there is no more than incidental variation between among things so described. In the art, such variation is typically no more than +/-10% of a predetermined target value.

[0030] Unless otherwise specified the use of the ordinal adjectives "first," "second," and "third," etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0031] For the purposes of the present disclosure, phrases "A and/or B" and "A or B" mean (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

[0032] The terms "left," "right," "front," "back," "top," "bottom," "over," "under," and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. For example, the terms "over," "under," "front side," "back side," "top," "bottom," "over," "under," and "on" as used herein refer to a relative position of one component, structure, or material with respect to other referenced components, structures or materials within a device, where such physical relationships are noteworthy. These terms are employed herein for descriptive purposes only and predominantly within the context of a device z-axis and therefore may be relative to an orientation of a device.

[0033] The term "between" may be employed in the context of the z-axis, x-axis or y-axis of a device. A device that is between two other devices may be directly connected to

one or both of those devices, or it may be separated from both of the other two devices by one or more intervening devices.

[0034] Here, the term "backend" generally refers to a section of a die which is opposite of a "frontend" and where an IC (integrated circuit) package couples to IC die bumps. For example, high level metal layers (e.g., metal layer 6 and above in a ten-metal stack die) and corresponding vias that are closer to a die package are considered part of the backend of the die. Conversely, the term "frontend" generally refers to a section of the die that includes the active region (e.g., where transistors are fabricated) and low-level metal layers and corresponding vias that are closer to the active region (e.g., metal layer 5 and below in the ten-metal stack die example).

[0035] It is pointed out that those elements of the figures having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0036] **Fig. 1A** illustrates a part of a computing system 100 having a processor with apparatus for proactive power management, in accordance with some embodiments. In some embodiments, system 100 comprises processor 101 coupled to a power management integrated circuit (PMIC) 102. Processor 101 can be any processor that is used for running applications. For example, processor 101 can be a central processing unit (CPU), a system-on-chip (SOC), a digital signal processor (DSP), an application specific integrated circuit (ASIC), a multi-die processor (e.g., multiple dies connected to one another side-by-side and/or in a vertical stack), etc.

[0037] In some embodiments, PMIC 102 receives a voltage identification from processor 101 and provides an input power supply to processor 101. This input power supply is then used by various power generating circuits to generate controllable regulated power supplies. In some embodiments, PMIC 102 is integrated within processor 101.

[0038] In some embodiments, processor 101 comprises one or more processor cores. Here, N cores are shows as $103_{1\text{-}n}$, where 'n' is an integer. In some embodiments, each core is paired with a corresponding cache. For example, core 103_1 is paired with cache 104_1, core 103_2 is paired with cache 104_2, core $103_{n\text{-}1}$ is paired with cache $104_{n\text{-}1}$, and core 103_n is paired with cache 104_n. In some embodiments, the cores $103_{1\text{-}n}$ are coupled to a shared cache (not shown). In various embodiments, each core is coupled to an associated power generator or regulator to provide controllable power to that core. In some embodiments, the entire processor 101 is powered by one or more power regulators instead of dedicated regulators per

core. In some embodiments, major logic blocks such as cores, caches, I/Os, fuses, have their corresponding voltage regulators to control power to them.

[0039] In some embodiments, processor 101 comprises power control unit (PCU) 105 to manage power consumption of processor 101 under various operating conditions. For example, PCU 105 monitors temperature(s) of various parts of processor 101 and lowers operating voltage or frequency in response to rising temperature. In some embodiments, processor 101 comprises a limiter circuitry 107 that monitors various performance metrics (e.g., output current, output voltage, temperature, switching frequency, etc.) of the VRs and then issues one or more control signals to cause the VRs to change their behavior to avoid unintentional shutdown of processor 101. In some embodiments, the controls from limiter 107 are directly received by the VR(s) 106. For sake of not obscuring the embodiments, VR(s) $106_{1\text{-}n}$ are also referred to as VR 106 which may refer to one VR or many VRs together depending on the context of the sentence. In some embodiments, the controls from limiter 107 are processed by PCU 105 which then issues controls to the various VRs and other parts of processor 101.

[0040] In some embodiments, limiter 107 and/or PCU 105 reduces the design limits of VR(s) 106 to a threshold value of an application consumption, where the application is executed on one or more cores of processor 101. As such, limiter 107 ensures that the design limit of VR(s) 106 is not exceeded as the application executes. For example, limiter 107 may instruct the VR(s) to switch OFF a high-side FET (field effect transistor) of the VR 106 when current generated by the VR 106 is higher than a threshold current. One reason for the current to increase is a greater demand by the load of the VR 106. To prevent a catastrophic failure that may originate from an abrupt stopping of the supply current, two complementary measures are used in various embodiments. In some embodiments, one or more cores $104_{1\text{-}n}$ are throttled to reduce the power consumption or demand for a short duration. In some embodiments, an alternative power circuitry is used to support the above-threshold current demand.

[0041] The following example is illustrated with reference to VR 106_1 and Core 103_1, where VR is a switching-type buck DC-DC converter coupled to an inductor and load capacitor. However, the example is applicable to other VRs, cores, and other architectures where a VR is used to provide power to a processing unit. In some embodiments, limiting circuitry 107 detects the inductor current from VR 106_1 has exceeded a pre-defined threshold level, and it limits the current through the inductor by turning off the high-side transistor of VR 106_1. When the inductor current is limited, VR 106_1 sends a fast throttling signal via

limiter 107 (or PCU 105) to processor 101 to initiate the power consumption reduction. In some embodiments, an alternative power source (e.g., a higher voltage VR, existing on the platform) is used to supply an additional charge that is consumed by processor 101 from the moment the high-FET of VR 106 is turned OFF until the throttling happens using a voltage clamp circuit. As such, an output voltage of the VR 106_1 dropping below a critically low level is avoided.

[0042] **Fig. 1B** illustrates architecture 120 where VR 106 is located external to processor 101 and provides power to the entire processor 101 through power supply rail Vout. In this example, limiter 107 is integrated in PMIC 102 along with VR 106. While the boundaries of various circuits are shown, these boundaries are just examples. For example, limiter 107 can be within the circuit boundary of VR 106. In another example, limiter 107 can be inside PCU 105. In one example, as shown in Fig. 1B, limiter 107 is part of PMIC 102 which also includes VR 106. In one such example, communication between limiter 107 and/or PCU 105 with VR 106 is via PMIC 102. Other locations of VR 106 are also contemplated. For example, processor 101 may have internal on-die VRs such as VRs 106_{1-n} and external VR 106.

[0043] **Fig. 2A** illustrates a high-level architecture 200 of the apparatus with a current sensor across a high-side switch, and a voltage droop detector used to proactively manage power of a processor, in accordance with some embodiments. Architecture 200 comprises VR 106_1 having VR Controller 201 and Current Sensor 202, high-side switch MP1, low-side switch MN1, inductor L1, capacitor C1, and power supply rail Vout. While the inductor L1, capacitor C1, and current sensor 202 are shown within the dotted boundary of VR 106_1, any of these components can be within or outside the VR boundary. In some embodiments, architecture 200 further comprises a voltage droop detector 203 coupled to limiter 107 and core 103_1. While Droop Detector 203 is illustrated outside of VR 106_1 boundary and outside of Core 103_1, Droop Detector 203 can be inside VR 106_1 or inside Core 103_1. Likewise, Limiter 107 can be part of VR 106_1 instead of residing outside of VR 106_1, in accordance with some embodiments.

[0044] In some embodiments, VR controller 201 comprises logic and circuitry to control the switching of low-side switch MN1 and high-side switch MP1 via switching signals swn and swp, respectively. VR controller 201 monitors the voltage on the power supply rail (or node) Vout and adjusts the duty cycle of a pulse width modulation (PWM) signal (not shown) that is used to generate the switching signals swn and swp. The duty cycle

of the PWM signal is adjusted to allow Vout voltage to be at an expected level compared to a reference voltage.

[0045] In some embodiments, current sensor 202 is coupled to the high-side switch MP1 to sense and/or measure current through the high-side switch MP1. Here, the high-side switch MP1 is controlled by switching signal swp while the low-side switch MN1 is controlled by switching signal swn. In some embodiments, current sensor 202 measures or senses the instantaneous current of the buck converter high-side transistor MP1. Measuring the high-side transistor MP1 current (e.g., the drain current) would also measure the peak current of the inductor L1. This measured current (herein also referred to as IccMax) is then compared with a threshold current by limiter 107. When the measured current exceeds a level that would saturate the buck converter inductor L1 (herein, the current level that saturates L1 is referred to as IccMax), limiter 107 sends a switch override signal to VR controller 201 to cause the high-side transistor MP1 to be turned off. For example, swp signal is forced to be at Vin (or any other supply) level when switch override signal is asserted.

[0046] In some embodiments, Current Sensor 202 is implemented using transistor current mirror of the high-side transistor switch MP1. In some embodiments, VR Controller 201 is implemented by measuring the voltage drop across the high-side transistor switch MP1 when the high-side transistor switch MP1 is turned on.

[0047] Inductors can be made from magnetic material and are sized for IccMax/Nph (where Nph is a number of phases) to avoid saturation. When inductor saturation happens, the VR 106_1 is at high risk of being damaged. In one example, inductor saturation is approximately 20A for a low z-height inductor and about 30A for a high z-height inductor. If the IccMax (under virus application scenario) is 60A, 3 phases for low z-height and 2 phases for high z-height are needed. When the core IccMax increases, the number of phases would increase and this increases the size of the inductor and hence the cost of the computing system. To manage cost and to avoid turning off of the VR 106_1, and hence the power supply to the processor core 103_1, architecture 200 measures the current for the VR and turns off the high-side transistor switch MP1 when the current exceeds IccMax.

[0048] In one example, the high-side transistor switch MP1 is turned off for a short time (e.g., one or a few pulse with modulation cycles) while the processor core 103_1 lowers its current draw requirement, and when that requirement is lowered (e.g., by throttling the frequency of the processor core 103_1), the high-side transistor switch MP1 is turned back on in regular switching mode. In some embodiments, when the inductor L1 current reaches a

current threshold (e.g., threshold of current that can be safely delivered by VR 106_1), limiter 107 would send a throttle signal to processor core 103_1 to force processor core 103_1 to quickly reduce the current draw from Vout power supply rail.

[0049] This current threshold (IccMax) value represents the maximal processor consumption during execution of a worst case real application or thread. The IccMax value includes additional guard band taken to factor measurement inaccuracy, system delays and other factors that may impact the current estimation result. Turing off the high-side transistor switch MP1 forces the inductor current to ramp down, in accordance with some embodiments.

[0050] In some embodiments, architecture 200 comprises droop detector 203. When the load (here processor core 103_1) suddenly draws a large current, the voltage Vout on the power supply rail will droop. Sometimes this droop is below a safe level and can cause logic of the processor core 103_1 to malfunction. As a result, outputs of various logic circuits can be compromised. Further, a voltage droop on the output power supply rail Vout can cause the VR Controller 201 to cause the high-side switch MP1 to provide more current to inductor L and hence the processor core 103_1 (load). This increase in current may cause VR 106_1 to hit its maximum current limit IccMax.

[0051] In some embodiments, droop detector 203 compares the voltage on Vout to a predetermined (or programmable) threshold, and when the voltage on Vout crosses that threshold, droop detector 203 generates a Droop signal. The Droop signal (e.g., a logic 1 signal) is then processed by limiter 107 which may then directly or through PCU 102 request processor core 103_1 to throttle (e.g., lower is operating frequency, postpone high energy or high power instructions, clock gate electrical paths not currently in use etc.).

[0052] For example, when processor core 103_1 draws virus IccMax, depending on the size of the L1 and capacitor C1, and also the load step; either the inductor L1 would exceed IccMax of the VR 106_1 or Vout would drop below a critically low level. When Vout is at the critically low level, limiter 107 needs to sends a throttling signal to processor core 103_1 and/or take additional measure to control voltage Vout from falling.

[0053] **Fig. 2B** illustrates a high-level architecture 220 of the apparatus with a current sensor across an inductor, and a voltage droop detector used to proactively manage power of a processor, in accordance with some embodiments. Compared to architecture 200, current sensor 202 is removed and current sensor 222 is added instead. In some embodiments, both current sensors 202 and 222 can be used. Current sensor 222 directly measures or senses the

inductor current L1 instead of the drain current of the high-side transistor switch MP1. Functionally, architecture 220 operates similarly to architecture 200.

[0054] **Fig. 3A** illustrates a high-level architecture 300 of the apparatus with a current sensor across a high-side transistor switch MP1, a voltage droop detector, 203 and a clamp 301 used to proactively manage power of a processor, in accordance with some embodiments. Architecture 300 is similar to architecture 200 but for the addition of clamp circuitry 301. As discussed with reference to **Fig. 2A**, when Droop detector 203 detects a droop on Vout that can cause IccMax violation of VR 106_1 because VR 106_1 may try to provide more current to compensate for the droop, Limiter 107 (and/or PCU 105) instructs clamp circuit 301 to clamp the voltage Vout of the power supply rail to a safe level. At the same time, processor core 103_1 is instructed to throttle (e.g., lower its frequency, turn off certain logic units etc.) to reduce current draw demand from the power supply rail Vout. In some embodiments, the duration of enabling clamp 301 is the duration of the expected or actual droop on Vout power supply rail.

[0055] In some embodiments, clamp circuitry 301 includes a temperature sensor to sense the temperature of clamp 301. If the temperature is higher than a threshold temperature, then high-side transistor switch MP1 may be instructed to turn off to reduce the current draw by the load. In some embodiments, if the temperature is higher than a threshold temperature, the clamp 301 may be turned off. In some embodiments, clamp 301 is a high frequency switching buck converter or a switched capacitor step-down converter.

[0056] Once the droop is over, clamp 301 is turned off and VR 106_1 operates as normal. In some embodiments, when clamp 301 is on, VR Controller 201 may switch off the high-side transistor switch MP1 to reduce the current supply to core 103_1. In some embodiments, limiter 107 and/or PCU 105 sets the clamp turn off threshold level for clamp 301. This threshold level is the safe level to turn off the clamp circuitry 301. In some embodiments, the threshold level is higher than the droop detect level to add hysteresis in the clamp control. The presence of the clamp circuitry 301 can also reduce the size of the load capacitor C1.

[0057] **Fig. 3B** illustrates a high-level architecture 320 of the apparatus with a current sensor across an inductor, a voltage droop detector 203, and a clamp 301 used to proactively manage power of a processor, in accordance with some embodiments. Architecture 320 is similar to architecture 300 but for the addition of current sensor 222 to directly measure or sense the current through inductor L1.

[0058] **Fig. 4** illustrates apparatus 400 (e.g. limiter 107) for generating control signals for proactively managing power of a processor, in accordance with some embodiments. In some embodiments, apparatus 400 comprises first comparator 401, second comparator 402, and an OR logic gate 403. In some embodiments, first comparator 401 compares the VR output voltage (e.g., voltage Vout on the power supply rail Vout) with a clamp setting voltage or threshold. In some embodiments, first comparator 401 is removed and its function is replaced by droop detector 203. In some embodiments, first comparator 401 is a voltage comparator. Any suitable voltage comparator can be used to implement first or second comparators 402.

[0059] In some embodiments, second comparator 402 compares the sensed current with a threshold current. In some embodiments, second comparator 402 is a current comparator as opposed to a voltage comparator. The outputs of both first and second comparators (401 and 402, respectively) are voltage signals—clamp and switch override, respectively. In some embodiments, sensed current is converted into a voltage representation and compared against a threshold which represents a current threshold in voltage. The thresholds here can be programmed by software (e.g., BIOS or operating system, PCU 105, etc.) or by hardware (e.g., fuses, registers, external capacitors, resistors, etc.). In various embodiments, when limiter 400 indicates that clamp 301 needs to be turned on (e.g., when clamp is asserted) or when the inductor current or current through the high-side switch MP1 is higher than a threshold (e.g., switch override is asserted), the processor core 103_1 (or the entire processor 101) is instructed to throttle.

[0060] In one example, Clamp signal, when asserted, causes Clamp circuitry 301 to clamp the power supply voltage to core 103_1. Switch override signal, when asserted, causes the high-side switch MP1 to turn off. When either the clamp or the switch override signal is asserted, the processor 101 or the individual core associated with the VR 103_1 is throttled. In some embodiments, when the processor 101 or the core 103_1 is requested to throttle, it may adjust or modify a divider ratio of a PLL and lower the operating frequency of the processor 101 or the core 103_1.

[0061] **Fig. 5** illustrates apparatus 500 for clamping a voltage on a power supply rail coupled to the processor, in accordance with some embodiments. In some embodiments, apparatus 500 comprises a p-type transistor MP2 to turn on or off the clamping function according to the logic level of the Clamp signal. In some embodiments, the p-type transistor MP2 is coupled in series with a diode 501 which adds voltage drop to ensure Vout is maintained at a required level to ensure correct clamping function. Apparatus 500 also

behaves as a linear regular. When p-type transistor MP2 is on, the voltage on node Vout is determined by diode 501. In some embodiments, to endure that apparatus 500 does not run into thermal runaway situation, the duty cycle of the high-side switch MP2 is controlled by VR controller 201. High-side switch MP2 and diode 501 may dissipate significant power in the short duration the voltage on Vout is being clamped. This can lead to high temperature which further increases dissipation causing thermal runaway and eventual failure. Adjusting the duty cycle of the switching activity of high-side switch MP2 can protect from such thermal runaway. In some embodiments, when clamp 301 is enabled and turned on, processor 101 or core 103_1 is instructed to lower its current draw requirements to ease the inductor current and thus the temperature of the clamp 301 (or apparatus 500).

[0062] **Fig. 6** illustrates apparatus 600 to sense or measure current through the inductor, in accordance with some embodiments. In some embodiments, apparatus 600 comprises current sensor 601 (e.g., sensor 222 coupled to inductor L1). In some embodiments, current sensor 601 comprises resistor R1, capacitor C2, differential amplifier 602, summing node 604, and replica high-side switch 605. The replica high-side switch 605 comprises a transistor MP1r modeled as a current source and switch, and coupled to capacitor C3. The current through MP1r mimics the inductor ripple current. Here, the average current through inductor L1 is determined by the voltage difference seen across the two inputs of amplifier 602. These inputs provide the voltage difference across inductor L1. The peak current through inductor L1 is the average current flow through Vout power supply line plus the ramp current from the high-side switch MP1 (mimicked by MP1r). By combining these two currents at summing node 604, sensed current is achieved. In some embodiments, the current ripple of inductor L1 can be imitated in voltage ramp by supplying a constant current source to a capacitor when the replica high-side switch 605 is turned on. The sensed currents from different phases of the VR may be summed to determine the total VR current.

[0063] **Fig. 7** illustrates timing diagram 700 and transient response of the apparatus without voltage clamp and with sufficiently large load capacitance, in accordance with some embodiments. The horizontal dashed line indicate various thresholds. The top threshold is processor IccMax, above which the processor may exhibit reliability issues such as electro-migration. The second from the top threshold is VR IccMax which is the current limit supply of the VR 106_1. The third threshold is the nominal Vout level.

[0064] At t0, the processor 101 or core 103_1 begins to draw more current. At t1, processor or core 103_1 is requested to throttle and reduce its current demand. Simultaneously, the VR high side switch MP1 is turned off by the switch override signal. As

such, the inductor current begins to reduce after point 701. The processor or core 103_1 current (e.g., current through Vout power supply rail) is reduced at t2, which allows the capacitor C1 to be charged back.

[0065] **Fig. 8** illustrates timing diagram 800 and trainset response of the apparatus with a voltage clamp and with relatively small load capacitance, in accordance with some embodiments. The horizontal dashed lines are similar to the ones of timing diagram 700 in addition to clamp threshold being added. Here, due to smaller C1 as compared to C1 used for timing diagram 700, the voltage Vout drops to Vclamp (the critically low Vout level) sooner as indicated by point 801. The voltage clamp circuitry 301 starts at t1 and ends at t4. The inductor current begins to reduce at t2 after high-side switch MP1 is turned off by the switch override signal. The clamp circuit 301 starts supplying the current to avoid continuation of discharging of capacitor C1. Here, the processor starts throttling current at time t3, and Vout goes above threshold at time t4.

[0066] **Fig. 9** illustrates a computing system 2400 with apparatus to proactively manage power of a processor, in accordance with some embodiments. In some embodiments, the device 2400 represents an appropriate computing device, such as a computing tablet, a mobile phone or smart-phone, a laptop, a desktop, an IOT device, a server, a wearable device, a set-top box, a wireless-enabled e-reader, or the like. It will be understood that certain components are shown generally, and not all components of such a device are shown in the device 2400.

[0067] In an example, the device 2400 comprises a SoC (System-on-Chip) 2401. An example boundary of the SOC 2401 is illustrated using dotted lines, with some example components being illustrated to be included within the SOC 2401 – however, the SOC 2401 may include any appropriate components of the device 2400.

[0068] In some embodiments, the device 2400 includes a processor 2404. The processor 2404 can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, processing cores, or other processing means. The processing operations performed by processor 2404 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, operations related to connecting the computing device 2400 to another device, and/or the like. The processing operations may also include operations related to audio I/O and/or display I/O.

[0069] In some embodiments, the processor 2404 includes multiple processing cores (also referred to as cores) 2408a, 2408b, 2408c. Although merely three cores 2408a, 2408b, 2408c are illustrated, the processor 2404 may include any other appropriate number of processing cores, e.g., tens, or even hundreds of processing cores. In some embodiments, the processor 2404 includes cache 2406. In an example, sections of the cache 2406 may be dedicated to individual cores 2408 (e.g., a first section of the cache 2406 dedicated to core 2408a, a second section of the cache 2406 dedicated to core 2408b, and so on). In an example, one or more sections of the cache 2406 may be shared among two or more of the cores 2408. The cache 2406 may be split in different levels, e.g., level 1 (L1) cache, level 2 (L2) cache, level 3 (L3) cache, etc.

[0070] In some embodiments, the device 2400 comprises connectivity circuitries 2431. For example, connectivity circuitries 2431 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and/or software components (e.g., drivers, protocol stacks), e.g., to enable the device 2400 to communicate with external devices. The device 2400 may be separate from the external devices, such as other computing devices, wireless access points or base stations, etc.

[0071] In an example, connectivity circuitries 2431 may include multiple different types of connectivity. To generalize, the connectivity circuitries 2431 may include cellular connectivity circuitries, wireless connectivity circuitries, etc. Cellular connectivity circuitries of the connectivity circuitries 2431 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, 3rd Generation Partnership Project (3GPP) Universal Mobile Telecommunications Systems (UMTS) system or variations or derivatives, 3GPP Long-Term Evolution (LTE) system or variations or derivatives, 3GPP LTE-Advanced (LTE-A) system or variations or derivatives, Fifth Generation (5G) wireless system or variations or derivatives, 5G mobile networks system or variations or derivatives, 5G New Radio (NR) system or variations or derivatives, or other cellular service standards. Wireless connectivity circuitries (or wireless interface) of the connectivity circuitries 2431 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), and/or other wireless communication. In an example, connectivity circuitries 2431 may include a network

interface, such as a wired or wireless interface, e.g., so that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant.

[0072] In some embodiments, the device 2400 comprises a control hub 2432, which represents hardware devices and/or software components related to interaction with one or more I/O devices. For example, the processor 2404 may communicate with one or more of a display 2422, one or more peripheral devices 2424, storage devices 2428, one or more other external devices 2429, etc., via the control hub 2432. The control hub 2432 may be a chipset, a Platform Control Hub (PCH), and/or the like.

[0073] For example, the control hub 2432 illustrates one or more connection points for additional devices that connect to device 2400, e.g., through which a user might interact with the system. For example, devices (e.g., devices 2429) that can be attached to the device 2400 include microphone devices, speaker or stereo systems, audio devices, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0074] As mentioned above, control hub 2432 can interact with audio devices, display 2422, etc. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the device 2400. Additionally, audio output can be provided instead of, or in addition to, display output. In another example, if the display 2422 includes a touch screen, the display 2422 also acts as an input device, which can be at least partially managed by the control hub 2432. There can also be additional buttons or switches on the computing device 2400 to provide I/O functions managed by the control hub 2432.

[0075] In one embodiment, control hub 2432 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in the device 2400. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0076] In some embodiments, the control hub 2432 may couple to various devices using any appropriate communication protocol, e.g., PCIe (Peripheral Component Interconnect Express), USB (Universal Serial Bus), Thunderbolt, High Definition Multimedia Interface (HDMI), Firewire, etc.

[0077] In some embodiments, the display 2422 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display

for a user to interact with the device 2400. The display 2422 may include a display interface, a display screen, and/or hardware device used to provide a display to a user. In some embodiments, the display 2422 includes a touch screen (or touch pad) device that provides both output and input to a user. In an example, the display 2422 may communicate directly with the processor 2404. In some embodiments and although not illustrated in the figure, in addition to (or instead of) the processor 2404, the device 2400 may include Graphics Processing Unit (GPU) comprising one or more graphics processing cores, which may control one or more aspects of displaying contents on the display 2422.

[0078] The control hub 2432 may include hardware interfaces and connectors, as well as software components (e.g., drivers, protocol stacks) to make peripheral connections, e.g., to the peripheral devices 2424. It will be understood that the device 2400 could both be a peripheral device to other computing devices, as well as have peripheral devices connected to it. The device 2400 may have a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on device 2400. Additionally, a docking connector can allow the device 2400 to connect to certain peripherals that allow the computing device 2400 to control content output, for example, to audiovisual or other systems.

[0079] In addition to a proprietary docking connector or other proprietary connection hardware, the device 2400 can make peripheral connections via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

[0080] In some embodiments, the connectivity circuitries 2431 may be coupled to the control hub 2432, e.g., in addition to, or instead of, being coupled directly to the processor 2404. In some embodiments, the display 2422 may be coupled to the control hub 2432, e.g., in addition to, or instead of, being coupled directly to the processor 2404.

[0081] In some embodiments, the device 2400 comprises a memory 2430 coupled to the processor 2404 via a memory interface 2434. The memory 2430 includes memory devices for storing information in the device 2400. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory 2430 can store application data, user data, music, photos, documents, or other data, as well as

system data (whether long-term or temporary) related to the execution of the applications and functions of the device 2400.

[0082] Elements of various embodiments and examples are also provided as a machine-readable medium (e.g., memory 2430) for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium (e.g., memory 2430) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[0083] In some embodiments, the device 2400 comprises temperature measurement circuitries 2440, e.g., for measuring temperature of various components of the device 2400. In an example, the temperature measurement circuitries 2440 may be embedded, or coupled or attached to various components, whose temperatures are to be measured and monitored. For example, the temperature measurement circuitries 2440 may measure temperature of (or within) one or more of the cores 2408a, 2408b, 2408c, a voltage regulator 2414, the memory 2430, a mother-board of the SOC 2401, and/or any appropriate component of the device 2400.

[0084] In some embodiments, the device 2400 comprises power measurement circuitries 2442, e.g., for measuring power consumed by one or more components of the device 2400. In an example, in addition to, or instead of, measuring power, the power measurement circuitries 2442 may measure voltage and/or current. In an example, the power measurement circuitries 2442 may be embedded, or coupled or attached to various components, whose power, voltage, and/or current consumption are to be measured and monitored. For example, the power measurement circuitries 2442 may measure power, current and/or voltage supplied by one or more voltage regulators 2414, power supplied to the SOC 2401, power supplied to the device 2400, power consumed by the processor 2404 (or any other component) of the device 2400, etc.

[0085] In some embodiments, the device 2400 comprises one or more voltage regulator circuitries, generally referred to as voltage regulator (VR) 2414. The VR 2414 generates signals at appropriate voltage levels, which may be supplied to operate any

appropriate components of the device 2400. Merely as an example, the VR 2414 is illustrated to be supplying signals to the processor 2404 of the device 2400. In some embodiments, the VR 2414 receives one or more Voltage Identification (VID) signals, and generates the voltage signal at an appropriate level, based on the VID signals.

[0086] In some embodiments, the device 2400 comprises one or more clock generator circuitries, generally referred to as clock generator 2416. The clock generator 2416 generates clock signals at appropriate frequency levels, which may be supplied to any appropriate components of the device 2400. Merely as an example, the clock generator 2416 is illustrated to be supplying clock signals to the processor 2404 of the device 2400. In some embodiments, the clock generator 2416 receives one or more Frequency Identification (FID) signals, and generates the clock signals at an appropriate frequency, based on the FID signals.

[0087] In some embodiments, the device 2400 comprises a battery 2418 supplying power to various components of the device 2400. Merely as an example, the battery 2418 is illustrated to be supplying power to the processor 2404. Although not illustrated in the figures, the device 2400 may comprise a charging circuitry, e.g., to recharge the battery, based on Alternating Current (AC) power supply received from an AC adapter.

[0088] In some embodiments, the device 2400 comprises a Power Control Unit (PCU) 2410 (also referred to as Power Management Unit (PMU), Power Controller, etc.). In an example, some sections of the PCU 2410 may be implemented by one or more processing cores 2408, and these sections of the PCU 2410 are symbolically illustrated using a dotted box and labelled as PCU 2410a. In an example, some other sections of the PCU 2410 may be implemented outside the processing cores 2408, and these sections of the PCU 2410 are symbolically illustrated using a dotted box and labelled as PCU 2410b. The PCU 2410 may implement various power management operations for the device 2400. The PCU 2410 may include hardware interfaces, hardware circuitries, connectors, registers, etc., as well as software components (e.g., drivers, protocol stacks), to implement various power management operations for the device 2400.

[0089] In some embodiments, the device 2400 comprises a Power Management Integrated Circuit (PMIC) 2412 (e.g., 102), e.g., to implement various power management operations for the device 2400. In an example, the PMIC is within an IC chip separate from the processor 2404. This may implement various power management operations for the device 2400. The PMIC 2412 may include hardware interfaces, hardware circuitries, connectors, registers, etc., as well as software components (e.g., drivers, protocol stacks), to implement various power management operations for the device 2400.

[0090] In an example, the device 2400 comprises one or both the PCU 2410 (e.g., 105) or the PMIC 2412. In an example, any one of the PCU 2410 or the PMIC 2412 may be absent in the device 2400, and hence, these components are illustrated using dotted lines.

[0091] Various power management operations of the device 2400 may be performed by the PCU 2410, by the PMIC 2412, or by a combination of the PCU 2410 and PMIC 2412. For example, the PCU 2410 and/or PMIC 2412 may select a power state (e.g., P-state) for various components of the device 2400. For example, the PCU 2410 and/or PMIC 2412 may select a power state (e.g., in accordance with the ACPI (Advanced Configuration and Power Interface) specification) for various components of the device 2400. Merely as an example, the PCU 2410 and/or PMIC 2412 may cause various components of the device 2400 to transition to a sleep state, to an active state, to an appropriate C state (e.g., C0 state, or another appropriate C state, in accordance with the ACPI specification), etc. In an example, the PCU 2410 and/or PMIC 2412 may control a voltage output by the VR 2414 and/or a frequency of a clock signal output by the clock generator, e.g., by outputting the VID signal and/or the FID signal, respectively. In an example, the PCU 2410 and/or PMIC 2412 may control battery power usage, charging of the battery 2418, and features related to power saving operation.

[0092] In an example, the PCU 2410 and/or PMIC 2412 may perform power management operations, e.g., based at least in part on receiving measurements from the power measurement circuitries 2442, temperature measurement circuitries 2440, charge level of the battery 2418, and/or any other appropriate information that may be used for power management.

[0093] Also illustrated is an example software stack of the device 2400 (although not all elements of the software stack are illustrated). Merely as an example, the processors 2404 may execute application programs 2450, an Operating System 2452, one or more Power Management (PM) specific application programs (e.g., generically referred to as PM applications 2458), and/or the like. The PM applications 2458 may also be executed by the PCU 2410 and/or PMIC 2412. The OS 2452 may also include one or more PM applications 2456a, 2456b, 2456c. The OS 2452 may also include various drivers 2454a, 2454b, 2454c, etc., some of which may be specific for power management purposes. In some embodiments, the device 2400 may further comprise a Basic Input/Output System (BIOS) 2420. The BIOS 2420 may communicate with the OS 2452 (e.g., via one or more drivers 2454), communicate with the processor 2404, etc.

[0094] For example, one or more of the PM applications 2458, 2456, drivers 2454, BIOS 2420, etc. may be used to implement power management specific tasks, e.g., to control voltage and/or frequency of various components of the device 2400, to control wake-up state, sleep state, and/or any other appropriate power state of various components of the device 2400, control battery power usage, charging of the battery 2418, features related to power saving operation, etc.

[0095] In some embodiments, voltage regulator 2414 has the feature of VR 106. In some embodiments, the apparatus for combined fast coordination of various mechanisms in VR 2414 and processor operation for effective and proactive power management. While the embodiments are described with reference to a buck DC-DC converter for VR 2414, the embodiments are not limited to such. Other forms of voltage generating circuitries such as low dropout (LDO) regulators, boost DC-DC converter, etc. can also be used in the overall system to proactively manage power of the processor and/or the entire computing system.

[0096] In some embodiments, VR 2414 goes into cycle-by-cycle current limit, and provides a signal to the processor that enacts throttling in response to certain performance metrics exceeding predetermined (or programmable) thresholds. For example, when the current through a high-side switch of VR 2414 increases a threshold current level between two VR switching cycles (or another number of cycles), then a PCU 2410b or any other suitable logic may instruct the processor to throttle its operating frequency. In one such embodiment, a divider ratio of a PLL (phase locked loop) is adjusted to reduce the operating frequency of the clock used by the processor without having the PLL lose phase lock. As such, fast throttling in the processor is executed with minimal latency when VR goes into current limit at real application level.

[0097] In some cases, the voltage on the power supply rail Vout providing power to the processor droops when the processor (or load) current exceeds the level expected for real application. In some embodiments, the apparatus monitors the droop and when the voltage drops below a certain threshold, PCU 2410b or any other suitable power management circuity may send a signal to the processor to throttle its operating frequency to reduce the load before the complete droop occurs. In some embodiments, the occurrence of the voltage droop or current spike is estimated based on execution of the real application on the processor 2404. For example, speculative execution of certain instructions or other instruction in a pipeline can provide an indication that a voltage droop may occur and so the processor may want to throttle its frequency to avoid a possible shutdown of the VR and hence the processing system.

[0098] These signals from PCU 2410b or power management circuitries to the processor are not alarm(s), but part of a mechanism that allows VR 2414 to be designed for a low current rating. In some embodiments, when a large droop occurs the decoupling capacitance or alternatively a clamp circuit support the voltage on the power supply rail during the time the load exceeds the VR voltage/current peak limit. As such, VR 2414 can be designed to operate for real application power delivery while allowing short durations of processor peak power.

[0099] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[00100] Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[00101] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[00102] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present

disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[00103] Following examples are provided to illustrate the various embodiments. These examples can depend from one another in any suitable manner.

[00104] Example 1: An apparatus comprising: a power supply generator (e.g., VR 106_1) to provide current and voltage to a power supply rail (e.g., rail Vout); a processor core (e.g., 103_1) coupled to the power supply rail, the processor core to operate with the current and voltage provided by the power supply generator; a first circuitry (e.g., sensor 202 or 222) to monitor the current provided by power supply generator; and a second circuitry (e.g., limiter 107 or VR controller 201) to at least partially turn off the power supply generator when the monitored current crosses a threshold current (e.g., IccMax threshold).

[00105] Example 2: The apparatus of example 1 further comprising: a third circuitry (e.g., PCU 105 or limiter 107) to request the processor core to reduce a current draw from the power supply rail when the second circuitry determines that the monitored current crossed the threshold current.

[00106] Example 3: The apparatus of example 2 further comprising: a fourth circuitry (e.g., droop detector 203) to monitor the voltage on the power supply rail, wherein the third circuitry is to request processor core to reduce one or more performance parameters when the fourth circuitry determines that the monitored voltage crossed a threshold voltage.

[00107] Example 4: The apparatus of example 3, wherein the one or more performance parameters include: an operating frequency, fan speed, current draw, and divider ratio.

[00108] Example 5: The apparatus of example 3 further comprising a clamp circuitry (e.g., circuitry 301) to clamp the voltage on the power supply rail to a predetermined voltage level when the fourth circuitry determines that the monitored voltage crossed a threshold voltage.

[00109] Example 6: The apparatus of example 1, wherein the power supply generator comprises a high-side switch (e.g., MP1) and a low-side switch (e.g., MN1), wherein the high-side switch is coupled in series with the low-side switch, and wherein the high-side switch is turned off (e.g., using switch override) by the second circuitry when the monitored current crosses the threshold current.

[00110] Example 7: The apparatus of example 6, wherein the second circuitry is to turn off the high-side switch for a duration of an expected voltage droop on the power supply rail.

[00111] Example 8: The apparatus of example 6, wherein the second circuitry is to turn off the high-side switch for a duration of a voltage droop on the power supply rail, and is to turn on the high-side switch when the voltage droop substantially ends.

[00112] Example 9: The apparatus of example 1, wherein the power supply generator is one of: a DC-DC converter, a buck converter, a boost converter, a low dropout (LDO) regulator, a switched capacitor voltage regulator, or a bi-directional DC-DC converter.

[00113] Example 10: An apparatus comprising: a power supply rail (e.g., Vout) to receive a current and a voltage from a power supply generator; a processor coupled to the power supply rail, wherein the processor (e.g., 101) is to operate with a current and a voltage provided by the power supply rail; and an interface (input of processor core 103_1) to receive a request to throttle one or more performance parameters of the processor when a monitored current through the power supply rail or a monitored voltage on the power supply rail crosses a threshold current or a threshold voltage, respectively, wherein the threshold current is below a catastrophic threshold current of the VR, or wherein the threshold voltage is above a catastrophic threshold voltage of the processor.

[00114] Example 11: The apparatus of example 10, wherein the one or more performance parameters include: an operating frequency, fan speed, current draw, and phase lock loop (PLL) divider ratio.

[00115] Example 12: The apparatus of example 10 further comprises a clamp circuitry to clamp the voltage on the power supply rail to a predetermined voltage level when the monitored voltage crosses the threshold voltage.

[00116] Example 13: The apparatus of example 10, wherein the power supply generator comprises a high-side switch and a low-side switch, wherein the high-side switch is coupled in series with the low-side switch, and wherein the high-side switch is turned off when the monitored current crosses the threshold current.

[00117] Example 14: The apparatus of example 10, wherein the power supply generator comprises a high-side switch and a low-side switch, wherein the high-side switch is coupled in series with the low-side switch, and wherein the high-side switch is turned off for a duration of an expected voltage droop on the power supply rail.

[00118] Example 15: The apparatus of example 10, wherein the power supply generator comprises a high-side switch and a low-side switch, wherein the high-side switch is coupled in series with the low-side switch, and wherein the high-side switch is turned off for

a duration of a voltage droop on the power supply rail, and wherein the high-side switch is turned back on when the voltage droop substantially ends.

[00119] Example 16: The apparatus of example 10, wherein the power supply generator is one of: a DC-DC converter, a buck converter, a boost converter, a low dropout (LDO) regulator, a switched capacitor voltage regulator, or a bi-directional DC-DC converter.

[00120] Example 17: A system comprising: a DC-DC converter coupled to an inductor and a capacitor; a processor coupled to the DC-DC converter, the processor comprising: a power supply rail coupled to the inductor and the capacitor; and a processor core coupled to the power supply rail, wherein the processor core is to operate with a current and a voltage provided by the DC-DC converter; wherein the DC-DC converter comprises: a first circuitry to monitor current, through the inductor, which is provided as the current to the power supply rail; and a second circuitry to turn off a high-side switch of the DC-DC converter when the monitored current crosses a threshold current; and an interface to allow the processor to communicate with another device.

[00121] Example 18: The system of example 17, wherein the processor comprises a clamp circuitry to clamp the voltage on the power supply rail to a predetermined voltage level when a monitored voltage of the power supply rail crosses the threshold voltage.

[00122] Example 19: The system of example 17 comprises a third circuitry to send a request to the processor to throttle one or more performance parameters of the processor when a monitored current through the power supply rail or a monitored voltage on the power supply rail crosses a threshold current or a threshold voltage, respectively, wherein the threshold current is below a catastrophic threshold current of the VR, or wherein the threshold voltage is above a catastrophic threshold voltage of the processor.

[00123] Example 20: The system of example 19, wherein the one or more performance parameters include: an operating frequency, fan speed, current draw, and phase lock loop (PLL) divider ratio.

[00124] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:

a power supply generator to provide current and voltage to a power supply rail;

a processor core coupled to the power supply rail, the processor core to operate with the current and voltage provided by the power supply generator;

a first circuitry to monitor the current provided by power supply generator; and

a second circuitry to at least partially turn off the power supply generator when the monitored current crosses a threshold current.

2. The apparatus of claim 1 further comprising: a third circuitry to request the processor core to reduce a current draw from the power supply rail when the second circuitry determines that the monitored current crossed the threshold current.

3. The apparatus of claim 2 further comprising: a fourth circuitry to monitor the voltage on the power supply rail, wherein the third circuitry is to request processor core to reduce one or more performance parameters when the fourth circuitry determines that the monitored voltage crossed a threshold voltage.

4. The apparatus of claim 3, wherein the one or more performance parameters include: an operating frequency, fan speed, current draw, and divider ratio.

5. The apparatus of claim 3 further comprising a clamp circuitry to clamp the voltage on the power supply rail to a predetermined voltage level when the fourth circuitry determines that the monitored voltage crossed a threshold voltage.

6. The apparatus according to any one of claims 1 to 5, wherein the power supply generator comprises a high-side switch and a low-side switch, wherein the high-side switch is coupled in series with the low-side switch, and wherein the high-side switch is turned off by the second circuitry when the monitored current crosses the threshold current.

7. The apparatus of claim 6, wherein the second circuitry is to turn off the high-side switch for a duration of an expected voltage droop on the power supply rail.

8. The apparatus of claim 6, wherein the second circuitry is to turn off the high-side switch for a duration of a voltage droop on the power supply rail, and is to turn on the high-side switch when the voltage droop substantially ends.

9. The apparatus according to any one of claims 1 to 5, wherein the power supply generator is one of: a DC-DC converter, a buck converter, a boost converter, a low dropout (LDO) regulator, a switched capacitor voltage regulator, or a bi-directional DC-DC converter.

10. An apparatus comprising:

a power supply rail to receive a current and a voltage from a power supply generator;

a processor coupled to the power supply rail, wherein the processor is to operate with a current and a voltage provided by the power supply rail; and

an interface to receive a request to throttle one or more performance parameters of the processor when a monitored current through the power supply rail or a monitored voltage on the power supply rail crosses a threshold current or a threshold voltage, respectively, wherein the threshold current is below a catastrophic threshold current of a voltage regulator, or wherein the threshold voltage is above a catastrophic threshold voltage of the processor.

11. The apparatus of claim 10, wherein the one or more performance parameters include: an operating frequency, fan speed, current draw, and phase lock loop (PLL) divider ratio.

12. The apparatus of claim 10 further comprises a clamp circuitry to clamp the voltage on the power supply rail to a predetermined voltage level when the monitored voltage crosses the threshold voltage.

13. The apparatus of claim 10, wherein the power supply generator comprises a high-side switch and a low-side switch, wherein the high-side switch is coupled in series with the low-side switch, and wherein the high-side switch is turned off when the monitored current crosses the threshold current.

14. The apparatus of claim 10, wherein the power supply generator comprises a high-side switch and a low-side switch, wherein the high-side switch is coupled in series with the low-side switch, and wherein the high-side switch is turned off for a duration of an expected voltage droop on the power supply rail.

15. The apparatus of claim 10, wherein the power supply generator comprises a high-side switch and a low-side switch, wherein the high-side switch is coupled in series with the low-side switch, and wherein the high-side switch is turned off for a duration of a voltage droop on the power supply rail, and wherein the high-side switch is turned back on when the voltage droop substantially ends.

16. The apparatus according to any one of claims 10 to 15, wherein the power supply generator is one of: a DC-DC converter, a buck converter, a boost converter, a low dropout (LDO) regulator, a switched capacitor voltage regulator, or a bi-directional DC-DC converter.

17. A system comprising:

a DC-DC converter coupled to an inductor and a capacitor;

a processor coupled to the DC-DC converter, the processor comprising:

a power supply rail coupled to the inductor and the capacitor; and

a processor core coupled to the power supply rail, wherein the processor core is to operate with a current and a voltage provided by the DC-DC converter;

wherein the DC-DC converter comprises:

a first circuitry to monitor current, through the inductor, which is provided as the current to the power supply rail; and

a second circuitry to turn off a high-side switch of the DC-DC converter when the monitored current crosses a threshold current; and

an interface to allow the processor to communicate with another device.

18. The system of claim 17, wherein the processor comprises a clamp circuitry to clamp the voltage on the power supply rail to a predetermined voltage level when a monitored voltage of the power supply rail crosses the threshold voltage.

19. The system of claim 17 comprises a third circuitry to send a request to the processor to throttle one or more performance parameters of the processor when a monitored current through the power supply rail or a monitored voltage on the power supply rail crosses a threshold current or a threshold voltage, respectively, wherein the threshold current is below a catastrophic threshold current of a voltage regulator, or wherein the threshold voltage is above a catastrophic threshold voltage of the processor.

20. The system of claim 19, wherein the one or more performance parameters include: an operating frequency, fan speed, current draw, and phase lock loop (PLL) divider ratio.

21. A method comprising:

providing, by a power supply generator, current and voltage to a power supply rail;

operating a processor core, coupled to the power supply rail, with the current and voltage provided by the power supply generator;

monitoring, the current provided by power supply generator; and

at least partially turning off the power supply generator when the monitored current crosses a threshold current.

22. The method of claim 21 further comprising: requesting the processor core to reduce a current draw from the power supply rail when it is determined that the monitored current crossed the threshold current.

23. The apparatus of claim 2 further comprising:

monitoring the voltage on the power supply rail; and

requesting the processor core to reduce one or more performance parameters when it is determined that the monitored voltage crossed a threshold voltage.

24. The apparatus of claim 23, wherein the one or more performance parameters include: an operating frequency, fan speed, current draw, and divider ratio.

25. The apparatus of claim 23 further comprising clamping the voltage on the power supply rail to a predetermined voltage level when it is determined that the monitored voltage crossed a threshold voltage.

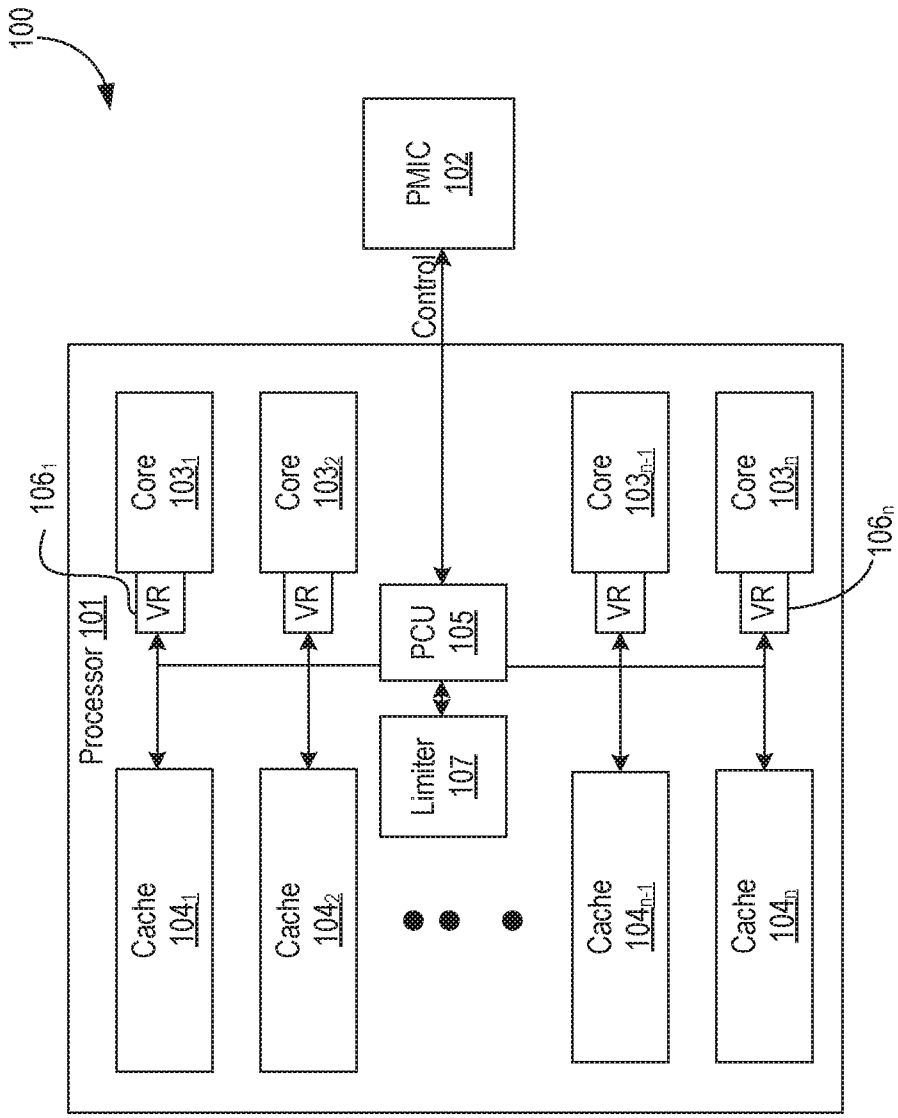

100
PMIC 102
Control
Processor 101
106_1
106_n
Core 103_1
Core 103_2
Core 103_{n-1}
Core 103_n
VR
PCU 105
Limiter 107
Cache 104_1
Cache 104_2
Cache 104_{n-1}
Cache 104_n

Fig. 1A

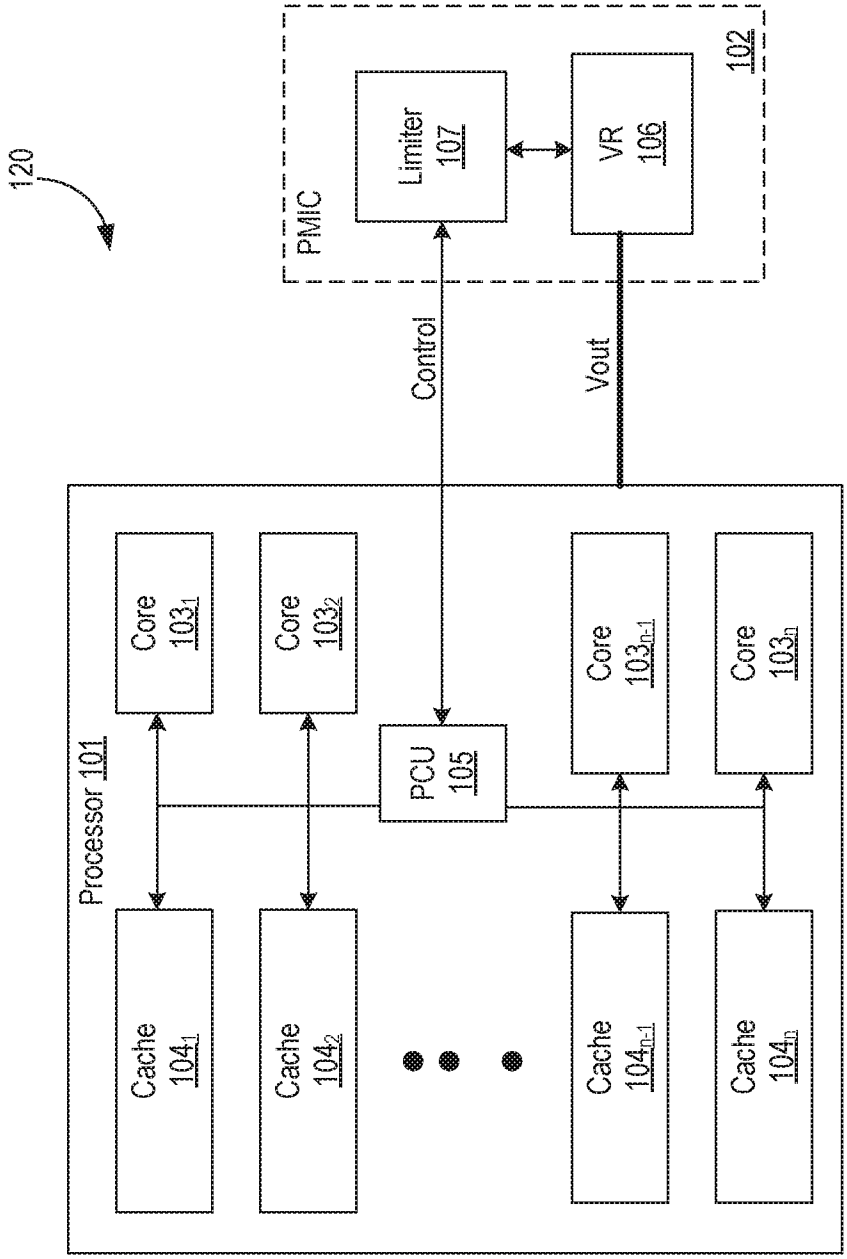

120
PMIC
102
Limiter 107
VR 106
Control
Vout
Processor 101
Core 103$_1$
Core 103$_2$
Core 103$_{n-1}$
Core 103$_n$
PCU 105
Cache 104$_1$
Cache 104$_2$
Cache 104$_{n-1}$
Cache 104$_n$

Fig. 1B

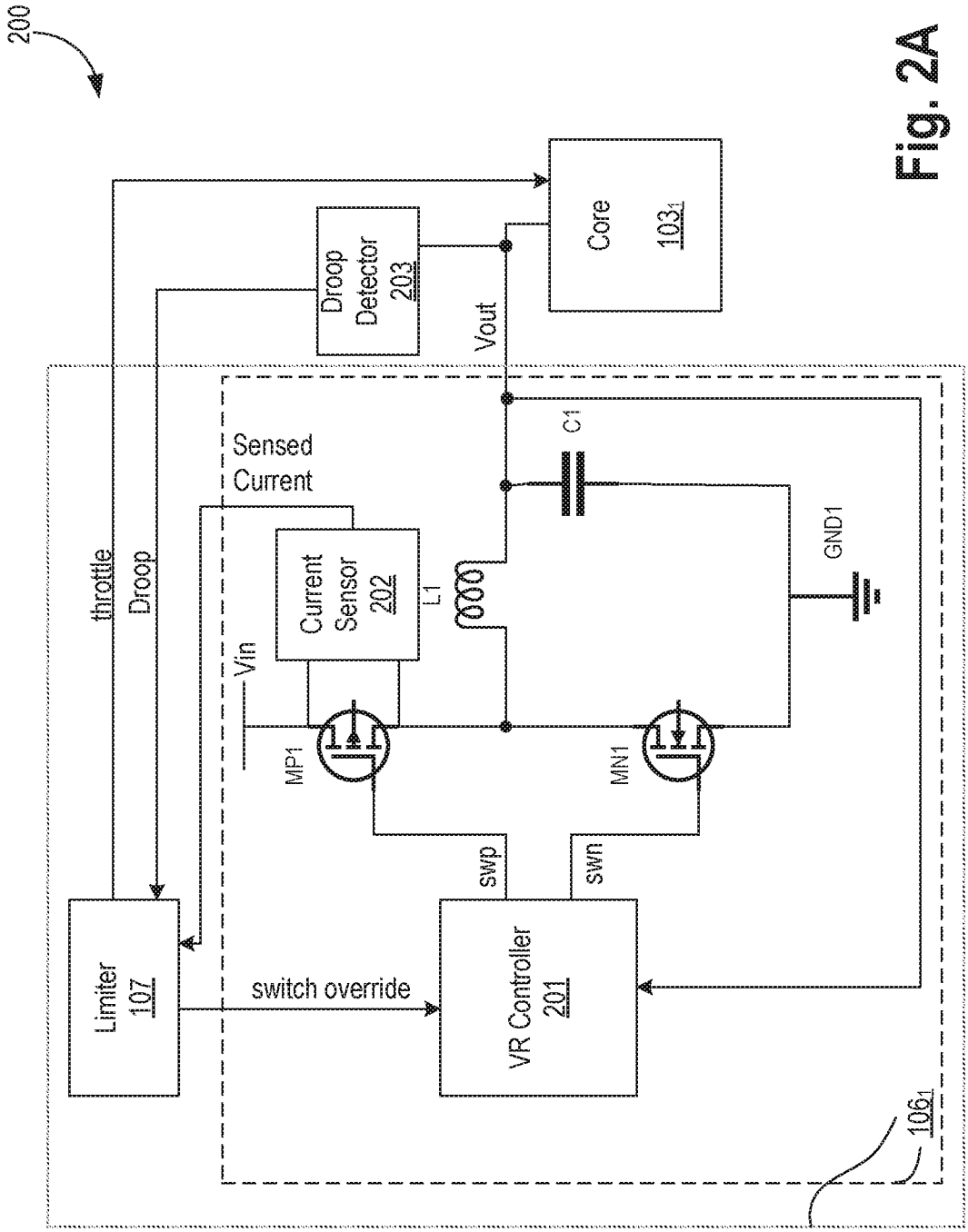

200
Core
103_1
Droop
Detector
203
Vout
C1
Sensed
Current
throttle
Droop
Current
Sensor
202
L1
GND1
Vin
MP1
MN1
swp
swn
Limiter
107
switch override
VR Controller
201
106_1

Fig. 2A

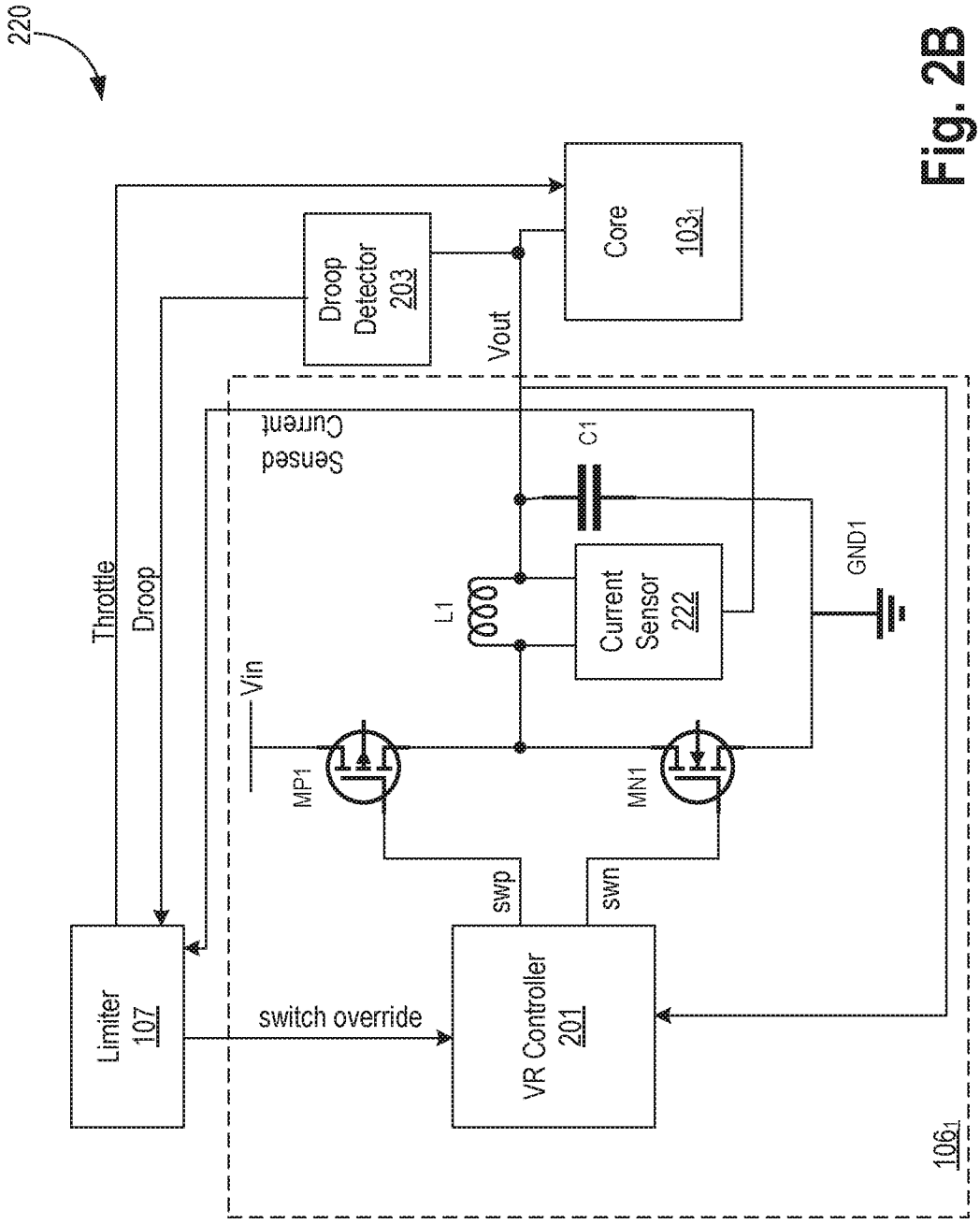

220
Core
103_1
Droop Detector
203
Vout
Sensed Current
C1
Throttle
Droop
L1
Current Sensor
222
GND1
Vin
MP1
MN1
swp
swn
Limiter
107
switch override
VR Controller
201
106_1

Fig. 2B

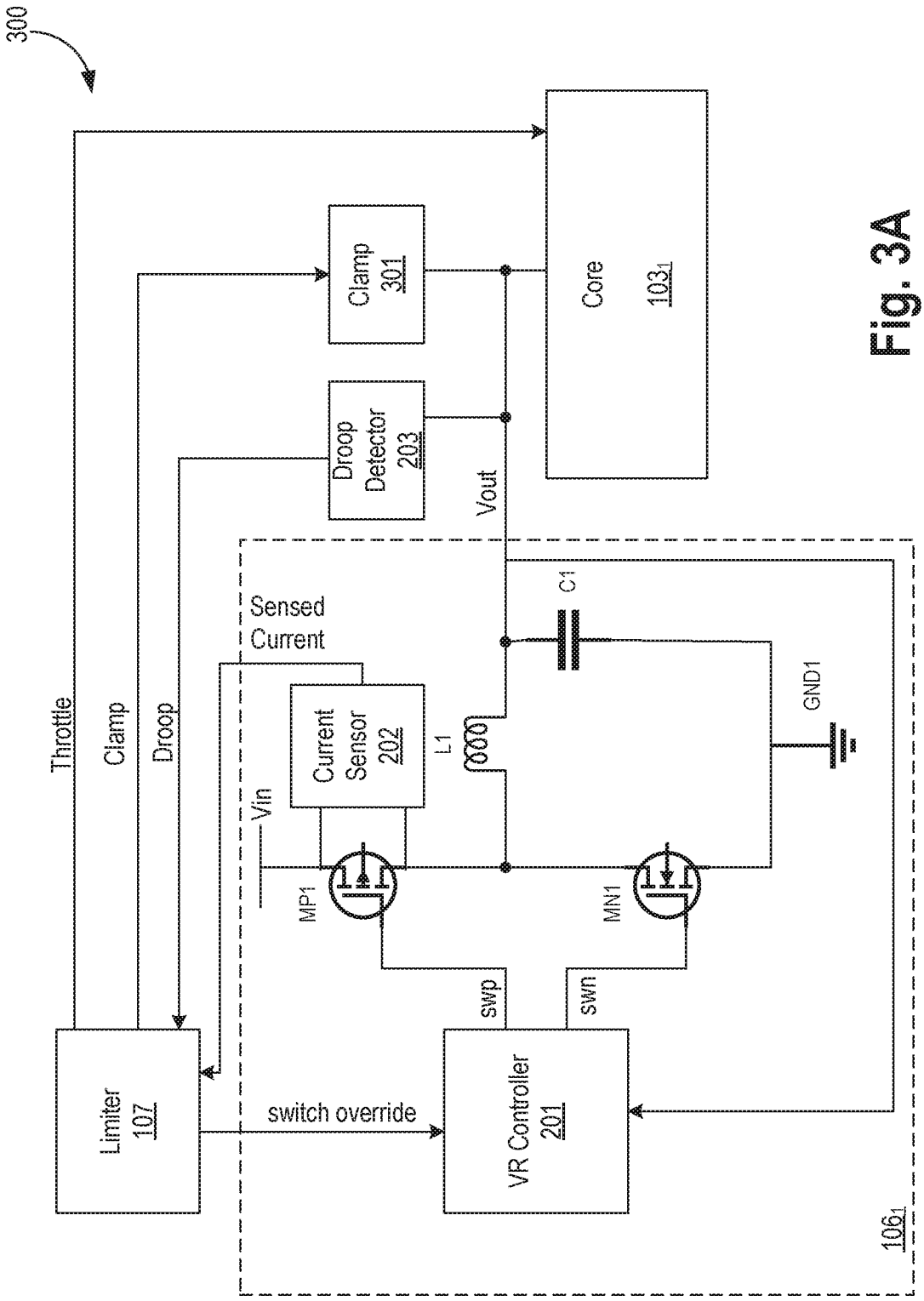

300
Core
103_1
Clamp
301
Droop
Detector
203
Vout
C1
Sensed
Current
Throttle
Clamp
Droop
Current
Sensor
202
L1
GND1
Vin
MP1
MN1
swp
swn
Limiter
107
switch override
VR Controller
201
106_1

Fig. 3A

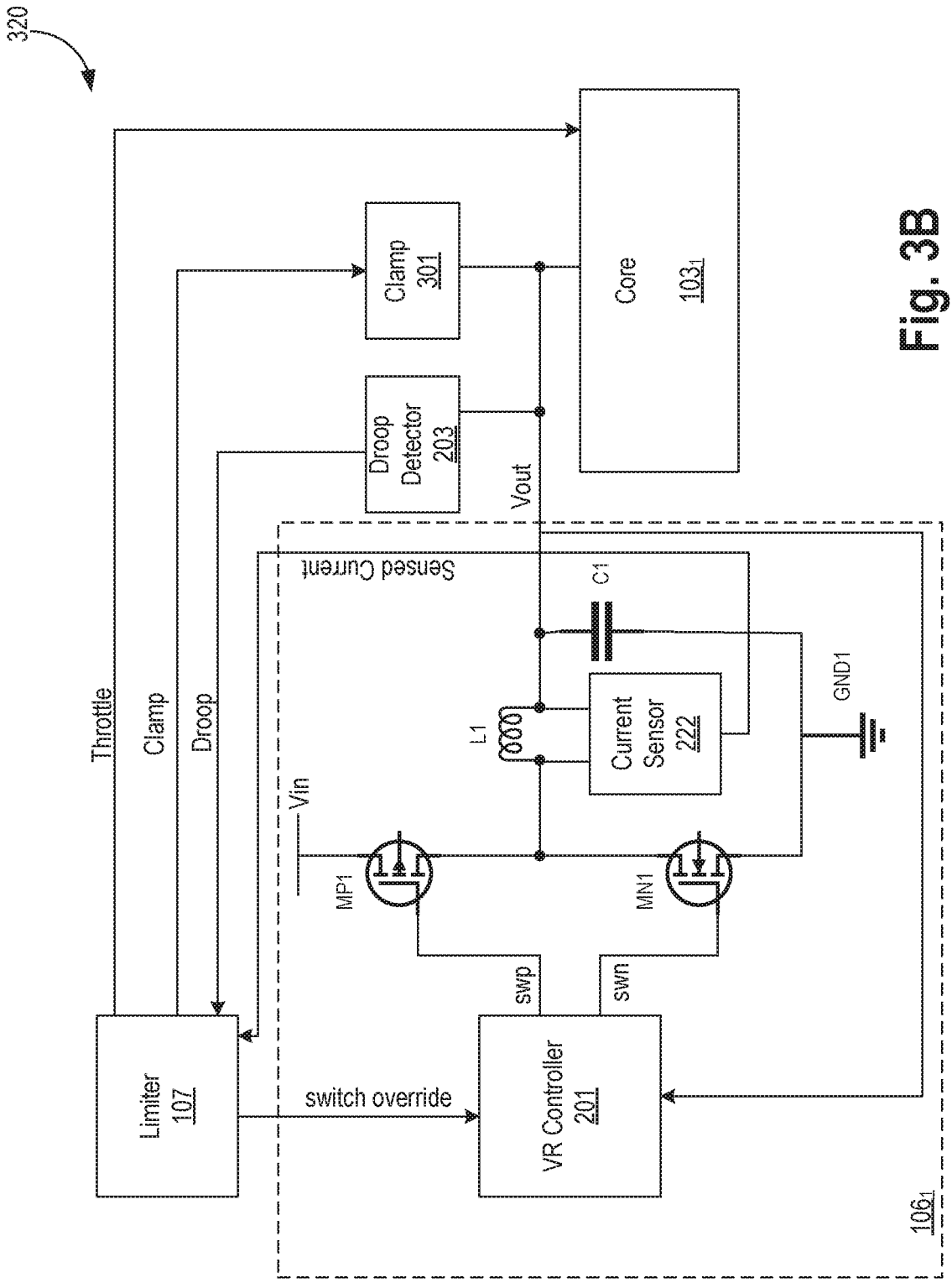

320
Core
103_1
Clamp
301
Droop
Detector
203
Vout
Sensed Current
C1
GND1
Throttle
Clamp
Droop
L1
Current
Sensor
222
Vin
MP1
MN1
swp
swn
Limiter
107
switch override
VR Controller
201
106_1

Fig. 3B

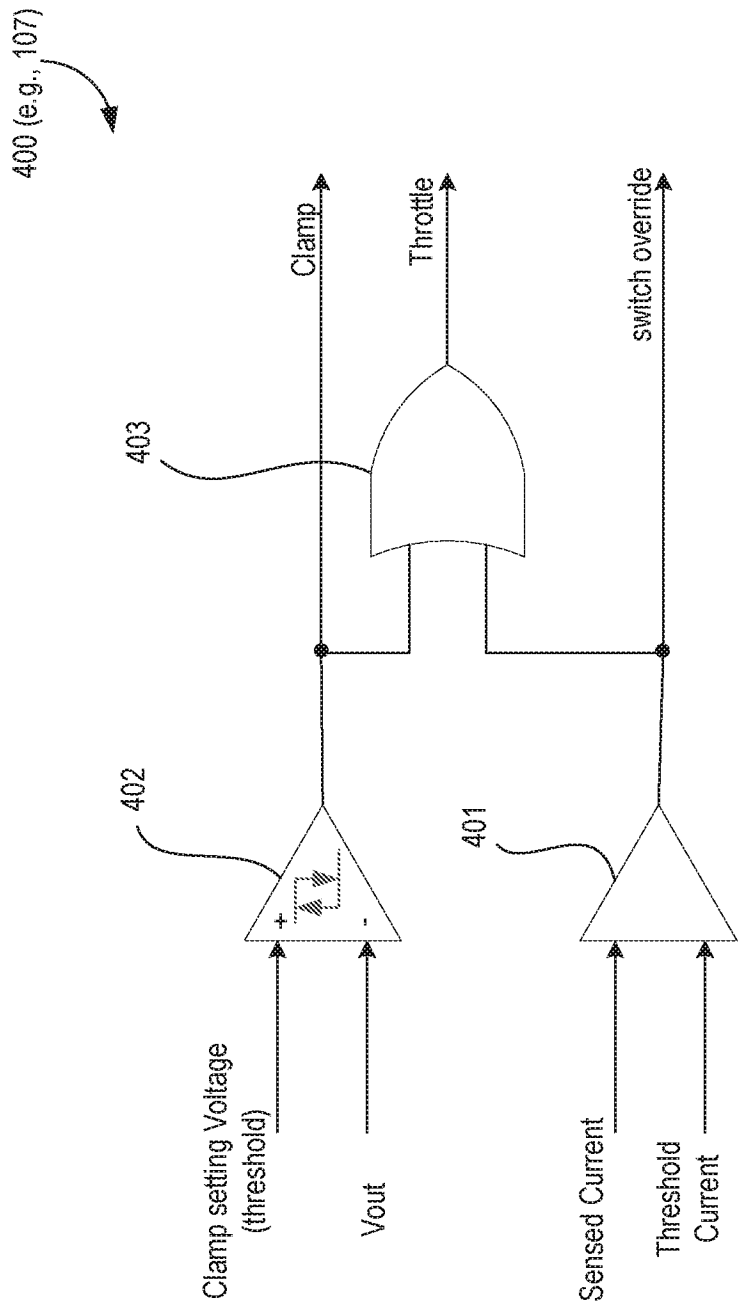

400 (e.g., 107)
Clamp
Throttle
switch override
403
402
401
+
-
Clamp setting Voltage (threshold)
Vout
Sensed Current
Threshold Current

Fig. 4

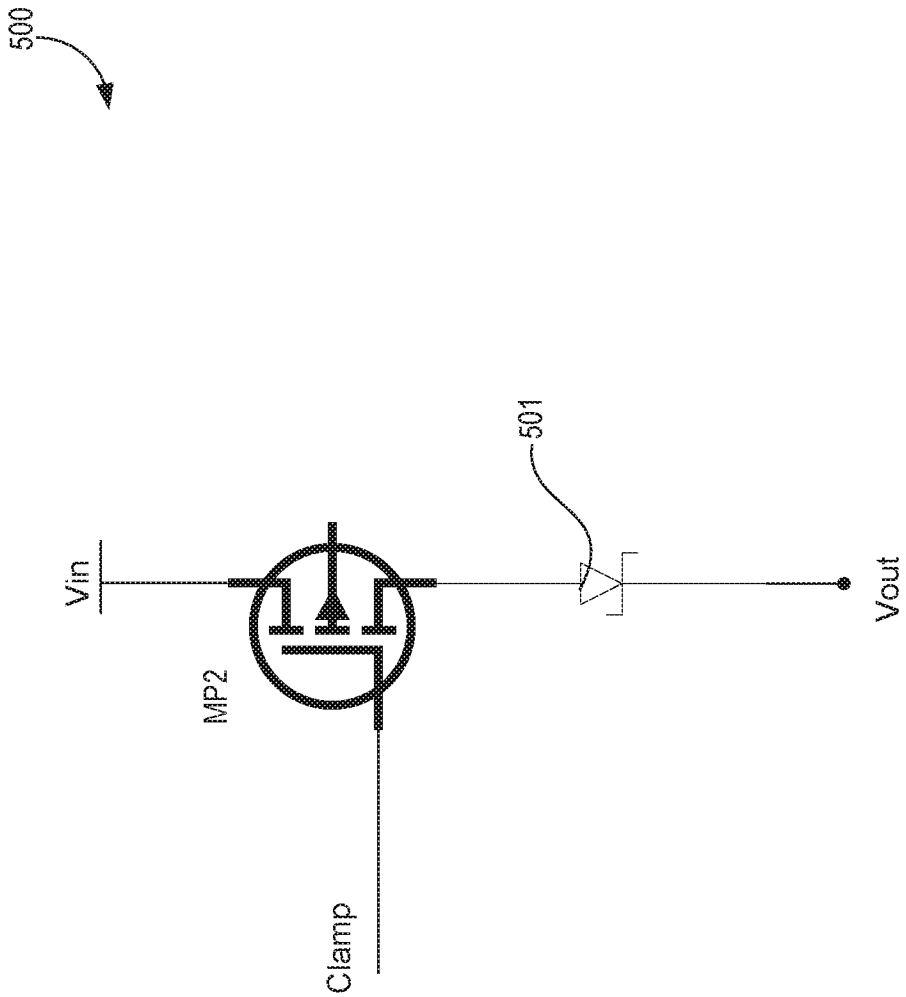


Fig. 5

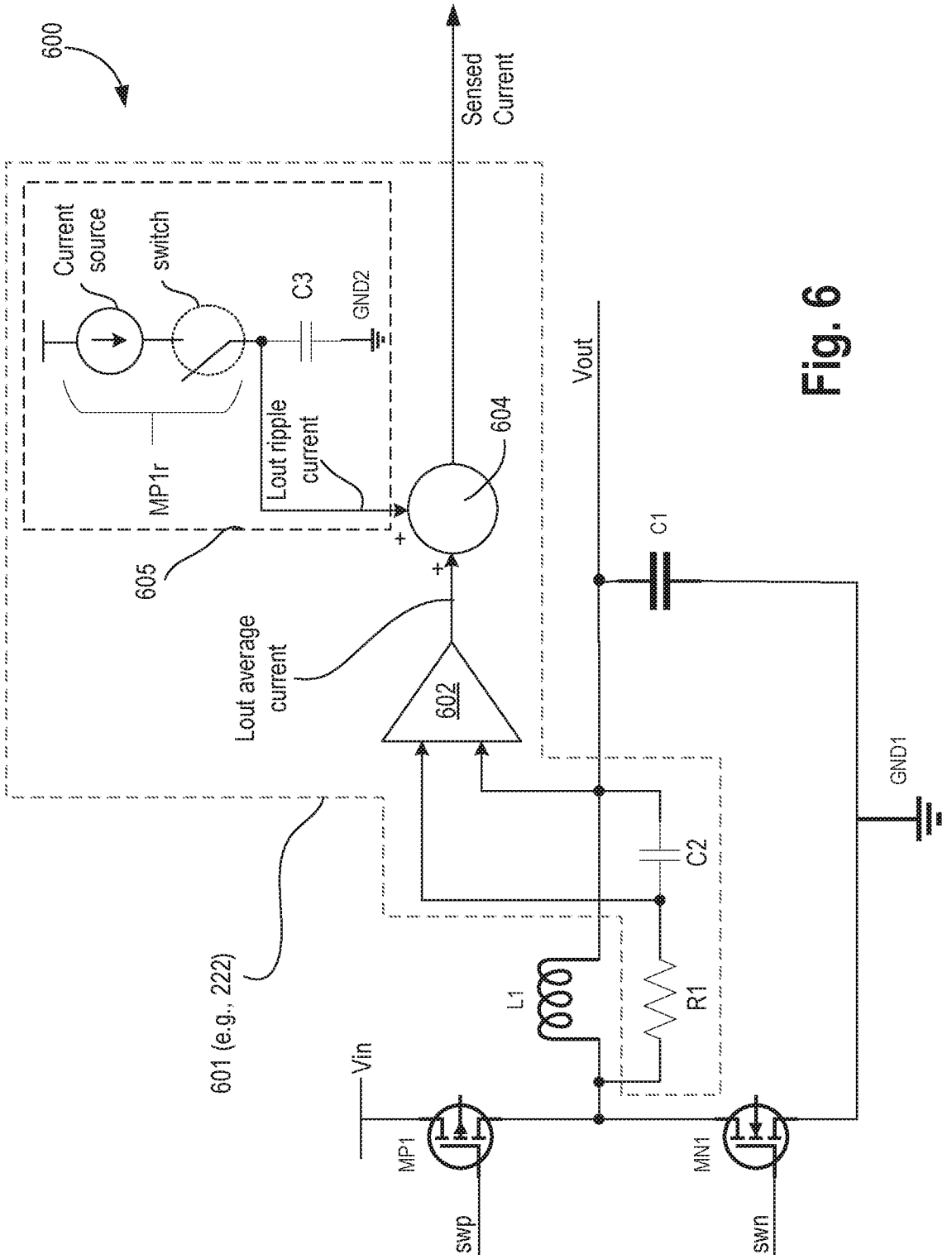

600
Sensed Current
Current source
switch
C3
GND2
MP1r
Lout ripple current
604
605
Vout
C1
Lout average current
602
GND1
C2
601 (e.g., 222)
L1
R1
Vin
MP1
MN1
swp
swn

Fig. 6

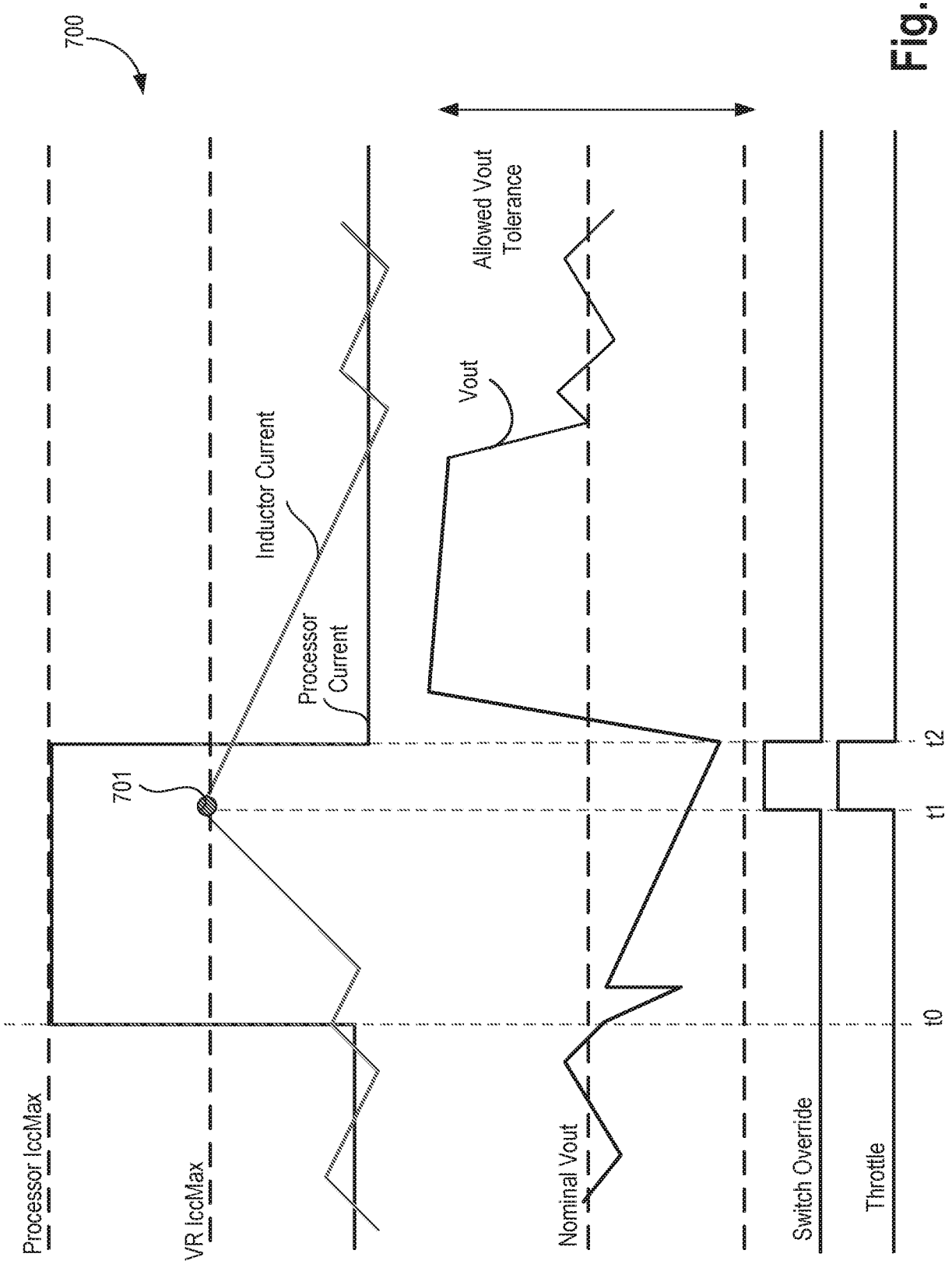

700
Processor IccMax
VR IccMax
701
Inductor Current
Processor Current
Vout
Allowed Vout Tolerance
Nominal Vout
Switch Override
Throttle
t0
t1
t2

Fig. 7

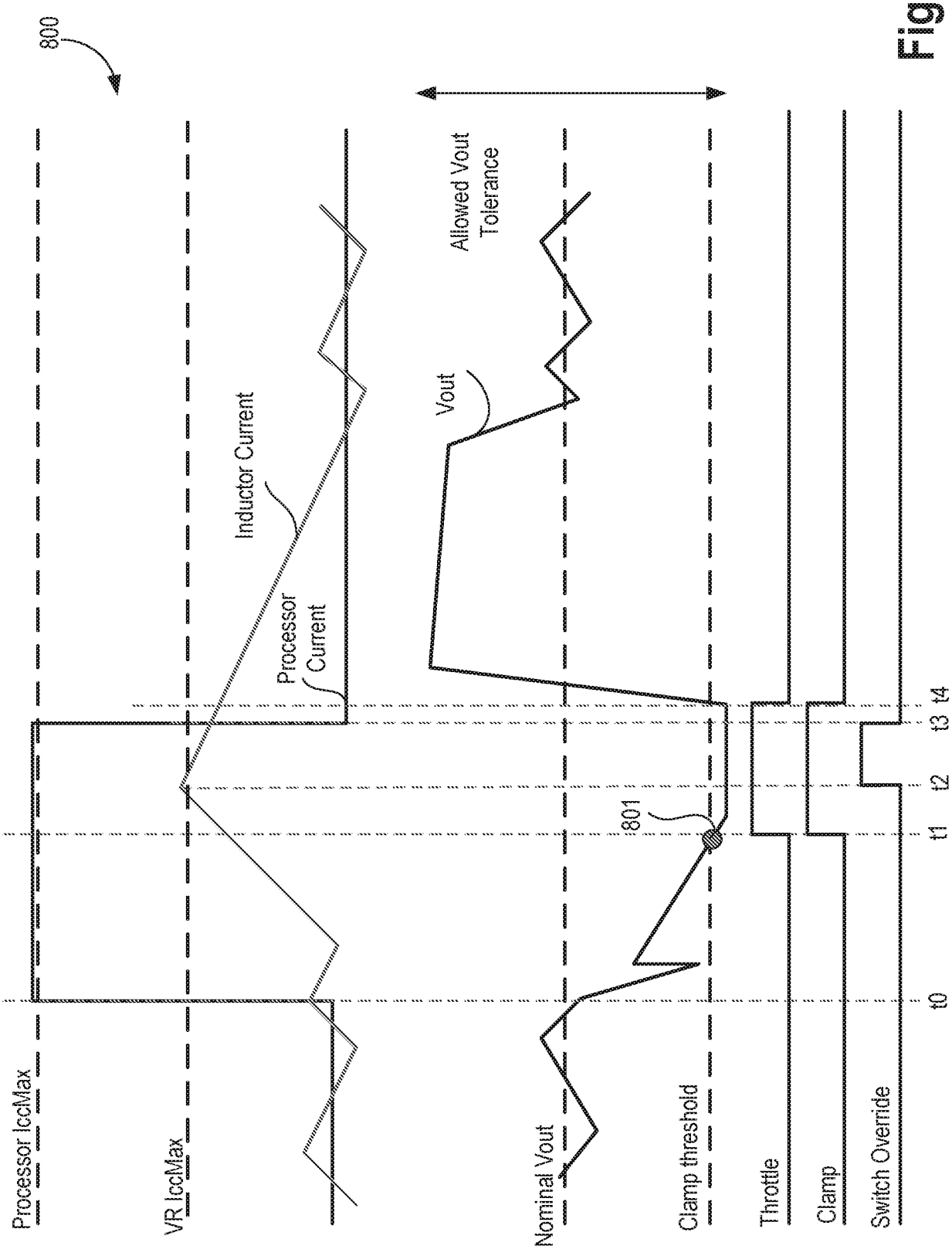

800
Processor IccMax
VR IccMax
Inductor Current
Processor Current
Vout
Allowed Vout Tolerance
Nominal Vout
Clamp threshold
801
Throttle
Clamp
Switch Override
t0
t1
t2
t3
t4

Fig. 8

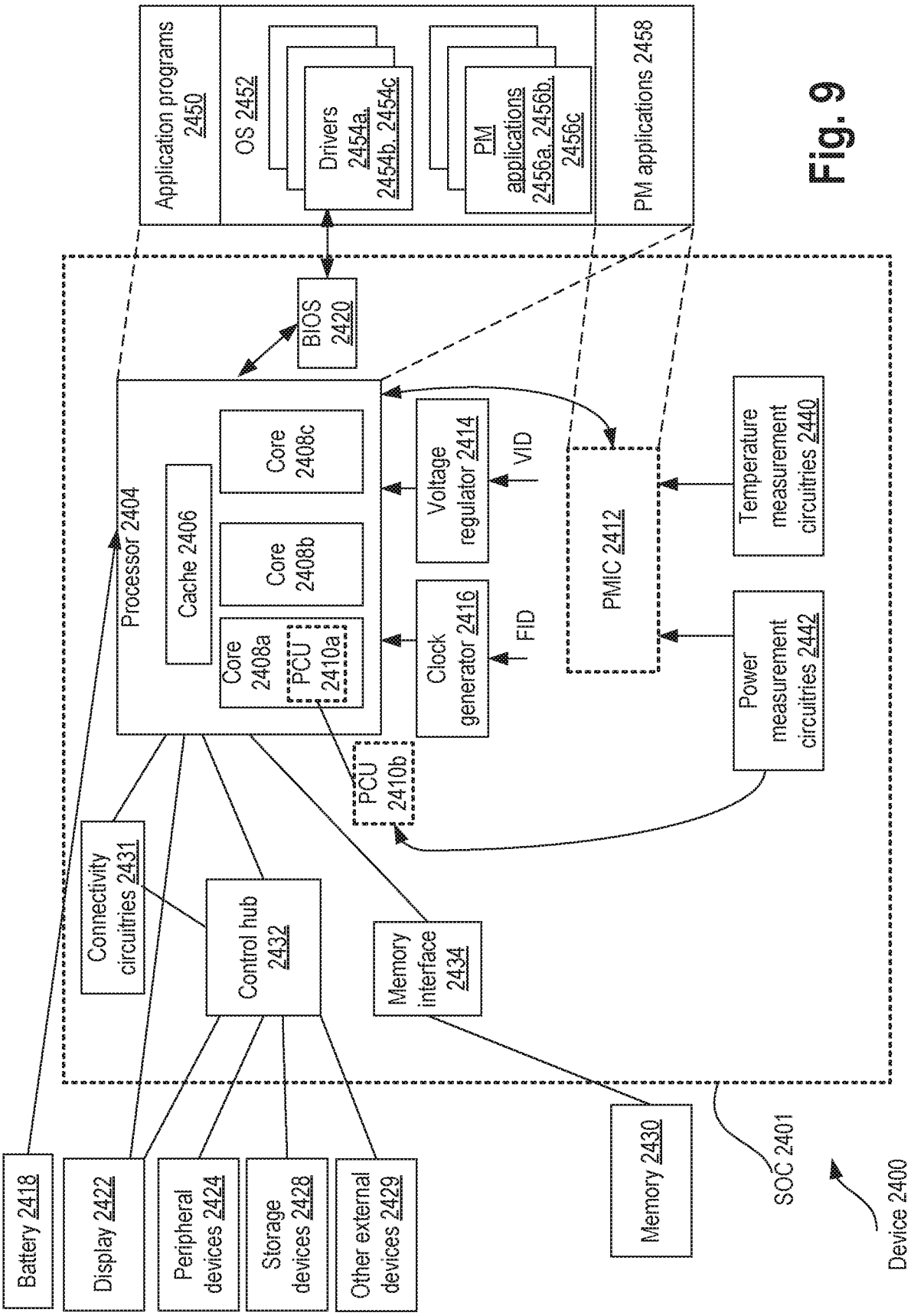

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Drivers 2454a, 2454b, 2454c
PM applications 2456a, 2456b, 2456c
PM applications 2458
BIOS 2420
Processor 2404
Cache 2406
Core 2408a
PCU 2410a
Core 2408b
Core 2408c
PCU 2410b
Voltage regulator 2414
VID
Clock generator 2416
FID
PMIC 2412
Temperature measurement circuitries 2440
Power measurement circuitries 2442
Connectivity circuitries 2431
Control hub 2432
Memory interface 2434
Battery 2418
Display 2422
Peripheral devices 2424
Storage devices 2428
Other external devices 2429
Memory 2430
SOC 2401
Device 2400

Fig. 9

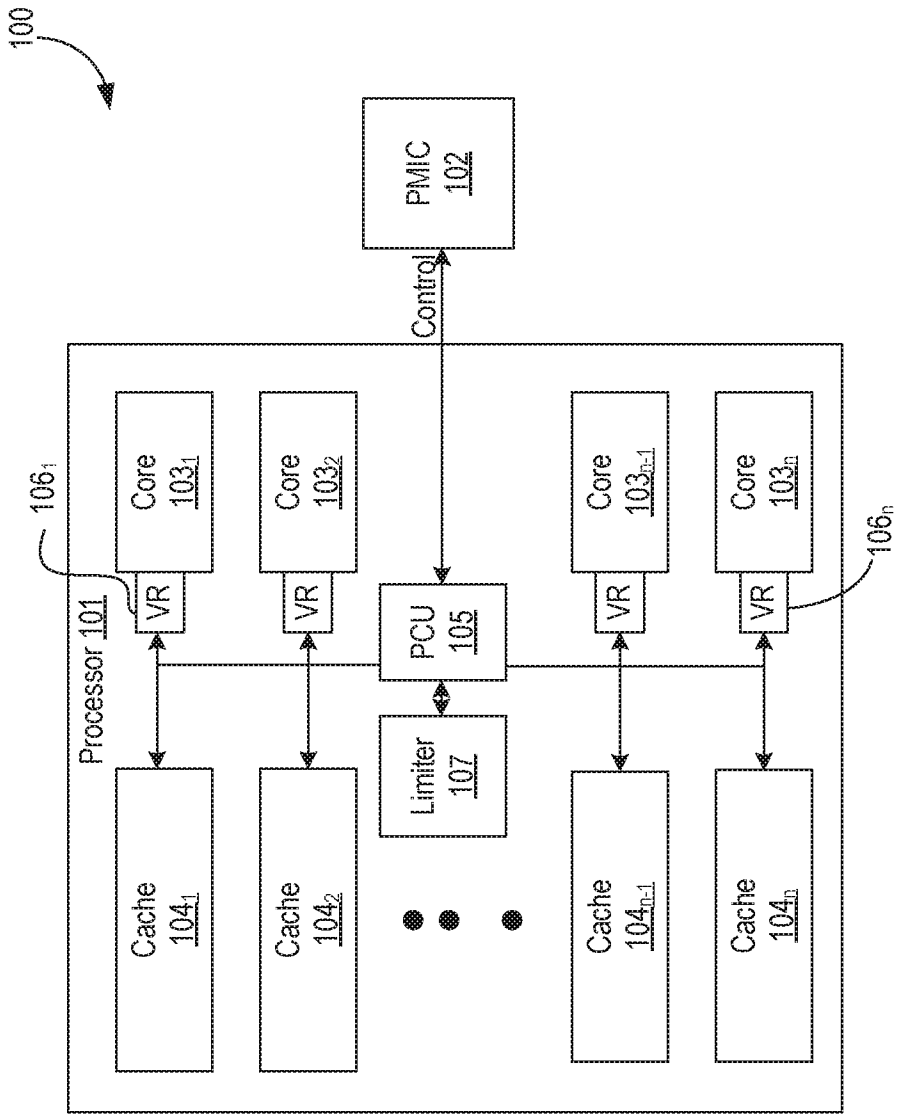

100
PMIC 102
Control
Processor 101
Core 103$_1$
Core 103$_2$
Core 103$_{n-1}$
Core 103$_n$
VR
PCU 105
Limiter 107
Cache 104$_1$
Cache 104$_2$
Cache 104$_{n-1}$
Cache 104$_n$
106$_1$
106$_n$

Fig. 1A

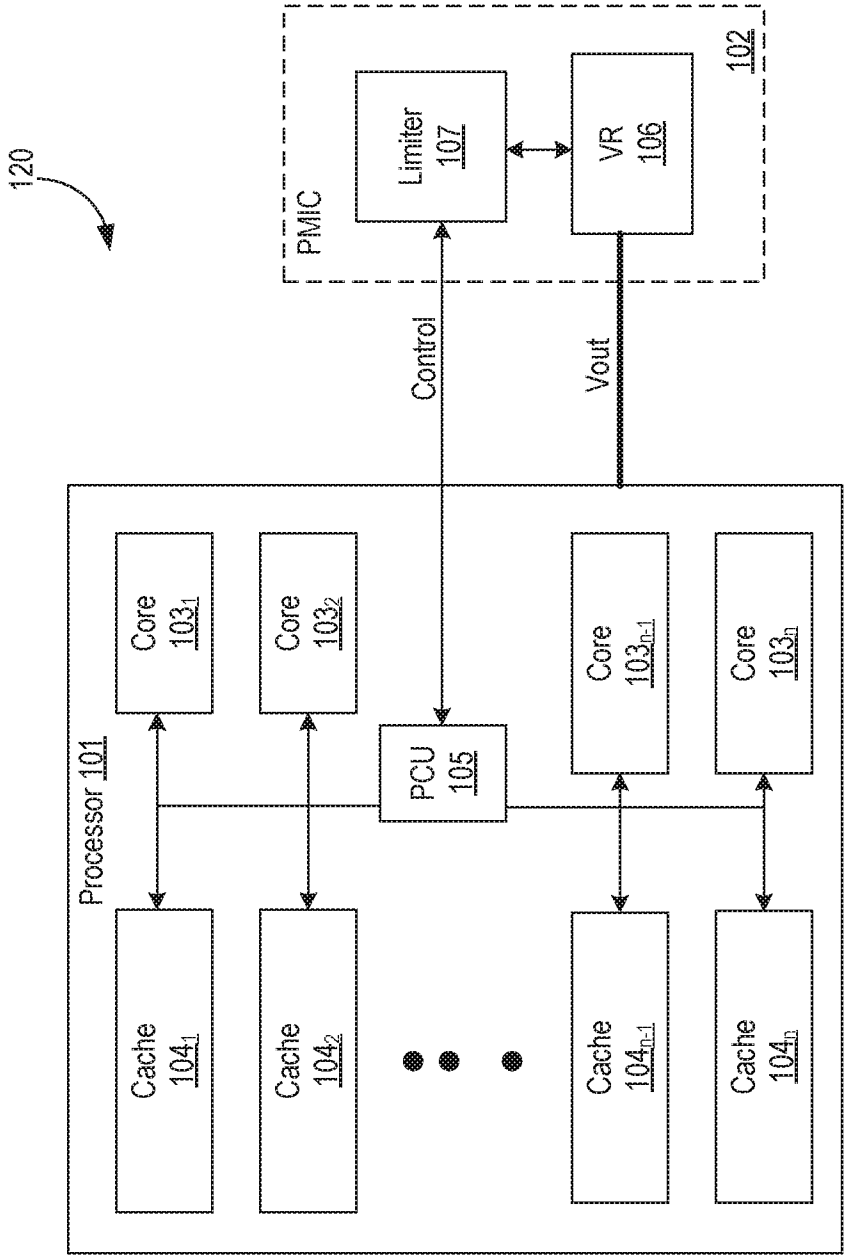

120
PMIC
102
Limiter 107
VR 106
Control
Vout
Processor 101
Core 103_1
Core 103_2
Core 103_n-1
Core 103_n
PCU 105
Cache 104_1
Cache 104_2
Cache 104_n-1
Cache 104_n

Fig. 1B

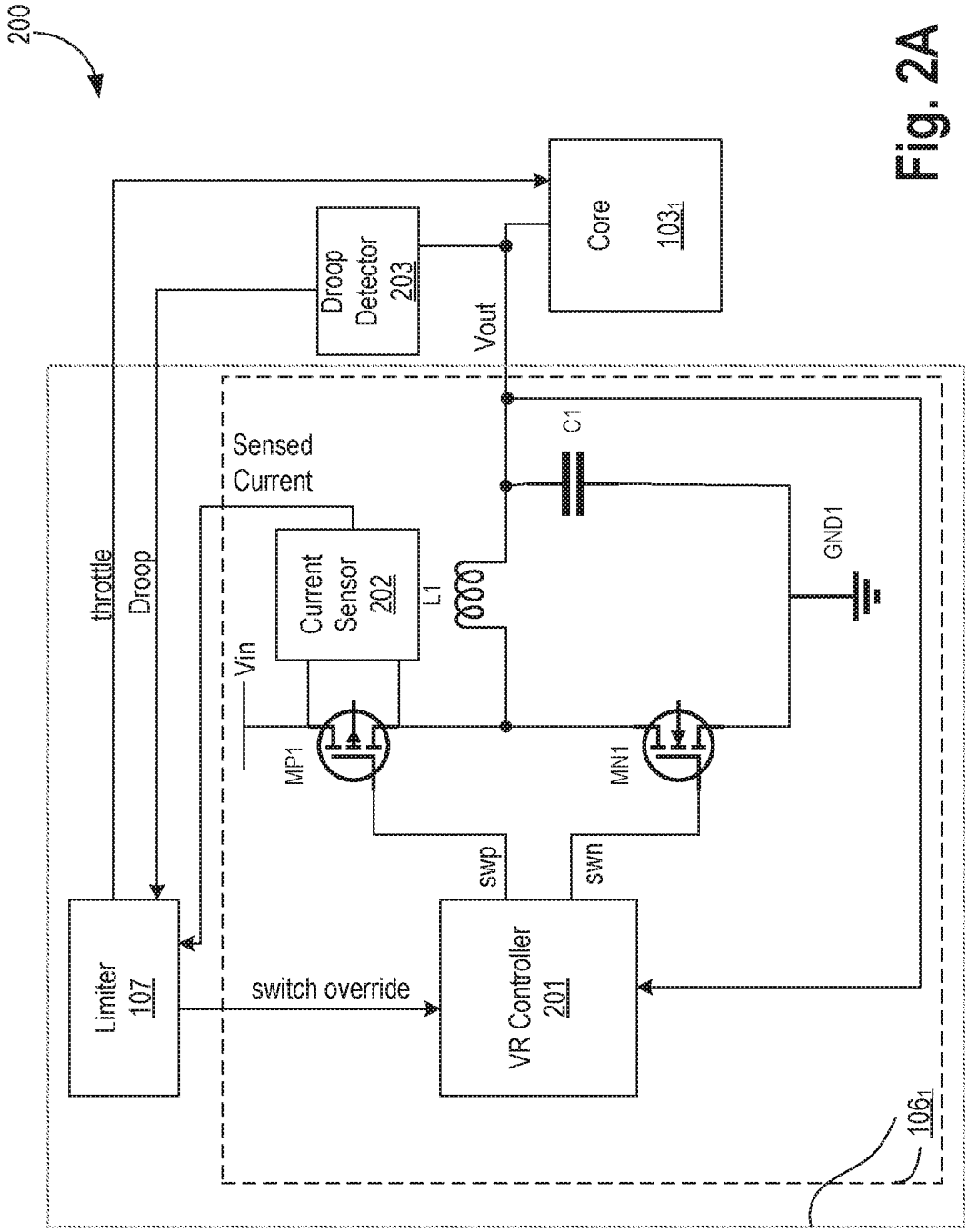

200
Core
103_1
Droop
Detector
203
Vout
C1
Sensed
Current
throttle
Droop
Current
Sensor
202
L1
GND1
Vin
MP1
MN1
swp
swn
Limiter
107
switch override
VR Controller
201
106_1

Fig. 2A

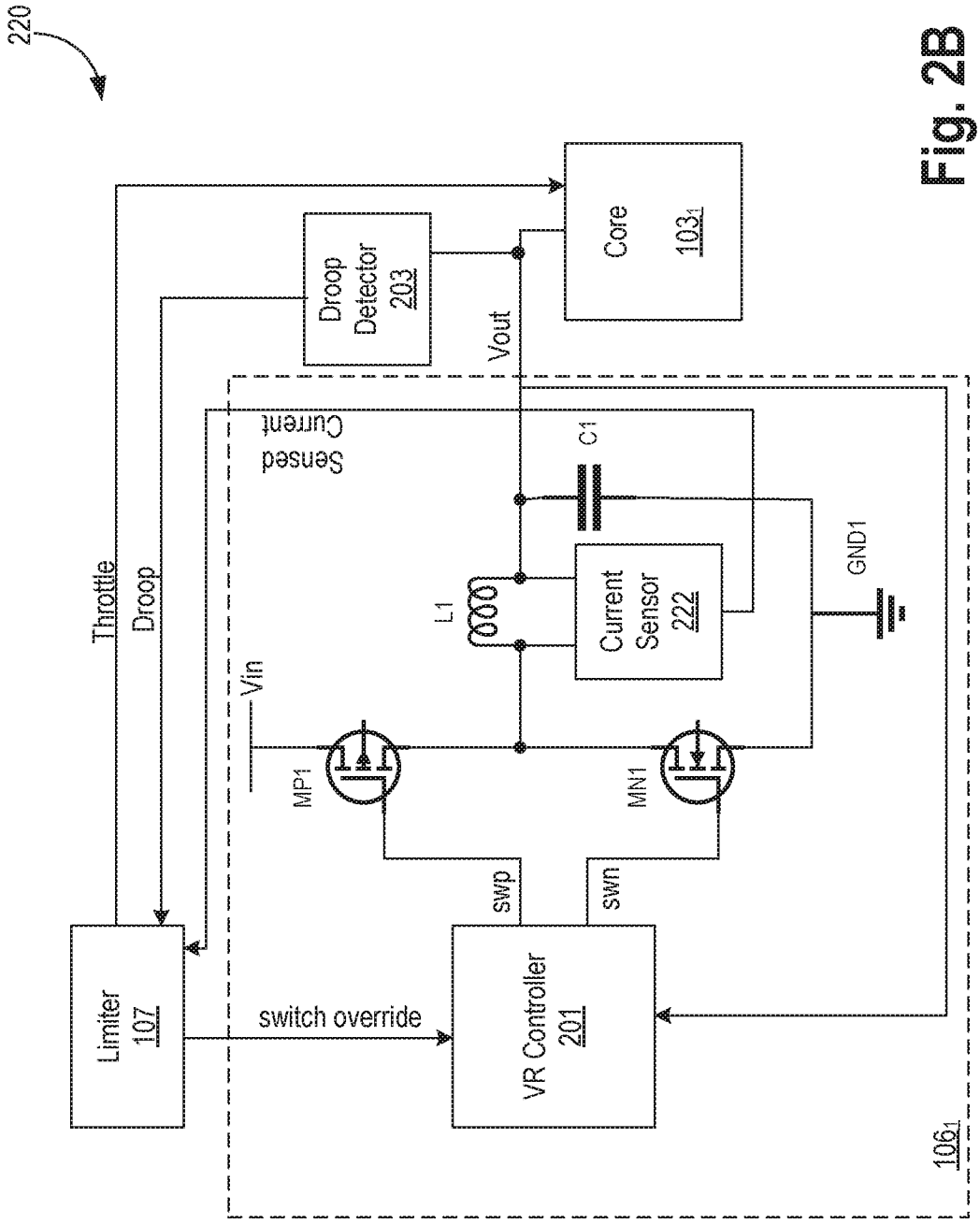

220
Core
103_1
Droop Detector
203
Vout
Sensed Current
C1
Throttle
Droop
L1
Current Sensor
222
GND1
Vin
MP1
MN1
swp
swn
Limiter
107
switch override
VR Controller
201
106_1

Fig. 2B

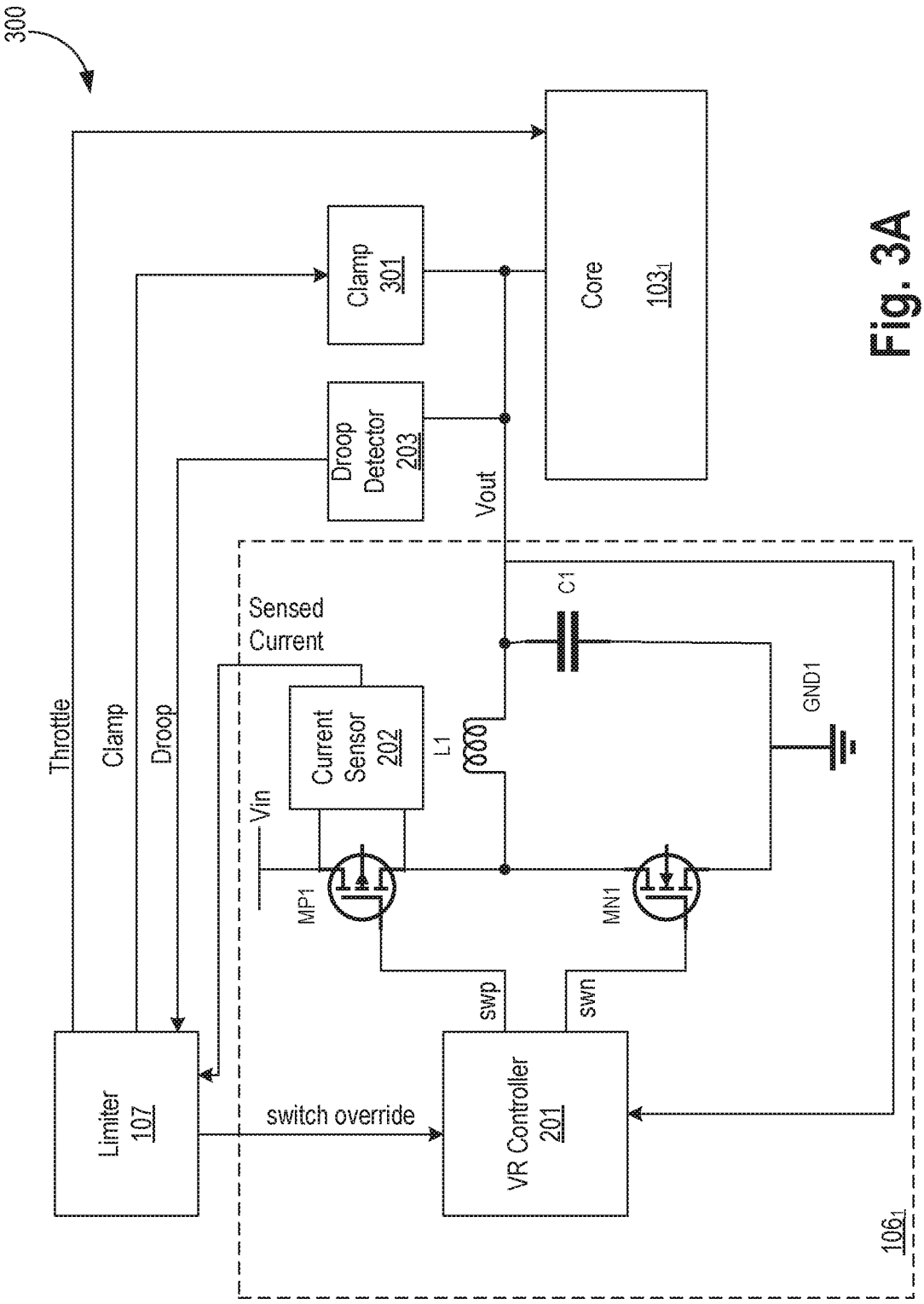

300
Core
103_1
Clamp
301
Droop
Detector
203
Vout
C1
Sensed
Current
Throttle
Clamp
Droop
Current
Sensor
202
L1
GND1
Vin
MP1
MN1
swp
swn
Limiter
107
switch override
VR Controller
201
106_1

Fig. 3A

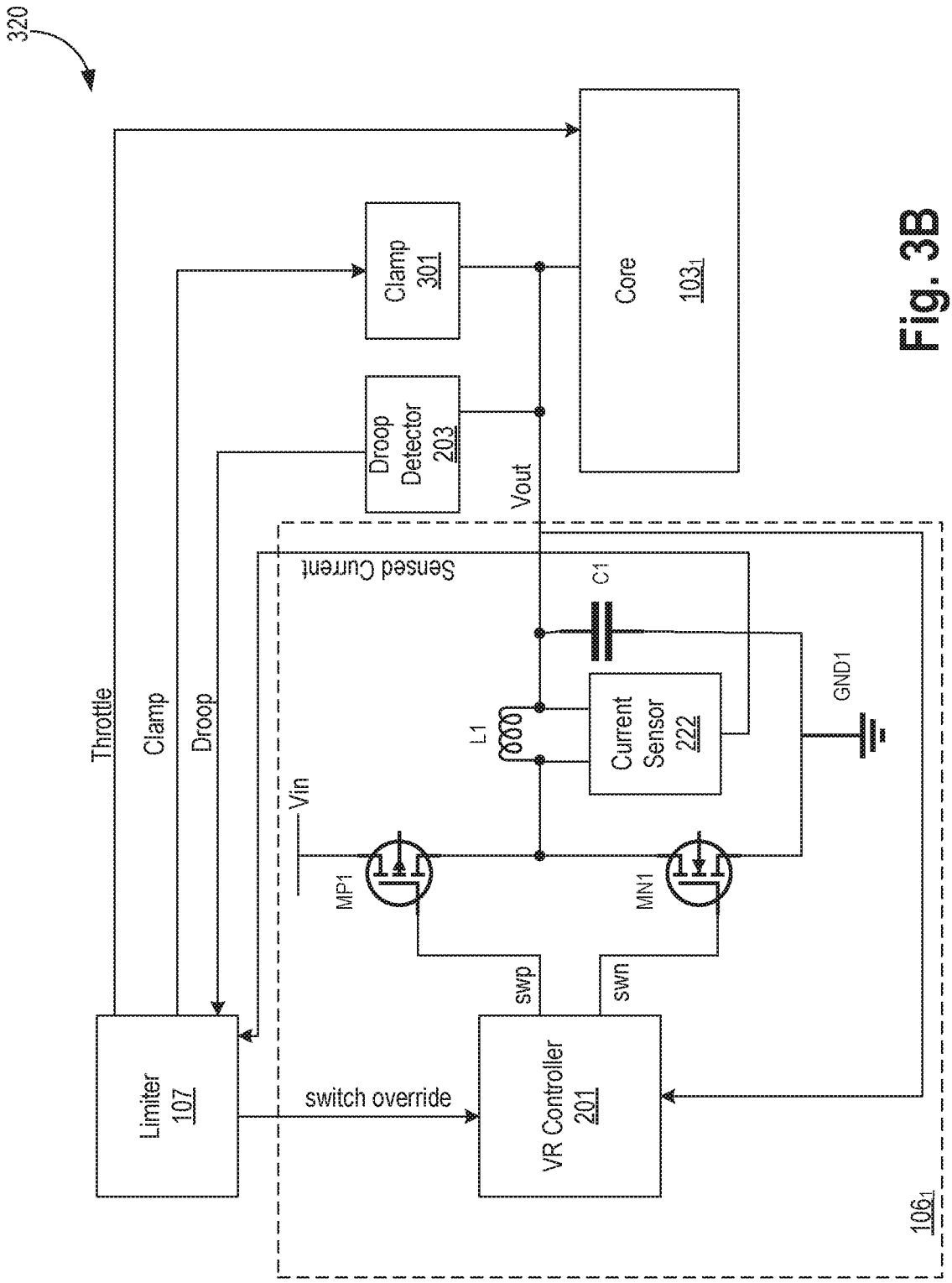

320
Core
103_1
Clamp
301
Droop
Detector
203
Vout
Sensed Current
C1
GND1
Throttle
Clamp
Droop
L1
Current
Sensor
222
Vin
MP1
MN1
swp
swn
Limiter
107
switch override
VR Controller
201
106_1

Fig. 3B

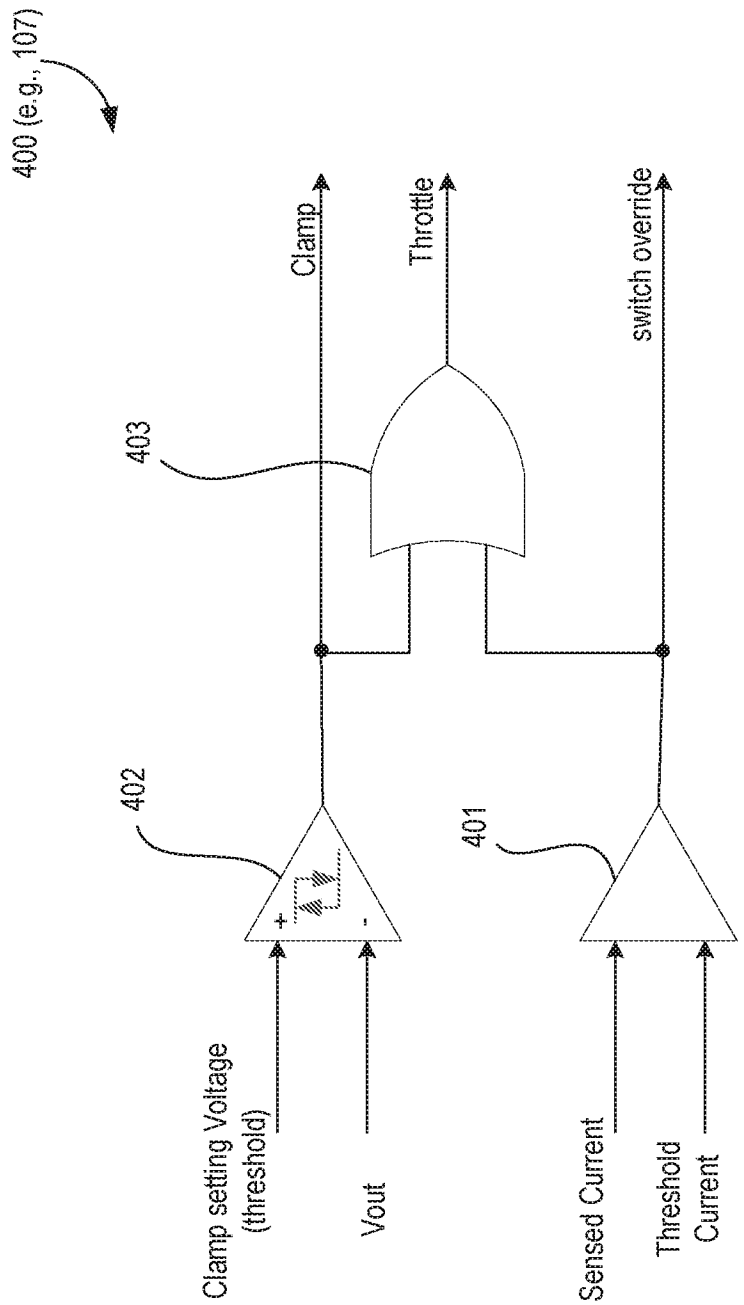

400 (e.g., 107)
Clamp
Throttle
switch override
403
402
401
+
-
Clamp setting Voltage (threshold)
Vout
Sensed Current
Threshold Current

Fig. 4

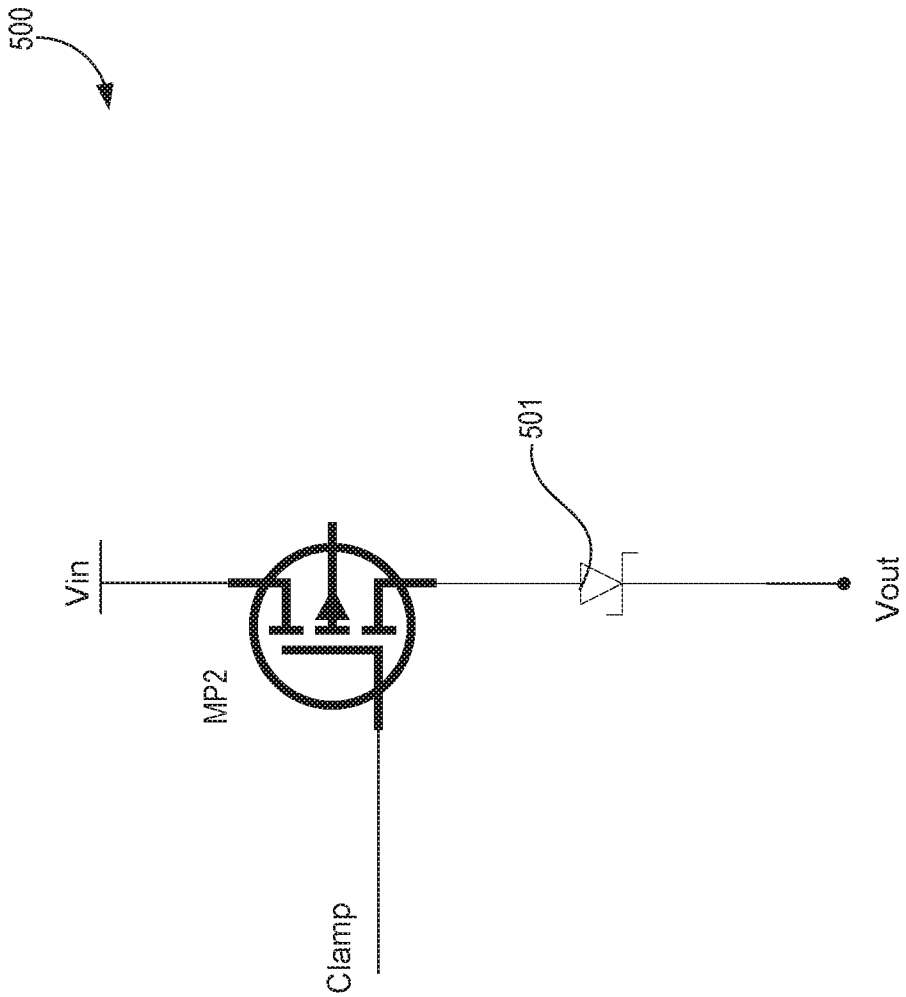


Fig. 5

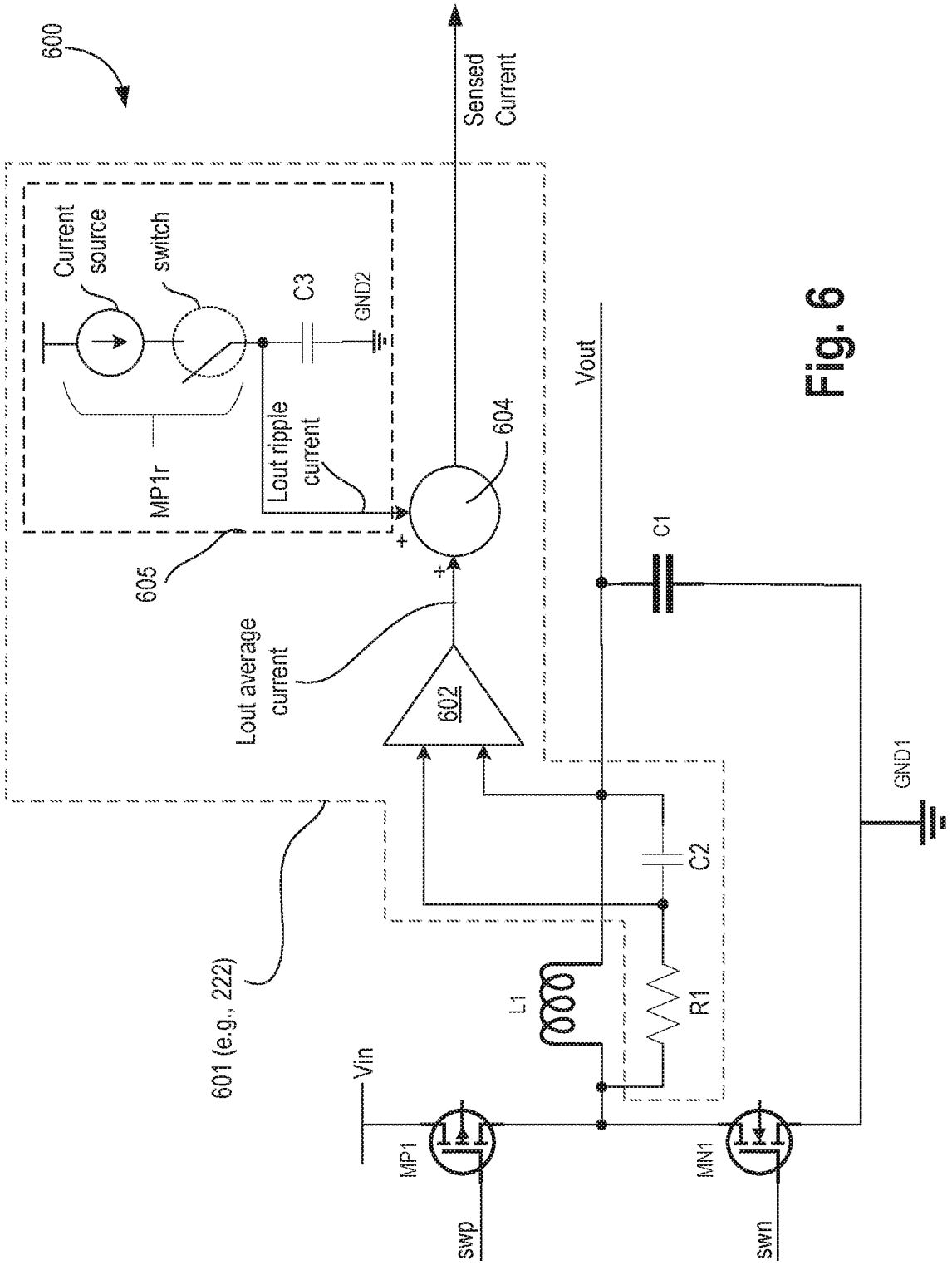

600
Sensed Current
Current source
switch
C3
GND2
MP1r
Lout ripple current
604
605
Vout
C1
Lout average current
602
GND1
C2
601 (e.g., 222)
L1
R1
Vin
MP1
MN1
swp
swn

Fig. 6

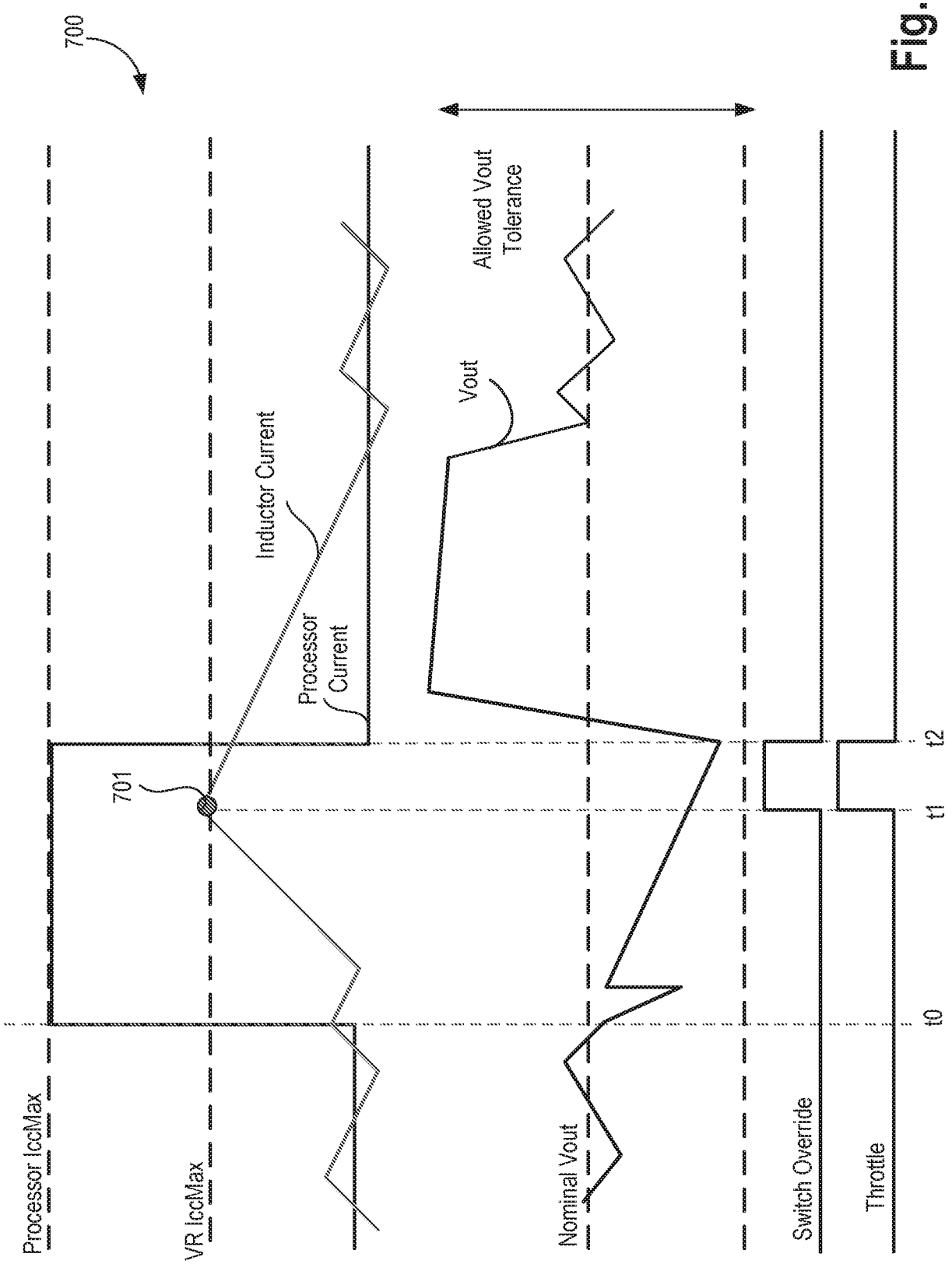

700
Processor IccMax
VR IccMax
701
Inductor Current
Processor Current
Vout
Allowed Vout Tolerance
Nominal Vout
Switch Override
Throttle
t0
t1
t2

Fig. 7

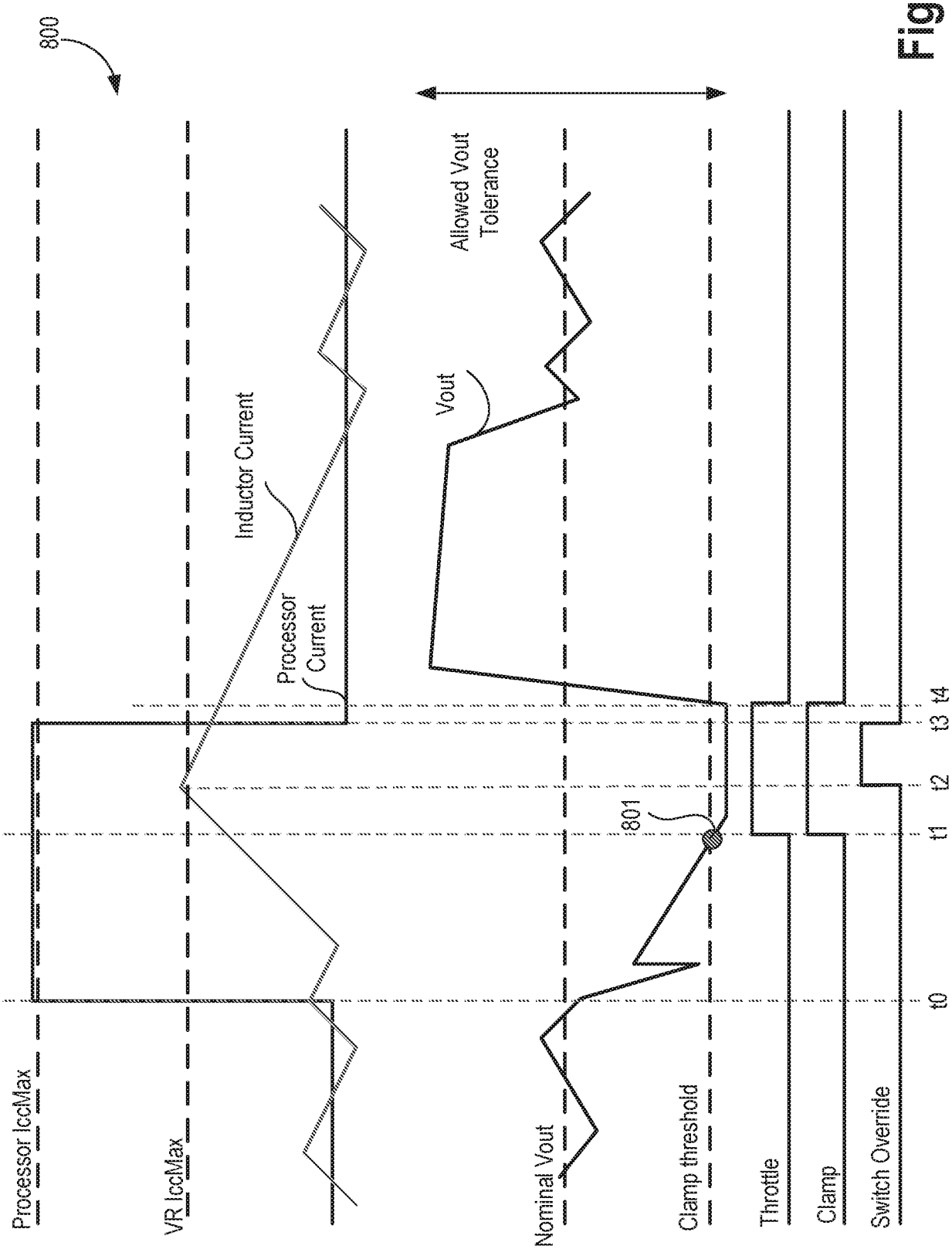

800
Processor IccMax
VR IccMax
Inductor Current
Processor Current
Vout
Allowed Vout Tolerance
Nominal Vout
Clamp threshold
801
Throttle
Clamp
Switch Override
t0
t1
t2
t3
t4

Fig. 8

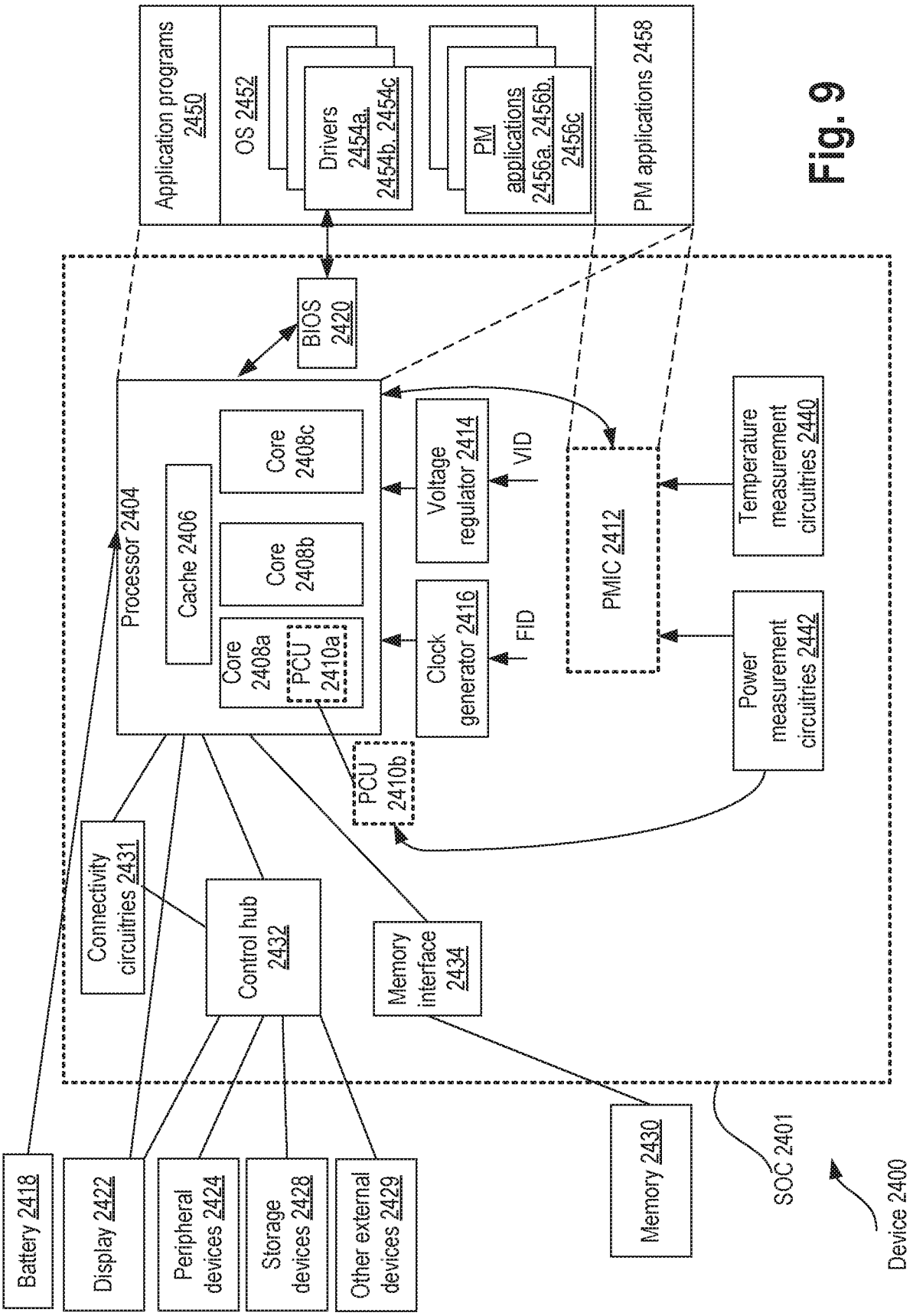

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Core 2408c
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Clock generator 2416
FID
PMIC 2412
Temperature measurement circuitries 2440
Power measurement circuitries 2442
Connectivity circuitries 2431
Control hub 2432
Memory interface 2434
Battery 2418
Display 2422
Peripheral devices 2424
Storage devices 2428
Other external devices 2429
Memory 2430
SOC 2401
Device 2400

Fig. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/057154

A. CLASSIFICATION OF SUBJECT MATTER

G06F 1/32(2006.01)i, H02M 3/158(2006.01)i, G06F 1/20(2006.01)i, H02M 1/08(2006.01)i, H02M 1/00(2007.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 1/32; G06F 1/28; G06F 1/3206; H02H 5/04; H02J 9/06; H02M 1/08; H02M 1/32; H02M 1/36; H02M 3/04; H02M 3/158; H02M 3/335; G06F 1/20; H02M 1/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: power supply generator, processor, current, voltage, monitor, threshold, turn off, DC-DC converter

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015-0146328 A1 (DENSO CORPORATION) 28 May 2015 See paragraphs [0010], [0031]-[0032], [0036], [0039], [0044]-[0045], [0089]; claims 1, 3; and figures 1, 14.	1-9,21-25
Y		10-20
Y	US 2015-0244207 A1 (KABUSHIKI KAISHA TOSHIBA) 27 August 2015 See paragraphs [0045]-[0046]; and figures 1, 6.	10-20
A	US 2017-0126140 A1 (INFINEON TECHNOLOGIES AUSTRIA AG) 04 May 2017 See paragraphs [0024]-[0030]; and figures 1-3.	1-25
A	US 2017-0329383 A1 (DELL PRODUCTS, L.P.) 16 November 2017 See paragraphs [0055]-[0066]; and figures 6-11.	1-25
A	KR 10-2010-0098826 A (LG ELECTRONICS INC.) 10 September 2010 See paragraphs [0031]-[0045]; and figures 1-3.	1-25
PX	US 2019-0146569 A1 (INTEL CORPORATION) 16 May 2019 See claims 1-20. * Note: The above document is a publication of the earlier application whose priority has been claimed in this international application.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 February 2020 (11.02.2020)	**11 February 2020 (11.02.2020)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
BYUN, Sung Cheal
Telephone No. +82-42-481-8262

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2019/057154

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