(51) **International Patent Classification:**
G11C 11/413 (2006.01)   G11C 7/20 (2006.01)
G11C 11/4193 (2006.01)

(21) **International Application Number:**
PCT/CA2008/001623

(22) **International Filing Date:**
15 September 2008 (15.09.2008)

(25) **Filing Language:** English

(26) **Publication Language:** English

(30) **Priority Data:**
61/015,724   21 December 2007 (21.12.2007)   US
61/048,737   29 April 2008 (29.04.2008)   US

(71) **Applicant** *(for all designated States except US)*: **MOSAID TECHNOLOGIES INCORPORATED** [CA/CA]; 11 Hines Road, Suite 203, Ottawa, Ontario K2K 2X1 (CA).

(72) **Inventor; and**
(75) **Inventor/Applicant** *(for US only)*: **OH, HakJune** [CA/CA]; 21 Cambior Crescent, Kanata, Ontario K2T 1J3 (CA).

(74) **Agent: SMART & BIGGAR**; 1000 De La Gauchetière Street West, Suite 3300, Montreal, Quebec H3B 4W5 (CA).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
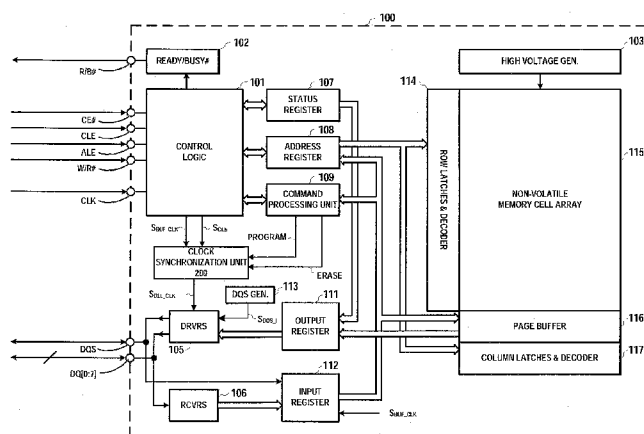
Declarations under Rule 4.17:
— as to the identity of the inventor (Rule 4.17(i))
— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:
— with international search report
— with amended claims

(54) Title: NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE WITH POWER SAVING FEATURE

Fig. 2

(57) **Abstract:** A non-volatile semiconductor memory device, which comprises (i) an interface having an input for receiving an input clock and a set of data lines for receiving commands issued by a controller including an erase command; (ii) a module having circuit components in a feedback loop configuration and being driven by a reference clock; (iii) a clock control circuit capable of controllably switching between a first state in which the reference clock tracks the input clock and a second state in which the reference clock is decoupled from the input clock; and (iv) a command processing unit configured to recognize the commands and to cause the clock control circuit to switch from the first state to the second state in response to recognizing the erase command. The module consumes less power when the reference clock is decoupled from the input clock than when the reference clock tracks the input clock.

NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE WITH POWER SAVING FEATURE

5   ## CROSS-REFERENCE TO RELATED APPLICATION

The present application claims the benefit under 35 U.S.C. 119(e) of United States Provisional Patent Application Serial No. 61/015,724, filed on December 21,
10 2007, hereby incorporated by reference herein.

The present application also claims the benefit under 35 U.S.C. 119(e) of United States Provisional Patent Application Serial No. 61/048,737, filed on April 29,
15 2008, hereby incorporated by reference herein.

BACKGROUND

20 Non-volatile memory is used for various purposes mainly related to persistent data storage with possibility of modification. Practical applications of non-volatile re-writable memory include storage of digital pictures, computer files, digitally recorded music and so on.
25 Thus, it is common to find non-volatile re-writable memory devices in everyday electronics such as computers, digital cameras, MP3 players, answering machines, cell phones, etc.

30 There are many ways in which data can be physically stored by a non-volatile memory device that also allows re-writing. One example is by using a magnetic disk as can be found in many computer hard drives. Another example is by way of an optical disk such as a CD-R/W.

Yet another example is by means of a solid state memory circuit such as an electrically erasable and programmable read-only memory (EEPROM), a specific example of which is a flash memory device. A flash memory device utilizes a

5   high voltage to erase a large block of non-volatile memory cells in one operation, allowing these cells to then be reprogrammed with new data. By virtue of their robustness, convenience and low cost, flash memory devices have gained immense popularity in the marketplace

10   for non-volatile memory and are expected to become even more dominant as the demand for non-volatile memory continues to grow unabated.

In the years since flash memory was first introduced,

15   technological refinements have been made in order to allow flash memory devices to be operated at increasingly higher speeds. This has further expanded the breadth of consumer applications such as, for example, certain video and photo related applications, in which flash memory

20   devices can be used. However, faster operation of a flash memory device can also lead to specific problems when attempting to create a large high-speed memory store from multiple devices. In particular, the electrical power consumption of flash memory, which increases with

25   operating frequency, can significantly limit the overall capacity of the memory store being created.

Against this background, there is clearly a need for a non-volatile semiconductor memory device with reduced

30   power consumption.

SUMMARY

A first aspect of the present invention seeks to provide a non-volatile semiconductor memory device, which comprises (i) an interface having an input port for receiving an input clock signal and a set of data lines

5   for receiving commands, including an erase command, the commands issued by a controller; (ii) a module having circuit components in a feedback loop configuration, the module being driven by a reference clock signal; (iii) a clock control circuit capable of controllably switching

10   between a first operational state in which the reference clock signal tracks the input clock signal and a second operational state in which the reference clock signal is decoupled from the input clock signal; and (iv) a command processing unit configured to recognize the commands

15   issued by the controller and to cause the clock control circuit to switch from the operational state to the second operational state in response to recognizing the erase command.   When the reference clock signal tracks the input clock signal, the module consumes a first

20   amount of power and wherein when the reference clock signal is decoupled from the input clock signal, the module consumes a second amount of power that is less than the first amount of power.

25   A second aspect of the present invention seeks to provide a non-volatile semiconductor memory device, which comprises first means for providing an input clock signal; second means having circuit components in a feedback loop configuration and being driven by a

30   reference clock signal; third means for controllably switching between a first operational state in which the reference clock signal tracks the input clock signal and a second operational state in which the reference clock signal is decoupled from the input clock signal; and

fourth means for recognizing commands issued by a controller, including an erase command, and varying the operational state of the third means in response to recognizing the erase command. When the reference clock signal tracks the input clock signal, the second means consumes a first amount of power and wherein when the reference clock signal is decoupled from the input clock signal, the second means consumes a second amount of power that is less than the first amount of power.

A third aspect of the present invention seeks to provide a method implemented by a non-volatile semiconductor memory device. The method comprises providing an input clock signal; providing a module with circuit components in a feedback loop configuration and being driven by a reference clock signal; producing the reference clock signal such that it follows the input clock signal in a first operational state of the device and such that it is decoupled from the input clock signal in a second operational state of the device, wherein when the reference clock signal follows the input clock signal, the module consumes a first amount of power and wherein when the reference clock signal is decoupled from the input clock signal, the module consumes a second amount of power that is less than the first amount of power ; and causing the device to switch from the first operational state to the second operational state in response to recognizing an erase command received from a controller.

A fourth aspect of the present invention seeks to provide a system, which comprises a controller configured to issue a master clock signal and to issue commands including an erase command; and a non-volatile

semiconductor   memory   device.   The   non-volatile
semiconductor memory device comprises (i) an interface
with an input port for receiving an input clock signal
related to the master clock signal and a set of data
5   lines   for   receiving   the   commands   issued   by   the
controller; (ii) a module having circuit components in a
feedback loop configuration, the module being driven by a
reference clock signal; (iii) a clock control circuit
capable   of   controllably   switching   between   a   first
10   operational state in which the reference clock signal
tracks the input clock signal and a second operational
state in which the reference clock signal is decoupled
from   the   input   clock   signal;   and   (iv)   a   command
processing unit configured to recognize the commands
15   issued by the controller and to cause the clock control
circuit to switch from the first operational state to the
second operational state in response to recognizing the
erase command.   When the reference clock signal tracks
the input clock signal, the module consumes a first
20   amount of power and wherein when the reference clock
signal is decoupled from the input clock signal, the
module consumes a second amount of power that is less
than the first amount of power.

25   A fifth aspect of the present invention seeks to provide
a computer-readable storage medium comprising computer-
readable instructions which, when processed, are used to
provide a non-volatile semiconductor memory device with
functionality for: producing a reference clock signal
30   such that it follows an input clock signal in a first
operational state of the device and such that it is
decoupled from the input clock signal in a second
operational state of the device, wherein when the
reference clock signal follows the input clock signal, a

first amount of power is consumed by a module with circuit components in a feedback loop configuration that is driven by the reference clock signal, and wherein when the reference clock signal is decoupled from the input clock signal, the module consumes a second amount of power that is less than the first amount of power; and causing the device to switch from the first operational state to the second operational state in response to recognizing an erase command received from a controller.

Thus, an improved non-volatile semiconductor memory device has been provided.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a memory system comprising a controller and a non-volatile memory device, in accordance with a non-limiting example embodiment.

Fig. 2 is a block diagram of the non-volatile memory device in Fig. 1 which includes a clock synchronization unit, in accordance with a non-limiting example embodiment.

Fig. 3A is a block diagram of the clock synchronization unit in Fig. 2, in accordance with a non-limiting example embodiment.

Fig. 3B is a block diagram of the clock synchronization unit in Fig. 2, in accordance with an alternative example embodiment.

Fig. 4A is a timing diagram that shows signal transitions
of various signals associated with the clock
synchronization unit of Fig. 3A.

5   Fig. 4B is a timing diagram that shows signal transitions
of various signals associated with the clock
synchronization unit of Fig. 3B.

10   **DETAILED DESCRIPTION**

Reference is made to Fig. 1, which illustrates a memory
system **80** in accordance with an example embodiment. The
memory system **80** comprises a controller **90**
15   communicatively coupled to a non-volatile memory device
100. The controller **90** may also be communicatively
coupled to other memory devices **100$_A$**.

The controller **90** comprises a set of ports **92A...92H**, which
20   are respectively connected to a set of ports **93A...93H** of
the non-volatile memory device **100**. The controller **90**
and the non-volatile memory device **100** exchange device-
external electrical signals **94A...94H** via their respective
sets of ports, **92A...92H** and **93A...93H**. The ports **93A...93H** of
25   the non-volatile memory device **100** and the device-
external signals **94A...94H** will be described in greater
detail subsequently herein.

Fig. 2 is a block diagram of the non-volatile memory
30   device **100** in accordance with an example embodiment.
Within the non-volatile memory device **100,** a non-volatile
memory cell array **115** includes a plurality of non-
volatile memory cells arranged in rows and columns. Each
non-volatile memory cell includes a floating-gate field-

effect transistor capable of holding a charge for the non-volatile storage of data. The non-volatile memory cells in the non-volatile memory cell array **115** can be electrically programmed by charging the floating gate.

The rows of the non-volatile memory cell array **115** can be arranged in blocks of pages. By way of non-limiting example, the rows of the non-volatile memory cell array **115** can be organized into 2048 blocks, with 64 pages per block.

The non-volatile memory device **100** comprises an interface that includes the aforementioned set of ports **93A..93H**. Among these, ports **93B**, **93C**, **93D**, **93E**, **93F** (also labeled CE#, CLE, ALE, W/R#, CLK, respectively) carry device-external signals from the controller **90** to the non-volatile memory device **100**. Ports **93A** (also labeled R/B#) carries device-external signals from the non-volatile memory device **100** to the controller **90**. Finally, ports **93G** and **93H** (also labeled DQS and DQ[0:7], respectively) are capable of carrying device-external signals in either direction depending on an operating mode of the non-volatile memory device **100**. More specifically, the ports of the non-volatile memory device **100** include, without limitation:

- a chip enable port (**93B**, also labeled CE#):

   The chip enable port CE# is an input port that allows the non-volatile memory device **100** to know whether or not it has been activated by the controller **90**. In the present non-limiting embodiment, when the device-external signal at the chip enable port CE# is de-asserted (LOW), this means that the non-volatile memory

device **100** has been selected, whereas when the device-external signal at the chip enable port CE# is asserted (HIGH), this means that the non-volatile memory device **100** has been de-selected.

- an input clock port (**93F**, also labeled CLK):

  The input clock port CLK is an input port that carries a clock signal (a system clock) used to synchronize operation of the non-volatile memory device **100**. Thus, it should be understood that by virtue of being synchronized to the system clock, the non-volatile memory device **100** differs from asynchronous or plesiochronous memory devices.

- a plurality of data lines (**93H**, also labeled DQ[0:7]):

  The data lines DQ[0:7] carry addresses, commands and write data from the controller **90**, as well as carry read data to the controller **90**. While in the illustrated embodiment there are eight (8) data lines, this should not be considered a limitation. For example, in other embodiments, a different number of data lines may be provided, such as sixteen (16). Still other possibilities exist.

- a command latch enable port (**93C**, also labeled CLE) and an address latch enable port (**93D**, also labeled ALE):

  The command latch enable port CLE and the address latch enable port ALE are input ports that carry device-external signals which parallel the device-external signals on the data lines DQ[0:7] and delineate the start and end of addresses, commands and/or write data.

- a data strobe port (**93G**, also labeled DQS):

     The data strobe port DQS carries a device-external

5   signal that indicates the presence of valid data on the
     data lines DQ[0:7]. When data is to be written to the
     non-volatile memory device **100** (in a non-limiting
     double data rate embodiment), the device-external
     signal at the data strobe port DQS is generated by the

10   controller **90**, has the same frequency as the device-
     external signal at the input clock port CLK, and is
     90°-shifted and center aligned with the device-external
     signal on the data lines DQ[0:7]. When data is being
     read from the non-volatile memory device **100** (in a non-

15   limiting double data rate embodiment), the device-
     external signal at the data strobe port DQS is
     generated by the non-volatile memory device **100**, has
     the same frequency as the device-external signal at the
     input clock port CLK, and is edge-aligned with the

20   device-external signal on the data lines DQ[0:7]. It
     should be appreciated that in the absence of valid data
     on the data lines DQ[0:7], the device-external signal
     at the data strobe port DQS can be made to not
     oscillate. As such, there will be periods when the

25   device-external signal at the data strobe port DQS
     oscillates and periods when it does not.

- a write/read port (**93E**, also labeled W/R#):

30   The write/read port W/R# is an input port that carries
     a device-external signal indicating whether the data
     lines DQ[0:7] carry write data from the controller **90**
     (i.e., when the device-external signal W/R# is HIGH) or

carry read data from the memory device **100** (i.e., when the device-external signal W/R# is LOW).

- a ready/busy port (**93A,** also labeled R/B#):

The ready/busy port R/B# is an output port that carries a device-external signal indicating whether the non-volatile memory device **100** is available to receive a command for accessing the memory cell array **115** (when the device-external signal is HIGH) or is busy processing a command for accessing the memory cell array **115** (when the device-external signal is LOW).

The controller **90** controls behavior of the non-volatile memory device **100** by varying the device-external signals at the various input ports and on the data lines. Accordingly, the non-volatile memory device **100** comprises control logic **101** that is configured to recognize when the input ports and data lines carry certain specific signals from the controller **90,** and to respond in a deterministic way based upon these signals.

For example, the control logic **101** is configured to recognize when the device-external signal at the command latch enable port CLE is HIGH and the device-external signal at the address latch enable port ALE is LOW. In this case, the control logic **101** considers that the information on the data lines DQ[0:7] is command information. Accordingly, the information on the data lines DQ[0:7] is received by an input receiver **106,** latched into an input register **112** on the rising edge of a buffered clock signal S_{BUF_CLK} (which is a buffered version of the device-external signal at the input clock port CLK and has the same polarity) and provided to a

command processing unit **109**. The command processing unit
109 may include a register into which the information is
loaded and a decoder for decoding the loaded information
into one or more commands. The command processing unit
5   **109** generates control signals, some of which are fed to
the control logic **101** and others of which are fed to the
clock synchronization unit **200,** as will be described in
further detail later on.

10 In some embodiments, the command processing unit **109** is
integrated with the control logic **101,** while in other
embodiments, the command processing **109** and the control
logic **101** may be distinct components of the memory device
100. In still other embodiments, portion of the command
15 processing unit **109** (such as a register) can be distinct
while the remainder of the command processing unit **109**
may be integrated with the control logic **101.**

There are several examples of commands that can be
20 processed by the non-volatile memory device **100,**
including BLOCK ERASE, PAGE PROGRAM, PAGE READ, STATUS
READ, to name a few non-limiting possibilities. Some of
these commands and their effects are described below by
way of non-limiting example.
25

A) BLOCK ERASE

When the control logic **101** recognizes a BLOCK ERASE
command (more precisely: an indicative first command
30   cycle of the BLOCK ERASE command), the control logic
101 is configured to subsequently expect to receive
address information on the data lines DQ[0:7]. Address
information is deemed to be present on the data lines
DQ[0:7] when the device-external signal at the command

latch enable port CLE is LOW and the device-external
signal at the address latch enable port ALE is HIGH.
Accordingly, the information on the data lines DQ[0:7]
is received by the input receiver **106**, latched into the
input register **112** on the rising edge of the
aforementioned buffered clock signal S_{BUF_CLK} and
transferred into an address register **108**. The address
information, which can span over multiple address
cycles, may include a plurality of bytes specifying the
address of a desired block to be erased. The address
information in its entirety can be loaded into a row
latches and decoder **114**.

The control logic **101** is configured to subsequently
expect to receive a second command cycle of the BLOCK
ERASE command on the data lines DQ[0:7]. Accordingly,
when the device-external signal at the command latch
enable port CLE is HIGH and the device-external signal
at the address latch enable port ALE is LOW, the
information on the data lines DQ[0:7] is received by
the input receiver **106**, latched into the input register
112 on the rising edge of the buffered clock signal
S_{BUF_CLK} and transferred to the command processing unit
109. The command processing unit **109** recognizes the
second command cycle of the BLOCK ERASE command.

The command processing unit **109** then asserts an ERASE
signal that is used by the clock synchronization unit
200 as will be described herein below. The control
logic **101** causes the device-external signal at the
ready/busy port R/B# to go LOW in order to indicate
that the non-volatile memory device 100 is busy. Also,
The control logic **101** then invokes a high voltage
generator **103** to apply high voltages in order to erase

the non-volatile memory cells that are within the desired block. This operation may take an extended period of time that, for current technology, is within the range of about 2 milliseconds to about 15 milliseconds, depending on a variety of factors.

After the non-volatile memory cells within desired block have been erased, the command processing unit **109** de-asserts the ERASE signal. Then, after a time interval needed by certain components of the clock synchronization unit 200 to re-acquire synchronization, the control logic **101** causes the device-external signal at the ready/busy port R/B# to go HIGH in order to indicate that the non-volatile memory device **100** is ready to receive another command.

B) PAGE PROGRAM

When the control logic **101** recognizes a PAGE PROGRAM command (more precisely: an indicative first command cycle of the PAGE PROGRAM command), the control logic **101** is configured to subsequently expect to receive address information on the data lines DQ[0:7]. Address information is deemed to be present on the data lines DQ[0:7] when the device-external signal at the command latch enable port CLE is LOW and the device-external signal at the address latch enable port ALE is HIGH. Accordingly, the information on the data lines DQ[0:7] is received by the input receiver **106**, latched into the input register **112** on the rising edge of the buffered clock signal S_{BUF_CLK} and transferred into the address register **108**. The address information, which can span over multiple address cycles, may include a plurality of bytes specifying a desired page to be programmed.

The address information can be loaded into the row
latches and decoder **114** and/or a column latches and
decoder **117**.

5   The control logic **101** then expects to receive write
data on the data lines DQ[0:7]. This occurs when the
device-external signals at both the command latch
enable port CLE and the address latch enable port ALE,
as well as the device-external signal at the write/read
10   port W/R#, are all HIGH. Additional use is made of the
device-external signal at the data strobe port DQS. In
this case, the write data being received by the input
receiver **106** is latched into the input register **112** at
both edges of the device-external signal at the data
15   strobe port DQS and is selected by the column latches
and decoder **117** to be loaded into a page buffer **116**.

When the device-external signals at the command latch
enable port CLE and the address latch enable port ALE
20   are no longer both HIGH, the non-volatile memory device
100 stops latching the write data, and thus the amount
of write data written to the non-volatile memory device
100 is determined by the length of time during which
the device-external signals at both the command latch
25   enable port CLE and the address latch enable port ALE
had remained HIGH. For example, if the device-external
signals at both the command latch enable port CLE and
the address latch enable port ALE had remained HIGH for
1024 clock cycles, the non-volatile memory device **100**
30   would have received 2048 bytes of write data (for an 8-
bit-wide data bus in a double data rate scenario).

The control logic **101** is configured to subsequently
expect to receive a second command cycle of the PAGE

PROGRAM command on the data lines DQ[0:7].
Accordingly, when the device-external signal at the
command latch enable port CLE is HIGH and the device-
external signal at the address latch enable port ALE is

5   LOW, the information on the data lines DQ[0:7] is
received by the input receiver **106,** latched into the
input register **112** on the rising edge of the buffered
clock signal S_{BUF_CLK} and transferred into the command
processing unit **109.** The command processing unit **109**

10   recognizes the second command cycle of the PAGE PROGRAM
command.

The command processing unit **109** then asserts a PROGRAM
signal that is used by the clock synchronization unit

15   200 as will be described herein below. In addition,
the control logic **101** causes the device-external signal
at the ready/busy port R/B# to go LOW in order to
indicate that the non-volatile memory device **100** is
busy. The control logic **101** then invokes the high

20   voltage generator **103** to apply high voltages in order
to transfer the write data in the page buffer **116** to
the desired page in the non-volatile memory cell array
115. This operation may take an extended period of
time that, for current technology, is within the range

25   of about 200 microseconds to about 2 milliseconds,
depending on a variety of factors.

After the non-volatile memory cells within the desired
page have been programmed, the command processing unit

30   **109** de-asserts the PROGRAM signal. Then, after a time
interval needed by certain components of the clock
synchronization unit 200 to re-acquire synchronization,
the control logic **101** causes the device-external signal
at the ready/busy port R/B# to go HIGH in order to

indicate that the non-volatile memory device **100** is
ready to receive another command.

C) PAGE READ

5

When the control logic **101** recognizes a PAGE READ
command (more precisely: an indicative first command
cycle of the PAGE READ command), the control logic **101**
is configured to subsequently expect to receive address

10   information on the data lines DQ[0:7]. Address
information is deemed to be present on the data lines
DQ[0:7] when the device-external signal at the command
latch enable port CLE is LOW and the device-external
signal at the address latch enable port ALE is HIGH.

15   Accordingly, the information on the data lines DQ[0:7]
is received by the input receiver **106,** latched into the
input register **112** on the rising edge of the buffered
clock signal S_{BUF_CLK} and transferred into the address
register **108.** The address information, which can span

20   over multiple address cycles, may include a plurality
of bytes specifying a desired page to be read. The
address information can be loaded into the row latches
and decoder **114** and/or the column latches and decoder
117.

25

The control logic **101** is configured to subsequently
expect to receive a second command cycle of the PAGE
READ command on the data lines DQ[0:7]. Accordingly,
when the device-external signal at the command latch

30   enable port CLE is HIGH and the device-external signal
at the address latch enable port ALE is LOW, the
information on the data lines DQ[0:7] is received by
the input receiver **106,** latched into the input register
112 on the rising edge of the buffered clock signal

S_{BUF_CLK} and transferred into the command processing unit **109**. The command processing unit **109** recognizes the second command cycle of the PAGE READ command.

5   In addition, the control logic **101** causes the device-external signal at the ready/busy port R/B# to go LOW in order to indicate that the non-volatile memory device **100** is busy. The control logic **101** then invokes the high voltage generator **103** to apply high voltages

10   in order to transfer the cell data in the desired page in the non-volatile memory cell array **115** to the page buffer **116**. This operation may take an extended period of time that, for current technology, is within the range of about 20 microseconds to about 60

15   microseconds, depending on a variety of factors.

After the contents of the desired page have been transferred to the page buffer **116**, the control logic **101** causes the device-external signal at the ready/busy

20   port R/B# to go HIGH in order to indicate that the non-volatile memory device **100** is ready to output the read data in the page buffer **116** or to receive another command.

25   The control logic **101** then expects to output read data onto the data lines DQ[0:7]. For this to happen, the device-external signals on both the command latch enable port CLE and the address latch enable port ALE have to be HIGH and the device-external signal at the

30   write/read port W/R# has to be LOW. Then, the data in the page buffer **116** is output to the data lines DQ[0:7] through an output register **111** and an output driver **105**. This is carried out in a synchronous manner. Specifically, the data from the page buffer **116** is

selected by the column latches and decoder **117** to be
loaded to the output register **111**. The output driver
105 thus sequentially receives the read data from the
output register **111**. The output driver **105** outputs the
5   read data received from the output register **111** onto
the data lines DQ[0:7] and references the read data to
rising and falling edges of a synchronizing clock
signal S_{DLL_CLK} received from the clock synchronization
unit **200** to be described later on in greater detail.

10

Meanwhile, the output driver **105** receives an internally
generated data strobe signal S_{DQS_I} that is produced by
a data strobe signal generator **113**. The internally
generated data strobe signal S_{DQS_I} is HIGH when there
15   is read data to be placed on the data lines DQ[0:7] and
is LOW otherwise. The output driver **105** transfers the
internally generated data strobe signal S_{DQS_I} onto the
data strobe port DQS but synchronizes it with the
rising and falling edges of the aforementioned
20   synchronizing clock signal S_{DLL_CLK}. The device-external
signal at the data strobe port DQS is used by the
controller **90** for latching data on the data lines
DQ[0:7] during read operations.

25   When the device-external signals at the command latch
enable port CLE and the address latch enable port ALE
are no longer both HIGH, the non-volatile memory device
100 stops outputting the read data, and thus the amount
of read data read from the non-volatile memory device
30   **100** is determined by the length of time during which
the device-external signals on both the command latch
enable port CLE and the address latch enable port ALE
had remained HIGH. For example, if the device-external
signals at the command latch enable port CLE and the

address latch enable port ALE had remained HIGH for
1024 clock cycles, the non-volatile memory device **100**
would have output 2048 bytes of read data (for an 8-
bit-wide data bus in a double data rate scenario).

5

D) STATUS READ

When the control logic **101** recognizes a STATUS READ
command, the control logic **101** is configured to expect
10   that it will subsequently need to output status
information on the data lines DQ[0:7]. For this to
take place, the device-external signals at both the
command latch enable port CLE and the address latch
enable port ALE have to be HIGH and the device-external
15   signal at the write/read port W/R# has to be LOW. In
this case, the contents of a status register **107** is
output to the data lines DQ[0:7] through the output
register **111** and the output driver **105**. This status
read operation is also done in synchronous manner with
20   DQS signal.

Thus, it will be apparent that the ERASE or PROGRAM
signal is asserted and de-asserted by the command
processing unit **109** based on commands that are received
25 from the controller **90**. Specifically, the command
processing unit **109** asserts the ERASE signal in response
to receipt of the BLOCK ERASE command. The command
processing unit **109** asserts the PROGRAM signal in
response to receipt of the PAGE PROGRAM command.
30

It should be appreciated that the non-volatile memory
device **100** may comprise other ports and be configured to
generate or receive other device-external signals. For
example, there could be provided a write protect port

that provides hardware protection against unwanted
programming or erasure operations. Thus, when the
device-external signal at the write protect port is
detected as being LOW, the non-volatile memory device **100**
5   can be configured to not accept the aforementioned PAGE
PROGRAM or BLOCK ERASE commands.

Also, the non-volatile memory device **100** comprises
ready/busy indicator logic **102**, which is coupled to the
10   control logic **101** and indicates whether the non-volatile
memory device **100** is busy.

One non-limiting example embodiment of the clock
synchronization unit **200** is now described with reference
15   to Fig. 3A. The clock synchronization unit **200** comprises
a clock control circuit **210** that derives a reference
clock signal S_{REF_CLK} from the aforementioned buffered clock
signal S_{BUF_CLK} and the aforementioned ERASE or PROGRAM
signal. The clock control circuit **210** feeds the
20   reference clock signal S_{REF_CLK} to a delay locked loop (DLL)
220, which produces the synchronizing clock signal S_{DLL_CLK}.

To generate the reference clock signal S_{REF_CLK}, the clock
control circuit **210** controllably switches between a first
25   operational state in which the reference clock signal
S_{REF_CLK} tracks the buffered clock signal S_{BUF_CLK} and a
second operational state in which the reference clock
signal S_{REF_CLK} is decoupled from the buffered clock signal
S_{BUF_CLK}. The ERASE or PROGRAM signal plays a role in
30   whether the reference clock signal S_{REF_CLK} tracks the
buffered clock signal S_{BUF_CLK} or is decoupled therefrom.
Specifically, and in accordance with a non-limiting
example embodiment, the clock control circuit 210 is
designed to enter into/remain in the first operational

state (i.e., in which the reference clock signal S_{REF_CLK}
tracks the buffered clock signal S_{BUF_CLK}) when neither the
ERASE signal nor the PROGRAM signal is asserted by the
command processing unit **109**.   Conversely, the clock

5 control circuit **210** is designed to enter into/remain in
the second operational state (i.e., in which the
reference clock signal S_{REF_CLK} is decoupled from the
buffered clock signal S_{BUF_CLK}) when at least one of the
ERASE and PROGRAM signals is asserted by the command

10 processing unit **109**.

Accordingly, in a specific non-limiting embodiment, the
clock control circuit **210** can be designed to include an
AND logic gate **211** and a NOR logic gate **213**.   The NOR

15 logic gate **213** is fed by the ERASE and PROGRAM signals
from the command processing unit **109**.   A first input of
the AND logic gate **211** is the buffered clock signal
S_{BUF_CLK}.   A second input of the AND logic gate **211** is a
signal S_{DLL_EN2} that is an output of the NOR logic gate **213**.

20 Thus, when the ERASE or PROGRAM signal is asserted, the
NOR logic gate **213** causes the signal S_{DLL_EN2} to go LOW,
which disables the AND logic gate **211** and causes its
output signal (i.e., the reference clock signal S_{REF_CLK}) to
go LOW.   This decouples the reference clock signal S_{REF_CLK}

25 from the buffered clock signal S_{BUF_CLK}.   On the other hand,
when the ERASE and PROGRAM signals are de-asserted, the
NOR logic gate **213** causes the signal S_{DLL_EN2} to go HIGH,
which enables the AND logic gate **211** and causes the
reference clock signal S_{REF_CLK} to track the buffered clock

30 signal S_{BUF_CLK} while it is provided to the DLL **220**.

In one alternative embodiment, the AND logic gate **211** can
be a 3-input AND logic gate, with the third input being a
signal S_{DLL_EN1}, which is at the output of an inverter logic

gate **212** fed by a buffered chip enable signal S_{CEb}. The buffered chip enable signal S_{CEb} is a buffered version of the device-external signal at the chip enable port CE# and has the same polarity. This modification of the clock control circuit **210** would cause the AND logic gate **211** to operate as described earlier whenever the buffered chip enable signal S_{CEb} goes LOW (i.e., whenever the non-volatile memory device **100** is selected), but would result in the output of the AND logic gate **211** going LOW whenever the buffered chip enable signal S_{CEb} goes HIGH (i.e., whenever the non-volatile memory device **100** is de-selected), irrespective of whether the ERASE or PROGRAM signal is asserted or not.

In another alternative embodiment, the functionality of the NOR logic gate **213** is implemented elsewhere than in the clock control circuit **210**. For example, the functionality of the NOR logic gate **213** could be implemented in the command processing unit **109**. As such, the command processing unit **109** may itself issue the signal S_{DLL_EN2} that is currently illustrated as being at the output of the NOR logic gate **213**.

The DLL **220** includes circuit components in a feedback loop configuration to produce the synchronizing clock signal S_{DLL_CLK} with a controllable delay relative to the reference clock signal S_{REF_CLK}. The controllable delay can be adjusted as needed to ensure that the output driver **105**, which receives the synchronizing clock signal S_{DLL_CLK}, outputs the device-external signals on the data lines DQ[0:7] and at the data strobe port DQS to meet desired timing specifications for the non-volatile memory device **100**. To achieve the requisite delay, the DLL **220** can be implemented as a conventional DLL that includes a

variable delay line **221**. The variable delay line **221** varies a delay of the synchronizing clock signal S_{DLL_CLK} relative to the reference clock signal S_{REF_CLK} in response to a delay adjustment signal S_{SHIFT}.

A feedback delay model **224** generates a feedback clock signal S_{FB_CLK} in response to the synchronizing clock signal S_{DLL_CLK}. The feedback delay model **224** may have a replica delay model which compensates for internal delays caused by some internal circuit blocks such as:

- the AND logic gate **211** in the clock control circuit **210**;
- an input buffer (not shown) that outputs the buffered clock signal S_{BUF_CLK} from the device-external signal at the input clock port CLK; and/or
- output buffers for the device-external signals on the data lines DQ[0:7] and at the data strobe port DQS.

The DLL **220** further includes a phase detector **222** that receives the feedback clock signal S_{FB_CLK} and the reference clock signal S_{REF_CLK}, and generates a phase error signal S_{PE} having a value indicating the phase difference between the reference clock signal S_{REF_CLK} the and feedback clock signal S_{FB_CLK}. A delay control **223** generates the delay adjustment signal S_{SHIFT} in response to the phase error signal S_{PE} from the phase detector **222**, and applies the delay adjustment signal S_{SHIFT} to the variable delay line **221** to adjust the delay applied by the variable delay line **221**.

The phase detector **222** and the delay control **223** operate in combination to adjust the delay applied by the

variable delay line **221** as a function of the detected phase difference between the reference clock signal S_{REF_CLK} and the feedback clock signal S_{FB_CLK}. Specifically, the phase detector **222** and the delay control **223** operate in combination to adjust the variable delay of the synchronizing clock signal S_{DLL_CLK} until the phase difference between the reference clock signal S_{REF_CLK} and feedback clock signal S_{FB_CLK} is approximately zero. More specifically, as the delay of the synchronizing clock signal S_{DLL_CLK} is adjusted, the phase of the feedback clock signal S_{FB_CLK} from the feedback delay model **224** is adjusted accordingly until the feedback clock signal S_{FB_CLK} has approximately the same phase as the reference clock signal S_{REF_CLK}. When the DLL **220** has adjusted the variable delay to a value causing the phase shift between the reference clock signal S_{REF_CLK} and the feedback clock signal S_{FB_CLK} to equal approximately zero, the DLL **220** is said to be "locked". At this point, the device-external signal at the input clock port CLK and the synchronizing clock signal S_{DLL_CLK} will be synchronized provided that the feedback delay model **224** accurately models the various internal delays.

Considering that the variable delay line **221** in the DLL **220** may contain a large number of delay stages, all of which are switched as an oscillating clock signal propagates through the variable delay line **221**, it is clear that a power savings will arise during times when the DLL **220** is not fed with an oscillating clock signal. This, in turn, occurs when the reference clock signal S_{REF_CLK} is decoupled from the buffered clock signal S_{BUF_CLK}, which is a direct consequence of asserting the ERASE or PROGRAM signal as described earlier. Overall, it will therefore be observed that the average number of signal

transitions per second that are effected by the DLL **220** will be less when the reference clock signal S_{REF_CLK} is decoupled from the buffered clock signal S_{BUF_CLK} than when the reference clock signal S_{REF_CLK} tracks the buffered

5   clock signal S_{BUF_CLK}. This results in a power savings that is particularly significant at higher clock signal frequencies.

Reference is now made to Fig. 3B, which illustrates a

10   clock synchronization unit **200$_B$** in accordance with another non-limiting example embodiment. The clock synchronization unit **200$_B$** in Fig. 3B comprises a modified clock control circuit **210$_B$** that is similar to the clock control circuit **210** in the clock synchronization unit **200**

15   of Fig. 3A, with the following main difference. Specifically, the second input of an AND logic gate **211$_B$** is a signal S_{DLL_EN} which is output by a 2-input OR logic gate **234**. The 2-input OR logic gate **234** is fed by the output of the NOR logic gate **213** (which, it is recalled,

20   is fed by the ERASE and PROGRAM signals) and the output of the inverter logic gate **212** (which, it is recalled, is fed by the buffered chip enable signal S_{CEb}).

In operation, the modified clock control circuit **210$_B$**

25   causes the AND logic gate **211$_B$** to transfer the buffered clock signal S_{BUF_CLK} over to its output (which carries the reference clock signal S_{REF_CLK}) whenever either one of the following conditions is met: (i) the buffered chip enable signal S_{CEb} goes LOW (i.e., whenever the non-volatile

30   memory device **100** is selected) or (ii) the ERASE and PROGRAM signals are de-asserted (= LOW). Conversely, the reference clock signal S_{REF_CLK} will be decoupled from the buffered clock signal S_{BUF_CLK} only when both (i) the buffered chip enable signal S_{CEb} goes HIGH (i.e., whenever

the non-volatile memory device 100 is de-selected) and
(ii) the ERASE or PROGRAM signal is asserted (= HIGH).
Simply stated, when compared to the clock control circuit
210 in Fig. 3A, the modified clock control circuit 210$_B$

5   in Fig. 3B does not automatically decouple the reference
clock signal S_{REF_CLK} from the buffered clock signal S_{BUF_CLK}
when the ERASE or PROGRAM signal is asserted, but
requires the additional condition whereby the non-
volatile memory device 100 has been de-selected. Stated

10   differently, selecting the non-volatile memory device 100
will activate the DLL 220, thus over-riding the effect of
the ERASE or PROGRAM signal. While this may lead to less
of a power savings than in the circuit of Fig. 3A, it
nevertheless allows greater control of the operation of

15   the non-volatile memory device 100 directly from the
controller 90.

Fig. 4A is a non-limiting example timing diagram that
shows signal transitions of various signals associated

20   with the clock synchronization unit 200 in Fig. 3A during
a BLOCK ERASE operation. Those skilled in the art will
appreciate that similar timing diagrams could be provided
for other commands (e.g., PAGE PROGRAM), but have been
omitted since it is believed that they are not required

25   in order for the reader to acquire an understanding of
example embodiments.

The control signals in the top portion of Fig. 4A (namely
those at the input clock port CLK, the chip enable port

30   CE#, the write/read port W/R#, the command latch enable
port CLE, the address latch enable port ALE, the data
lines DQ[0:7], the data strobe port DQS and the
ready/busy port R/B#) are issued by the controller 90.

Between times T1 through T7, the non-volatile memory
device **100** receives a first cycle of the BLOCK ERASE
command (60h), row address information (RA1, RA2 & RA3)
and a second cycle of the BLOCK ERASE command (D0h).
5   Once the non-volatile memory device **100** receives and
decodes the second cycle of the BLOCK ERASE command
(D0h), the ERASE signal is asserted at time T8 and the
S_{DLL_EN2} signal (at the output of the NOR logic gate **213**)
goes LOW. The AND logic gate **211** is then disabled by the
10 LOW state of the S_{DLL_EN2} signal. Therefore, the reference
clock signal S_{REF_CLK} goes to the LOW state at around time
T8. As a result, the synchronizing clock signal S_{DLL_CLK}
stops toggling even though the buffered cock signal S_{BUF_CLK}
keeps toggling. In addition, the device-external signal
15 at the ready/busy port R/B# signal goes LOW.

The non-volatile memory device **100** then performs an
internal "erase and verify" operation on the non-volatile
memory cell array **115** for a time specified as t_{BERS} (Block
20 Erase Time), which varies and can be, for example, 2ms
for a SLC (Single Level Cell) type NAND flash memory
device or, for example, 15ms maximum for some types of
MLC (Multi-Level-Cell) NAND flash memory devices. During
the time that the non-volatile memory device **100** is
25 completing the internal "erase and verify" operation, the
DLL **220** is effectively disabled, thus leading to less
power consumption than if it were enabled during this
time.

30 Somewhere between times T14 and T15, the non-volatile
memory device **100** finishes its final "erase and verify"
operation and the ERASE signal goes to the LOW state. As
a result, the S_{DLL_EN2} signal goes back to the HIGH state at
time T15, which enables the AND logic gate **211**.

Therefore, the reference clock signal S_{REF_CLK} starts to track the buffered clock signal S_{BUF_CLK} again, and the DLL **220** tries to lock the synchronizing clock signal S_{DLL_CLK} according to the reference clock signal S_{REF_CLK} and the

5   feedback clock signal S_{FB_CLK}.   Those skilled in the art will appreciate that when the DLL **220** comprises a delay locked loop, a certain number of clock cycles may be needed for the synchronizing clock signal S_{DLL_CLK} to re-acquire synchronization (i.e., to "re-lock"). The timing

10   diagram in Fig. 4A assumes a simplified and short re-locking sequence such that the synchronizing clock signal S_{DLL_CLK} is already locked at time T16. Suitable re-locking sequences are known in the art and therefore not described here.

15   After the synchronizing clock signal S_{DLL_CLK} has re-acquired synchronization, the device-external signal at the ready/busy port R/B# signal goes HIGH as shown between times T16 and T17. The non-volatile memory device **100** now becomes "ready" and the controller **90** may

20   issue another command such as, without limitation, STATUS READ, PAGE READ and PAGE PROGRAM.

Fig. 4B is a non-limiting example timing diagram for the signals of the clock synchronization unit **200B** in Fig. 3B

25   during a BLOCK ERASE operation.   The timing diagram in Fig. 4B is similar to that of Fig. 4A, with the following exceptions.   Specifically, between times T7 and T8, it will be noted that the S_{DLL_EN} signal at the second input of the AND logic gate **211B** has not dropped to the LOW

30   state even though the ERASE signal is asserted. This is because buffered chip enable signal S_{CEb} signal is still in the LOW state (meaning that the non-volatile memory device **100** remains selected), which in this embodiment overrides the clock signal decoupling effect otherwise

controlled by the ERASE signal. Then, after the device-
external signal at the chip enable port CE# goes to the
HIGH state (between times T8 and T9), the buffered chip
enable signal S_{CEb} also goes to the HIGH state, and now
5   the S_{DLL_EN} signal goes to the LOW state. This disables
the AND logic gate **211$_B$**, causing the reference clock
signal S_{REF_CLK} to stop toggling so that the DLL **220** does
not expend power needlessly.

10   Those skilled in the art will appreciate that instead of
the DLL **220**, the clock synchronization unit **200** may
utilize include other modules having circuit components
in a feedback loop configuration. An example of such
other module is a phase-locked loop (PLL). Thus, the
15   phase-locked loop could be deactivated for a period of
time while the ERASE or PROGRAM signal is asserted.

Those skilled in the art will also appreciate that the
above description of the BLOCK ERASE, PAGE PROGRAM, PAGE
20   READ and STATUS READ commands is merely illustrative, and
that various modifications are possible without departing
from the scope of embodiments of the invention. In
addition, other current or future commands may trigger
assertion of the ERASE and/or PROGRAM signals. For
25   instance, consider the case of a hypothetical PAGE ERASE
command analogous to the above described BLOCK ERASE
command, but which allows a single page of a particular
multi-page block to be erased without affecting the other
block(s) in the page. An example of such a command is
30   described in United States Patent Application Serial No.
11/779,685 to Jin-Ki KIM, entitled "Partial Block Erase
Architecture for Flash Memory", hereby incorporated by
reference herein.

It will be understood that the non-volatile memory devices **100, 100ₐ** described above can be implemented using various types of non-volatile memory integrated circuit technology, including but not limited to NAND Flash EEPROM, NOR Flash EEPROM, AND Flash EEPROM, DiNOR Flash EEPROM, Serial Flash EEPROM, Read-Only Memory (ROM), Erasable Programmable ROM (EPROM), Ferroelectric Random-Access Memory (FRAM), Magnetoresistive RAM (MRAM) and Phase-Change RAM (PCRAM).

It should also be appreciated that in some embodiments, certain signals, in particular but without limitation the clock signals and the data strobe signals, can be single-ended while in other embodiments these signals can be differential.

It should also be appreciated that in some embodiments, certain devices, in particular the input register **112** and the output driver **105**, can be responsive to rising edges, falling edges or both rising edges and falling edges, thereby exhibiting single data rate (SDR), double data rate (DDR) or quadruple data rate (QDR) functionality.

Referring again to Fig. 1, the memory system 80 may, in some examples, be at least substantially compliant with the flash standard described in "Open NAND Flash Interface Specification", Revision 2.0, Feb. 27/08, the entire contents of which are herein incorporated by reference. Of course the memory system 80 may, in other examples, be at least substantially compliant with some other flash standard that is consistent with providing memory devices that include DLLs and/or PLLs.

It should also be appreciated that in some embodiments, the memory devices **100**, **100$_A$** can be provided with the above-described functionality at least partly through the use of a software program that is run on a computer.

5   Such a software program could be encoded as computer-readable instructions on a computer-readable storage medium, the instructions being designed to convert the above-described functionality into low-level circuit diagrams and/or integrated circuit configurations for

10   achieving the above describe functionality.

Certain adaptations and modifications of the described embodiments can be made. Therefore, the above discussed embodiments are considered to be illustrative and not

15   restrictive.

CLAIMS:

1. A non-volatile semiconductor memory device, comprising:

   - an interface comprising:

      - an input port for receiving an input clock signal; and

      - a set of data lines for receiving commands, including an erase command, the commands issued by a controller;

   - a module having circuit components in a feedback loop configuration, the module being driven by a reference clock signal;

   - a clock control circuit capable of controllably switching between a first operational state in which the reference clock signal tracks the input clock signal and a second operational state in which the reference clock signal is decoupled from the input clock signal; and

   - a command processing unit configured to recognize the commands issued by the controller and to cause the clock control circuit to switch from the first operational state to the second operational state in response to recognizing the erase command;

   - wherein when the reference clock signal tracks the input clock signal, the module consumes a first amount of power and wherein when the reference clock signal is decoupled from the input clock signal, the module consumes a second amount of power that is less than the first amount of power.

2. The non-volatile semiconductor memory device defined in claim 1, further comprising control circuitry for outputting a signal indicative that the device is busy in response to the command processing unit recognizing the erase command.

3. The non-volatile semiconductor memory device defined in claim 2, wherein the control circuitry is configured to output the signal indicative that the device is busy after the command processing unit causes the clock control circuit to switch from the first operational state to the second operational state.

4. The non-volatile semiconductor memory device defined in claim 1, wherein the command processing unit is configured to start an erase operation in response to receipt of the erase command.

5. The non-volatile semiconductor memory device defined in claim 4, wherein the command processing unit is configured to cause the clock control circuit to switch back to the first operational state after the erase operation is complete.

6. The non-volatile semiconductor memory device defined in claim 5, further comprising control circuitry configured to issue a signal indicating that the device is ready after the erase operation is complete.

7. The non-volatile semiconductor memory device defined in claim 6, wherein the clock synchronization circuit comprises a delay locked loop that loses synchronization when the reference clock signal is decoupled from the input clock signal, wherein the signal indicating that the device is ready is issued after the delay locked loop has regained synchronization following the clock control circuit having switched back to the first operational state.

8. The non-volatile semiconductor memory device defined in claim 4, wherein the command processing unit is configured to cause the clock control circuit to switch back to the first operational state before the erase operation is complete.

9. The non-volatile semiconductor memory device defined in claim 8, further comprising control circuitry configured to issue a signal indicating that the device is ready after the command processing unit causes the clock control circuit to switch back to the second operational state.

10. The non-volatile semiconductor memory device defined in claim 8, wherein the clock synchronization circuit comprises a delay locked loop that loses synchronization when the reference clock signal is decoupled from the input clock signal, wherein the signal indicating that the device is ready is issued after the delay locked loop has regained synchronization following the clock control circuit having switched back to the first operational state.

11. The non-volatile semiconductor memory device defined in claim 1, further comprising a plurality of non-volatile memory cells, wherein the command processing unit is configured to cause the clock control circuit to switch back to the first operational state after at least some of the non-volatile memory cells have been erased.

12. The non-volatile semiconductor memory device defined in claim 1, wherein the module comprises a clock synchronization circuit configured to generate a synchronizing clock signal based on the reference clock signal.

13. The non-volatile semiconductor memory device defined in claim 12, wherein the clock synchronization circuit comprises a delay locked loop.

14. The non-volatile semiconductor memory device defined in claim 12, wherein the clock synchronization circuit comprises a phase locked loop.

15. The non-volatile semiconductor memory device defined in claim 12, wherein the data lines are also for outputting read data from the device.

16. The non-volatile semiconductor memory device defined in claim 15, further comprising an output driver configured to vary a data strobe signal in synchronism with the synchronizing clock signal.

17. The non-volatile semiconductor memory device defined in claim 16, wherein the output driver is configured to synchronize outputting of the read data with the data strobe signal.

18. The non-volatile semiconductor memory device defined in claim 17, wherein the interface comprises a port for outputting the data strobe signal from the device.

19. The non-volatile semiconductor memory device defined in claim 1, wherein the clock control circuit implements a logic AND function producing an output corresponding to the reference clock signal, wherein the logic AND function has a first input corresponding to the input clock signal and a second input corresponding to a signal that is asserted when the erase command is recognized by the command processing unit.

20. The non-volatile semiconductor memory device defined in claim 1, wherein said commands include a different command and wherein the command processing unit is further configured to cause the clock control circuit to switch from said one of the first and second operational state to said other of the first and second operational state in response to recognizing the different command issued by the controller.

21. The non-volatile semiconductor memory device defined in claim 20, wherein the non-volatile semiconductor memory device further implements a logic OR function

having a first input corresponding to a signal that is
asserted when the erase command is recognized by the
command processing unit and a second input
corresponding to a signal that is asserted when the

5   different command is recognized by the command
processing unit.

22. The non-volatile semiconductor memory device defined
in claim 20, further comprising a plurality of non-
volatile memory cells, wherein the different command is

10   a command to program at least some of the non-volatile
memory cells.

23. The non-volatile semiconductor memory device defined
in claim 22, wherein the command processing unit is
configured to cause the clock control circuit to switch

15   back to the first operational state after at least some
of the non-volatile memory cells have been programmed.

24. The non-volatile semiconductor memory device defined
in claim 22, wherein the different command is a PAGE
PROGRAM command.

20 25. The non-volatile semiconductor memory device defined
in claim 1, wherein the interface comprises an input
port for receiving a device select signal from the
controller, the device select signal being indicative
of whether the device has been selected or deselected.

25 26. The non-volatile semiconductor memory device defined
in claim 25, wherein the command processing unit is
configured to allow the clock control circuit to switch
to the second operational state even when the device
select signal is indicative of the device having been

30   selected.

27. The non-volatile semiconductor memory device defined
in claim 25, wherein the command processing unit is
configured to prevent the clock control circuit from
switching to the second operational state unless the

device select signal is indicative of the device having been deselected.

28. The non-volatile semiconductor memory device defined in claim 1, wherein when the reference clock signal tracks the input clock signal, the module effects a first average number of signal transitions per unit time and wherein when the reference clock signal is decoupled from the input clock signal, the module effects a second average number of signal transitions per unit time that is less than the first average number of signal transitions per unit time.

29. The non-volatile semiconductor memory device defined in claim 1, wherein the commands issued by the controller are encoded, wherein the command processing unit comprises a decoder and wherein to recognize a particular command issued by the controller, the decoder is configured to decode the particular command.

30. The non-volatile semiconductor memory device defined in claim 1, wherein the erase command is a BLOCK ERASE command.

31. The non-volatile semiconductor memory device defined in claim 1, implemented as a NAND flash memory device.

32. A non-volatile semiconductor memory device, comprising:

- first means for providing an input clock signal;

- second means having circuit components in a feedback loop configuration and being driven by a reference clock signal;

- third means for controllably switching between a first operational state in which the reference clock signal tracks the input clock signal and a second operational state in which the reference clock signal is decoupled from the input clock signal; and

- fourth means for recognizing commands issued by a
  controller, including an erase command, and varying
  the operational state of the third means in response
  to recognizing the erase command;

5   - wherein when the reference clock signal tracks the
         input clock signal, the second means consumes a
         first amount of power and wherein when the reference
         clock signal is decoupled from the input clock
         signal, the second means consumes a second amount of

10   power that is less than the first amount of power.

   33.   A method implemented by a non-volatile semiconductor
        memory device that is provided with an input clock
        signal and that comprises a module with circuit
        components in a feedback loop configuration, the

15   circuit components being driven by a reference clock
        signal, comprising:

        - producing the reference clock signal such that it
          follows the input clock signal in a first
          operational state of the device and such that it is

20   decoupled from the input clock signal in a second
          operational state of the device, wherein when the
          reference clock signal follows the input clock
          signal, the module consumes a first amount of power
          is consumed and wherein when the reference clock

25   signal is decoupled from the input clock signal, the
          module consumes a second amount of power that is
          less than the first amount of power is consumed; and

        - causing the device to switch from the first
          operational state to the second operational state in

30   response to recognizing an erase command received
          from a controller.

   34.   A system, comprising:

- a controller configured to issue a master clock
  signal and to issue commands including an erase
  command; and

5 - a non-volatile semiconductor memory device, which
  comprises:

- an interface comprising:

- an input port for receiving an input clock signal
  related to the master clock signal; and

- a set of data lines for receiving the commands
10 issued by the controller;

- a module having circuit components in a feedback
  loop configuration, the module being driven by a
  reference clock signal;

- a clock control circuit capable of controllably
15 switching between a first operational state in
  which the reference clock signal tracks the input
  clock signal and a second operational state in
  which the reference clock signal is decoupled from
  the input clock signal; and

20 - a command processing unit configured to recognize
  the commands issued by the controller and to cause
  the clock control circuit to switch from the first
  operational state to the second operational state
  in response to recognizing the erase command;

25 - wherein when the reference clock signal tracks the
  input clock signal, the module consumes a first
  amount of power and wherein when the reference clock
  signal is decoupled from the input clock signal, the
  module consumes a second amount of power that is
30 less than the first amount of power.

35. A computer-readable storage medium comprising
  computer-readable instructions which, when processed,
  are used to provide a non-volatile semiconductor memory
  device with functionality for:

-       producing a reference clock signal such that it
        follows an input clock signal in a first
        operational state of the device and such that
        it is decoupled from the input clock signal in

5   a second operational state of the device,
        wherein when the reference clock signal follows
        the input clock signal, a first amount of power
        is consumed by a module with circuit components
        in a feedback loop configuration that is driven

10   by the reference clock signal, and wherein when
        the reference clock signal is decoupled from
        the input clock signal, the module consumes a
        second amount of power that is less than the
        first amount of power; and

15 -   causing the device to switch from the first
        operational state to the second operational
        state in response to recognizing an erase
        command received from a controller.

**AMENDED CLAIMS received by the International Bureau on 21
April 2009 (21.04.09)**

1. A non-volatile semiconductor memory device, comprising:

   - an interface comprising:

     - an input port for receiving an input clock signal;
       and

     - a set of data lines for receiving commands,
       including an erase command, the commands issued by
       a controller;

   - a module having circuit components in a feedback
     loop configuration, the module being driven by a
     reference clock signal;

   - a clock control circuit capable of controllably
     switching between a first operational state in which
     the reference clock signal tracks the input clock
     signal and a second operational state in which the
     reference clock signal is decoupled from the input
     clock signal; and

   - a command processing unit configured to recognize
     the commands issued by the controller and, in
     response to recognizing the erase command, to cause
     the clock control circuit to switch from the first
     operational state to the second operational state;

   - wherein when the reference clock signal tracks the
     input clock signal, the module consumes a first
     amount of power and wherein when the reference clock
     signal is decoupled from the input clock signal, the
     module consumes a second amount of power that is
     less than the first amount of power.

2. The non-volatile semiconductor memory device defined in
   claim 1, further comprising control circuitry for
   outputting a signal indicative that the device is busy
   in response to the command processing unit recognizing
   the erase command.

3. The non-volatile semiconductor memory device defined in
   claim 2, wherein the control circuitry is configured to

AMENDED SHEET (ARTICLE 19)

output the signal indicative that the device is busy
after the command processing unit causes the clock
control circuit to switch from the first operational
state to the second operational state.

4. The non-volatile semiconductor memory device defined in
   claim 1, wherein the command processing unit is
   configured to start an erase operation in response to
   recognizing the erase command.

5. The non-volatile semiconductor memory device defined in
   claim 4, wherein the command processing unit is
   configured to cause the clock control circuit to switch
   back to the first operational state after the erase
   operation is complete.

6. The non-volatile semiconductor memory device defined in
   claim 5, further comprising control circuitry
   configured to issue a signal indicating that the device
   is ready after the erase operation is complete.

7. The non-volatile semiconductor memory device defined in
   claim 6, wherein the clock synchronization circuit
   comprises a delay locked loop that loses
   synchronization when the reference clock signal is
   decoupled from the input clock signal, wherein the
   signal indicating that the device is ready is issued
   after the delay locked loop has regained
   synchronization following the clock control circuit
   having switched back to the first operational state.

8. The non-volatile semiconductor memory device defined in
   claim 4, wherein the command processing unit is
   configured to cause the clock control circuit to switch
   back to the first operational state before the erase
   operation is complete.

9. The non-volatile semiconductor memory device defined in
   claim 8, further comprising control circuitry
   configured to issue a signal indicating that the device

34

is ready after the command processing unit causes the clock control circuit to switch back to the first operational state.

10. The non-volatile semiconductor memory device defined in claim 9, wherein the clock synchronization circuit comprises a delay locked loop that loses synchronization when the reference clock signal is decoupled from the input clock signal, wherein the signal indicating that the device is ready is issued after the delay locked loop has regained synchronization following the clock control circuit having switched back to the first operational state.

11. The non-volatile semiconductor memory device defined in claim 1, further comprising a plurality of non-volatile memory cells, wherein the command processing unit is configured to cause the clock control circuit to switch back to the first operational state after at least some of the non-volatile memory cells have been erased.

12. The non-volatile semiconductor memory device defined in claim 1, wherein the module comprises a clock synchronization circuit configured to generate a synchronizing clock signal based on the reference clock signal.

13. The non-volatile semiconductor memory device defined in claim 12, wherein the clock synchronization circuit comprises a delay locked loop.

14. The non-volatile semiconductor memory device defined in claim 12, wherein the clock synchronization circuit comprises a phase locked loop.

15. The non-volatile semiconductor memory device defined in claim 12, wherein the data lines are also for outputting read data from the device.

35

16. The non-volatile semiconductor memory device defined in claim 15, further comprising an output driver configured to vary a data strobe signal in synchronism with the synchronizing clock signal.

17. The non-volatile semiconductor memory device defined in claim 16, wherein the output driver is configured to synchronize outputting of the read data with the data strobe signal.

18. The non-volatile semiconductor memory device defined in claim 17, wherein the interface comprises a port for outputting the data strobe signal from the device.

19. The non-volatile semiconductor memory device defined in claim 1, wherein the clock control circuit implements a logic AND function producing an output corresponding to the reference clock signal, wherein the logic AND function has a first input corresponding to the input clock signal and a second input corresponding to a signal that is asserted when the erase command is recognized by the command processing unit.

20. The non-volatile semiconductor memory device defined in claim 1, wherein said commands further include a different command and wherein the command processing unit is further configured to cause the clock control circuit to switch from the first operational state to the second operational state in response to recognizing the different command issued by the controller.

21. The non-volatile semiconductor memory device defined in claim 20, wherein the non-volatile semiconductor memory device further implements a logic OR function having a first input corresponding to a signal that is asserted when the erase command is recognized by the command processing unit and a second input corresponding to a signal that is asserted when the

36

different command is recognized by the command
processing unit.

22. The non-volatile semiconductor memory device defined
in claim 20, further comprising a plurality of non-
volatile memory cells, wherein the different command is
a command to program at least some of the non-volatile
memory cells.

23. The non-volatile semiconductor memory device defined
in claim 22, wherein the command processing unit is
configured to cause the clock control circuit to switch
back to the first operational state after at least some
of the non-volatile memory cells have been programmed.

24. The non-volatile semiconductor memory device defined
in claim 22, wherein the different command is a PAGE
PROGRAM command.

25. The non-volatile semiconductor memory device defined
in claim 1, wherein the interface comprises an input
port for receiving a device select signal from the
controller, the device select signal being indicative
of whether the device has been selected or deselected.

26. The non-volatile semiconductor memory device defined
in claim 25, wherein the command processing unit is
configured to allow the clock control circuit to switch
to the second operational state even when the device
select signal is indicative of the device having been
selected.

27. The non-volatile semiconductor memory device defined
in claim 25, wherein the command processing unit is
configured to prevent the clock control circuit from
switching to the second operational state unless the
device select signal is indicative of the device having
been deselected.

28. The non-volatile semiconductor memory device defined
in claim 1, wherein when the reference clock signal

37

tracks the input clock signal, the module effects a first average number of signal transitions per unit time and wherein when the reference clock signal is decoupled from the input clock signal, the module effects a second average number of signal transitions per unit time that is less than the first average number of signal transitions per unit time.

29. The non-volatile semiconductor memory device defined in claim 1, wherein the commands issued by the controller are encoded, wherein the command processing unit comprises a decoder and wherein to recognize a particular command issued by the controller, the decoder is configured to decode the particular command.

30. The non-volatile semiconductor memory device defined in claim 1, wherein the erase command is a BLOCK ERASE command.

31. The non-volatile semiconductor memory device defined in claim 1, implemented as a NAND flash memory device.

32. The non-volatile semiconductor memory device defined in claim 1, wherein to recognize the commands issued by the controller, the command processing unit is configured to load information received via the data lines into at least one register and to decode the information into said commands.

33. A non-volatile semiconductor memory device, comprising:

   - first means for providing an input clock signal;

   - second means having circuit components in a feedback loop configuration and being driven by a reference clock signal;

   - third means for controllably switching between a first operational state in which the reference clock signal tracks the input clock signal and a second

38

AMENDED SHEET (ARTICLE 19)

operational state in which the reference clock
signal is decoupled from the input clock signal; and

- fourth means for recognizing commands issued by a
  controller, including an erase command, and varying
  the operational state of the third means in response
  to recognizing the erase command;

- wherein when the reference clock signal tracks the
  input clock signal, the second means consumes a
  first amount of power and wherein when the reference
  clock signal is decoupled from the input clock
  signal, the second means consumes a second amount of
  power that is less than the first amount of power.

34. A method implemented by a non-volatile semiconductor
    memory device that is provided with an input clock
    signal and that comprises a module with circuit
    components in a feedback loop configuration, the
    circuit components being driven by a reference clock
    signal, comprising:

- producing the reference clock signal such that it
  follows the input clock signal in a first
  operational state of the device and such that it is
  decoupled from the input clock signal in a second
  operational state of the device, wherein when the
  reference clock signal follows the input clock
  signal, the module consumes a first amount of power
  is consumed and wherein when the reference clock
  signal is decoupled from the input clock signal, the
  module consumes a second amount of power that is
  less than the first amount of power is consumed; and

- causing the device to switch from the first
  operational state to the second operational state in
  response to recognizing an erase command received
  from a controller.

35. A system, comprising:

39

- a controller configured to issue a master clock signal and to issue commands including an erase command; and
- a non-volatile semiconductor memory device, which comprises:
- an interface comprising:
    - an input port for receiving an input clock signal related to the master clock signal; and
    - a set of data lines for receiving the commands issued by the controller;
    - a module having circuit components in a feedback loop configuration, the module being driven by a reference clock signal;
    - a clock control circuit capable of controllably switching between a first operational state in which the reference clock signal tracks the input clock signal and a second operational state in which the reference clock signal is decoupled from the input clock signal; and
    - a command processing unit configured to recognize the commands issued by the controller and to cause the clock control circuit to switch from the first operational state to the second operational state in response to recognizing the erase command;
- wherein when the reference clock signal tracks the input clock signal, the module consumes a first amount of power and wherein when the reference clock signal is decoupled from the input clock signal, the module consumes a second amount of power that is less than the first amount of power.

36. A computer-readable storage medium comprising computer-readable instructions which, when processed, are used to provide a non-volatile semiconductor memory device with functionality for:

40

- producing a reference clock signal such that it follows an input clock signal in a first operational state of the device and such that it is decoupled from the input clock signal in a second operational state of the device, wherein when the reference clock signal follows the input clock signal, a first amount of power is consumed by a module with circuit components in a feedback loop configuration that is driven by the reference clock signal, and wherein when the reference clock signal is decoupled from the input clock signal, the module consumes a second amount of power that is less than the first amount of power; and

- causing the device to switch from the first operational state to the second operational state in response to recognizing an erase command received from a controller.

37. A non-volatile semiconductor memory device, comprising:

an interface for receiving commands issued by a controller, the commands including an erase command;

a functional module with circuit components and having a terminal;

a node;

switchable circuitry capable of controllably switching between a first operational state in which the terminal is electrically connected to the node and a second operational state in which the terminal is electrically decoupled from the node, the node being configured to have a signal for the functional module communicated through it when the switchable circuitry is in the first operational state; and

41

AMENDED SHEET (ARTICLE 19)

a command processing unit configured to recognize the
commands issued by the controller and, in response
to recognizing the erase command, to cause the
switchable circuitry to switch from the first
operational state to the second operational state.

38. The non-volatile semiconductor memory device defined
in claim 37, wherein the circuit components are in a
feedback loop configuration and wherein said signal for
the functional module comprises an input clock signal
for synchronizing operation of the functional module
when the terminal is electrically connected to the
node.

39. The non-volatile semiconductor memory device defined
in claim 38, wherein the interface comprises a set of
data lines and wherein the commands are received over
the set of data lines.

40. The non-volatile semiconductor memory device defined
in claim 38, wherein when the terminal is electrically
connected to the node, the module consumes a first
amount of power and wherein when terminal is
electrically decoupled from the node, the module
consumes a second amount of power that is less than the
first amount of power.

41. The non-volatile semiconductor memory device defined
in claim 38, further comprising control circuitry for
outputting a signal indicative that the device is busy
in response to the command processing unit recognizing
the erase command.

42. The non-volatile semiconductor memory device defined
in claim 41, wherein the control circuitry is
configured to output the signal indicative that the
device is busy after the command processing unit causes

42

AMENDED SHEET (ARTICLE 19)

the switchable circuitry to switch from the first
operational state to the second operational state.

43.   The non-volatile semiconductor memory device defined
      in claim 38, wherein the command processing unit is
      configured to start an erase operation in response to
      recognizing the erase command.

44.   The non-volatile semiconductor memory device defined
      in claim 43, wherein the command processing unit is
      configured to cause the switchable circuitry to switch
      back to the first operational state after the erase
      operation is complete.

45.   The non-volatile semiconductor memory device defined
      in claim 44, further comprising control circuitry
      configured to issue a signal indicating that the device
      is ready after the erase operation is complete.

46.   The non-volatile semiconductor memory device defined
      in claim 45, wherein the circuit components implement a
      delay locked loop that loses synchronization when the
      terminal is electrically decoupled from the node,
      wherein the signal indicating that the device is ready
      is issued after the delay locked loop has regained
      synchronization following the switchable circuitry
      having switched back to the first operational state.

47.   The non-volatile semiconductor memory device defined
      in claim 43, wherein the command processing unit is
      configured to cause the switchable circuitry to switch
      back to the first operational state before the erase
      operation is complete.

48.   The non-volatile semiconductor memory device defined
      in claim 47, further comprising control circuitry
      configured to issue a signal indicating that the device
      is ready after the command processing unit causes the

43

switchable circuitry to switch back to the first
operational state.

49. The non-volatile semiconductor memory device defined
     in claim 48, wherein the circuit components implement a
     delay locked loop that loses synchronization when the
     terminal is electrically decoupled from the node, ·
     wherein the signal indicating that the device is ready
     is issued after the delay locked loop has regained
     synchronization following the switchable circuitry
     having switched back to the first operational state.

50. The non-volatile semiconductor memory device defined
     in claim 38, further comprising a plurality of non-
     volatile memory cells, wherein the command processing
     unit is configured to cause the switchable circuitry to
     switch back to the first operational state after at
     least some of the non-volatile memory cells have been
     erased.

51. The non-volatile semiconductor memory device defined
     in claim 38, wherein the circuit components of the
     functional module implements a clock synchronization
     circuit configured to generate a synchronizing clock
     signal based on a signal at the terminal.

52. The non-volatile semiconductor memory device defined
     in claim 51, wherein the clock synchronization circuit
     comprises a delay locked loop.

53. The non-volatile semiconductor memory device defined
     in claim 51, wherein the clock synchronization circuit
     comprises a phase locked loop.

54. The non-volatile semiconductor memory device defined
     in claim 51, wherein the interface is also for
     outputting read data from the device.

55. The non-volatile semiconductor memory device defined
     in claim 54, further comprising an output driver
     configured to vary a data strobe signal in synchronism
     with the synchronizing clock signal.

56. The non-volatile semiconductor memory device defined
     in claim 55, wherein the output driver is configured to
     synchronize outputting of the read data with the data
     strobe signal.

57. The non-volatile semiconductor memory device defined
     in claim 56, wherein the interface comprises a port for
     outputting the data strobe signal from the device.

58. The non-volatile semiconductor memory device defined
     in claim 38, wherein the switchable circuitry
     implements a logic AND function producing an output at
     the terminal, wherein the logic AND function has a
     first input corresponding to the input clock signal and
     a second input corresponding to a signal that is
     asserted when the erase command is recognized by the
     command processing unit.

59. The non-volatile semiconductor memory device defined
     in claim 38, wherein the commands issued by the
     controller further include a different command and
     wherein the command processing unit is further
     configured to cause the switchable circuitry to switch
     from the operational state to the second operational
     state in response to recognizing the different command
     issued by the controller.

60. The non-volatile semiconductor memory device defined
     in claim 59, wherein the non-volatile semiconductor
     memory device further implements a logic OR function
     having a first input corresponding to a signal that is
     asserted when the erase command is recognized by the
     command processing unit and a second input

45

corresponding to a signal that is asserted when the
different command is recognized by the command
processing unit.

61. The non-volatile semiconductor memory device defined
     in claim 59, further comprising a plurality of non-
     volatile memory cells, wherein the different command is
     a command to program at least some of the non-volatile
     memory cells.

62. The non-volatile semiconductor memory device defined
     in claim 61, wherein the command processing unit is
     further configured to cause the switchable circuitry to
     switch back to the first operational state after at
     least some of the non-volatile memory cells have been
     programmed.

63. The non-volatile semiconductor memory device defined
     in claim 61, wherein the different command is a PAGE
     PROGRAM command.

64. The non-volatile semiconductor memory device defined
     in claim 38, wherein the interface comprises an input
     port for receiving a device select signal from the
     controller, the device select signal being indicative
     of whether the device has been selected or deselected.

65. The non-volatile semiconductor memory device defined
     in claim 64, wherein the command processing unit is
     further configured to allow the switchable circuitry to
     switch to the second operational state even when the
     device select signal is indicative of the device having
     been selected.

66. The non-volatile semiconductor memory device defined
     in claim 64, wherein the command processing unit is
     further configured to prevent the switchable circuitry
     from switching to the second operational state unless

the device select signal is indicative of the device
having been deselected.

67. The non-volatile semiconductor memory device defined
    in claim 38, wherein when the terminal is electrically
    connected to the node, the circuit components of the
    functional module carry out a first average number of
    signal transitions per unit time and wherein when the
    terminal is electrically decoupled from the node, the
    circuit components of the functional module carry out a
    second average number of signal transitions per unit
    time that is less than the first average number of
    signal transitions per unit time.

68. The non-volatile semiconductor memory device defined
    in claim 38, wherein the commands issued by the
    controller are encoded into coded signals, wherein the
    command processing unit comprises a decoder configured
    to extract the erase command from a particular coded
    signal when the particular coded signal encodes the
    erase command.

69. The non-volatile semiconductor memory device defined
    in claim 37, wherein the erase command is a BLOCK ERASE
    command.

70. The non-volatile semiconductor memory device defined
    in claim 38, implemented as a NAND flash memory device.

71. The non-volatile semiconductor memory device defined
    in claim 38, wherein to recognize the commands issued
    by the controller, the command processing unit is
    configured to load information received via the
    interface into at least one register and to decode the
    information into said commands.

72. A method implemented by a non-volatile semiconductor
    memory device that includes a node and a functional

47

module with circuit components and a terminal, the
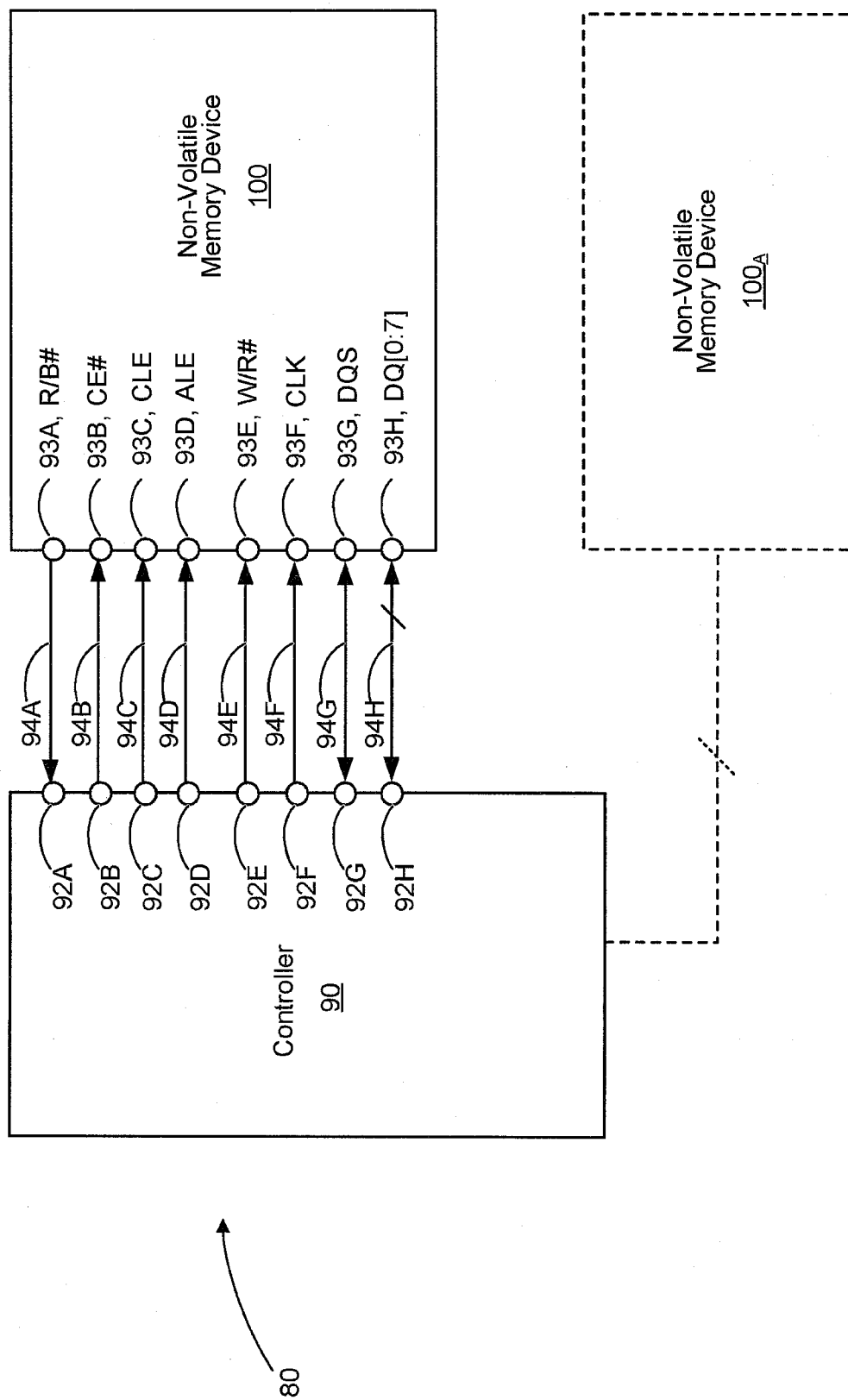method comprising:

- causing the device to switch from a first
  operational state to a second operational state in
  response to recognizing an erase command received
  from a controller;

- electrically connecting the terminal to the node
  when the device is in the first operational state;
  and

- electrically decoupling the terminal from the node
  when the device is in the second operational state.

73. A computer-readable storage medium comprising
    computer-readable instructions which, when processed,
    are used to generate a non-volatile semiconductor
    memory device that includes a node and a functional
    module with circuit components and a terminal, and
    having functionality for:

- switching from a first operational state to a second
  operational state in response to recognizing an
  erase command received from a controller;

- electrically connecting the terminal to the node
  when the device is in the first operational state;
  and

- electrically decoupling the terminal from the node
  when the device is in the second operational state.

74. A system, comprising:

- a controller configured to issue commands including
  an erase command; and

- a non-volatile semiconductor memory device, which
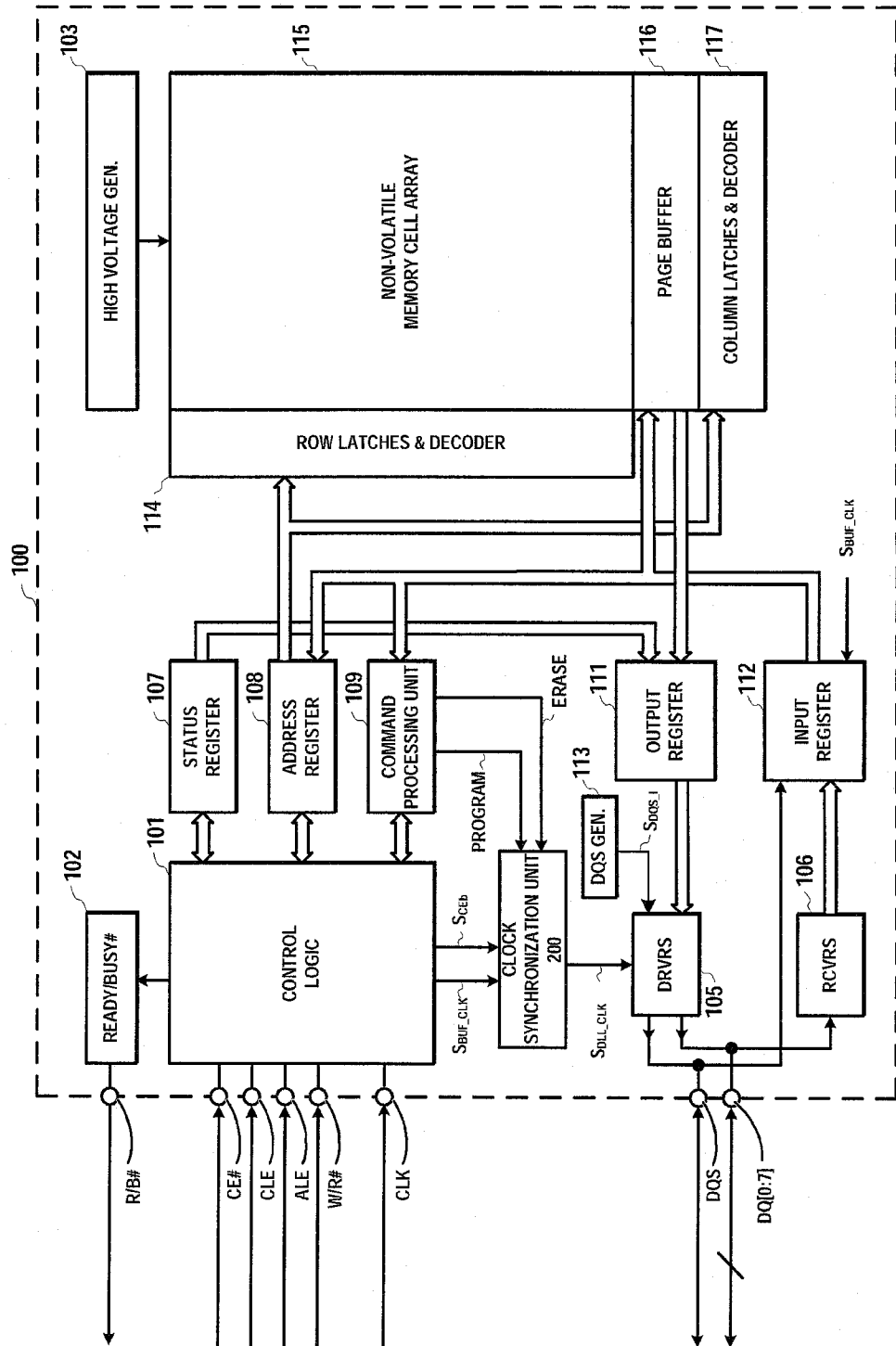 comprises:

AMENDED SHEET (ARTICLE 19)

- an interface for receiving commands issued by a controller, the commands including an erase command;

- a functional module with circuit components and having a terminal;

- a node;

- switchable circuitry capable of controllably switching between a first operational state in which the terminal is electrically connected to the node and a second operational state in which the terminal is electrically decoupled from the node, the node being configured to have a signal for the functional module communicated through it when the switchable circuitry is in the first operational state; and

- a command processing unit configured to recognize the commands issued by the controller and, in response to recognizing the erase command, to cause the switchable circuitry to switch from the first operational state to the second operational state.
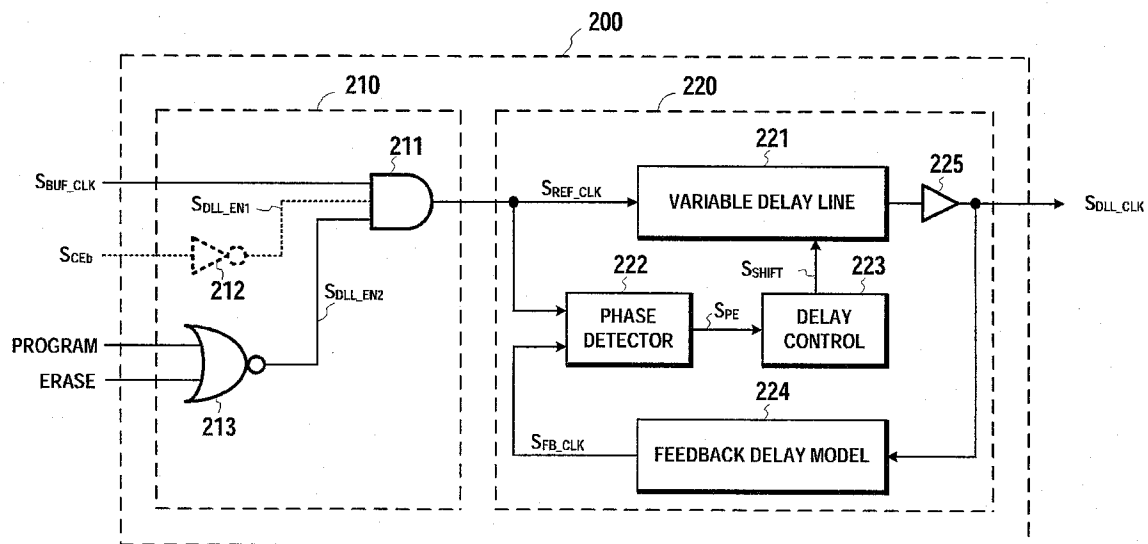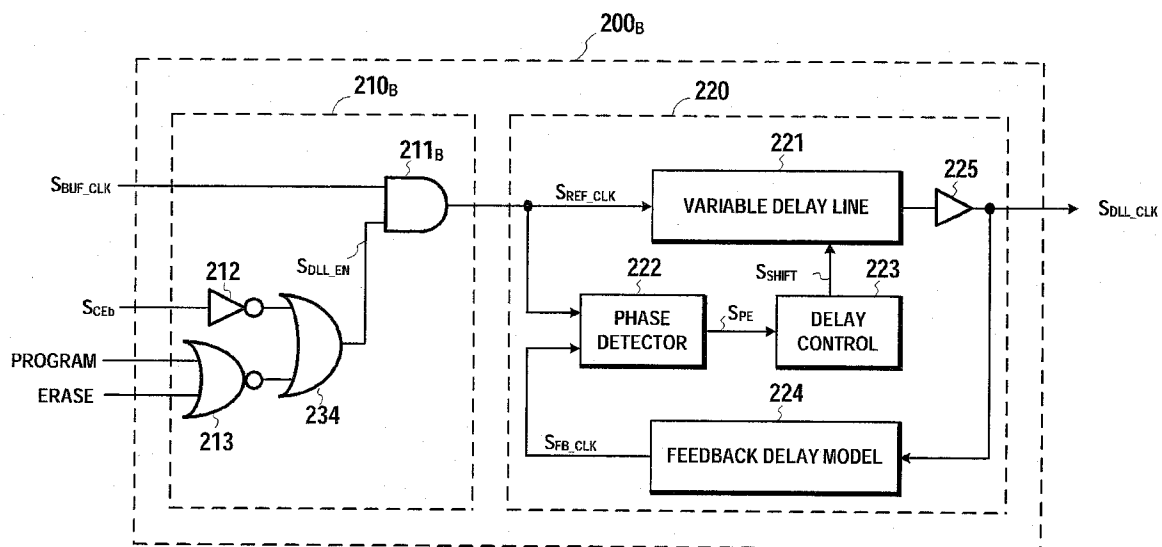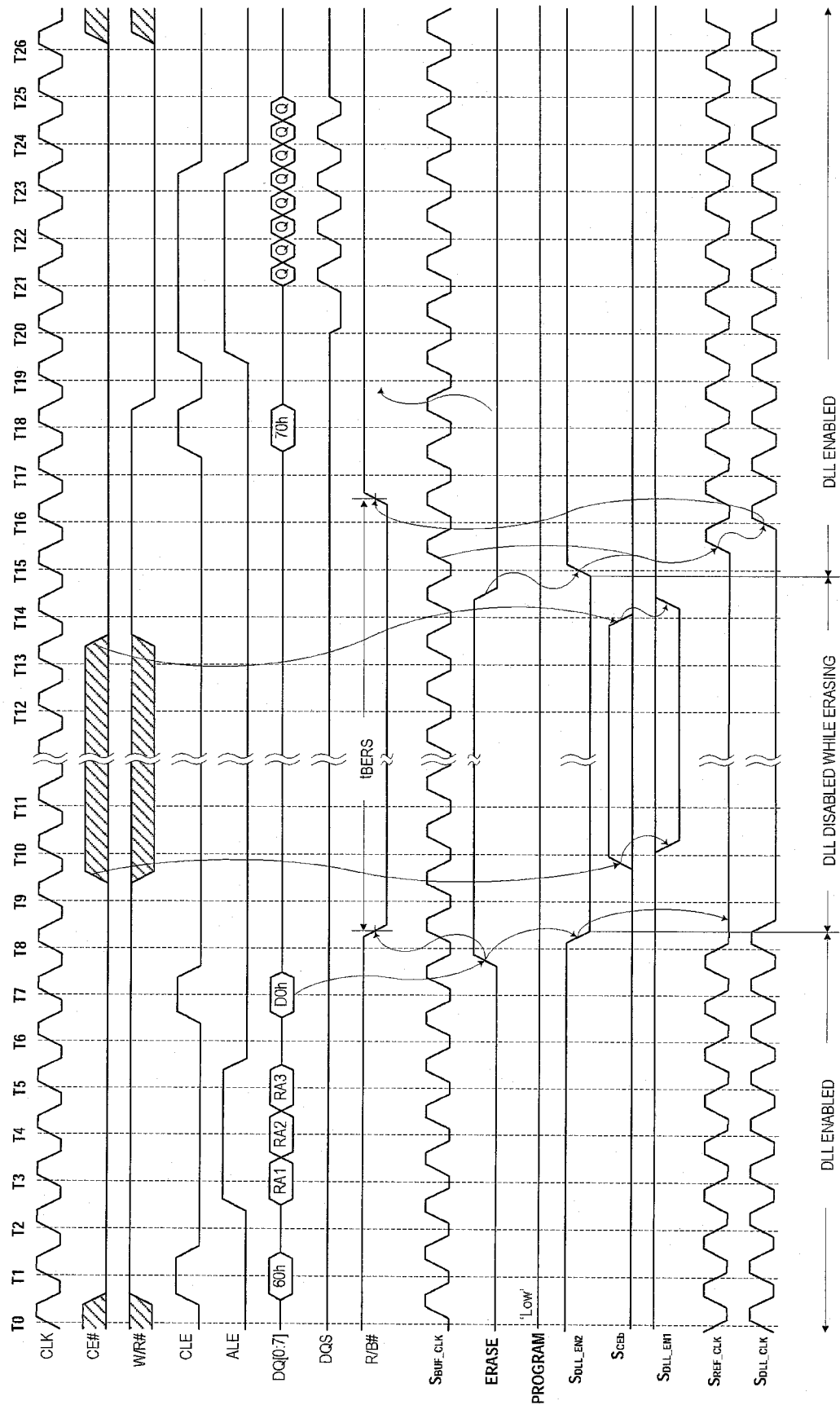
49

Fig. 1

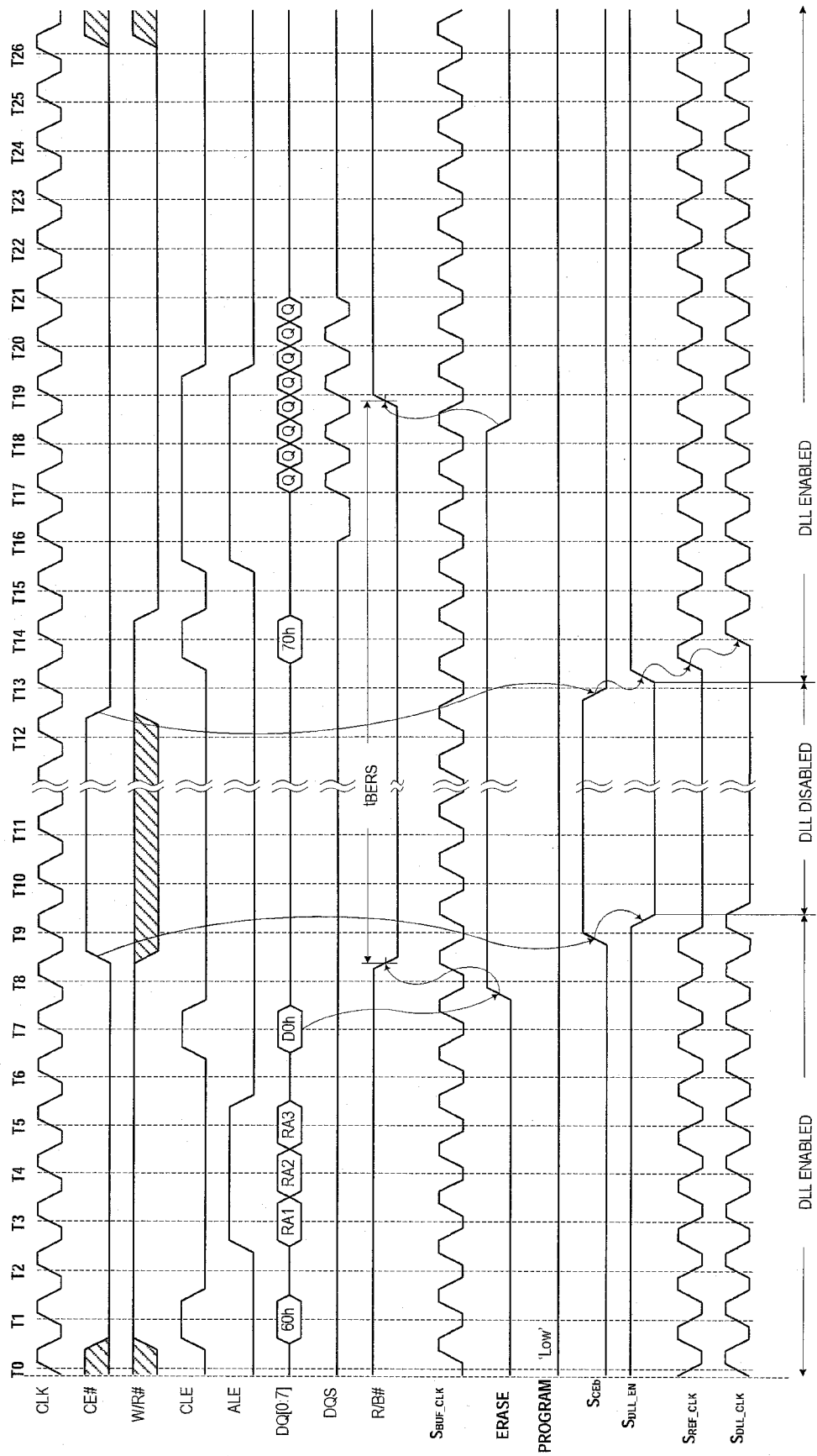Fig. 2

3/5

Fig. 3A

Fig. 3B

Fig. 4A

Fig. 4B

A.	CLASSIFICATION OF SUBJECT MATTER

IPC: *G11C 11/413* (2006.01) , *G11C 11/4193* (2006.01) , *G11C 7/20* (2006.01)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
          IPC: G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
Databases: Canadian Patent Database, WEST, Delphion
Search terms used: clock, synchronization, circuit, DLL, power, memory, flash

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/0279112 A1, 6 December 2007, Maeda et al. *see entire document	1-35
A	US 2005/0105363 A1, 19 March 2005, Ko *see entire document	1-35
A	US 6,842,396 B2, 11 January 2005, Kono *see entire document	1-35
A	US 2001/0010650 A1, 2 August 2001, Lee *see entire document	1-35

[ ] Further documents are listed in the continuation of Box C.   [X] See patent family annex.

*	Special categories of cited documents :	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
05 November 2008 (05-11-2008)	20 November 2008 (20-11-2008)

Name and mailing address of the ISA/CA	Authorized officer
Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001-819-953-2476	Kazem Ziaie 819- 934-2667

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US 2007279112A1	06-12-2007	CN 1942976A	04-04-2007
		JP 2005228427A	25-08-2005
		KR 20060134980A	28-12-2006
		TW 277981B	01-04-2007
		WO 2005078735A1	25-08-2005
US 2005105363A1	19-05-2005	DE 102004050080A1	07-07-2005
		KR 20050035637A	19-04-2005
		US 7102939B2	05-09-2006
US 6842396B2	11-01-2005	JP 2004110906A	08-04-2004
		US 2004052152A1	18-03-2004
US 2001010650A1	02-08-2001	DE 10102626A1	02-08-2001
		JP 4061029B2	12-03-2008
		JP 2001236785A	31-08-2001
		KR 20010076844A	16-08-2001
		TW 504704B	01-10-2002
		US 6356489B2	12-03-2002