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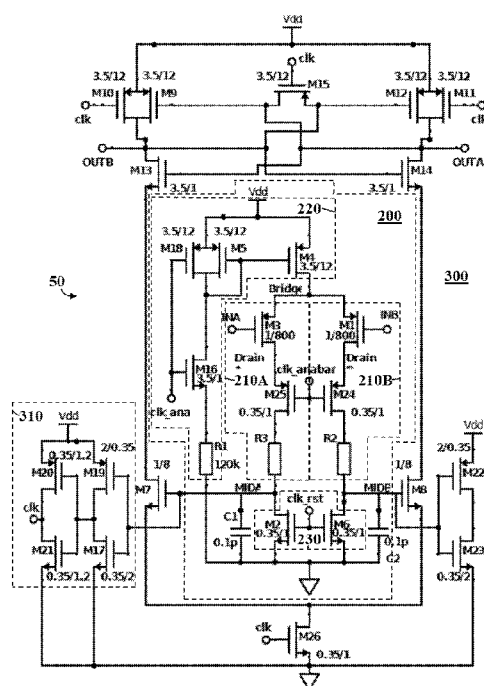
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Figure 2



(57) Abstract: A detector for detecting neural spike signals, the detector comprising a core amplifier. The core amplifier comprises two current paths, each current path integrating a current on a respective integrating node. Each current path comprises an input transistor receiving an analogue input signal, and a tunable load configured to tune an offset voltage of the core amplifier. The core amplifier further comprises a reset element configured to reset the integrating nodes periodically. The detector further comprises a read out element configured to process the integrated currents at the two integrating nodes.

DETECTOR FOR DETECTING NEURAL SPIKE SIGNALS, NEURAL SPIKE RECORDING SYSTEM, AND METHOD OF USING A DETECTOR

The present invention relates to a detector for detecting neural spike signals, a neural spike recording system, and a method of using a detector for detecting neural spike signals.

Modern neuroscience relies on the ability to read brain activity across large swathes of cortex at very high resolution both spatially and temporally. To read brain activity, probe needles are inserted into brain tissue (e.g. a Utah array [1]) and feed weak signals in the 10s-100s μ V range to an analogue front-end, which consists of a preamplifier, analogue filtering and typically a digitisation stage. The preconditioned and digitised waveform can then be fed into a back-end stage which carries out additional processing such as threshold detection, which is often enough to detect neural spiking activity [2]. The extremely weak nature of the input signal translates into demanding preamplifier block specifications. The preamplifier needs to provide significant amplification (of a factor of 100-1000) before other circuitry can make use of the signal, whilst maintaining extremely low noise levels and - in the case of implantable devices - achieving all this with a very low power and area budget.

A traditional approach to solving this issue is using a Harrison topology introduced in [3] and quickly optimised in [4]. However, problems persist: a) The pseudo resistors (2x back-to-back diodes) used for the feedback loop suffer from variability and drift, b) the sensing nodes of the amplifier (+ and - terminals) are effectively floating rendering them extremely sensitive to noise, charge injection etc. and therefore making it difficult to time multiplex (but see [5]) and c) power-gating the amplifier is difficult because of long amplifier settling times. Whilst DC-coupled approaches have also been proposed [6], the Harrison topology remains the most popular option.

There is thus a need for neural spike detectors that can work directly with the minute input signals normally fed into a Harrison amplifier, thus achieving a basic form of neural spike detection while obviating the need for pre-amplification.

According to an aspect of the invention, there is provided a detector for detecting neural spike signals. The detector comprises a core amplifier. The core amplifier comprises two current paths, each of the current paths integrating a current on a respective integrating node. Each current path comprises an input transistor receiving an analogue input signal and a tunable load configured to tune an offset voltage of the core amplifier. The tunable load may be a memristor, for example. The core amplifier further comprises a reset element that

resets the integrating nodes periodically. The detector further comprises a read out element that processes the integrated currents at the two integrating nodes.

The analogue input signals applied to the input transistors of the core amplifier modulate the currents flowing through each of the current paths with a high gain, thereby amplifying differences in the analogue input signals. The resistive state of the tunable loads (or memristors) can be programmed to finely tune the offset voltage of the core amplifier. This allows accurate setting of the difference in analogue input signals (and thereby the desired height of a neural spike) that is to be detected, making the detector highly flexible. The current that is modulated by the input transistors is integrated on the integrating nodes over time, thereby further amplifying differences in the input signals and blurring noise in the input signals. Current integration during operation of the detector also avoids DC paths to ground, thereby reducing power dissipation. Resetting the integrating nodes periodically allows the timing and duration of voltage spikes to be determined, making the detector suitable for basic detection of neural spikes. The reset period sets the sampling rate of the detector, which is preferably well below the duration of a neural spike, for example in the range from 10 – 20 kHz). The combination of current integration on the integrating nodes, tuning of the offset voltage by the tunable loads, resetting the integrating nodes periodically, and processing the integrated current using a read out element allows the duration of a tunable and minute input voltage difference to be accurately determined.

In an embodiment, the reset element is configured to reset the integrating nodes at a pre-set fixed frequency. This may allow for a simple and accurate determination of the duration of voltage spikes. In another embodiment, the reset element is configured to reset the integrating nodes at an adaptable frequency. This may allow for trading off resolution for power dissipation. The reset element may reset at a higher frequency, for example, when a voltage spike of interest is detected, and at a lower resolution when a voltage spike of interest is not detected. In another embodiment, the reset element is configured to reset the integrating nodes when the read out element indicates that the integrated currents at the two integrating nodes have been processed. This ensures that the read out element has enough time to process the voltage at the integrating nodes while minimizing the delay before the integrating nodes are reset.

In an embodiment, each current path of the core amplifier further comprises a cascoding transistor that is connected between the input transistor and the integrating node. The cascoding transistor effectively acts as a buffer between the input transistor and the integrating node, and prevents or at least reduces the effect of a variable charge and voltage at

the integrating node on the behavior of the input transistor. This reduces voltage fluctuations at the drains of the input transistors so as to reduce kickback effects of changing drain voltages on the gate voltages of the input transistors, and improves the stability of operation of the detector.

In a further embodiment, the core amplifier comprises a switchable current source that provides a current to each of the two current paths. In each current path, the input transistor is connected between the switchable current source and the cascoding transistor. The switchable current source and the cascoding transistor switch simultaneously. As the input transistor is connected between the current source and the cascoding transistor, it may be electrically isolated by simultaneously switching off (disconnecting) the current source and the cascoding transistor. Charges present at the source and drain terminal nodes of the input transistor may thus be trapped, and are prevented from being dumped to electrical ground. This reduces charge injection effects when the core amplifier is turned both off and on again, reducing the overall power dissipation of the detector and allowing faster operation due to lower activation times, as no power and time are wasted replenishing the trapped charges.

In a further embodiment, the read out element operates only when the voltage at one of the integrating nodes exceeds a threshold voltage. This prevents the read out element from trying to process the integrated current too early, for example when the voltage at the integrating nodes is too low to trigger an input transistor of the read out element. Operation of the detector may thus be more reliable and power dissipation of the read out element may be reduced.

In a further embodiment, the core amplifier comprises a plurality of pairs of current paths. Each pair of current paths may comprise or consist of a different one of a plurality of first current paths and a different one of a plurality of second current paths. Alternatively, each pair of current paths may comprise or consist of a different one of a plurality of first current paths, and a shared second current path, which is shared among all pairs of current paths. Each of the plurality of first current paths is configured to selectively connect and disconnect to and from one of the two integrating nodes, whereas each of the plurality of second current paths is configured to selectively connect and disconnect to and from the other of the two integrating nodes. Each current path comprises a respective input transistor. As such, a first pair of current paths may connect to the integrating nodes and integrate current on the integrating nodes during a first time interval (during which first time interval all other pairs may be disconnected from the integrating node), a subsequent pair may connect to the integrating nodes and integrate current on the integrating nodes during a subsequent time

interval (during which subsequent time interval all other pairs may be disconnected from the integrating node), etc. This allows the detector to detect spike signals in a plurality of different analogue inputs, each analogue input provided to an input transistor in a different pair of current paths.

In a further embodiment, each current path comprises a respective tunable load, i.e. a different tunable load is provided in each current path. Providing a different tuneable load in each current path allows the offset voltage in each pair of current paths to be adjusted separately, such that each pair of current paths may have a different offset voltage. This allows each pair of current paths to be used to detect spike signals of different magnitudes. For example, a first pair of current paths may be provided with a relatively low offset voltage to detect spike signals of relatively small magnitude, whereas a second pair of current paths may be provided with a relatively high offset voltage to detect spike signals of relatively large magnitude. A detector with such two pairs of current paths may thus be used to detect spike signals with varying magnitude in one analogue input signal, improving the detector's detection capabilities.

According to an alternative aspect of the invention, there is provided a neural spike recording system for recording neuronal activity. The neural spike recording system comprises the detector and a neurological sensor. The neurological sensor measures neuronal activity and outputs a corresponding analogue electrical signal. The analogue electrical signal is (directly) applied to one of the two input transistors of the detector. Such a neural spike recording system is suitable for recording neuronal activity while obviating the need for pre-amplification before processing of neural spike signals, thereby reducing the cost and power dissipation of recording neuronal activity.

According to a further alternative aspect of the invention, there is provided a method of using the detector. The method comprises the steps of: a) applying an analogue input signal to each of the two input transistors; b) supplying a current to the current paths and resetting the charge at the integrating nodes; c) after the charge at the integrating nodes has been reset, integrating the current flowing through each of the current paths on the integrating nodes; d) processing the voltage at the integrating nodes using the read out element; and e) performing steps b) to d) periodically.

According to a further alternative aspect of the invention, there is provided a method for detecting neural spike signals. The method comprises the steps of: a) supplying a current to two current paths, each current path comprising an input transistor and a tunable load; b) applying an analogue input signal to each of the two input transistors, thereby modulating the

current in a respective current path; c) integrating the current flowing through each of the current paths on a respective integrating node; d) after the current has been integrated on the integrating nodes, processing the voltage at the integrating nodes using a read out element; e) resetting the integrating nodes using a reset element; f) performing steps c) to e) periodically.

The invention will be more clearly understood from the following description, given by way of example only, with reference to the accompanying drawings, in which:

Figure 1 schematically depicts a typical neural spike recording system for processing data from a neurological event;

Figure 2 depicts a detector for detecting a neural spike signal in accordance with an embodiment; and

Figure 3 shows simulation data as an example of the operation of the detector of Figure 2.

The same references are used for similar features throughout the drawings. The features shown in the figures are not necessarily to scale and the size or arrangements depicted are not limiting. It will be understood that the figures may include optional features which are not essential to any embodiments. Furthermore, not all of the features are depicted in each figure and the figures may only show a few of the components relevant for a describing a particular feature.

A major issue facing the field of recording neural activity in the brain is the enormous amount of generated data. This data consists of voltage-time series representing the overall electrical activity in the vicinity of each recording electrode in the system, each voltage-time series being much akin to an oscilloscope trace. However, the useful information embedded within that signal merely consists of the timings and unique category IDs (or shapes) of each action potential (spike). This is a much lower bandwidth signal. This low bandwidth signal may be extracted by the neural spike recording system 100 of Figure 1.

Figure 1 depicts a typical single-unit neural activity monitoring system channel architecture as an example of a neural spike recording system 100 for recording neuronal activity. The system includes a neurological sensor 10 that may be used to take measurements of a neuron 5. The neurological sensor 10 may detect neurological events, such as firing of a neuron 5. Thus, the neurological sensor 10 may measure raw neuronal data based on a neural waveform at a particular location. A spike in the neural waveform during a neurological event may be caused by an action potential being generated by a neuron 5, which results in a sharp deviation from the baseline of the neural waveform. Each neuron 5 may have a characteristic neural spike form, allowing different neurons 5 to be

distinguished. The neurological sensor 10 outputs raw neuronal data as an electrical output which has a voltage, or as an analogue electrical signal. The output has a variation of voltage over time. The voltage of the output varies depending on the neural waveform, and spikes in the neural waveform lead to corresponding spikes in the voltage of the output. Thus there are large, sharp increases in the voltage of the output when a neurological event occurs. It is particularly beneficial to determine certain characteristics of these voltage spikes relating to the neurological event, such as the occurrence, timings, durations and unique category ID of the spikes. A unique category ID corresponds to a specific action potential activity of a specific neuron 5, which may be detected as a specific spike form or shape by the neurological sensor 10.

The output of the neurological sensor 10 is typically sent to an analogue front end, or signal processing circuitry 20. The signal processing circuitry 20 pre-processes the raw neuronal data, for example by applying amplification and filtering to the raw neuronal data. The pre-processed neuronal data may then be provided to a processing module 30, for example in real-time. The processing module 30 may isolate neural spike signals from the pre-processed neuronal data, so as to create a succession or stream of neural spike signals. The processing module 30 may also categorize each of the stream of neural spike signals, so as to attribute a unique category ID to each different characteristic neural spike signal. An output stage 40 may store and/or transmit the characteristics of each determined match. The output of the output stage 40 is thus a low bandwidth signal containing useful information extracted from the raw neuronal data. The output stage 40 may comprise a storage device, a telemetry and antenna module, another communication device or a wire or data connection to another device.

The neurological sensor 10 may be any sensor capable of detecting waveforms described above and capable of detecting events in the waveform. The neurological sensor 10 may comprise an electrode. The neurological sensor 10 may be used in various ways, for example, in vitro or in vivo. The neurological sensor 10 may store measurements. Alternatively, the measurements may be passed in real time (or with minor delay) to the signal processing circuitry 20 or may be stored in another device which can send the measurements to the signal processing circuitry 20 at a desired time. The neurological sensor 10 may be configured and used, as depicted in Figure 1, to detect and measure neurological changes.

Currently, the signal processing circuitry 20 is required to provide significant amplification before the processing module 30 can operate on the signal. However, when the

objective is to detect neural spikes, the input signals of interest are inherently sparse, and much energy is spent amplifying data points that are ultimately discarded. This makes the typical approach shown in Figure 1 inefficient and cost intensive.

The present invention aims to at least partly solve this problem by providing a basic form of spike detection that does not require pre-amplification, but operates directly on the neural spike signals generated by a neurological sensor.

Figure 2 schematically depicts an embodiment of a detector 50 that is configured to detect neural spike signals, such as signals with a voltage in the range from $10\mu\text{V}$ to 1mV . The detector 50 may operate directly on neural spike signals, without the need for pre-amplification. In the context of Figure 1, the detector 50 may be provided in place of the signal processing circuitry 20 and the processing module 30. The input of the detector 50 may be connected to the neurological sensor 10, and the output of the detector 50 may be connected to the output stage 40.

The detector 50 comprises a core amplifier 200 and a read out element 300. The output nodes or integrating nodes MIDA, MIDB of the core amplifier 200 are connected to the input nodes of the read out element 300, such that the read out element 300 is wrapped around the core amplifier 200. The read out element 300 processes the integrated currents (or the accumulated charge or the built-up voltage) at the two integrating nodes MIDA, MIDB.

The core amplifier comprises two current paths 210A, 210B, a current source 220 and a reset element 230. The current source 220 provides a current to each of the two current paths 210A, 210B. The two current paths 210A, 210B are electrically connected in parallel, such that the provided current is split between the two current paths 210A, 210B. The two current paths 210A, 210B may be two symmetric branches of the core amplifier 200, and may consist of the same components. The current paths 210A, 210B may electrically connect the current source 220 and the integrating nodes MIDA, MIDB. The components of the current paths 210A, 210B may be connected in series, as shown in Figure 2. The components of the current paths 210A, 210B modulate the current flowing through the current paths 210A, 210B. The current paths 210A, 210B may integrate the current on a respective integrating node MIDA, MIDB, such that a charge accumulates and a voltage builds up on the integrating nodes MIDA, MIDB over time. The reset element 230 resets the integrating nodes MIDA, MIDB periodically, so as to periodically remove the accumulated charge and the built-up voltage from the integrating nodes MIDA, MIDB.

Each current path 210A, 210B comprises a respective input transistor M1, M3. An analogue input signal may be applied at a respective input node INA, INB of each of the

input transistors M1, M3, such that each input transistor M1, M3 may receive an analogue input signal. Variations in the analogue input signals modulate the current flow through the respective input transistor M1, M3 in each of the two current paths 210A, 210B. Differences in the analogue input signals lead to different effective drain source resistances of the input transistors M1, M3, and (in the absence of any other components) to different current flows in the current paths 210A, 210B to the integrating nodes MIDA, MIDB.

Each current path 210A, 210B further comprises a respective tunable load R2, R3 or tunable resistor R2, R3. The tunable load R2, R3 may be a memristor. The resistive value of the tunable load is adjustable or programmable. This allows tuning of the offset voltage of the core amplifier 200. The offset voltage of the core amplifier 200 is the difference in the analogue input signals applied to the input nodes INA, INB that leads to a symmetric or equal output of the core amplifier. Tuning the offset voltage thus allows setting the voltage difference between the analogue input signals applied to the input nodes INA, INB that leads to the same current flow in each of the current paths 210A, 210B, and ultimately to an equal accumulation of charge and build-up of voltage on the integrating nodes MIDA, MIDB.

In use, a fixed, constant voltage signal, such as a reference electrode voltage, may be applied at the input node INA, whereas an analogue voltage signal comprising neural spikes (for example a signal outputted by the neurological sensor 10) may be applied at the input node INB. Tuning the offset voltage by means of the tunable loads R2, R3 allows setting the voltage difference between the neural spike signal and the constant voltage signal that leads to an equal accumulation of charge or build-up of voltage on the two integrating nodes MIDA, MIDB. A neural spike may be detected as such when the integrated current on integrating node MIDB is equal to or exceeds the integrated current on integrating node MIDA. The tunable loads R2, R3 thus enable accurate tuning of the minimum height of a neural spike that is to be detected.

Each current path 210A, 210B may further comprise a respective cascoding transistor M24, M25. Each cascoding transistor M24, M25 may be connected between the input transistor M1, M3 and the integrating node MIDA, MIDB in each current path 210A, 210B. The cascoding transistors M24, M25 may thus act as a buffer between the input transistors M24, M25 and the integrating nodes MIDA, MIDB. The cascoding transistors M24, M25 may ensure that the charge and voltage on the integrating nodes MIDA, MIDB does not influence the behavior of the input transistors M1, M3, by preventing the drain voltages of the input transistors M1, M3 from fluctuating excessively. The cascoding transistors M24,

M25 further may be designed to prevent negative effects of capacitive coupling between the integrating nodes MIDA, MIDB and the input nodes INA, INB.

The core amplifier 200 may further comprise capacitors C1, C2. A respective capacitor C1, C2 may be connected to each of the integrating nodes MIDA, MIDB, so as to contribute to the capacitance at the integrating nodes MIDA, MIDB. In the embodiment of Figure 2, the capacitance at the integrating nodes MIDA, MIDB may also be affected by parasitic capacitances at transistors M7, M8 and M2, M6, and M17, M19, M22, M23. These parasitic capacitances may be large enough to obviate the need for capacitors C1, C2. The capacitors C1, C2 are thus optional. The capacitance at the integrating nodes MIDA, MIDB affects the accumulation of charge on the integrating nodes MIDA, MIDB. The capacitors C1, C2 may be designed to allow control of the current integration rate (or charge accumulation, or voltage build-up) on the integrating nodes MIDA, MIDB.

The reset element 230 resets the integrating nodes MIDA, MIDB periodically, so as to periodically remove the charge and the voltage at the integrating nodes MIDA, MIDB. In the embodiment of Figure 2, the reset element 230 comprises two reset transistors M2, M6, each reset transistor M2, M6 connecting a respective integrating node MIDA, MIDB to electrical ground. However, the reset element 230 may be any other device suitable for resetting the integrating nodes MIDA, MIDB periodically. A reset clock signal clk_rst may be applied to the reset element 230, thereby periodically switching the reset element 230. The reset clock signal clk_rst may have a fixed, pre-set frequency. Alternatively, the reset clock signal clk_rst may be adaptable. The reset element 230 may be opened, thereby disconnecting the integrating nodes MIDA, MIDB from electrical ground, such that current is integrated on the integrating nodes MIDA, MIDB. The voltage difference arising between the integrating nodes MIDA and MIDB is given by $\Delta V = \Delta i \cdot t_{\text{int}} / C_{\text{int}}$, where t_{int} and C_{int} are the integration time and the capacitance at the integrating nodes MIDA, MIDB respectively. The integration time t_{int} thus contributes to the gain of the core amplifier, by affecting the voltage difference at the integrating nodes MIDA, MIDB that is a result of the integration of the currents flowing through the current paths 210A, 210B. This voltage difference ΔV may be processed by the read out element 300. The reset element 230 may be closed, thereby connecting the integrating nodes MIDA, MIDB to electrical ground. This resets the integrating nodes MIDA, MIDB by at least partially, or fully, removing the current integrated on the integrating nodes MIDA, MIDB during the time that the reset element 230 was open.

The current source 220 provides a current to each of the two current paths 210A, 210B. The current source 220 may be a switchable current source 220, and switch between

an on state and an off state. In the embodiment of Figure 2, the current source 220 comprises transistors M4, M5, M18, M16 and resistor R1. However, any current source 220 suitable for providing current to each of the current paths 210A, 210B may be used.

The input transistors M1, M3 may be connected between the current source 220 and the cascoding transistors M24, M25. The current source 220 and the cascoding transistors M24, M25 may switch simultaneously. A current source clock signal clk_ana may be applied at the current source 220, so as to switch the current source 220 between an on state and an off state. A cascoding clock signal clk_anabar may be applied at the cascoding transistors M24, M25, so as to switch the cascoding transistors M24, M25 between a closed (activated) state and an open (deactivated) state. The current source clock signal clk_ana and the cascoding clock signal clk_anabar may switch simultaneously and be in anti-phase (as in the embodiment of Figure 2) or in phase. The cascoding clock signal clk_anabar may alternate between a high voltage V_{dd} and a pre-determined intermediate voltage. Turning the current source 220 off at the same time as opening the cascoding transistors M24, M25 isolates the input transistors M1, M3, thereby trapping any residual charges at the input transistors M1, M3 when the core amplifier 200 is turned off. This mitigates charge injection effects when the core amplifier 200 is turned on again.

In the detector of Figure 2, the entire current source 220 is switched by the current source clock signal clk_ana . Turning the entire current source 220 off reduces the power dissipation in the resistor R1 and in the transistors M5, M16 and M18. In an alternative embodiment (not shown), instead of turning the entire current source 220 off, the current source 220 may be disconnected from the current paths 210A, 210B by using a further switch transistor. This obviates the need to switch the entire current source 220 between an off state and an on state, thereby reducing the time and power spent charging the gates of the transistors M4, M5.

The read out element 300 may comprise a comparator, specifically a dynamic latched comparator (DLC), as shown in Figure 2. The DLC outputs a binary digital pulse signal that can be easily and reliably processed and analysed by any subsequent device, such as the output stage 40. The DLC of the embodiment of Figure 2 comprises transistors M7-M15 and M26. Alternatively, the read out element 300 may comprise any other device suitable for processing the integrated current (or the accumulated charge, or the built-up voltage) at the integrating nodes MIDA, MIDB. In the embodiment of Figure 2, the comparator (specifically the DLC) compares the integrated currents at the two integrating nodes MIDA,

MIDB. This comparison may be made before the reset element 230 resets the integrating nodes MIDA, MIDB.

The read out element 300 may be triggered when the voltage at one or both of the integrating nodes MIDA, MIDB exceeds a threshold voltage. This guarantees that by the time the comparison of the DLC is triggered, enough voltage has accumulated on the integrating nodes MIDA, MIDB to drive the DLC input transistors M7, M8 of the DLC. A trigger signal clk may be applied to the DLC. The DLC may be designed to make a comparison of the voltage at the integrating nodes MIDA, MIDB at the rising edge of the trigger signal clk. The trigger signal clk may be generated only when the voltage at one of the integrating nodes MIDA, MIDB exceeds the threshold voltage. For this purpose, the read out element 300 may comprise a trigger generating circuit 310 for triggering the trigger signal clk. The trigger signal clk may be triggered based on the voltage at only one of the integrating nodes MIDA, MIDB because the difference in voltages between the integrating nodes MIDA, MIDB is expected to be small.

The current integrated by integrating node MIDB may be affected, for example, by a signal comprising voltage spikes (such as neural spikes) that is applied to input node INB. The current integrated by integrating node MIDA may be affected, for example, by a constant reference signal that is applied to input node INA. The trigger signal clk may be triggered based on the voltage on the integrating node MIDB that depends on an input signal comprising voltage spikes. The integrating node MIDB is expected to have a higher voltage than the integrating node MIDA when a voltage spike is applied at the input node INB. Using the voltage at the integrating node MIDB to generate the trigger signal clk may thus ensure that the read out element 300 is able to process the voltage at the integrating node MIDB, even if the voltage at the integrating node MIDA is too low to be processed by the read out element 300. Alternatively, the trigger signal clk may be triggered based on the voltage on the integrating node MIDA that depends on a constant reference signal, so based on the integrating node MIDA that integrates a pre-determined current. This may be preferable in situations in which the read out element 300 is an analogue amplifier, for example, and a difference between the voltages on the integrating nodes MIDA, MIDB is to be determined.

The threshold voltage may be pre-set and/or may be adjustable. The clock generating circuit 310 of the embodiment of Figure 2 comprises a cascade of two inverters M17, M19 and M20, M21 that trigger the trigger signal clk when the voltage at the integrating node MIDA exceeds the threshold voltage. The inverter M22, M23 in the embodiment of Figure 2

is provided for the purpose of maintaining a uniform capacitive load at each of the integrating nodes MIDA, MIDB. The inverter M22, M23 thus mirrors the inverter M17, M19. In the embodiment of Figure 2, the threshold voltage corresponds to the switching point of inverter M17, M19, and may be set by appropriately selecting the transistors M17 and M19, or by introducing memristors (not shown) in the inverter M17, M19.

An example of the operation of the detector 50 of Figure 2 is illustrated in Figure 3. Figure 3a shows input/output characteristic of the detector as the analogue input voltage at input node INA is kept constant (at 1V), and as the analogue input voltage applied to input node INB is slowly swept between 0.9999V and 1.0001V over 2 ms, as shown in the first graph of Figure 3a. The second graph of Figure 3a shows the output of the DLC, sampled every 16 μ s. The voltage at output node OUTB is high only when the voltage applied to input node INB exceeds the voltage applied to input node INA. The detector 50 thus can reliably detect voltage spikes of 10s to 100s of μ V, such as neural spikes outputted by the neurological sensor 10.

The first graph of Figure 3b shows an example of one cycle of operation of the detector 50. The cycle of operation comprises a first phase (i), a second phase (ii), a third phase (iii) and an off mode (rst). Before the cycle of operation starts, the resistive value of the tunable loads R2, R3 of the detector 50 may be tuned or programmed. This sets the minimum height of the neural spike signal, or comparable minute signal, that is to be detected by the detector. An analogue input signal is applied to each of the two input transistors M1, M3 throughout the cycle of operation. For example, a signal comprising a neural spike signal may be applied to one of the input nodes INB, and a constant reference signal may be applied to the other of the input nodes INA.

In the first phase (i), the integrating nodes MIDA, MIDB are reset. As shown in Figure 3b, clk_rst and clk_ana go high and clk_anabar goes low. This respectively causes the reset element 230 to reset the integrating nodes MIDA, MIDB, the current source 220 to supply a current to the current paths 210A, 210B, and the cascoding transistors M24, M25 to be activated or opened. This may ensure that the charge in the core amplifier is dumped to electrical ground, so as to remove any charges resulting from initial charge injection as the core amplifier 200 is activated. Preferably, the first phase (i) is kept long enough to ensure that charges initially injected are reliably removed from the core amplifier 200, but short enough to limit the power dissipation of the core amplifier 200 during start-up. In the example of Figure 3, the first phase (i) lasts about 0.2 μ s.

The second phase (ii) commences after the integrating nodes MIDA, MIDB have been reset, such that electrical charges at the integrating nodes MIDA, MIDB have been removed. As shown in Figure 3b, clk_rst goes low at the beginning of the second phase. This causes the reset element 230 to open or deactivate, so as to disconnect the integrating nodes MIDA, MIDB from electrical ground. The current source 220 continues to supply current to the two current paths 210A, 210B. The current in each current path 210A, 210B is modulated by the analogue input signals applied to the input nodes INA, INB. The current flowing through each of the current paths 210A, 210B is integrated on the integrating nodes MIDA, MIDB. The duration of the second phase (ii) may be chosen such that the voltage built up at the integrating nodes MIDA, MIDB is sufficient to trigger the read out element 300, for example the clock generating circuit 310 of the read out element 300 of the detector 50 of Figure 2. The duration of the second phase (ii) may, alternatively or additionally, be chosen such that the voltages built up at the two integrating nodes MIDA, MIDB are sufficient to allow the read out element 300 to process, for example to compare, the built-up voltages. The duration of the second phase (ii) may not be fixed. With reference to the embodiment of Figure 2, the second phase (ii) may end when the voltage built up at the integrating nodes MIDA, MIDB exceeds the threshold voltage (the switching voltage of the inverter M17, M19).

The third phase (iii) starts after the second phase (ii). At the beginning of the third phase (iii), the trigger signal clk is activated. The third phase (iii) may start, for example, only when the voltage at an integrating node MIDA, MIDB exceeds a threshold voltage. This triggers the read out circuit 300, such as the DLC of Figure 2. During the third phase (iii), the integrated current (or accumulated charge, or built-up voltage) is processed by the read out circuit 300. For example, the DLC of the detector 50 of Figure 2 may compare the voltages at the integrating nodes. Once the DCL has committed to a decision, the third phase (iii) may end and the off mode (rst) may commence.

In the off mode (rst) the input transistors M1, M3 may be isolated, thereby trapping any charges across the gate-source and gate-drain capacitances of the input transistors M1, M3. At the beginning of the off mode (rst), clk_ana goes low and clk_anabar goes high, simultaneously stopping the current supply to the current paths 210A, 210B, by turning off or disconnecting the current source 220, and turning off (or opening) the cascoding transistors M24, M25. Charges may distribute between the source and the drain of the input transistors M1, M3, but the overall potential difference across the gate of the input transistors M1, M3 remains practically constant. This mitigates charge injection effects both when the core amplifier 200 is deactivated and when the core amplifier is activated again (i.e. during both

on/off and off/on transitions). The core amplifier 200 thus may simultaneously remain completely off and charges may remain trapped until the first phase (i) starts again. When the first phase (i) starts again, the charges trapped on the input transistors M1, M3 help the core amplifier 200 to maintain its previous state and reactivate the potential gradient from the current source 220 to electrical ground. This may reduce the duration of the first phase (i), thus reducing the power dissipation of the detector 50.

The cycle of operation described above may be repeated periodically at a fixed pre-set frequency. The pre-set frequency may be greater than 1kHz, and preferably greater than 50 kHz. This may allow the detector 50 to process a single neural spike signal, which typically has a length of several milliseconds, multiple times. By counting the times the neural spike signal is detected by the detector 50, the duration of the neural spike signal can be calculated. Using a higher frequency allows the duration of the neural spike signal to be determined more accurately. Using higher frequencies for sampling may also allow down-sampling by combining neighbouring samples to obtain a smaller number of overall samples. This may average out and reduce the noise of the samples further.

The detector 50 shown in Figure 2 is only one possible implementation of the present invention. In the following, several variations of the detector 50 are disclosed. The present invention is not limited to the embodiment of Figure 2 or the variations described hereinafter. The scope of the invention is defined in the claims.

In the example of Figure 3, the cycle of operation is repeated periodically at a fixed, pre-set frequency. Alternatively, the cycle of operation may be repeated periodically at an adaptable frequency, such that the reset element resets the integrating nodes at an adaptable frequency. The frequency of operation may be adapted, for example, by reducing the duration of the off mode (rst) or even excluding the off mode (rst) from the cycle of operation, so as to achieve the fastest possible frequency of operation. For example, before a voltage spike (such as a neural spike) is detected, the reset element 230 may reset the integrating nodes MIDA, MIDB at a lower frequency (for example at 5kHz), so as to reduce the power consumption of the detector 50. When a voltage spike is first detected by the detector 50, the frequency at which the reset element 230 resets the integrating nodes MIDA, MIDB may be increased to a higher frequency (for example to 10-20kHz), so as to improve the resolution of the detector 50 for the duration of the voltage spike. The detector 50 may operate at the higher frequency for a predetermined time after first detecting a voltage spike, or may operate at the higher frequency until a voltage spike is no longer detected. Operating the detector 50 at an adaptable frequency is preferable in particular when using a read out

element 300 comprising an analogue amplifier, which allows the voltage differences over time between the integrating nodes MIDA, MIDB, and therefore the shape of the voltage spike, to be determined.

Alternatively, the first phase (i), the second phase (ii), the third phase (iii) and the off mode (rst) shown in Figure 3 may be triggered automatically by completion of a preceding phase, and not be triggered based on the clock signals `clk_ana`, `clk_anabar` and `clk_rst`. For example, the third phase (iii) may start when the voltage at an integrating node MIDA, MIDB exceeds a threshold voltage. The read out element 300 may process the voltage at the integrating nodes MIDA, MIDB during the third phase (iii), and the off mode (rst) may start when this processing has been completed. The off mode (rst) may commence, for example, when the read out element 300 indicates that processing is complete or after a first pre-set time delay after starting the third phase (iii). The off mode (rst) may end and the first phase (i) may start after a second time delay, which may be a pre-set fixed time delay or an adaptable time delay (for example dependent on whether a voltage spike is detected, as described above in relation to the adaptable frequency). Alternatively, the off mode (rst) may be dispensed with to achieve the fastest possible sampling frequency. The first phase (i) may end and the second phase (ii) may start after a third time delay, for example when the integrating nodes MIDA, MIDB have been reset (when the charge on the integrating nodes is below a threshold) or after a fixed pre-set time. Finally, the third phase (iii) may start again when the voltage at the integrating nodes MIDA, MIDB exceeds the threshold voltage. The different phases of the cycle of operation of the detector 50 may thus be performed in a fixed sequence, but not be dependent on fixed or adaptable clock signals.

In an alternative embodiment, a control circuit may switch between the different mechanisms for starting the phases of the cycle of operation shown in Figure 3. For example, the detector may operate based on the clock signals `clk_ana`, `clk_anabar` and `clk_rst` when no voltage spike is detected, and may trigger phases (i)-(iii) (and optionally the off mode (rst)) automatically upon completion of a preceding phase when a voltage spike is detected. The embodiment of Figure 2 shows a clock generating circuit 310 and a DLC as one example of a read out element 300. However, the clock generating circuit 310 of the detector 50 of Figure 2 is optional. The read out element 300 may, alternatively, be triggered by a fixed clock signal, such that the read out element 300 processes the integrated currents at the two integrating nodes MIDA, MIDB periodically at a fixed read-out frequency. In such a case, the read-out frequency may be the same as, or a multiple of, the pre-set frequency at which for example, the current source 220, the cascoding transistors M23, M24, and the reset

element 230 of the core amplifier 200 are switched. The read out element 300 may thus process the integrated current at the integrating nodes MIDA, MIDB once (or multiple times) per cycle of operation. The duration of the second phase (ii) of the cycle of operation may thus be fixed. Applying a fixed clock signal, and obviating the need for the clock generating circuit 310 of Figure 2, may improve the sharpness of signal transitions and reduce power dissipation of the read out element 300.

The read out element 300 may comprise, in addition or as an alternative to the DLC, an analogue comparator (such as a differential amplifier) or an analogue amplifier. Such an analogue element may provide an indication of the absolute voltage difference between the integrating nodes MIDA, MIDB (instead of providing a binary comparison as the DLC), and so a measure of the height of a spike in an analogue input signal, such as a neural spike signal, may be provided. By processing a single neural spike signal multiple times, the height of the neural spike signal over time, and so the shape of a neural spike signal, may be determined. This allows identification not only of the occurrence and duration of a neural spike signal, but of the unique category ID of a neural spike signal, and so enables neural spike sorting in addition to neural spike detection.

In a further variation (not shown), the clock generating circuit 310 comprises a fuzzy logic inverter. The fuzzy logic inverter comprises a CMOS inverter and a tunable load (such as a memristor) provided on a current path connected to an output node of the fuzzy logic inverter. For example, the inverters M17, M19 and M20, M21 of the clock generating circuit 310 may be connected in series with tunable loads, such as memristors. The tunable loads may be connected in series with the drain or the source of the transistors M17, M19, M20, M21. As such, one or both of the inverters M17, M19 and M20, M21 may be fuzzy logic inverters. The tunable load may tune of the threshold voltage above which the clock signal clk is generated, improving the flexibility of the detector 50.

The current source 220 may be any device suitable for providing current to the two current paths 210A, 210B, and is not limited to the specific embodiment of Figure 2. In a variation, the resistor R1 of the current source 220 of the detector of Figure 2 may be replaced with a tunable load R1, such as a memristor R1. The current source 220 may comprise a tunable load configured to tune the current source 220, thereby allowing a trade-off of speed and instantaneous power dissipation of the current source 220. This improves the flexibility of the current source 220.

In the embodiment shown in Figure 2, the tunable load R2, R3 (memristor R2, R3) is connected between the cascoding transistor M24, M25 and the integrating node MIDA,

MIDB. In an alternative embodiment, the tunable loads R2, R3 may be connected between the input transistors M1, M3 and the cascoding transistors M24, M25. In a further alternative embodiment, the tunable loads R2, R3 may be connected between the current source 220 and the input transistors M1, M3. In each of these variations, the tunable loads R2, R3 are connected in the current paths 210A, 210B, thereby affecting the resistance of each current path 210A, 210B and allowing tuning of the offset voltage of the core amplifier 200.

Dependent on the location of the tunable loads R2, R3 in the current paths, the effect of the tunable loads R2, R3 on the offset voltage of the core amplifier 200 may vary. For example, changing the resistance of a memristor R2, R3 located between the cascoding transistor M24, M25 and the integrating node MIDA, MIDB by 100 k Ω might adjust the offset voltage by 100 μ V. The same adjustment of 100 μ V of the offset voltage might be achieved by changing the resistance of a memristor R2, R3 located between the cascoding transistor M24, M25 and the input transistor M1, M3 by only 10 k Ω . The sensitivity of the offset voltage on the resistances of the tunable loads R2, R3 may thus depend on the location of the tunable loads R2, R3 in the current paths 210A, 210B. Multiple memristors may be connected in each of the current paths 210A, 210B. For example, each current path 210A, 210B may comprise two memristors. The two memristors can be provided in the same location (i.e. directly in series or in parallel) or in different locations in the current paths 210A, 210B. The first memristor may coarsely tune the offset voltage of the core amplifier 200 over a wide voltage range. The second memristors may finely tune the offset voltage of the core amplifier 200 over a narrow voltage range. This provides a large range of offset voltage tuning (using the coarsely tunable memristor) without sacrificing the accuracy of such tuning (which is achieved using the finely tunable memristor). This may be particularly useful to compensate for component (transistor) mismatch between the two current paths 210A, 210B, which may necessitate comparably large offset voltage correction. The first memristors and the second memristors may be different types of memristors to respectively achieve coarse and fine tuning of the offset voltage. Alternatively, the first memristors and the second memristors may be of the same type, but be provided in different locations in the current paths 210A, 210B.

Connecting multiple memristors directly in series at the same location in the current paths 210A, 210B may provide additional flexibility in tuning the offset voltage of the core amplifier. Memristors typically have a non-linear current-voltage characteristic, so the effective static resistance of a memristor depends on the voltage applied across its terminals. For example, a memristor exhibiting a resistance of 10 k Ω when a voltage of 1V is applied to

it may exhibit a resistance of 100 k Ω when a voltage of 0.5 V is applied to it. Connecting two such memristors in series (such that the voltage of 1V is split between the two memristors) thus may lead to an effective resistance of 200 k Ω . The non-linear current-voltage characteristics of memristors thus allow a high flexibility in controlling the offset voltage by combining multiple memristors in series. The reset element 230 of the detector 50 of Figure 2 comprises two transistors M2, M6. The reset element 230 may be closed completely to reset the integrating nodes MIDA, MIDB, and opened completely to allow integration of current on the integrating nodes MIDA, MIDB. The integrating nodes MIDA, MIDB may thus either be connected to or disconnected from electrical ground. Alternatively, core amplifier 200 may be configured such that current is allowed to continuously leak from each of the integrating nodes MIDA, MIDB. This allows continuous operation of the detector 50, as opposed to the integrate/reset cycle shown in Figure 3. Continuously leaking current from the integrating nodes MIDA, MIDB may be achieved, for example, by keeping the reset element 230 semi-open at all times. This allows the integrating nodes MIDA, MIDB to act as a leaky integrator, which can effectively result in low-pass filtering of the analogue input signals applied to the input nodes INA, INB.

Alternatively, memristors may replace, or be connected in parallel with, the transistors M2, M6 of the reset element 230 to allow continuous operation. When transistors M2, M6 are connected in parallel with memristors, control of the leakage current is enabled both by appropriately tuning the memristors, and by switching of the transistors M2, M6 using the reset clock signal `clk_rst`. The reset element 230 is preferably configured such that the leakage current substantially balances the current supplied to the integrating nodes MIDA, MIDB during one cycle of operation.

In embodiments in which current is allowed to continuously leak from the integrating nodes MIDA, MIDB, the tunable load R2, R3 may also be provided between the integrating node MIDA, MIDB and electrical ground in each current path 210A, 210B to tune the offset voltage of the core amplifier 200. For example, the tunable load R2, R3 may be provided between the transistors M2, M6 of the reset element 230 and electrical ground, or between the integrating nodes MIDA, MIDB and the transistors M2, M6 of the reset element 300.

Simulations were performed on the detector 50 of Figure 2, using LTSPICE with TSMC's 0.35 micron MOSIS models. The detector 50 was simulated in transient mode to confirm functionality and assess performance throughout the full cycle of operation. Furthermore, in order to understand the effect of circuitry imperfections, controlled mismatch

was added at strategically chosen points in order to discover and assess any specific sensitivities of the design.

Figure 3 show transient analysis results. As shown in Figure 3a, for input differential voltages with common mode about 1V and maximum excursion $\pm 100\mu\text{V}$, the nominally operating detector is capable of differentiating between $V_A > V_B$ and $V_A < V_B$. Figure 3b shows the detailed function of the detector 50 throughout an entire cycle of operation, illustrating: i) clock behaviour, ii) power dissipation profile core amplifier clocked comparator and sum total, but excluding clock driving costs), iii) input voltages, iv) node voltages within the core amplifier evidencing the relative stability of voltages at the drains of the input differential pair throughout and v) output voltage evolution. The precise sequence of events during critical second and third phases (ii) and (iii) can be observed: `clk_rst` drops, integration starts on the integrating node MIDB, `clk` is triggered high and the DLC makes a decision by separating OUTA and OUTB. Additionally, Figure 3b shows that: i) In the beginning of the first phase (i) it takes some time for the core amplifier 200 to reach steady state, but subsequently there is no reason to keep `clk_rst` high; integration may commence safely. ii) The power dissipation profile is a result of a stable power draw by the core amplifier 200 dominating phase (i) and the DLC ‘twin peak’ dissipation indicating the cycle of DLC activation (1st peak), race condition (inter-peak plateau) and race resolution where the positive feedback in the amplifier commits the outputs 2nd peak).

Mismatch analysis has been performed in order to have a preliminary understanding of how practical non-idealities will affect operation. The components of the detector 50 of Figure 2 have been altered by introducing very targeted W and L value alterations at key transistor pairs. The influence of these changes on whole-system offset voltage was then assessed as summarised in table 1. The same approach was used to assess the influence memristor resistance values summarised in table 2. Results indicate that mismatch in the DLC input transistors M7, M8 and in the cascode transistors M24, M25 has the most severe effects on operation. This is expected since the DLC input transistors M7, M8 determine the DLC’s own offset voltage and the cascode transistors M24, M25 are small and play a key role in determining the currents in the current paths 210A, 210B. To mitigate the mismatch effect (in exchange for higher parasitic capacitance), larger cascode transistors M24, M25 may be used. The large size of the input transistors M1, M3 and the inactivity of the reset element M2, M6 during the critical integration phase render mismatch effects at these devices less significant. Similarly, results indicate that memristive devices capable of achieving even modest on/off ratios (here merely $\times 2.5$) can trim the offset voltage of the whole system very

finely (especially if they match the state resolution achieved in [8]) over a range of approximately 200V.

	M2		M7		M25		M3	
	(L/W)	V_{os}	(L/W)	V_{os}	(L/W)	V_{os}	(L/W)	V_{os}
Nom.	0.35/1.0	0	1.0/8.0	0	0.35/1.0	0	1.0/800	0
Test 1	0.40/1.0	-30	1.005/8	+45	0.36/1.0	+50	1.01/800	+30
Test 2	0.45/1.0	-50	1.01/8	+85	0.34/1.0	-20	1.02/800	+50
Test 3	0.35/0.9	-50	0.99/8	-75	0.33/1.0	-20	0.98/800	-50
Test 4	-	-	1.0/7.65	-15	0.35/1.05	-60	1.0/802	-95
Test 5	-	-	1.0/7.0	-25	0.35/0.95	+70	1.0/801	-45
Test 6	-	-	-	-	-	-	1.0/799	+50

Table 1: Mismatch exploration. Sizings in μm , V_{os} in μV . Nom. = nominal. Results taken with slightly modified detector 50 of Figure 2 (M26 missing).

$R_{\text{left}}/R_{\text{right}}$	50k	75k	100k	125k
50k	0 μV	-25 μV	-60 μV	-90 μV
75k	+30 μV	0 μV	-30 μV	-65 μV
100k	+60 μV	+35 μV	0 μV	-30 μV
125k	+95 μV	+65 μV	+35 μV	0 μV

Table 2: Core amplifier offset voltage vs memristive device resistive states. 5 μV resolution. Results taken with slightly modified detector 50 of Figure 2 (M26 missing).

In an alternative embodiment to the detector 50 depicted in Figure 2, the integrating nodes MIDA, MIDB are connected to a plurality of pairs of current paths 210A, 210B. Each pair of current paths 210A, 210B may comprise a first current path 210B configured to integrate current on the first integrating node MIDB and a second current path 210A configured to integrate current on the second integrating node MIDA. Each pair of current paths 210A, 210B may be formed of any configuration of the two current paths 210A, 210B described in relation to Figure 2. Preferably, each pair of current paths 210A, 210B comprises identical or corresponding components.

Each current path 210A, 210B of each pair of current paths 210A, 210B comprises a respective (so non-shared) input transistor M1, M3, a respective (so non-shared) tunable load R2, R3 and a respective (so non-shared) cascoding transistor M24, M25, as described in relation to the Figure 2 embodiment. Put another way, different input transistors M1, M3, tunable loads R2, R3 and cascoding transistors M24, M25 may be provided in each current path. Compared to the embodiment shown in Figure 2, a plurality of first current paths 210B may be connected in parallel to the first integrating node MIDB, and a plurality of second current paths 210A may be connected in parallel to the second integrating node MIDA. A

plurality of tunable loads R2, R3 are thus connected to each integrating node MIDA, MIDB, which may increase the capacitance on the integrating nodes MIDA, MIDB, thus obviating the need for separate capacitors C1, C2. Each pair of current paths 210A, 210B may be configured to selectively connect to and disconnect from the integrating nodes MIDA, MIDB, for example by being interrupted. The reset element 230 and the read out element 300 may be shared, for example time-shared, by each of the plurality of pairs of current paths 210A, 210B, i.e. only a single common reset element 230 and a single common read out element 300 may be provided.

The current source 220 may or may not be shared, for example time-shared, by each of the plurality of pairs of current paths 210A, 210B. If the current source 220 is not shared by all pairs of current paths 210A, 210B, a plurality of current sources 220 may be provided, each configured to provide current to one or more of the plurality of pairs of current paths 210A, 210B. This improves the capability of the detector 50 to stop the supply of current to each pair of current paths 210A, 210B separately, thus improving the capability of the detector 50 to fully isolate each pair of current paths 210A, 210B from the integrating nodes MIDA, MIDB when appropriate, as described further below. If the current source 220 is shared by all pairs, a single common current source 220 may be provided, which is configured to provide current to all of the current paths 210A, 210B. This reduces the size and cost of the detector 50.

The plurality of pairs of current paths 210A, 210B may use the common, shared circuit elements (for example the integrating nodes MIDA, MIDB, the reset element 230, the read out element 300, and optionally the current source 220) in a time-shared manner. For example, the plurality of pairs of current paths 210A, 210B may use the common, shared circuit elements sequentially, such that at any one time at most one of the pairs of current paths 210A, 210B is used to integrate current on the integrating nodes MIDA, MIDB. For example, with reference to Figure 3, the shared circuit elements and a first pair of current paths 210A, 210B may cycle through each phase (e.g. the first phase (i), second phase (ii), third phase (iii) and off mode (rst)) of the operation cycle in a first time interval. During this first time interval, all of the other pairs of current paths 210A, 210B remain disconnected from the integrating nodes MIDA, MIDB (i.e. are interrupted) at least during the second phase (ii), the third phase (iii) and the off mode (rst). During the first phase (i) of the first time interval, all of the other pairs of current paths 210A, 210B may be connected to or disconnected from the integrating nodes MIDA, MIDB.

For example, when each pair of current paths 210A, 210B comprises respective (i.e. not shared) cascoding transistors M24, M25, then the respective signal `clk_anabar` applied to the cascoding transistors M24, M25 of all other pairs of current paths 210A, 210B may remain low (as in the off mode (rst)) at least during the second phase (ii), third phase (iii) and off mode (rst). During the first phase (i), the respective signal `clk_anabar` may remain low or switch to high. If each current path 210A, 210B is provided with current from a different respective current source 220, then the signal `clk_ana` applied to the current source 220 of all other pairs of current paths 210A, 210B may remain high (as in the off mode (rst)) at least during the second phase (ii), third phase (iii) and off mode (rst), and may be high or low during the first phase (i).

Alternatively, separate switching elements (not shown) may be provided to isolate (i.e. interrupt) all of the other pairs of current paths 210A, 210B from the integrating nodes MIDA, MIDB at least during the second phase (ii), third phase (iii) and off mode (rst) of the first time interval. Such separate switching elements are preferably provided between the tunable loads R2, R3 and the integrating nodes MIDA, MIDB, or between the cascoding transistors M24, M25 and the tunable loads R2, R3, or between the input transistors M1, M3 and the cascoding transistors M24, M25, or between the current source 220 and the input transistors M1, M3, or at the input nodes INA, INB of the input transistors M1, M3 (to allow M1, M3 to be selectively closed so as to interrupt the respective current paths 210A, 210B).

After (for example immediately after) the first time interval, during a subsequent second time interval, a second pair of current paths 210A, 210B and the shared circuit elements may cycle through the phases of the operation cycle described in relation to Figure 3, while all other pairs of current paths 210A, 210B remain disconnected from the integrating nodes MIDA, MIDB at least during the second phase (ii), the third phase (iii) and the off mode (rst). In subsequent time intervals, other ones of the plurality of pairs of current paths 210A, 210B may undergo the operation cycle in the same manner. Optionally, the sequence in which the pairs of current paths 210A, 210B are used may be altered, for example in dependence of a detected spike signal. For example, if the detector 50 detects a spike signal while using one particular pair of current paths 210A, 210B in any given time interval, then the detector 50 may use this pair of current paths 210A, 210B in one or more immediately subsequent time intervals, for example until the spike signal is no longer detected. This allows more sampling points for each detected spike signal to be generated, thus improving the accuracy of determining the length of the detected spike signal.

The detector 50 of the alternative embodiment may be used to detect spike signals in a plurality of different channels, i.e. in analogue signals originating from different neurological sensors 10. The input node INB of each of the plurality of pairs of current paths 210A, 210B, or alternatively subsets of input nodes INB in each of several of the plurality of pairs of current paths 210A, 210B, may each receive a different analogue signal. Each of these different analogue signals may be sampled for the presence of neural spikes sequentially, in the manner described above. The detector 50 is thus capable of monitoring multiple different channels.

Alternatively or additionally, the detector 50 of the alternative embodiment may be used to detect spike signals of varying magnitudes. This can be achieved by individually tuning the offset voltage of each pair of current paths 210A, 210B. For this purpose, each of the pairs of current paths 210A, 210B preferably comprises respective (non-shared) tunable loads R2, R3. These respective tunable loads R2, R3 may be used to tune the offset voltage in each pair of current paths 210A, 210B individually. This allows a different magnitude spike signal to be detected using each differently tuned pair of current paths 210A, 210B. The input node INB of each of the plurality of pairs of current paths 210A, 210B, or alternatively the input nodes INB of each of several pairs of current paths 210A, 210B, may each receive the same analogue signal. This analogue signal can then be sampled sequentially using the different sets of current paths 210A, 210B to detect spike signals of varying magnitudes in the one analogue signal. This improves the detection capabilities of the detector 50 significantly.

Alternatively, the tunable loads R2, R3 may be shared by each or several (but not all) of the plurality of pairs of current paths 210A, 210B. In this case, each pair of current paths 210A, 210B may comprise respective (non-shared) input transistors M1, M3, respective (non-shared) cascoding transistors M24, M25 and shared tunable loads R2, R3. This reduces the size and cost of the detector 50, but also reduces the flexibility of individually tuning the offset voltage in each pair of current paths 210A, 210B. Instead, each of the plurality of pairs of current paths 210A, 210B, or each pair of several of the plurality of pairs of current paths 210A, 210B, may have the same or substantially the same offset voltage. Some individual tuning of the offset voltage may still be possible by appropriate choice of the non-shared components of each pair of current paths 210A, 210B, such as the input transistors M1, M3, although to a smaller extent than using the tunable loads R2, R3. Optionally, additional respective tunable loads (in addition to the shared tunable loads R2, R3) may be provided in each pair of current paths 210A, 210B to tune the offset voltage of each pair individually.

Alternatively or additionally, the cascoding transistors M24, M25 may be shared by each pair of the plurality of sets of current paths 210A, 210B, or each pair of several of the plurality of sets of current paths 210A, 210B. In this case, each of the pairs of current paths 210A, 210B may comprise respective (non-shared) input transistors M1, M3, shared cascoding transistors M24, M25 and shared tunable loads R2, R3. Additional switching elements (not shown) may be provided, for example connected to one of the source, drain and gate of the input transistors M1, M3, to selectively interrupt each pair of current paths 210A, 210B.

Alternatively, the core amplifier 200 may comprise a plurality of first current paths 210B and only one second current path 210A. The one second current path 210A may be shared by the plurality of first current paths 210B. Put another way, the plurality of pairs of current paths 210A, 210B may comprise or consist of a respective one of the plurality of first current paths 210B and one shared current path 210A. In this embodiment, preferably only a single shared current source 220 is provided for providing current to each pair of current paths 210A, 210B. In each of a plurality of time intervals, the shared current path 210A and one of the plurality of first current paths 210B may cycle through the phases of the operation cycle as described in relation to Figure 3. In this time interval, the other of the plurality of first current paths 210B remain interrupted at least in the second phase (ii), the third phase (iii) and the off mode (rst).

When introducing elements or features of the present disclosure and the exemplary embodiments, the articles "a", "an", "the" and "said" are intended to mean that there are one or more of such elements or features. The terms "comprising", "including" and "having" are intended to be inclusive and mean that there may be additional elements or features other than those specifically noted. It is further to be understood that the method steps, processes, and operations described herein are not to be construed as necessarily requiring their performance in the particular order discussed or illustrated, unless specifically identified as an order of performance. It is also to be understood that additional or alternative steps may be employed.

It is specifically intended that the present invention not be limited to the embodiments and illustrations contained herein and the claims should be understood to include modified forms of those embodiments including portions of the embodiments and combinations of elements of different embodiments as come within the scope of the following claims. It is explicitly stated that all value ranges or indications of groups of entities disclose every possible intermediate value or intermediate entity for the purpose of original disclosure as

well as for the purpose of restricting the claimed invention, in particular as limits of value ranges.

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CLAIMS

1. A detector for detecting neural spike signals, the detector comprising:
a core amplifier comprising:
two current paths, each current path configured to integrate a current on a respective integrating node and each current path comprising:
an input transistor configured to receive an analogue input signal, and
a tunable load configured to tune an offset voltage of the core amplifier;
wherein the core amplifier further comprises a reset element configured to reset the integrating nodes periodically;
and
wherein the detector further comprises a read out element configured to process the integrated currents at the two integrating nodes.
2. The detector of claim 1, wherein the tunable load is a memristor.
3. The detector of any preceding claim, wherein the reset element is configured to reset the integrating nodes at a pre-set fixed frequency, or at an adaptable frequency, or when the read out element indicates that the integrated currents at the two integrating nodes have been processed.
4. The detector of any preceding claim, wherein each current path of the core amplifier further comprises a cascoding transistor connected between the input transistor and the integrating node.
5. The detector of claim 4, wherein the core amplifier further comprises a switchable current source configured to provide a current to each of the two current paths, wherein, in each current path, the input transistor is connected between the switchable current source and the cascoding transistor and wherein the switchable current source and the cascoding transistor are configured to switch simultaneously.
6. The detector of claim 5, wherein the switchable current source is configured to switch at the same frequency as the reset element.

7. The detector of any preceding claim, wherein the reset element is configured to reset the integrating nodes at a frequency that is greater than 1 kHz, preferably greater than 50 kHz.
8. The detector of any preceding claim, wherein the read out element is configured to operate only when the voltage at one of the integrating nodes exceeds a threshold voltage.
9. The detector of any preceding claim, wherein the read out element comprises a comparator, such as a dynamic latched comparator, and wherein the two integrating nodes of the core amplifier are connected to two input nodes of the comparator.
10. The detector of claim 9, wherein the read out element further comprises a trigger generating circuit configured to generate a trigger signal when the voltage at the integrating nodes exceeds a threshold voltage, the trigger signal being applied to the comparator.
11. The detector of claim 10, wherein the trigger generating circuit comprises a fuzzy logic inverter, the fuzzy logic inverter comprising a CMOS inverter and a tunable load provided on a current path connected to an output node of the fuzzy logic inverter, the tunable load being configured to tune the threshold voltage.
12. The detector of claim 4, wherein the tunable load is connected between the cascoding transistor and the integrating node in each current path, or wherein the tunable load is connected between the cascoding transistor and the input transistor in each current path, or wherein the tunable load is connected between the current source and the input transistor in each current path.
13. The detector of any preceding claim, wherein the tunable load comprises a first tunable load configured to coarsely tune an offset voltage of the core amplifier over a wide voltage range and a second tunable load configured to finely tune an offset voltage of the core amplifier over a narrow voltage range.
14. The detector of any preceding claim, wherein the core amplifier is configured such that current is allowed to continuously leak from each of the integrating nodes.

15. The detector of any preceding claim, wherein the core amplifier comprises a plurality of first current paths configured to integrate current on one of the two integrating nodes,

wherein each of the plurality of first current paths comprises a respective input transistor, and each of the plurality of first current paths is configured to selectively connect to and disconnect from the one of the two integrating nodes.

16. The detector of claim 15, wherein the core amplifier comprises a plurality of second current paths configured to integrate current on the other of the two integrating nodes,

wherein each of the plurality of second current paths comprises a respective input transistor, and each of the plurality of second current paths is configured to selectively connect to and disconnect from the other of the two integrating nodes

17. The detector of claim 15 or 16, wherein each current path comprises a respective tunable load, optionally wherein the respective tunable load is a memristor.

18. The detector of any one of claims 15 to 17, wherein each current path comprises a respective cascoding transistor connected between the respective input transistor and the integrating node on which the current path may integrate current,

wherein each cascoding transistor is configured to selectively connect and disconnect the respective current path to and from the integrating node on which the current path may integrate current.

19. The detector of any one of claims 16 to 18, further comprising a plurality of switchable current sources, each configured to provide a current to one or more pairs of current paths, each pair of current paths comprising one first current path of the plurality of first current paths and one second current path of the plurality of second current paths.

20. The detector of any one of claims 15 to 19, wherein each first current path is configured to periodically connect to and disconnect from the one of the two integrating nodes in such a way that at most one of the first current path integrates current on the integrating nodes at any one time.

21. A neural spike recording system for recording neuronal activity, the neural spike recording system comprising:

the detector of any of claims 1 to 20;

a neurological sensor configured to measure neuronal activity and to output a corresponding analogue electrical signal, the analogue electrical signal being applied to one of the two input transistors of the detector.

22. A method of using a detector comprising

a core amplifier comprising two current paths, each current path configured to integrate a current on a respective integrating node, and each current path comprising an input transistor configured to receive an analogue input signal, and a tunable load configured to tune an offset voltage of the core amplifier; wherein the core amplifier further comprises a reset element configured to reset the integrating nodes periodically; and wherein the detector further comprises a read out element configured to process the integrated currents at the two integrating nodes,

the method comprising the steps of:

- a) applying an analogue input signal to each of the two input transistors;
- b) supplying a current to the current paths and resetting the charge at the integrating nodes;
- c) after the charge at the integrating nodes has been reset, integrating the current flowing through each of the current paths on the integrating nodes;
- d) processing the integrated currents at the integrating nodes using the read out element;
- e) performing steps b) to d) periodically.

23. The method of claim 22, wherein step b) further comprises activating two cascoding transistors that are connected in the two current paths between the input transistor and the integrating node.

24. The method of claim 23, further comprising entering an off mode after step d) and before step e) by simultaneously stopping to supply current to the current paths and turning off the cascoding transistors so as to isolate the input transistors.

25. The method of any one of claims 22 to 24, wherein step d) is performed only when the voltage at an integrating node exceeds a threshold voltage.

26. The method of any one of claims 22 to 25, further comprising tuning the resistive value of the tunable loads of the detector.

27. The method of any one of claims 22 to 26, wherein step a) comprises applying a signal comprising a neural spike signal to one of the input transistors, and applying a constant reference signal to the other of the input transistors.

28. A method for detecting neural spike signals, the method comprising the steps of:

- a) supplying a current to two current paths, each current path comprising an input transistor and a tunable load;
- b) applying an analogue input signal to each of the two input transistors, thereby modulating the current in a respective current path;
- c) integrating the current flowing through each of the current paths on a respective integrating node;
- d) after the current has been integrated on the integrating nodes, processing the voltage at the integrating nodes using a read out element;
- e) resetting the integrating nodes using a reset element;
- f) performing steps c) to e) periodically.

29. The method of any one of claims 22 to 28, wherein the method is for using a detector according to one of claims 15 to 20, the method comprising the steps of:

- a) applying a respective analogue input signal to each input transistor in each current path;
- b) supplying a current to at least a first pair of current paths, the first pair of current paths comprising one current path for integrating current on one integrating node and another current path for integrating current on the other integrating node, and resetting the charge at the integrating nodes;
- c) after the charge at the integrating nodes has been reset, integrating the current flowing through the first pair of current paths on the integrating nodes;
- d) processing the integrated currents at the integrating nodes using the read out element;
- e) performing steps b) to d) for one or more other pairs of current paths; and
- f) performing steps b) to e) periodically.

Figure 1

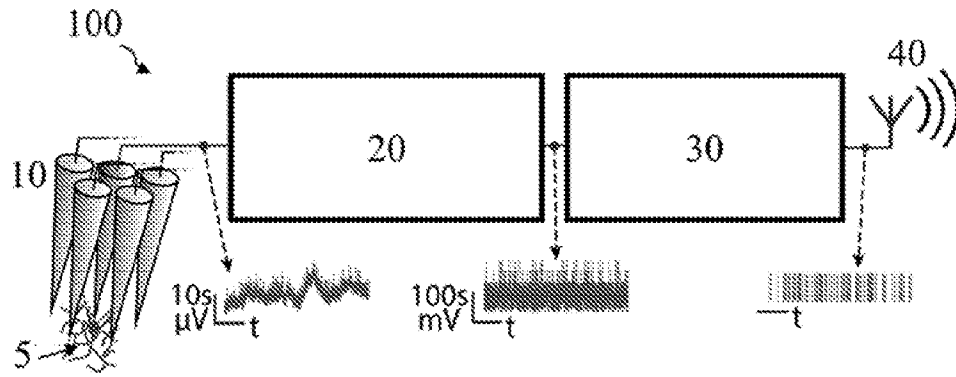


Figure 2

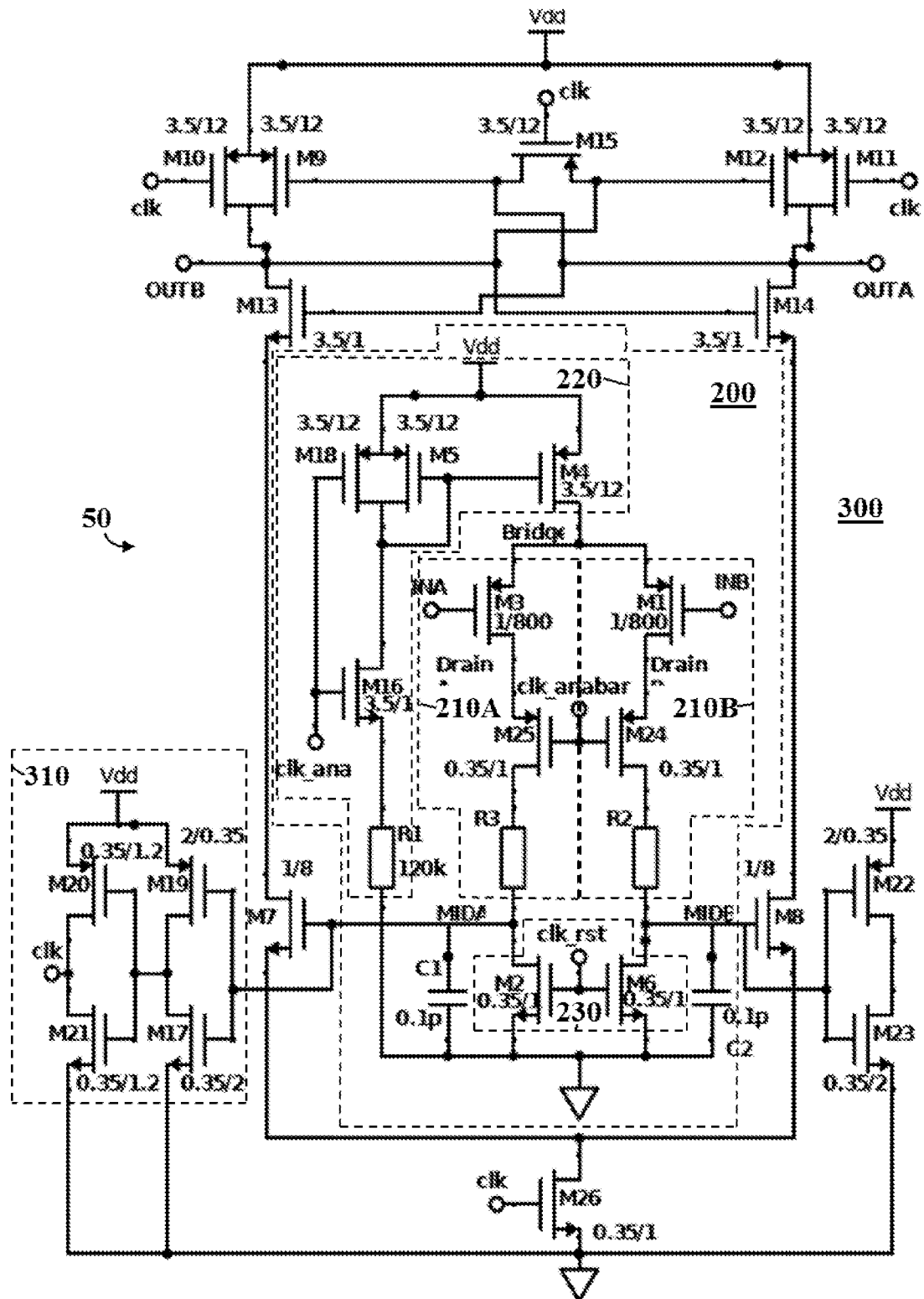
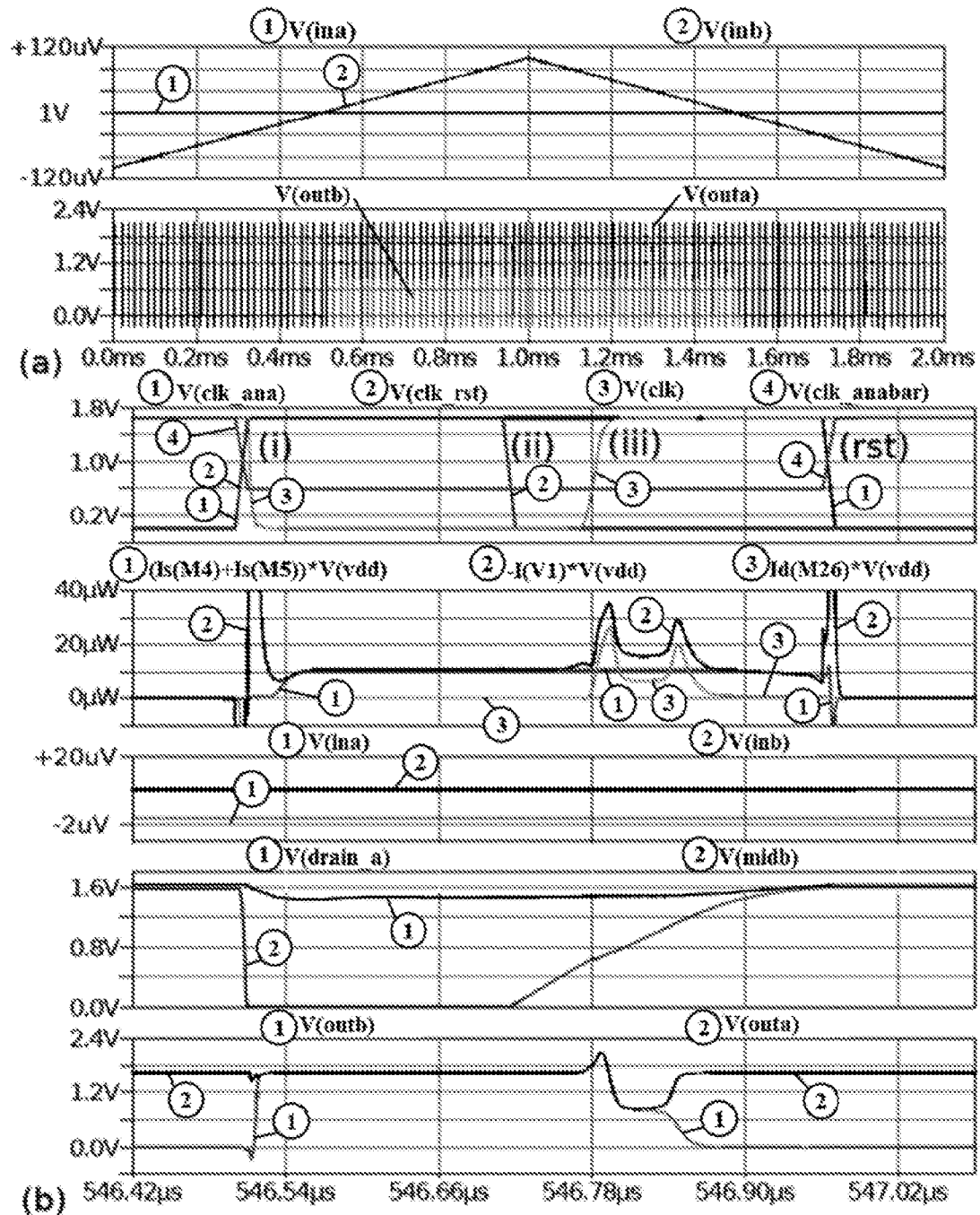


Figure 3



INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2019/051243

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/45 A61B5/04
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F A61B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	WO 2016/054274 A1 (UNIV CALIFORNIA [US]) 7 April 2016 (2016-04-07)	1-3, 5-11, 22-29 4,12-21
A	paragraphs [0034], [0054], [0059], [0069]; figures 6,8 -----	
A	US 2009/082691 A1 (DENISON TIMOTHY J [US] ET AL) 26 March 2009 (2009-03-26) paragraphs [0270], [0276]; figure 27 -----	1-29
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A	US 9 515 635 B1 (SADD MICHAEL A [US] ET AL) 6 December 2016 (2016-12-06) abstract; figures 3,4 ----- -/-	1-29



Further documents are listed in the continuation of Box C.



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INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2019/051243

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