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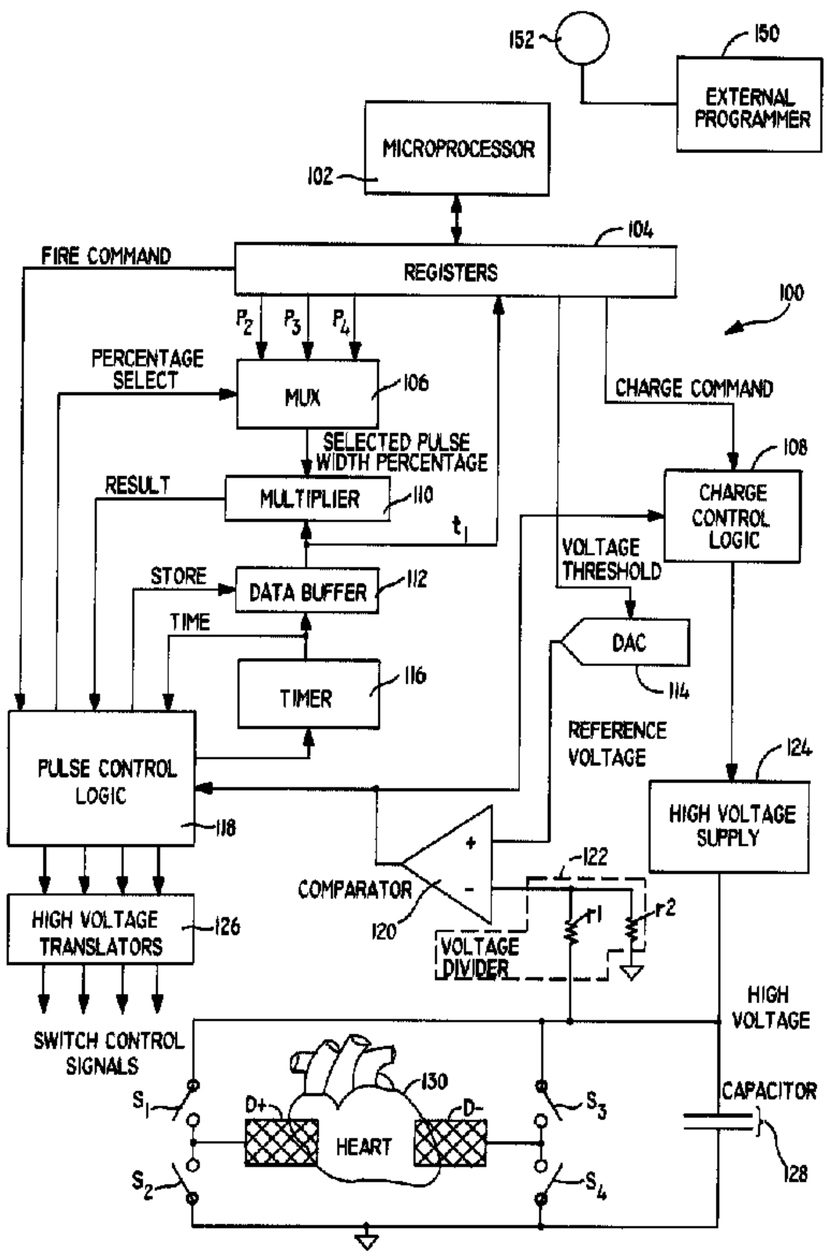
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(54) METHODE ET APPAREIL DE GENERATION DE TENSIONS DE DEFIBRILLATION MULTIPHASEES UTILISANT DES RAPPORTS DE DUREES D'IMPULSIONS

(54) METHOD AND APPARATUS FOR GENERATING MULTIPHASIC DEFIBRILLATION WAVEFORMS BASED ON PULSE WIDTH RATIOS



(57) A method and apparatus for generating a multiphasic defibrillation/cardioversion waveform. The multiphasic defibrillation/cardioversion waveform is generated by specifying only the initial voltage and end voltage of the first phase and the percentage of time duration of each subsequent phase relative to the time duration of the first phase. Therefore, only two voltage measurements need to be made for the first phase, while for the remaining phases, only the time duration is detected.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for generating a multiphasic defibrillation/cardioversion waveform. The multiphasic defibrillation/cardioversion waveform is generated by specifying only the initial voltage and end voltage of the first phase and the percentage of time duration of each subsequent phase relative to the time duration of the first phase. Therefore, only two voltage measurements need to be made for the first phase, while for the remaining phases, only the time duration is detected.

METHOD AND APPARATUS FOR GENERATING MULTIPHASIC DEFIBRILLATION WAVEFORMS BASED ON PULSE WIDTH RATIOS

BACKGROUND OF THE INVENTION

The present invention relates to cardioversion/defibrillation systems and more particularly to a method and apparatus for generating multiphasic defibrillation waveforms.

Techniques for defibrillation/cardioversion have evolved over the years from a truncated exponentially decaying waveform of a capacitor to more sophisticated waveforms, such as multiphasic waveforms. In this regard, it has been found that multiphasic waveforms often are more effective in defibrillating the heart.

There are several methods known for generating multiphasic defibrillation waveforms. One method is disclosed in U.S. Patent No. 4,800,883 to Winstrom and in U.S. Patent No. 4,821,723 to Baker, Jr. et al. These patents disclose multiple capacitor networks for generating multiphasic waveforms according to a fixed-duration format, whereby the duration of each pulse is fixed but the tilt of each pulse varies with patient system impedance.

Commonly assigned U.S. Patent No. 4,850,357 to Bach discloses a biphasic pulse generator providing a fixed tilt waveform which automatically compensates for changes in lead impedance. However, the apparatus disclosed in this patent detects several voltage levels in order to deliver the required pulse shape. Consequently, circuitry is required to detect the voltage levels.

While these prior systems generally are effective, there is room for improvement.

SUMMARY OF INVENTION

It is therefore an object of the present invention to provide a novel method and apparatus for generating a multiphasic difibrillation/cardioversion waveform.

Briefly, the present invention is directed to a method and apparatus for generating a multiphasic defibrillation/cardioversion waveform by specifying only the initial voltage and end voltage of the first phase and the percentage of pulse widths for each subsequent phase relative to the pulse width of the first phase. Therefore, only two voltage measurements need to be made for the first phase, while for the remaining phases, only the time duration (pulse width) is detected.

According to one aspect of the present invention there is provided a method for generating a time radiometric multiphasic defibrillation/cardioversion waveform comprising the steps of:

setting an initial voltage level of a capacitor corresponding to an initial voltage level of a first phase of a multiphasic defibrillation/cardioversion waveform;

setting for each phase in the multiphasic waveform subsequent to the first phase a desired time ratio of the duration of the respective phase to a time duration of the first phase of the multiphasic waveform;

setting the end voltage level of the first phase of a multiphasic waveform;

charging the capacitor to the initial voltage level;

discharging the capacitor from the initial voltage level to the end voltage level to cause the first phase of the multiphasic waveform;

determining the time duration of the first phase of the multiphasic waveform;

computing time durations of subsequent phases of the multiphasic waveform based on the time duration of the first phase and the ratios of the time durations of the subsequent phases relative to the first phase;

controlling the discharge of the capacitor according to the time durations of subsequent phases to generate the subsequent phases of the multiphasic defibrillation/cardioversion waveform.

According to another aspect of the present invention there is provided a method for generating a multiphasic defibrillation/cardioversion waveform comprising the steps of:

setting parameters for charging a capacitor to an initial voltage level of a first phase of a multiphasic defibrillation/cardioversion waveform and discharging the capacitor to an end voltage level of the first phase;

setting for each phase in the multiphasic waveform subsequent to the first phase parameters-for defining the shape of phases subsequent the first phase in terms relative to the shape of the first phase of the multiphasic waveform;

charging the capacitor to the initial voltage level;

discharging the capacitor from the initial voltage level to the end voltage level to effect the first phase of the multiphasic waveform;

determining the time duration of the first phase of the multiphasic waveform;

computing waveshape parameters of subsequent phases of the multiphasic waveform based on the time duration of the first phase, the parameters of the subsequent phases, the initial voltage level of the first phase and the end voltage level of the first phase; and

controlling the discharge of the capacitor according to the waveshape parameters of subsequent phases to generate the subsequent phases of the multiphaic defibrillation/cardioverion waveform.

In yet another aspect of the present invention there is provided an apparatus for generating a multiphasic waveform, said apparatus comprising:

capacitive means for storing electrical energy;

programmable processing means for controlling the charging and discharging of said capacitive means;

at least one addressable register for storing command bit codes and waveform parameters provided by said programmable processing means;

timing means for measuring the time duration of the first phase of the multiphasic waveform;

data storage means responsive to said timing means for storing a value corresponding to the time duration of the first phase;

comparison means for comparing voltage-related waveform parameters stored in said at least one addressable register to the voltage across the capacitive means;

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multiplexing means connected to said at least one register for selectively choosing a waveform parameter corresponding to a desired pulse width percentage;

multiplication means responsive to the selectively chosen waveform parameter from said multiplexing means and also responsive to said timing means for multiplying the time duration of the first phase by the desired pulse width percentage and for generating a signal indicative of the result thereof;

at least two defibrillation electrodes located near a patient's heart;

switch means for selectively discharging said capacitive means through the heart via said at least two defibrillation electrodes;

pulse control means for controlling said switch means to discharge the capacitive means in accordance with voltage-related waveform parameters for the first phase and waveform parameters corresponding to pulse width percentages for subsequent phases, said pulse control means being responsive to the comparison means, the timing means, the multiplication means, and said at least one register;

charging means for charging the capacitive means; and

charge control means responsive to the comparison means and responsive to said at least one register, for controlling the charging means.

In still yet another aspect of the present invention there is provided a method for generating a multiphasic defibrillation/cardioversion waveform, said method comprising the steps of:

loading into a voltage threshold register, a value corresponding to a desired initial voltage of the first phase of the multiphasic waveform;

comparing said value corresponding to a desired initial voltage to a voltage currently across a capacitor;

loading a charge command bit code into a command register;

charging the capacitor whenever the charge command bit code is in the command register and the voltage across the capacitor is less than the value corresponding to the desired initial voltage of the first phase;

terminating said charging of the capacitor when the voltage across said capacitor reaches the desired initial voltage of the first phase;

loading into the voltage threshold register, a value corresponding to the desired termination voltage of the first phase;

loading a fire command bit code into the command register;

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discharging the capacitor in response to the fire command bit code being loaded into the command register thereby commencing the first phase of the multiphasic waveform;

terminating said discharging of the capacitor upon said voltage across the capacitor decaying to the value most recently loaded into the voltage threshold register thereby terminating said first phase;

determining the time duration of the first phase;

storing said time duration in a data buffer;

selecting a pulse width percentage corresponding to a next phase of the multiphasic waveform;

multiplying the time duration of the first phase by said pulse width percentage to thereby determine the time duration of the next phase of the multiphasic waveform;

further discharging said capacitor for the time duration resulting from said step of multiplying;

repeating the steps of selecting, multiplying, and further discharging for subsequent phases of the multiphasic waveform.

In still yet another aspect of the present invention there is provided a method for generating a multiphasic defibrillation/cardioversion waveform comprising the steps of:

determining an initial voltage of a first phase of said multiphasic waveform, an end voltage of the first phase of said multiphasic waveform, and time duration ratios of subsequent phases with respect to the first phase of said multiphasic waveform;

applying the initial voltage across a pair of electrodes to begin the first phase;

reducing the initial voltage to said end voltage over a phase duration to end the first phase;

deriving a subsequent phase duration from the previous phase duration and said time duration ratios;

applying a subsequent voltage across said pair of electrodes;

reducing the subsequent voltage to a subsequent end voltage over said subsequent phase duration.

In still yet another aspect of the present invention there is provided

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a method for generating a multiphasic defibrillation/cardioversion waveform comprising the steps of:

determining an initial voltage of a first phase of said multiphasic waveform, and end voltage of the first phase of said multiphasic waveform, and time duration ratios of subsequent phases with respect to the first phase of said multiphasic waveform;

charging a capacitor to the initial voltage;

discharging the capacitor to the end voltage over a phase duration to end the first phase;

deriving a subsequent phase duration from the previous phase duration and said time duration ratios;

discharging the capacitor to a subsequent voltage across a pair of electrodes for the subsequent phase duration.

In still yet another aspect of the present invention there is provided an apparatus for generating a multiphasic defibrillation/cardioversion waveform comprising:

a means for storing an initial voltage of a first phase of said multiphasic waveform, and end voltage of the first phase of said multiphasic waveform, and time duration ratios of subsequent phases with respect to the first phase of said multiphasic waveform;

means for applying the initial voltage across a pair of electrodes to begin the first phases;

means for reducing the initial voltage to said end voltage over a phase duration to end the first phase;

means for deriving a subsequent phase duration from the previous phase duration and said time duration ratios;

means for applying a subsequent voltage across said pair of electrodes;

means for reducing the subsequent voltage to a subsequent end voltage over said subsequent phase duration; and

means for reversing the voltage across said pair of electrodes during said subsequent phase.

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The above and other objects and advantages will become more readily apparent when reference is made to the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a graphical representation of a multiphasic defibrillation waveform which is generated by the method and apparatus according to the present invention.

Figure 2 is a flow chart illustrating the steps of generating a multiphasic defibrillation/cardioversion waveform according to the present invention.

Figure 3 is a schematic diagram of circuitry for generating a multiphasic defibrillation waveform according to the present invention.

Figure 4 is a flow chart illustrating the operation of the circuitry shown in Figure 3.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring first to Figure 1, a multiphasic defibrillation waveform is shown comprising four phases. According to the present invention the waveform shown in Figure 1 is generated by specifying the initial voltage V_0, the first truncate voltage V_1 and the pulse width of each of the phases 2 through 4 as a percentage of the pulse width of phase 1. Consequently, only two voltage measurements must be performed by the waveform generating circuitry and over a small voltage range (V_0 to V_1). Moreover, the time measurements may

be accomplished more reliably and accurately for the higher order phases (phases 2-4) using much simpler hardware.

In general, for an n-phasic waveform (where n is any positive number), phase 1 would be specified in terms of the initial voltage V_0 and the truncate voltage V_1, and the higher order phases ($n \geq 2$) are specified as a percentage of t_1 where t_1 is the time duration (also referred to as pulse width) of the first phase.

The following is an explanation of the underlying theory of the present invention to illustrate how the method and apparatus according to the present invention is equivalent to specifying all of the cutoff (truncated) voltages for all phases. A legend for the discussion follows.

V_0 = initial voltage of the capacitor

V_1 = truncate (end) voltage of phase 1

V_n = truncate voltage of phase n

t_1 = time duration of phase 1

t_n = time duration of phase n

$P_2 = t_2/t_1$, time phase 2: time phase 1

$P_n = t_n/t_1$, time phase n: time phase 1

The truncate voltage of the first phase is found according to the discharge of a capacitor:

$V_1 = V_0 e^{-t1/RC}$, where R and C are values of the discharge resistance and capacitor. The time duration of phase 1 is, then:

$t_1 = -RC\ln(V_1/V_0)$, where ln is the natural logarithm.

According to the ratio or percentage relationship between the time duration of the phases, $t_2 = P_2 t_1 = -RC\ln(V_2/V_1)$. Consequently, substituting the expression for t1 it follows that,

$$P_2 = \frac{\ln\ (V_2/V_1)}{\ln\ (V_1/V_0)}.$$

Therefore, the truncate voltage of phase 2 is, $V_2 = (V_1/V_0)^{P2}V_1$. In general, the percentage for phase n and truncate voltage for phase n is:

$$P_n = \frac{\ln\ (V_n/V_{n-1})}{\ln\ V_1/V_0)}$$

$$V_n = (V_1/V_0)^{P3}V_{n-1} = (V_1/V_0)^{P2+P3+\ldots+Pn-1+Pn}.$$

Thus, the cutoff or truncate voltage of each phase is directly related to a percentage of the pulse width of the initial phase and is independent of the actual time and RC time constant. With the knowledge of the initial and final voltages and the capacitance, the total energy delivered by the multiphase waveform can be calculated. The values of $P_1, \ldots, P_n$ could also be calculated from percentage tilt (T), where

$$T_n = 1 - V_n/V_0.$$

With reference to Figure 2, a method using the foregoing theory, is illustrated for generating the multiphasic waveform of Figure 1 without having to detect voltages for each phase of the waveform.

In step 20, the initial voltage level V_0 of the first phase is set, which voltage level also corresponds to the initial voltage level of the capacitor.

Next, in step 21, the pulse width percentages P_2, P_3, ..., P_n are set for each phase, each pulse width percentage P_2, P_3, ..., P_n being a ratio of the duration of the respective phase to the time duration t_1 of the first phase of the multiphasic waveform. As noted in the foregoing theoretical discussion, each of the pulse width percentages P_2, P_3, ..., P_n can be calculated from the desired cutoff or truncate voltage of each phase, knowing the initial voltage and the termination voltage of the first phase.

In step 22, the termination voltage V_1 is set for the first phase of the multiphasic waveform.

In step 23, the capacitor is charged to the initial voltage V_0 of the first phase.

In step 24, the capacitor is discharged from its initial voltage V_0 to the termination voltage V_1 hence providing the first phase of the multiphasic waveform.

In step 25, the time duration of the first phase is determined.

In step 26, the time durations $t2_2$ t_3, ..., t_n for subsequent phases are computed by multiplying each of the pulse width percentages P_2, P_3, ..., P_n by the time duration t_1 of the first phase.

Finally, in step 27, subsequent phases of the multiphasic waveform are generated by discharging the capacitor for the time durations computed in step 26. Specifically, the phases are generated with alternating polarity, for example, positive polarity for odd values of n and negative polarity for even values of n.

Figure 3 illustrates electrical circuitry for generating a multiphasic defibrillation waveform according to the present invention. The circuitry 100 comprises a microprocessor 102; a set of addressable registers 104 connected to the microprocessor 102; a multiplexer (MUX) 106; charge control logic 108; a multiplier 110; a data buffer 112; a digital to analog converter (DAC) 114; a timer 116; pulse control logic 118; a comparator 120; a voltage divider 122; a high voltage supply 124; high voltage translators 126; a 125 to 150 microfarad capacitor 128; four switches S1, S2, S3, and S4; and two defibrillation electrodes D+ and D- located in close proximity to a patient's heart 130.

The circuitry 100 is primarily controlled by the microprocessor 102 which itself can be either directly preprogrammed by a physician with values for V_0, V_1, P_2, P_3, ..., P_n or indirectly preprogrammed using other parameters provided by the physician through means well known in the art. The physician, for example, could specify percentage tilt, voltages, and/or pulse width percentages, while an external module takes these values and calculates the proper values for V_0, V_1, P_2, P_3, ..., P_n on behalf of the microprocessor 102. This data is then fed to the microprocessor 102, which either causes a defibrillation shock to

be delivered immediately or causes one to be delivered automatically in response to a detected cardiac arrhythmia. A preferred microprocessor 102 is the model 68HC11 manufactured by Motorola.

The set of addressable registers 104 is connected to the microprocessor 102 and comprises a voltage threshold register for storing the values V_0 and V_1; a pulse width percentage register for storing each of the values P_2, P_3, ..., P_n; a command register for storing a "charge command" bit code or a "fire command" bit code; and a register for storing t_1. The microprocessor 102 by first storing the values for either V_0 or V_1, along with P_2, P_3, ..., P_n in the set of addressable registers 104, and then selectively storing either the "fire command" bit code or the "charge command" bit code in the command register, is able to cause either delivery of a desired multiphasic defibrillation shock or the charging of the capacitor 128 to the desired peak voltage V_0 of the first phase, respectively.

The digital to analog converter (DAC) 114 is responsive to the value of V_0 or V_1 whichever is digitally stored in the voltage threshold register. The primary function of the DAC 114 is to take this digital value for V_0 or V_1, and in accordance therewith, provide an output reference voltage proportional to the desired peak value V_0 or termination value V_1 of the first phase. This output reference voltage is within the input range of, and is fed into, the positive input of the comparator 120.

The charge control logic 108 is responsive to the output from the comparator 120 and the bit code contained in the command register, so as to selectively enable the high voltage supply 124. By selectively enabling the high voltage supply 124 in response to detecting a "charge command" bit code in the command register, the charge control logic 108 is able to cause charging of the capacitor 128 to the peak voltage V_0 of the first phase. The high voltage supply itself is well known to the art. The charge control logic 108 is a sequencer which powers up the analog circuit and then charges the capacitor 128 until the comparator 120 switches.

The voltage divider 122 comprises two series-connected resistors r1 and r2 arranged such that the voltage present across the capacitor 128 is also applied across the series-connected resistors r1 and r2. In practice, the resistors have resistance values ranging from 9.7M to 10.7M ohms for r1, and 15K to 25K ohms for r2. More specifically though, the value of each resistor r1 and r2 is chosen such that the voltage at the center tap (the voltage across r2 at a ratio of 480 plus or minus 2 percent) is at a level within the input range of the comparator 120. This center tap voltage is then fed into the negative input of the comparator 120, and as a result, the negative input of the comparator 120 receives a voltage proportional to, but smaller than, that which is present across the capacitor 128.

The timer 116 is connected and responsive to the pulse control logic 118 such that, upon commencement of the first phase, the timer 116 begins counting elapsed time. The timer's output is

connected to the data buffer 112 and is thereby able to provide the data buffer 112 with a measure of the time elapsed after application of the first phase. This measure of elapsed time is also provided to the pulse control logic 118.

The data buffer 112 is connected to the pulse control logic 118 via a "store" signal, and is responsive to the "store" signal such that upon the signal being applied, the data buffer 112 stores the current value of the timer's output. Since the "store" signal is applied, as will be discussed hereinafter, upon termination of the first phase, the stored value corresponds to the pulse width t_1 of the first phase.

The multiplexer (MUX) 106 is responsive to a "percentage select" signal from the pulse control logic 118 and, in accordance therewith, selects one of the pulse width percentage values P_2, P_3, ..., or P_n from the corresponding register. The selected pulse width percentage P_2, P_3, ..., or P_n is then supplied to the multiplier 110.

The multiplier 110 is connected to both the data buffer 102 and the multiplexer 106. As a result, the multiplier 110 receives both the selected pulse width percentage value P_2, P_3, ..., or P_n from the multiplexer 106 and the stored value corresponding to the pulse width t1 °f the first phase. Both of these values are multiplied by the multiplier 110 with the result being provided to the pulse control logic 118.

The pulse control logic 118 is connected and responsive to the command register, the result from the multiplier 110, the

elapsed time measured by the timer 116, and the output from the comparator 120. In addition, the pulse control logic 118 provides the "percentage select" signal to the multiplexer 106, the "store" signal to the data buffer 112, and four low voltage control signals to the high voltage translators 126. The pulse control logic 118 is a digital logic sequencer that controls the pulse generator circuitry 106, 110, 112, 116 and 126.

The high voltage translators 126 are connected and receive the four low voltage control signals from the pulse control logic 118. In response to the low voltage control signals, the high voltage translators 126 produce four switch control signals corresponding to the low voltage control signals, but of higher voltage. In this regard, the translators 126 simply step-up the voltage of the low voltage control signals.

Although the actual connections are not shown in Figure 3, each of the switch control signals is connected to one of the switches S1, S2, S3, and S4. The switches S1, S2, S3, and S4 are arranged and responsive to the switch control signals so as to selectively make or break a series electrical circuit through the heart 130, the capacitor 128, and the defibrillation electrodes D+ and D-. Depending on which switches are closed, the circuitry 100 either provides the heart 130 with a positive polarity voltage (where D- is connected to ground) or a negative polarity voltage (where D+ is connected to ground). As can be seen from Figure 3, closing switches s1 and s4 provides the heart 130 with a positive

polarity voltage, while closing switches s2 and s3 provides a negative polarity voltage.

With reference to Figure 4, operation of the circuitry 100 in delivering the multiphasic defibrillation shock of Figure 1, will now be described. In step 30, the microprocessor 102 loads the peak voltage value V_0 into the voltage threshold register, and sets the "charge command" bit code into the command register. The actual value of V_0 depends on several external factors including electrode configuration, the patient's defibrillation threshold, patient and electrode impedances, etc. Nevertheless, typical values for V0 range from 45 to 715 volts.

In step 32, the DAC 114 detects the value V_0 and, in response thereto, creates the output reference voltage proportional to the desired peak voltage value V_0 of the first phase, the reference voltage being provided to the positive input of the comparator 120. Meanwhile, the voltage divider 122 divides the voltage present on the capacitor 128 to a level within the input range of the comparator 120, and provides this lower voltage to the negative input of the comparator 120.

In step 34, the charge control logic 108 detects the output from the comparator 120, and in response to this output selectively enables the high voltage supply 124. More specifically, when the voltage across the capacitor 128 is less than V_0, the input to the negative terminal of the comparator 120 is less than that of the positive terminal. This, in turn, causes a high output on the comparator 120. The charge control logic 108 responds to

this high output by enabling the high voltage supply 124 which begins charging the capacitor 128. If, on the other hand, the comparator's output begins low, then this may be an indication that the capacitor 128 is over-charged. Accordingly, the capacitor 128 is discharged through a dump resistor (not shown), which can be of any design generally known in the art. Examples of such dump resistors are shown in U.S. Patents Nos. 4,316,472 and 4,488,555 to Imran and Mirowski, respectively.

In step 36, when the voltage on the capacitor 128 reaches V_0 while being charged, the comparator's output goes from high to low, signalling the charge control logic 108 to disable the high voltage supply 124. A signal from the charge control logic 108 is provided to the microprocessor 102 when the capacitor 128 is fully charged.

Next, in step 38, the microprocessor 102 loads the first phase termination voltage value V_1 into the voltage threshold register and sets the "fire command" bit code in the command register. The actual value for V_1, like V_0, depends upon several external factors, but nevertheless may range between 18 and 286 volts.

In step 40, the DAC 114 detects the digitally stored value for V_1 and, in response thereto, creates a reference voltage proportional to the termination voltage V_1 of the first phase, the reference voltage being provided to the positive input of the comparator 120. In the meantime, the voltage divider 122 continues to divide the voltage present on the capacitor 128 to a level

within the input range of the comparator 120, and provides this lower voltage to the negative input of the comparator 120.

In step 42, upon detecting the "fire command" bit code in the command register, the pulse control logic 118 sends appropriate control signals to the switches S1, S2, S3, and S4 through the high voltage translators 126, which signals are output by the translators 126 as higher voltage switch control signals.

Next, in step 44, the switch control signals cause the switches S1 and S4 to close, thus creating a positive polarity series circuit through the capacitor 128, the heart 130, and the defibrillation electrodes D+ and D-. As a result, the capacitor 128 begins to discharge through the heart 130 thereby commencing the first phase of the multiphasic defibrillation shock.

In step 46, while the first phase is being applied to the heart 130, the timer 116 counts elapsed time and the pulse control logic 118 detects the output from the comparator 120 awaiting a transition from a low output to a high output. When the voltage on the capacitor 128 decays to the first phase termination voltage V_1 the comparator 120 output goes from low to high, thereby signalling the pulse control logic 118 to open the switches S1 and S4 and terminate the first phase.

In step 50, the pulse control logic 118 detects the low to high transition in the comparator's output, and in response thereto, sends the "store" signal to the data buffer 112. The pulse control logic 118 further causes a set of switch control signals

co be sent from the high voltage translators 126 to open switches S1 and S4.

In step 52, upon receiving the "store signal", the data buffer 112 stores the elapsed time corresponding to the pulse width t_1 of the first phase. The pulse width t_1 may be between 1 and 24 milliseconds long. In addition, the switches S1 and S4 are opened to prevent further discharge of the capacitor 12 8 and to thereby terminate the first phase.

Next, in step 54, the pulse control logic 118, using the "percentage select" signal, causes the multiplexer (Mm) 106 to select the second pulse width percentage P_2 from the corresponding register, which pulse width percentage P_2 is provided to the multiplier 110 for multiplication with the first phase pulse width t_1.

In step 56, the multiplier 110 receives the value of P_2 from the multiplexer 106, as well as the value of t_1 from the data buffer 112, and multiplies both values to obtain a result which corresponds to the pulse width t_2 of the second phase, this result t2 being provided to the pulse control logic 118.

In step 58, after a delay time t_d, the pulse control logic 118 sends appropriate control signals to the switches S1, S2, S3, and S4 through the high voltage translators 126, which signals are output by the translators 126 as higher voltage switch control signals.

In step 60, the switch control signals emitted in step 58 cause switches S2 and S3 (since the value of n is even) to close thus creating a negative polarity series circuit through the capacitor 128, the heart 130, and the defibrillation electrodes D+ and D-. As a result, the capacitor 128 again begins to discharge through the heart 130, but this time with negative polarity. The second phase of the multiphasic defibrillation shock is thereby commenced.

In step 61, at the end of the pulse width t_2, the pulse control logic 118 causes the switches S2 and S3 to open, thus terminating the second phase of the multiphasic shock.

In step 62, the next consecutive pulse width percentage P_3, P_4, ..., or P_n is selected using the multiplexer 106, and the steps 56 - 61 are repeated for each value of P_3, P_4, ..., or P_n and each value of t_3, ..., t_4, or t_n or tn until the final percentage Pn has been selected and the last phase has been delivered to the heart 130 with the respective pulse width t_n. When step 60 is repeated for odd values of n, switches S1 and S4 are closed to deliver a positive polarity voltage to the heart 130. For even values of n, switches S2 and S3 are closed to deliver a negative polarity voltage to the heart 130. In this manner, successive phases continue to alternate polarity until the last phase has been delivered.

For defibrillation purposes, the pulse width percentages P_2, P_3, P_4, ..., P_n preferably range in value from 25% to 150% such that the pulse widths t_2, t_3, ..., t_n range in value from to 1 to

36 milliseconds. Likewise, the delay time t_d ranges from 0.8 to 1.2 milliseconds.

In addition to the foregoing, it is well understood that the external programmer 150 and other similar devices can also be used to program the values of V_0, V_1, P_2, P_3, ..., P_n into the microprocessor 102 of the present invention. Programming of defibrillator operating parameters using an external programmer device is well known in the art.

Furthermore, modifications may be made to the circuitry 100 shown in Figure 3 without departing from the scope and spirit of the present invention. Particularly, many functions performed by the microprocessor 102 may be performed by analog circuitry. Also, the charging and discharging of the capacitor 128 may actually be accomplished using two separate circuits, one circuit for charging the capacitor 128 and one circuit for enabling and disabling the discharge of the capacitor 128.

The above description is intended by way of example only and is not intended to limit the present invention in any way except as set forth in the following claims.

CLAIMS:

1. A method for generating a time radiometric multiphasic defibrillation/cardioversion waveform comprising the steps of:

setting an initial voltage level of a capacitor corresponding to an initial voltage level of a first phase of a multiphasic defibrillation/cardioversion waveform;

setting for each phase in the multiphasic waveform subsequent to the first phase a desired time ratio of the duration of the respective phase to a time duration of the first phase of the multiphasic waveform;

setting the end voltage level of the first phase of a multiphasic waveform;

charging the capacitor to the initial voltage level;

discharging the capacitor from the initial voltage level to the end voltage level to cause the first phase of the multiphasic waveform;

determining the time duration of the first phase of the multiphasic waveform;

computing time durations of subsequent phases of the multiphasic waveform based on the time duration of the first phase and the ratios of the time durations of the subsequent phases relative to the first phase;

controlling the discharge of the capacitor according to the time durations of subsequent phases to generate the

subsequent phases of the multiphasic defibrillation/cardioversion waveform.

2. The method of claim 1, wherein said step of computing time durations of the subsequent phases comprises multiplying the time duration ratio for the corresponding phase by the time duration of the first phase.

3. The method of claim 1, further comprising the step of alternating the polarity of successive phases of the multiphasic defibrillation/cardioversion waveform.

4. A method for generating a multiphasic defibrillation/cardioversion waveform comprising the steps of:

setting parameters for charging a capacitor to an initial voltage level of a first phase of a multiphasic defibrillation/cardioversion waveform and discharging the capacitor to an end voltage level of the first phase;

setting for each phase in the multiphasic waveform subsequent to the first phase parameters-for defining the shape of phases subsequent the first phase in terms relative to the shape of the first phase of the multiphasic waveform;

charging the capacitor to the initial voltage level;

discharging the capacitor from the initial voltage level to the end voltage level to effect the first phase of the multiphasic waveform;

determining the time duration of the first phase of the multiphasic waveform;

computing waveshape parameters of subsequent phases of the multiphasic waveform based on the time duration of the first phase, the parameters of the subsequent phases, the initial voltage level of the first phase and the end voltage level of the first phase; and

controlling the discharge of the capacitor according to the waveshape parameters of subsequent phases to generate the subsequent phases of the multiphasic defibrillation/cardioversion waveform.

5. The method of claim 4, wherein the step of controlling the discharge of the capacitor further comprises alternating the polarity of subsequent phases.

6. Apparatus for generating a multiphasic waveform, said apparatus comprising:

capacitive means for storing electrical energy;

programmable processing means for controlling the charging and discharging of said capacitive means;

at least one addressable register for storing command bit codes and waveform parameters provided by said programmable processing means;

timing means for measuring the time duration of the first phase of the multiphasic waveform;

data storage means responsive to said timing means for storing a value corresponding to the time duration of the first phase;

comparison means for comparing voltage-related waveform parameters stored in said at least one addressable register to the voltage across the capacitive means;

multiplexing means connected to said at least one register for selectively choosing a waveform parameter corresponding to a desired pulse width percentage;

multiplication means responsive to the selectively chosen waveform parameter from said multiplexing means and also responsive to said timing means for multiplying the time duration of the first phase by the desired pulse width percentage and for generating a signal indicative of the result thereof;

at least two defibrillation electrodes located near a patient's heart;

switch means for selectively discharging said capacitive means through the heart via said at least two defibrillation electrodes;

pulse control means for controlling said switch means to discharge the capacitive means in accordance with voltage-related waveform parameters for the first phase and waveform parameters corresponding to pulse width percentages for subsequent phases, said pulse control means being responsive to the comparison means, the timing means, the multiplication means, and said at least one register;

charging means for charging the capacitive means; and

charge control means responsive to the comparison means and responsive to said at least one register, for controlling the charging means.

7. The apparatus of claim 6, wherein said capacitive means is a 125 to 150 microfarad capacitor.

8. The apparatus of claim 6 wherein said comparison means comprises a comparator, a voltage divider, and a digital-to-analog converter; said voltage divider providing the comparator with a first input voltage proportional to, but less than, the voltage across the capacitive means, and said digital-to-analog converter provides the comparator with a second input voltage proportional to the value of a voltage-related parameter currently stored in said at least one addressable register.

9. A method for generating a multiphasic defibrillation/cardioversion waveform, said method comprising the steps of:

loading into a voltage threshold register, a value corresponding to a desired initial voltage of the first phase of the multiphasic waveform;

comparing said value corresponding to a desired initial voltage to a voltage currently across a capacitor;

loading a charge command bit code into a command register;

charging the capacitor whenever the charge command bit code is in the command register and the voltage across the capacitor is less than the value corresponding to the desired initial voltage of the first phase;

terminating said charging of the capacitor when the voltage across said capacitor reaches the desired initial voltage of the first phase;

loading into the voltage threshold register, a value corresponding to the desired termination voltage of the first phase;

loading a fire command bit code into the command register;

discharging the capacitor in response to the fire command bit code being loaded into the command register thereby commencing the first phase of the multiphasic waveform;

terminating said discharging of the capacitor upon said voltage across the capacitor decaying to the value most recently loaded into the voltage threshold register thereby terminating said first phase;

determining the time duration of the first phase;

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storing said time duration in a data buffer;

selecting a pulse width percentage corresponding to a next phase of the multiphasic waveform;

multiplying the time duration of the first phase by said pulse width percentage to thereby determine the time duration of the next phase of the multiphasic waveform;

further discharging said capacitor for the time duration resulting from said step of multiplying;

repeating the steps of selecting, multiplying, and further discharging for subsequent phases of the multiphasic waveform.

10. The method of claim 9, wherein the step of further discharging further comprises the step of alternating the polarity of each phase such that successive phases have opposite polarity.

11. A method for generating a multiphasic defibrillation/cardioversion waveform comprising the steps of:

determining an initial voltage of a first phase of said multiphasic waveform, an end voltage of the first phase of said multiphasic waveform, and time duration ratios of subsequent phases with respect to the first phase of said multiphasic waveform;

applying the initial voltage across a pair of electrodes to begin the first phase;

reducing the initial voltage to said end voltage over a phase duration to end the first phase;

deriving a subsequent phase duration from the previous phase duration and said time duration ratios;

applying a subsequent voltage across said pair of electrodes;

reducing the subsequent voltage to a subsequent end voltage over said subsequent phase duration.

12. The method according to claim 11, further comprising sequentially repeating the derivation step, subsequent voltage application step and the subsequent voltage reduction step after the subsequent voltage reduction step.

13. The method according to claim 11, further comprising charging a capacitor to the initial voltage prior to applying the initial voltage.

14. The method according to claim 13 wherein the phase duration is proportional to a

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time consent for the capacitor.

15. The method according to claim 11, wherein said initial voltage is applied to the pair of electrodes through a polarity reversing switch, further comprising, after the initial voltage reduction step;

reversing said polarity reversing switch to produce an inverted voltage as applied across said pair of electrodes.

16. The method according to claim 11 wherein the subsequent voltage is equal in magnitude to the end voltage.

17. A method for generating a multiphasic defibrillation/cardioversion waveform comprising the steps of:

determining an initial voltage of a first phase of said multiphasic waveform, and end voltage of the first phase of said multiphasic waveform, and time duration ratios of subsequent phases with respect to the first phase of said multiphasic waveform;

charging a capacitor to the initial voltage;

discharging the capacitor to the end voltage over a phase duration to end the first phase;

deriving a subsequent phase duration from the previous phase duration and said time duration ratios;

discharging the capacitor to a subsequent voltage across a pair of electrodes for the subsequent phase duration.

18. The method according to claim 17 further comprising sequentially repeating the subsequent phase derivation step and the subsequent phase discharge step until the capacitor is effectively discharged.

19. The method according to claim 17, wherein said initial voltage is applied to the pair of electrodes through a polarity reversing switch, further comprising, after the first phase discharging step, reversing said polarity reversing switch to produce an inverted voltage as applied across said pair of electrodes.

20. The method according to claim 17 wherein the subsequent voltage is equal in magnitude to the end voltage.

21. An apparatus for generating a multiphasic defibrillation/cardioversion waveform comprising:

a means for storing an initial voltage of a first phase of said multiphasic waveform, and end voltage of the first phase of said multiphasic waveform, and time duration ratios of subsequent phases with respect to the first phase of said multiphasic waveform;

means for applying the initial voltage across a pair of electrodes to begin the first phases;

means for reducing the initial voltage to said end voltage over a phase duration to end the first phase;

means for deriving a subsequent phase duration from the previous phase duration and said time duration ratios;

means for applying a subsequent voltage across said pair of electrodes;

means for reducing the subsequent voltage to a subsequent end voltage over said subsequent phase duration; and

means for reversing the voltage across said pair of electrodes during said subsequent phase.

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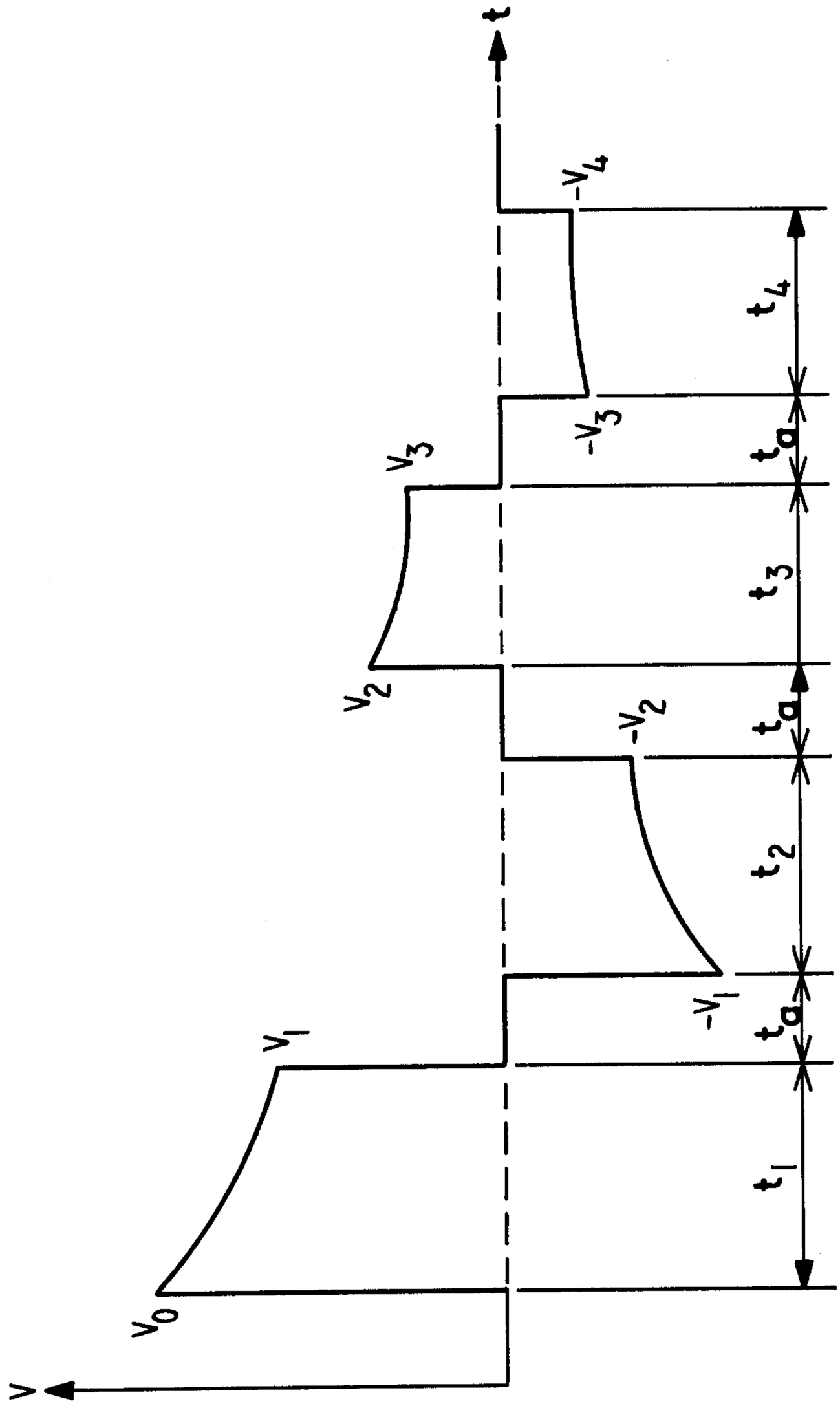


FIG. 1

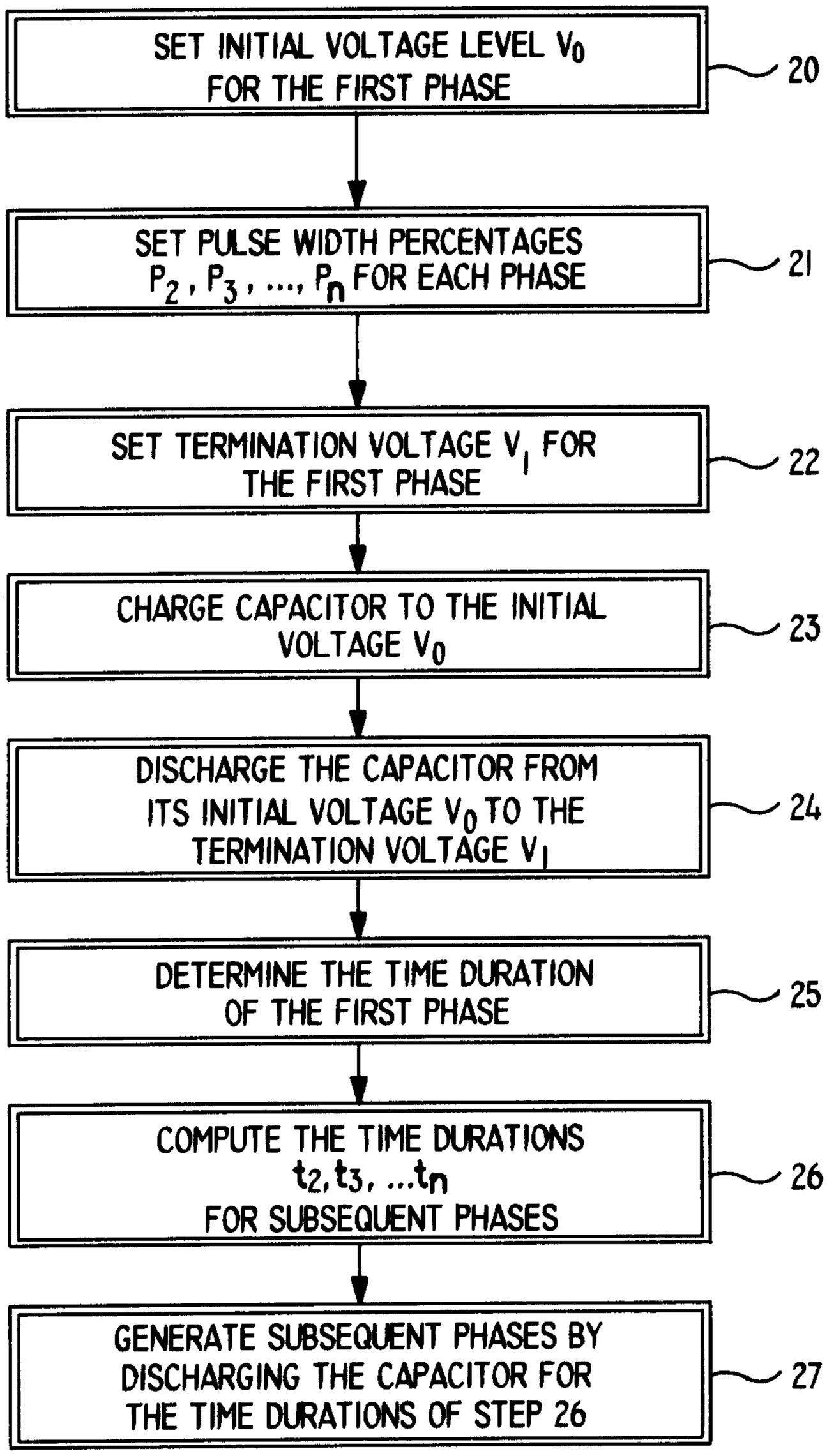
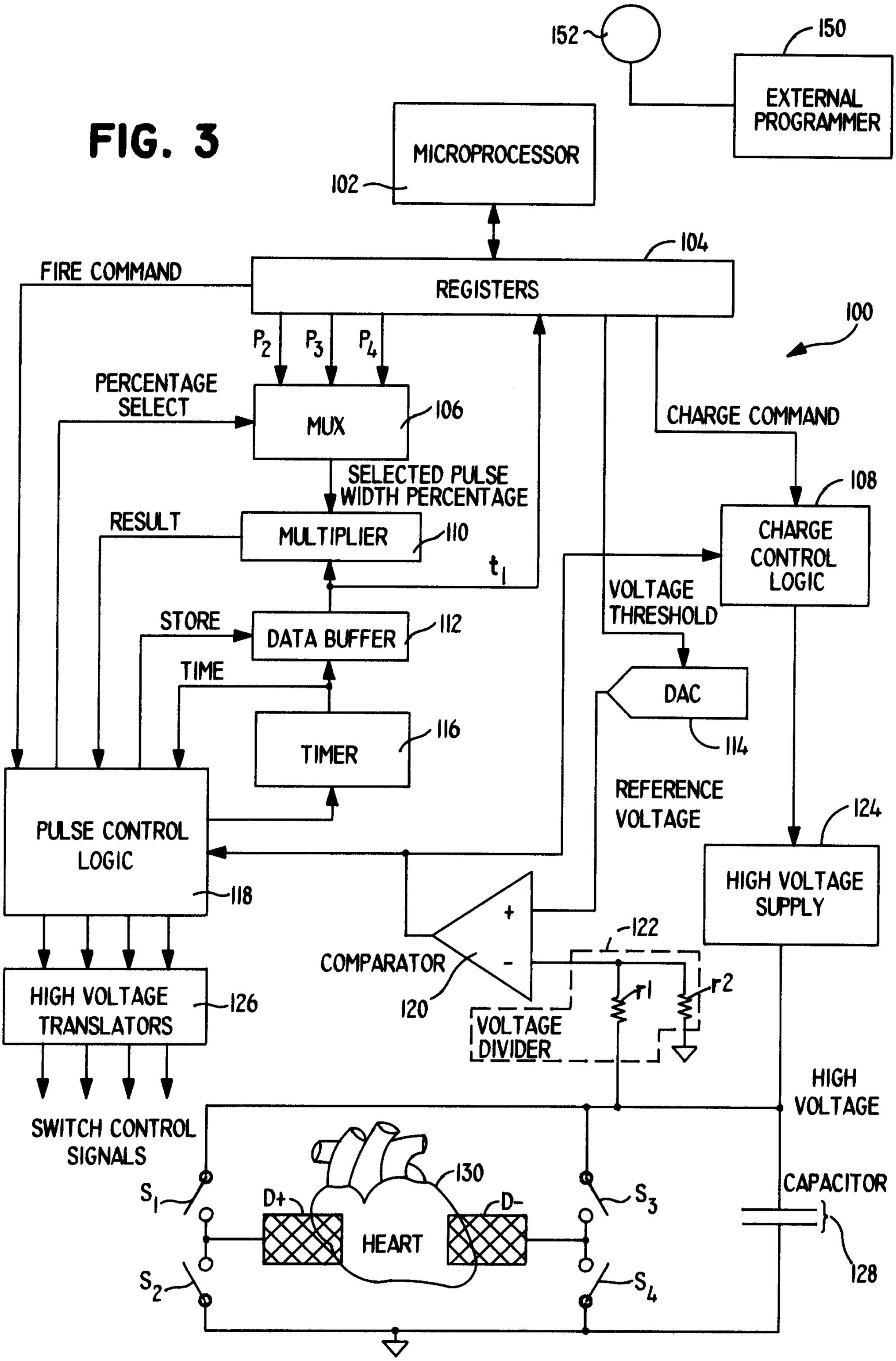

SET INITIAL VOLTAGE LEVEL V_0 FOR THE FIRST PHASE
20
SET PULSE WIDTH PERCENTAGES $P_2, P_3, \ldots, P_n$ FOR EACH PHASE
21
SET TERMINATION VOLTAGE V_1 FOR THE FIRST PHASE
22
CHARGE CAPACITOR TO THE INITIAL VOLTAGE V_0
23
DISCHARGE THE CAPACITOR FROM ITS INITIAL VOLTAGE V_0 TO THE TERMINATION VOLTAGE V_1
24
DETERMINE THE TIME DURATION OF THE FIRST PHASE
25
COMPUTE THE TIME DURATIONS $t_2, t_3, \ldots t_n$ FOR SUBSEQUENT PHASES
26
GENERATE SUBSEQUENT PHASES BY DISCHARGING THE CAPACITOR FOR THE TIME DURATIONS OF STEP 26
27

FIG. 2

FIG. 3


152
150
EXTERNAL PROGRAMMER
MICROPROCESSOR
102
104
REGISTERS
FIRE COMMAND
100
P_2
P_3
P_4
PERCENTAGE SELECT
MUX
106
CHARGE COMMAND
SELECTED PULSE WIDTH PERCENTAGE
108
RESULT
MULTIPLIER
110
CHARGE CONTROL LOGIC
t_1
VOLTAGE THRESHOLD
STORE
DATA BUFFER
112
TIME
DAC
TIMER
116
114
REFERENCE VOLTAGE
124
PULSE CONTROL LOGIC
118
HIGH VOLTAGE SUPPLY
+
-
122
COMPARATOR
120
r1
r2
HIGH VOLTAGE TRANSLATORS
126
VOLTAGE DIVIDER
HIGH VOLTAGE
SWITCH CONTROL SIGNALS
130
S_1
S_3
D+
D-
HEART
CAPACITOR
S_2
S_4
128

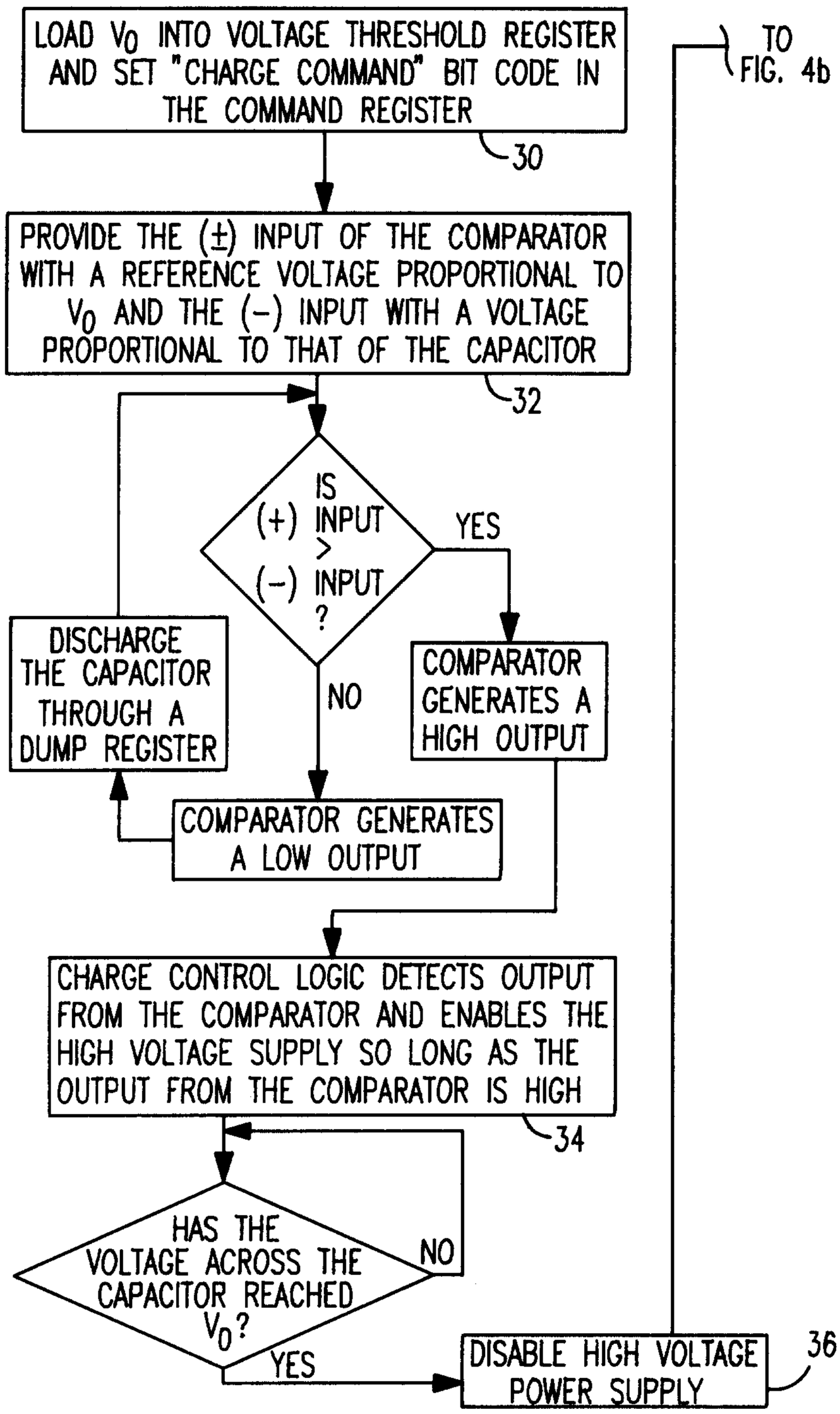

LOAD V_0 INTO VOLTAGE THRESHOLD REGISTER AND SET "CHARGE COMMAND" BIT CODE IN THE COMMAND REGISTER
30
PROVIDE THE (±) INPUT OF THE COMPARATOR WITH A REFERENCE VOLTAGE PROPORTIONAL TO V_0 AND THE (−) INPUT WITH A VOLTAGE PROPORTIONAL TO THAT OF THE CAPACITOR
32
IS (+) INPUT > (−) INPUT ?
YES
NO
DISCHARGE THE CAPACITOR THROUGH A DUMP REGISTER
COMPARATOR GENERATES A HIGH OUTPUT
COMPARATOR GENERATES A LOW OUTPUT
CHARGE CONTROL LOGIC DETECTS OUTPUT FROM THE COMPARATOR AND ENABLES THE HIGH VOLTAGE SUPPLY SO LONG AS THE OUTPUT FROM THE COMPARATOR IS HIGH
34
HAS THE VOLTAGE ACROSS THE CAPACITOR REACHED V_0?
NO
YES
DISABLE HIGH VOLTAGE POWER SUPPLY
36
TO FIG. 4b

FIG. 4a

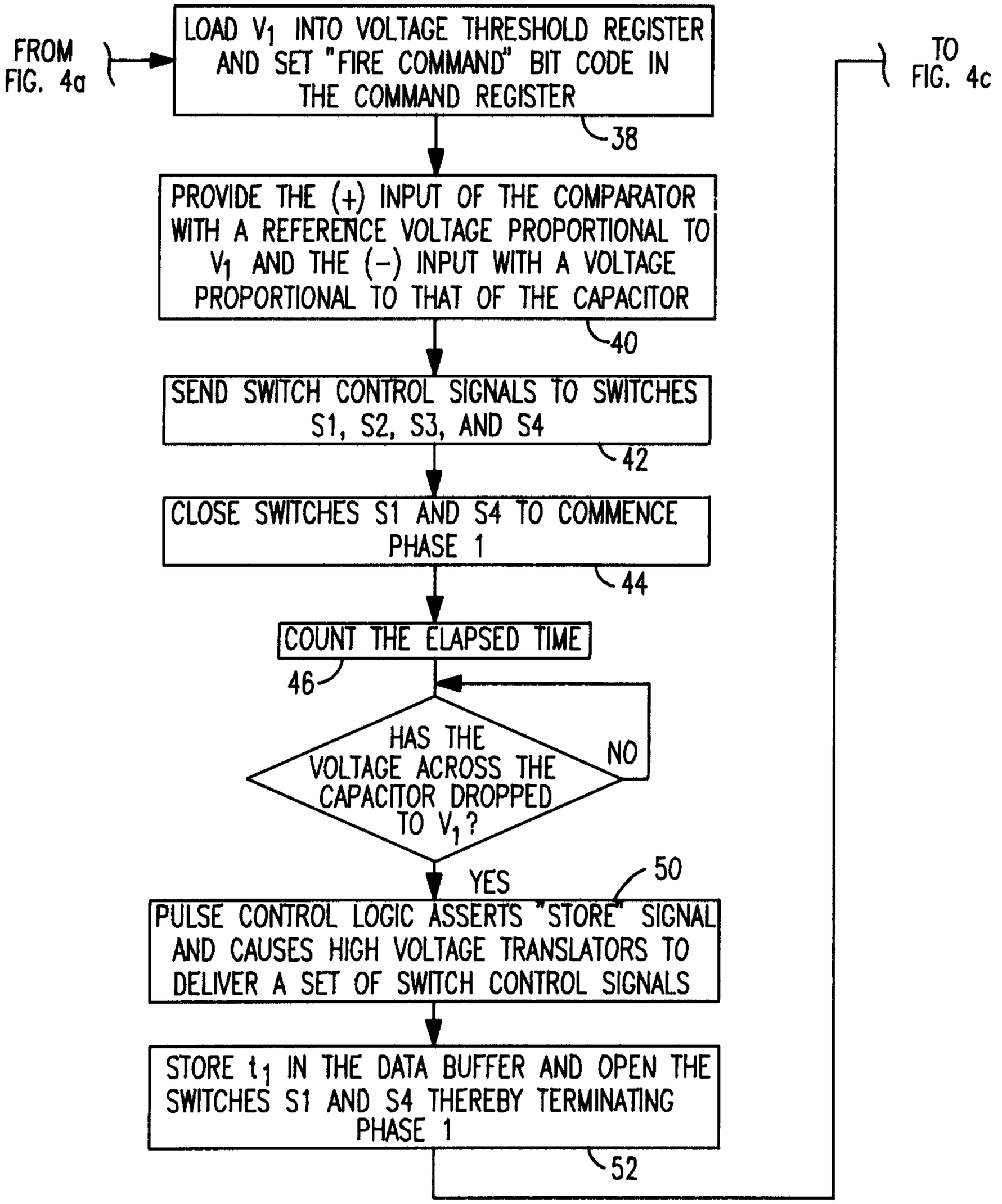

FROM FIG. 4a
LOAD V_1 INTO VOLTAGE THRESHOLD REGISTER AND SET "FIRE COMMAND" BIT CODE IN THE COMMAND REGISTER
38
PROVIDE THE (+) INPUT OF THE COMPARATOR WITH A REFERENCE VOLTAGE PROPORTIONAL TO V_1 AND THE (−) INPUT WITH A VOLTAGE PROPORTIONAL TO THAT OF THE CAPACITOR
40
SEND SWITCH CONTROL SIGNALS TO SWITCHES S1, S2, S3, AND S4
42
CLOSE SWITCHES S1 AND S4 TO COMMENCE PHASE 1
44
COUNT THE ELAPSED TIME
46
HAS THE VOLTAGE ACROSS THE CAPACITOR DROPPED TO V_1?
NO
YES
50
PULSE CONTROL LOGIC ASSERTS "STORE" SIGNAL AND CAUSES HIGH VOLTAGE TRANSLATORS TO DELIVER A SET OF SWITCH CONTROL SIGNALS
STORE t_1 IN THE DATA BUFFER AND OPEN THE SWITCHES S1 AND S4 THEREBY TERMINATING PHASE 1
52
TO FIG. 4c

FIG. 4b

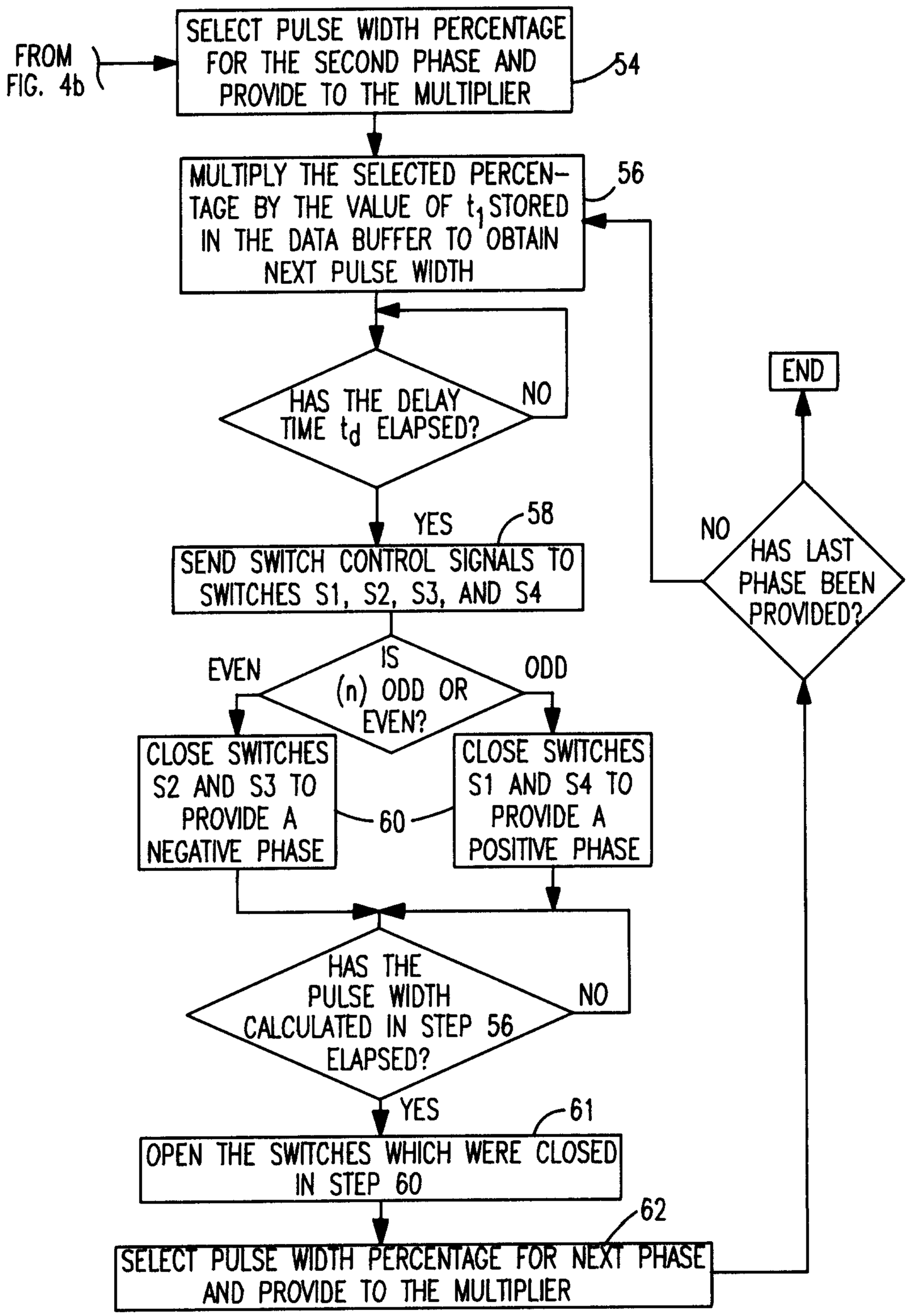
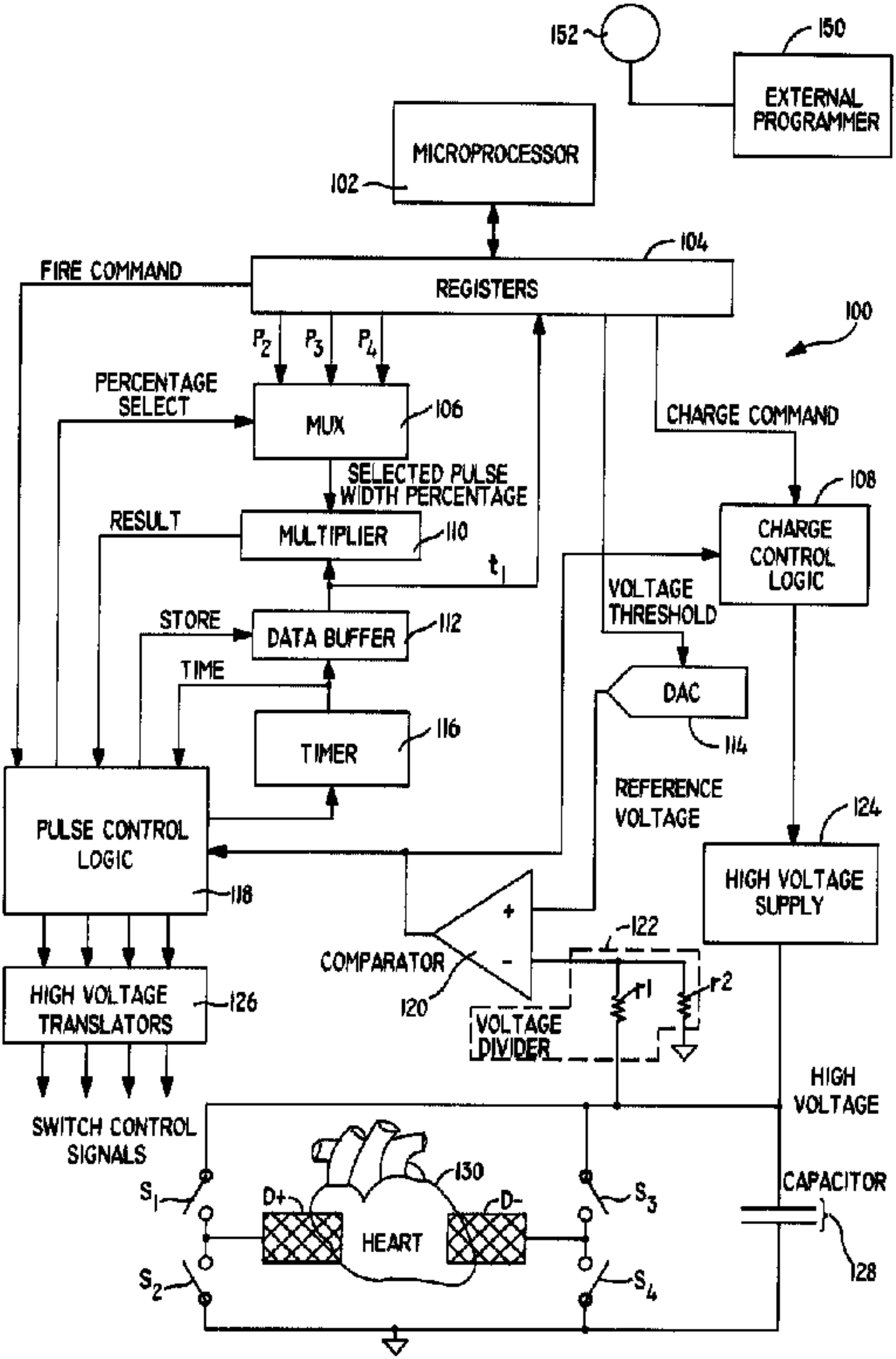

FROM FIG. 4b
SELECT PULSE WIDTH PERCENTAGE FOR THE SECOND PHASE AND PROVIDE TO THE MULTIPLIER
54
MULTIPLY THE SELECTED PERCENTAGE BY THE VALUE OF t_1 STORED IN THE DATA BUFFER TO OBTAIN NEXT PULSE WIDTH
56
HAS THE DELAY TIME t_d ELAPSED?
NO
YES
58
SEND SWITCH CONTROL SIGNALS TO SWITCHES S1, S2, S3, AND S4
IS (n) ODD OR EVEN?
EVEN
ODD
CLOSE SWITCHES S2 AND S3 TO PROVIDE A NEGATIVE PHASE
CLOSE SWITCHES S1 AND S4 TO PROVIDE A POSITIVE PHASE
60
HAS THE PULSE WIDTH CALCULATED IN STEP 56 ELAPSED?
NO
YES
61
OPEN THE SWITCHES WHICH WERE CLOSED IN STEP 60
62
SELECT PULSE WIDTH PERCENTAGE FOR NEXT PHASE AND PROVIDE TO THE MULTIPLIER
HAS LAST PHASE BEEN PROVIDED?
NO
END

FIG. 4c


152
150
EXTERNAL PROGRAMMER
MICROPROCESSOR
102
104
FIRE COMMAND
REGISTERS
100
P_2
P_3
P_4
PERCENTAGE SELECT
MUX
106
CHARGE COMMAND
SELECTED PULSE WIDTH PERCENTAGE
108
RESULT
MULTIPLIER
110
CHARGE CONTROL LOGIC
t_1
VOLTAGE THRESHOLD
STORE
DATA BUFFER
112
TIME
DAC
TIMER
116
114
REFERENCE VOLTAGE
PULSE CONTROL LOGIC
118
124
HIGH VOLTAGE SUPPLY
+
122
COMPARATOR
-
120
r1
r2
VOLTAGE DIVIDER
HIGH VOLTAGE TRANSLATORS
126
HIGH VOLTAGE
SWITCH CONTROL SIGNALS
130
S_1
D+
D-
S_3
CAPACITOR
HEART
S_2
S_4
128