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SYNAPSE MEMORY

TECHNICAL FIELD

[0001] The present invention relates to a synapse memory.

BACKGROUND

[0002] Recently, various techniques have been known regarding a synapse memory.

SUMMARY

[0003] According to an embodiment of the present invention, there is provided a synapse memory. The synapse memory includes plural synapse memory cells provided at cross points of plural axon lines and plural dendrite lines. Each synapse memory cell includes a memory device, a write transistor, and a common transistor. The memory device is configured to store a weight value, and is provided with a read terminal, a write terminal, and a common terminal. The read terminal is configured to receive a read signal to read the weight value stored in the memory device. The write terminal is configured to receive a write signal to write the weight value to the memory device. The common terminal is configured to output an output signal from the memory device or input an input signal to the memory device having received the read signal or the write signal, respectively. The write transistor is provided between the write terminal of the memory device and a write signal line configured to send the write signal. The common transistor is provided between the common terminal of the memory device and one of the dendrite lines.

[0004] According to another embodiment of the present invention, there is provided a synapse memory. The synapse memory includes plural synapse memory cells provided at cross points of plural axon lines and plural dendrite lines. Each synapse memory cell includes a memory device and a switch. The memory device is configured to store a weight value, and is provided with a read terminal, a write terminal, and a common terminal. The read terminal is configured to receive a read signal to read the weight value stored in the memory device. The write terminal is configured to receive a write signal to write the weight value to the memory device. The common terminal is configured to output an output signal from the memory device or input an input signal to the memory device having received the read signal or the write signal, respectively. The switch is configured to switch connection and disconnection between one of the dendrite lines and the common terminal of the memory device. If the weight value stored in a part of the plural synapse memory cells is to be read, each switch provided in the part of the plural synapse memory cells connects the one of the dendrite lines and the common terminal of the memory

device, and each switch provided in the other part of the plural synapse memory cells disconnects the one of the dendrite lines and the common terminal of the memory device.

[0005] According to yet another embodiment of the present invention, there is provided a device including a synapse memory. The synapse memory includes plural synapse memory cells provided at cross points of plural axon lines and plural dendrite lines. Each synapse memory cell includes a memory device, a write transistor, and a common transistor. The memory device is configured to store a weight value, and is provided with a read terminal, a write terminal, and a common terminal. The read terminal is configured to receive a read signal to read the weight value stored in the memory device. The write terminal is configured to receive a write signal to write the weight value to the memory device. The common terminal is configured to output an output signal from the memory device or input an input signal to the memory device having received the read signal or the write signal, respectively. The write transistor is provided between the write terminal of the memory device and a write signal line configured to send the write signal. The common transistor is provided between the common terminal of the memory device and one of the dendrite lines.

[0006] According to yet another embodiment of the present invention, there is provided a synapse memory. The synapse memory includes plural synapse memory cells provided at cross points of plural axon lines and plural dendrite lines. Each synapse memory cell includes a memory device, a write transistor, a common transistor, a read transistor. The memory device is configured to store a weight value, and is provided with a read terminal, a write terminal, and a common terminal. The read terminal is configured to receive a read signal to read the weight value stored in the memory device. The write terminal is configured to receive a write signal to write the weight value to the memory device. The common terminal is configured to output an output signal from the memory device or input an input signal to the memory device having received the read signal or the write signal, respectively. The write transistor is provided between the write terminal of the memory device and a write signal line configured to send the write signal. The common transistor is provided between the common terminal of the memory device and one of the dendrite lines. The read transistor is provided between the read terminal of the memory device and one of the axon lines. A first subgroup of the synapse memory cells is connected in common to one of the axons. A second subgroup of the synapse memory cells is connected in common to one of the dendrite lines. A gate of the common transistor provided in each of the first subgroup of the synapse memory cells is connected in common to a common control line configured to send a common transistor control signal. A gate of the write transistor provided in each of the second sub-plural synapse memory cells is connected in common to one of the write control lines. A gate of the read transistor provided in each of the second subgroup of the synapse memory cells is connected in common to a read signal line configured to send a read transistor control signal.

[0007] These and other features and advantages will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The following description will provide details of preferred embodiments with reference to the following figures wherein:

FIG. 1 depicts a synapse memory having a cross-bar array according to an exemplary embodiment of the present invention.

FIG. 2 depicts a synapse memory according to the exemplary embodiment.

FIG. 3 depicts a synapse memory cell system according to the exemplary embodiment.

FIG. 4 depicts one synapse memory cell at i-th row and j-th column and another synapse memory cell at m-th row and j-th column in the normal direction read operation.

FIG. 5 depicts time charts of the normal direction read operation.

FIG. 6 depicts one synapse memory cell at i-th row and j-th column and another synapse memory cell at i-th row and n-th column in the reverse direction read operation.

FIG. 7 depicts time charts of the reverse direction read operation.

FIG. 8 depicts one synapse memory cell at i-th row and j-th column and another synapse memory cell at m-th row and j-th column in the normal increment write operation.

FIG. 9 depicts time charts of the normal increment write operation.

FIG. 10 depicts one synapse memory cell at i-th row and j-th column and another synapse memory cell at m-th row and j-th column in the normal decrement write operation.

FIG. 11 depicts time charts of the normal decrement write operation.

FIG. 12 depicts an example of a device which includes the synapse memory.

FIG. 13 depicts one synapse memory cell at i-th row and j-th column and another synapse memory cell at m-th row and j-th column in the normal direction read operation according to the second exemplary embodiment of the present invention.

FIG. 14 depicts time charts of the normal direction read operation according to the second exemplary embodiment of the present invention.

FIG. 15 depicts one synapse memory cell at i-th row and j-th column and another synapse memory cell at m-th row and j-th column in the normal write operation according to the second exemplary embodiment of the present invention.

FIG. 16 depicts time charts of the normal write operation.

FIG. 17 depicts one synapse memory cell at i-th row and j-th column and another synapse memory cell at i-th row and n-th column in the reverse direction read operation according to the third exemplary embodiment of the present invention.

FIG. 18 depicts time charts of the reverse direction read operation according to the third exemplary embodiment of the present invention.

DETAILED DESCRIPTION

[0009] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the attached drawings.

[0010] It is to be noted that the present invention is not limited to these exemplary embodiments to be given below and may be implemented with various modifications within the scope of the present invention. In addition, the drawings used herein are for purposes of illustration, and may not show actual dimensions.

[0011] FIG. 1 depicts a synapse memory 100 having a cross-bar array according to an exemplary embodiment of the present invention.

[0012] Hardware implementation of a neuromorphic system may include synapse memories as well as neuron bodies and network connection with axons and dendrites. As shown in FIG. 1, the synapse memory 100 may include synapse memory cells 10 arranged/placed at all cross points of all axons (axon lines) 20 and all dendrites (dendrite lines) 30. Each of the synapse memory cells 10 may be configured to store a synapse weight value, which indicates a weight of synapse connection of the corresponding synapse memory cell 10. Note that the axons 20 correspond to respective axons of pre-neurons and the dendrites 30 correspond to respective dendrites of post-neurons.

[0013] In the present exemplary embodiment, the synapse memory cell 10 may include a memory device MD (see FIG. 3) to store the synapse weight value. The memory device MD may be a magnetoresistive random access memory (MRAM). For example, the memory device MD may be a spin transfer torque magnetoresistive random access memory (STT-MRAM).

[0014] Writing data to the memory device MD is executed by applying a voltage or a current to the memory device MD. The memory device MD can store a continuous value (analog value) or a multi-value (discrete value). Controlling the voltage value or the current value to be applied to the memory device MD enables to control the synapse weight value stored in the memory device MD. Note that the memory device MD can be used as an analog memory. In other words, the memory device MD can store and hold a value being one of at least three kinds of values. The memory device MD may have continuous mid-range resistance values, not only two very large and very small values.

[0015] FIG. 2 depicts a synapse memory 100 according to the exemplary embodiment.

[0016] As shown in FIG. 2, the synapse memory 100 may include the synapse memory cells 10 arranged in an array of $m \times n$ (m rows and n columns). The synapse memory 100 may also include lines extending along a row direction (the horizontal direction in FIG. 2) and lines extending along a column direction (the vertical direction in FIG. 2) to connect the synapse memory cells 10 to each other.

[0017] Here, the row lines include read-row lines $r_{rl0} - r_{rlm-1}$, write-row lines $w_{rl0} - w_{rlm-1}$, and read-write-row selects $rw_{rs0} - rw_{rsm-1}$. Note that the read-row lines $r_{rl0} - r_{rlm-1}$ correspond to the axons 20. That is to say, the write-row lines $w_{rl0} - w_{rlm-1}$ and the read-write-row selects $rw_{rs0} - rw_{rsm-1}$ are extending along the axons 20. The column lines include read-column selects $r_{cs0} - r_{csn-1}$, write-column selects $w_{cs0} - w_{csn-1}$, and read-write-column lines $rw_{cl0} - rw_{cln-1}$. Note that the read-write-column lines $rw_{cl0} - rw_{cln-1}$ correspond to the dendrites 30. That is to say, the read-column selects $r_{cs0} - r_{csn-1}$ and the write-column selects $w_{cs0} - w_{csn-1}$ are extending along the dendrites 30. Further, the read-write-row selects $rw_{rs0} - rw_{rsm-1}$, the read-column selects $r_{cs0} - r_{csn-1}$, and the write-column selects $w_{cs0} - w_{csn-1}$ are lines for signals to switch the circuits of the synapse memory cells 10. Details of each line will be described later.

[0018] Here, the synapse memory 100 performs read operation and write operation using the row lines and the column lines. In other words, the synapse memory 100 requires the row lines and the column lines to perform read and write accesses to each synapse memory cell 10.

[0019] The read operation for the synapse memory cell 10 is performed with multiple concurrent axon lines' (the row lines') activation to read a total current at one dendrite line. That is to say, in the read operation of the synapse weight value, a total synapse weight value is read for each dendrite 30. The total synapse weight value is a sum of the synapse weight values of the respective synapse memory cells 10 which are selected to be read.

[0020] Here, if array size of the synapse memory 100 is large (e.g. 1024×1024), the number of unselected synapse memory cell(s) 10, which is connected all in parallel, will be large. This may cause read disturb for the selected synapse memory cell(s) 10. The term "read disturb" may refer to an influence of the unselected synapse memory cell(s) on a result of the read operation. The unselected synapse memory cell(s) 10 is provided on the same dendrite 30 selected to be read in the read operation, as the selected synapse memory cell(s) 10.

[0021] FIG. 3 depicts a synapse memory cell system 1 according to the exemplary embodiment. In the following explanation, the synapse memory cell 10_{00} will be described as an example. The other synapse memory cells 10 (e.g. synapse memory cells 10_{10} , 10_{01} , 10_{11}) are configured similarly to the synapse memory cell 10_{00} .

[0022] As shown in FIG. 3, the synapse memory cell system 1 may include the synapse memory 100, read drivers 40, write drivers 50, and switching portions 60. The synapse memory cell system 1 can be a neuromorphic system on silicon. This exemplary embodiment assumes that writing the synapse weight value to the memory device MD included in the synapse memory 100 is executed by controlling the voltage value.

[0023] Here, as mentioned above referring to FIG. 1, the synapse memory 100 has the cross-bar array of the axons 20 and the dendrites 30, and includes the synapse memory cells 10 arranged at all cross points of the axons 20 and the dendrites 30. Each of the synapse memory cells 10 may include the memory device MD and three transistors, namely: a read transistor T_{RD} ; a write transistor T_{WT} ; and a common transistor T_{CM} . The three transistors are elements for switching circuits of the memory device MD (the synapse memory cell 10).

[0024] The memory device MD, i.e. the MRAM, may be provided with three independent ports. In other words, the memory device MD may be a three terminal device. Specifically, the memory device MD is provided with a read terminal RD, a write terminal WT, and a common terminal CM. The read terminal RD receives a read signal from the read driver 40. The write terminal WT receives a write signal from the write driver 50. The common terminal CM outputs a signal (output signal) from the memory device MD that has received the read signal or input a signal (input signal) to the memory device MD that has received the write signal.

[0025] The three transistors, i.e. the read transistor T_{RD} , the write transistor T_{WT} , and the common transistor T_{CM} , are respectively provided on the read terminal RD, the write terminal WT, and the common terminal CM. In other words, the three transistors are provided between ports of the memory device MD and row and column access lines.

[0026] For example, in the synapse memory cell 1000, the read transistor T_{RD} is provided between the read terminal RD and the read-row line r_{rl0} . The gate of the read transistor T_{RD} is connected to the read-column select r_{cs0} . The read transistor T_{RD} connects/disconnects the read terminal RD and the read-row line r_{rl0} . The write transistor T_{WT} is provided between the write terminal WT and the write-row line w_{rl0} . The gate of the write transistor T_{WT} is connected to the write-column select w_{cs0} . The write transistor T_{WT} connects/disconnects the write terminal WT and the write-row line w_{rl0} . The common transistor T_{CM} is provided between the common terminal CM and the read-write-column line rw_{cl0} . The gate of the common transistor T_{CM} is connected to the read-write-row select rw_{rs0} . The common transistor T_{CM} connects/disconnects the common terminal CM and the read-write-column line rw_{cl0} . The write-column select w_{cs0} is an example of the claimed write control line. The

read-write-row select rw_rs0 is an example of the claimed common control line. The read-column select r_cs0 is an example of the claimed read signal line.

[0027] A transistor driver (not shown) applies the voltage to the respective three transistors via the read-column select r_cs0 , the write-column select w_cs0 , and the read-write-row select rw_rs0 . In the shown example, the applied voltage to the gates of the respective three transistors is switched between a high voltage V_H and a low voltage V_L . If the high voltage V_H is applied to the gate, the transistor is turned ON, i.e. in a zero resistance state. If the low voltage V_L is applied to the gate, the transistor is turned OFF, i.e. in a high impedance (Hi-Z) state. That is to say, the three transistors independently connect/disconnect the memory device MD and the lines, i.e. the read-row line r_rl0 , the write-row line w_rl0 , and the read-write-column line rw_cl0 . Note that applying the voltage to the gate means assigning a control signal to the transistor. The applied voltage to the gate may define control timing and levels which implement read and write access. The applied voltage to the gate of the common transistor T_{CM} is an example of the claimed common transistor control signal. The applied voltage to the gate of the read transistor T_{RD} is an example of the claimed read transistor control signal.

[0028] The read driver 40 is connected to the synapse memory cells 10 via the read-row line r_rl0 (the axon 20). The read driver 40 may be configured to read the synapse weight value from the synapse memory cells 10 in response to a recognition operation input. In the example shown in the figure, the read driver 40 may be a digital driver to apply the voltage of a supply voltage V_{DC} or a read drive voltage $V_{DC}+V_{RD}$ to the read-row line r_rl0 .

[0029] The write driver 50 is connected to the synapse memory cells 10 via the write-row line w_rl0 . The write driver 50 may be configured to write (update) the synapse weight value to the respective synapse memory cells 10 in response to a learning operation input. In the shown example in the figure, the write driver 50 may be a digital or analog driver to apply the voltage of the supply voltage V_{DC} , an increment write voltage $V_{DC}+V_{WT}$, or a decrement write voltage $V_{DC}-V_{WT}$ to the write-row line w_rl0 .

[0030] To update the weight to be stored in the respective synapse memory cells 10 in the synapse memory 100 may be referred to as learning. The learning may include online learning and offline learning. In the online learning, every time the synapse memory 100 receives a set of data (or a part of all data), the weight of the synapse memory cell 10 receiving the set of data is updated using only the received set of data. In the offline learning, the weight of the respective synapse memory cells 10 is set based on data prepared in advance.

[0031] The switching portion 60 is connected to the read-write-column line rw_cl_0 (the dendrite 30). The switching portion 60 may include a three position switch 61, a current sensor 63, and a connecting line 65. The switching portion 60 switches a circuit via the current sensor 63 or via the connecting line 65.

[0032] Hereinafter, operation of the synapse memory cell 100 will be explained. As mentioned above, the synapse memory cell 100 performs the read operation and the write operation. In the example shown in the figure, the read operation may include a normal direction read operation which is performed in both the recognition and the learning operations, and a reverse direction read operation which is performed in only the learning operation. Further, the write operation may include a normal increment write operation which is performed to increase the weight value stored in the memory device MD, and a normal decrement write operation which is performed to decrease the weight value stored in the memory device MD. Both these write operations are performed in the learning operation.

[0033] In the following, the normal direction read operation, the reverse direction read operation, the normal increment write operation, and the normal decrement write operation will be explained in this order.

[0034] FIG. 4 depicts one synapse memory cell 10_{ij} at i -th row and j -th column and another synapse memory cell 10_{mj} at m -th row and j -th column in the normal direction read operation. FIG. 5 depicts time charts of the normal direction read operation.

[0035] Referring to FIGs. 4 and 5, the normal direction read operation of the synapse memory 100 will be explained. Here, the operation of the synapse memory cell 10_{ij} and the synapse memory cell 10_{mj} arranged along the column direction in the synapse memory 100 will be explained. The synapse memory cell 10_{ij} and the synapse memory cell 10_{mj} are an example of the claimed subgroup or the claimed second subgroup of the synapse memory cells. The present embodiment assumes that the synapse memory cell 10_{ij} is selected to be read and the synapse memory cell 10_{mj} is unselected to be read.

[0036] Firstly, at time t_{11} , the transistor driver (not shown) applies the high voltage V_H to the read-column select r_cs_j , so that the read transistors TR_{Dij} , TR_{Dmj} are turned ON. Further, the read driver 40 (see FIG. 3) applies the read drive voltage $V_{DC}+V_{RD}$ to the read-row line r_rl_i . That is to say, the read driver 40 outputs the read signal (read voltage $V_{DC} + V_{RD}$) to the read terminal RD of the synapse memory cell 10_{ij} .

[0037] Next, at time t_{12} , the transistor driver applies the high voltage V_H to the read-write-row select rw_rs_i , so that the common terminal CM of the memory device MD_{ij} outputs the signal from the memory device MD_{ij} that has received the read signal (read voltage) at its read terminal RD. This enables the current sensor 63 (see FIG. 3) provided on the read-write-column line rw_cl_j to read out the current including the current from the memory device MD_{ij} .

[0038] Next, at time t_{13} , the transistor driver applies the low voltage V_L to the read-write-row select rw_rs_i . Further, at time t_{14} , the transistor driver applies the low voltage V_L to the read-column select r_cs_j , and the read driver 40 applies the supply voltage V_{DC} to the read-row line r_rl_i .

[0039] Note that at time t_{12} , the transistor driver applies the low voltage V_L to the read-write-row select rw_rs_m while the transistor driver applies the high voltage V_H to the read-write-row select rw_rs_i . That is to say, the common transistor $T_{CM_{mj}}$ disconnects the memory device MD_{mj} and the read-write-column line rw_cl_j . This prevents the common terminal CM of the memory device MD_{mj} from outputting the signal from the memory device MD_{mj} , which is unselected to be read. Disconnecting the memory device MD_{mj} unselected to be read and the read-write-column line rw_cl_j enables to avoid the read disturb. In this example, the read-row line r_rl_m may be in any voltage or a high-impedance. In other words, care for the voltage of the read-row line r_rl_m is optional.

[0040] FIG. 6 depicts one synapse memory cell 10_{ij} at i -th row and j -th column and another synapse memory cell 10_{in} at i -th row and n -th column in the reverse direction read operation. FIG. 7 depicts time charts of the reverse direction read operation.

[0041] Referring to FIGs. 6 and 7, the reverse direction read operation of the synapse memory 100 will be explained. Here, the operation of the synapse memory cell 10_{ij} and the synapse memory cell 10_{in} arranged along the row direction in the synapse memory 100 will be explained. The synapse memory cell 10_{ij} and the synapse memory cell 10_{in} are an example of the claimed subgroup or the first subgroup of the synapse memory cells. The present embodiment assumes that the synapse memory cell 10_{ij} is selected to be read and the synapse memory cell 10_{in} is unselected to be read. In the reverse direction read operation, the signal flows in a direction opposite to the normal direction read operation shown in FIG. 4.

[0042] Specifically, at time t_{21} , the transistor driver (not shown) applies the high voltage V_H to the read-write-row select rw_rs_i , so that the common transistors T_{CMij} , T_{CMin} are turned ON. Further, the read-write-column line rw_cl_j is applied with the read drive voltage $V_{DC}+V_{RD}$. That is to say, the memory device MD_{ij} receives the read signal (read voltage) at its common terminal CM.

[0043] Next, at time t_{22} , the transistor driver applies the high voltage V_H to the read-column select r_cs_j , so that the read terminal RD of the memory device MD_{ij} outputs the signal from the memory device MD_{ij} that has received the read signal (read voltage) at its common terminal CM. The current from the memory device MD_{ij} is read at the end of the read-row line r_rl_i .

[0044] Next, the transistor driver applies the low voltage V_L to the read-column select r_cs_j at time t_{23} , and then applies the low voltage V_L to the read-write-row select rw_rs_i at time t_{24} . Further, the read-write-column line rw_cl_j is applied with the supply voltage V_{DC} at time t_{24} .

[0045] Note that at time t_{22} , the transistor driver applies the low voltage V_L to the read-column select r_cs_n while the transistor driver applies the high voltage V_H to the read-column select r_cs_j . That is to say, the read transistor T_{RDin} disconnects the memory device MD_{in} and the read-row line r_rl_i . This prevents the read terminal RD of the memory device MD_{in} from outputting the signal from the memory device MD_{in} , which is unselected to be read. Disconnecting the memory device MD_{in} unselected to be read and the read-row line r_rl_i enables to avoid the read disturb. In this example, the read-write column line rw_cl_n may be in any voltage or a high-impedance. In other words, care for the voltage of the read-write-column line rw_cl_n is optional.

[0046] FIG. 8 depicts one synapse memory cell 10_{ij} at i -th row and j -th column and another synapse memory cell 10_{mj} at m -th row and j -th column in the normal increment write operation. FIG. 9 depicts time charts of the normal increment write operation.

[0047] Referring to FIGs. 8 and 9, the normal increment write operation of the synapse memory 100 will be explained. The present embodiment assumes that the synapse memory cell 10_{ij} is selected to be written and the synapse memory cell 10_{mj} is unselected to be written.

[0048] Firstly, at time t_{31} , the transistor driver (not shown) applies the high voltage V_H to the read-write-row select rw_rs_i , so that the common transistor T_{CMij} is turned ON.

[0049] Next, at time t_{32} , the write driver 50 (see FIG. 3) applies the increment write voltage $V_{DC}+V_{WT}$ to the write-row line w_rl_i .

[0050] Next, at time t_{33} , the transistor driver applies the high voltage V_H to the write-column select w_cs_j , so that the write transistor T_{WTij} is turned ON. This enables the write terminal WT of the memory device MD_{ij} to receive the increment write signal (write voltage $V_{DC} + V_{WT}$) from the write driver 50 to increase the weight value stored in the memory device MD_{ij} .

[0051] Next, at time t_{34} , the transistor driver applies the low voltage V_L to the write-column select w_cs_j . At time t_{35} , the write driver 50 then applies the supply voltage V_{DC} to the write-row line w_rl_i . At time t_{36} , the transistor driver then applies the low voltage V_L to the read-write-row select rw_rs_i .

[0052] Note that at time t_{31} , the transistor driver applies the low voltage V_L to the read-write-row select rw_rs_m while the transistor driver applies the high voltage V_H to the read-write-row select rw_rs_i . That is to say, the common transistor T_{CMmj} disconnects the memory device MD_{mj} and the read-write-column line rw_cl_j . This prevents the common terminal CM of the memory device MD_{mj} from outputting the write current from the memory device MD_{mj} , which is unselected to be written. In this example, the write-row line w_rl_m may be in any voltage or a high-impedance. In other words, care for the voltage of the write-row line w_rl_m is optional.

[0053] FIG. 10 depicts one synapse memory cell 10_{ij} at i -th row and j -th column and another synapse memory cell 10_{mj} at m -th row and j -th column in the normal decrement write operation. FIG. 11 depicts time charts of the normal decrement write operation.

[0054] Referring to FIGs. 10 and 11, the normal decrement write operation of the synapse memory 100 will be explained. The present embodiment assumes that the synapse memory cell 10_{ij} is selected to be written and the synapse memory cell 10_{mj} is unselected to be written. The normal decrement write operation is generally the same

as the above normal increment write operation shown in FIGs. 8 and 9 except for the applied voltage to the write-row line w_{rli} .

[0055] Firstly, at time $t41$, the transistor driver (not shown) applies the high voltage V_H to the read-write-row select rw_{rsi} , so that the common transistor T_{CMij} is turned ON.

[0056] Next, at time $t42$, the write driver 50 (see FIG. 3) applies the decrement write voltage $V_{DC}-V_{WT}$ to the write-row line w_{rli} .

[0057] Next, at time $t43$, the transistor driver applies the high voltage V_H to the write-column select w_{csj} , so that the write transistor T_{WTij} is turned ON. This enables the write terminal WT of the memory device MD_{ij} to receive the decrement write signal (write voltage $V_{DC} - V_{WT}$) from the write driver 50 to decrease the weight value stored in the memory device MD_{ij} .

[0058] Next, at time $t44$, the transistor driver applies the low voltage V_L to the write-column select w_{csj} . At time $t45$, the write driver 50 then applies the supply voltage V_{DC} to the write-row line w_{rli} . At time $t46$, the transistor driver then applies the low voltage V_L to the read-write-row select rw_{rsi} .

[0059] Note that at time $t41$, the transistor driver applies the low voltage V_L to the read-write-row select rw_{rsm} while the transistor driver applies the high voltage V_H to the read-write-row select rw_{rsi} . This prevents the common terminal CM of the memory device MD_{mj} from inputting the write current to the memory device MD_{mj} , which is unselected to be written. In this example, the write-row line w_{rlm} may be in any voltage or a high-impedance. In other words, care for the voltage of the write-row line w_{rlm} is optional.

[0060] As mentioned above, the common transistors T_{CM} are used to prevent unselected memory devices MDs from connecting with the read-write-column lines $rw_{cl0} - rw_{rsn-1}$. This may address the read disturb problem and enable an array size to be larger. Further, the read operation and the write operation are implemented independently without any undesired input to the memory devices MDs and undesired output from the memory devices MDs.

[0061] FIG. 12 depicts an example of a device 1010 which includes the synapse memory 100.

[0062] As shown in FIG. 12, the synapse memory 100 may be provided on the device 1010, such as a computer. In the shown example, multiple neuro-synaptic core systems 1000 are provided on a chip 1001, such as a semiconductor chip. The chip 1001 is then mounted on the device 1010.

[0063] Each of the neuro-synaptic core systems 1000 includes the synapse memory 100 and a neuron body 700. The neuron body 700 performs neuron operations. Specifically, the neuron body 700 obtains the product-sum value of the synapse weight value and input value based on the total current sensed by the current sensor 63 (see FIG. 3). The total current sensed by the current sensor 63 may represent the product-sum value of the synapse weight values stored in the synapse memory cells 10 on the cross points of the selected axon(s) 20 and the dendrites 30 and the input values. Then, the neuron body 700 outputs neuron output corresponding to the total current value.

[0064] Here, the neuro-synaptic core systems 1000 are connected to each other via the axons 20. The synapse memory 100 is connected to a pre-neuron via the axon 20. The neuron body 700 is a part of the post-neuron and its output is axon 20 which is connected to synapse memories 100 in the same or other neuro-synaptic core systems 1000. The synapse memory 100 receives an output signal from the pre-neuron to accumulate the weight values of the synapses whose inputs are activated via their axons 20. If the accumulated synapse weight value reaches a predetermined threshold, the neuron body 700 outputs the output signal as the neuron output of the post-neuron.

[0065] FIG. 13 depicts one synapse memory cell $10A_{ij}$ at i -th row and j -th column and another synapse memory cell $10A_{mj}$ at m -th row and j -th column in the normal direction read operation according to the second exemplary embodiment of the present invention. FIG. 14 depicts time charts of the normal direction read operation according to the second exemplary embodiment of the present invention. In FIGs. 13 and 14, the same structures as those of the exemplary embodiment shown in FIG. 3 are denoted by the same reference numerals, and the detailed explanation thereof will be omitted.

[0066] The configuration of the synapse memory cell 10 is not limited to the above mentioned exemplary embodiment. For example, if the reverse direction read operation, i.e. the back propagation, is not required for the synapse memory 100, the synapse memory cell 10 may be configured as shown in FIG. 13.

[0067] In the synapse memory cell $10A_{ij}$ and the synapse memory cell $10A_{mj}$, the read transistor T_{RD} (shown in FIG. 3) is not provided. In other words, the synapse memory cell $10A_{ij}$ and the synapse memory cell $10A_{mj}$ may respectively include two transistors, namely: the write transistor T_{WT} and the common transistor T_{CM} .

[0068] A cell size of the synapse memory cell 10A_{ij} (the synapse memory cell 10A_{mj}) may be smaller than the synapse memory cell 10 shown in FIG. 3 by a space for the read transistor T_{RD}. In other words, the synapse memory cells 10A_{ij} and 10A_{mj} are smaller than the synapse memory cell 10 by one (1) transistor space.

[0069] Further, in the synapse memory 100A, control of the read transistor T_{RD} is not required. That is to say, timing control is simpler than the synapse memory shown in FIG. 3 due to fewer control signals.

[0070] Referring to FIGs. 13 and 14, the normal direction read operation of the synapse memory 100A will be explained. The second exemplary embodiment assumes that the synapse memory cell 10A_{ij} is selected to be read and the synapse memory cell 10A_{mj} is unselected to be read.

[0071] Firstly, at time t₅₁, the read driver 40 (see FIG. 3) applies the read drive voltage V_{DC}+V_{RD} to the read-row line r_{rl}_i. That is to say, the read driver 40 outputs the read signal to the synapse memory cell 10A_{ij}.

[0072] Next, at time t₅₂, the transistor driver applies the high voltage V_H to the read-write-row select rw_{rs}_i, so that the common terminal CM of the memory device MD_{ij} outputs the signal from the memory device MD_{ij} that has received the read signal. This enables the current sensor 63 (see FIG. 3) to read out the current including the current from the memory device MD_{ij}.

[0073] Next, at time t₅₃, the transistor driver applies the low voltage V_L to the read-write-row select rw_{rs}_i. Further, at time t₅₄, the read driver 40 applies the supply voltage V_{DC} to the read-row line r_{rl}_i.

[0074] Note that at time t₅₂, the transistor driver applies the low voltage V_L to the read-write-row select rw_{rs}_m while the transistor driver applies the high voltage V_H to the read-write-row select rw_{rs}_i. That is to say, the common transistor T_{CM}_{mj} disconnects the memory device MD_{mj} and the read-write-column line rw_{cl}_j. This prevents the common terminal CM of the memory device MD_{mj} from outputting the signal from the memory device MD_{mj}, which is unselected to be read.

[0075] FIG. 15 depicts one synapse memory cell 10A_{ij} at *i*-th row and *j*-th column and another synapse memory cell 10A_{mj} at *m*-th row and *j*-th column in the normal write operation according to the second exemplary embodiment of the present invention. FIG. 16 depicts time charts of the normal write operation.

[0076] Referring to FIGs. 15 and 16, the normal write operation including the normal increment write operation and the normal decrement write operation of the synapse memory 100A will be explained. The present embodiment assumes that the synapse memory cell $10A_{ij}$ is selected to be written and the synapse memory cell $10A_{mj}$ is unselected to be written.

[0077] Firstly, at time $t71$, the transistor driver (not shown) applies the high voltage V_H to the read-write-row select rw_rs_i , so that the common transistor T_{CMij} is turned ON. Further, the write driver 50 (see FIG. 3) applies the increment write voltage $V_{DC}+V_{WT}$ to the write-row line w_rl_i .

[0078] Next, at time $t72$, the transistor driver applies the high voltage V_H to the write-column select w_cs_j , so that the write transistor T_{WTij} is turned ON. This enables the write terminal WT to receive the write signal from the write driver 50 to increase the weight value stored in the memory device MD_{ij} .

[0079] Next, at time $t73$, the transistor driver applies the low voltage V_L to the write-column select w_cs_j , so that the write transistor T_{WTij} is turned OFF.

[0080] Next, at time $t74$, the write driver 50 then applies the supply voltage V_{DC} to the write-row line w_rl_i . Further, the transistor driver applies the low voltage V_L to the read-write-row select rw_rs_i , so that the common transistor T_{CMij} is turned OFF.

[0081] Next, at time $t75$, the transistor driver applies the high voltage V_H to the read-write-row select rw_rs_i , so that the common transistor T_{CMij} is turned ON. Further, the write driver 50 applies the decrement write voltage $V_{DC}-V_{WT}$ to the write-row line w_rl_i .

[0082] Next, at time $t76$, the transistor driver applies the high voltage V_H to the write-column select w_cs_j , so that the write transistor T_{WTij} is turned ON. This enables the write terminal WT of the memory device MD_{ij} to receive the write signal from the write driver 50 to decrease the weight value stored in the memory device MD_{ij} .

[0083] Next, at time t_{77} , the transistor driver applies the low voltage V_L to the write-column select w_{csj} . Further, at time t_{78} , the write driver 50 then applies the supply voltage V_{DC} to the write-row line w_{rli} , and the transistor driver applies the low voltage V_L to the read-write-row select rw_{rsi} .

[0084] FIG. 17 depicts one synapse memory cell $10A_{ij}$ at i -th row and j -th column and another synapse memory cell $10A_{in}$ at i -th row and n -th column in the reverse direction read operation according to the second exemplary embodiment of the present invention. FIG. 18 depicts time charts of the reverse direction read operation according to the second exemplary embodiment of the present invention.

[0085] As shown in FIGs. 17 and 18, if the synapse memory 100A was required to conduct the reverse direction read operation (the back propagation operation), the read disturb would occur due to the influence of the memory cells 10 provided on the same read-row line r_{rli} (the identical axon 20) as the synapse memory cell $10A_{ij}$ to be read. To avoid the read disturb in the reverse direction read operation, the read transistor T_{RD} (shown in FIG. 3) is required to be provided on the read terminal RD.

[0086] Next, an alternative exemplary embodiment will be described. In the above exemplary embodiments, the memory device MD is the MRAM. As long as the memory device MD is the three terminal device, the memory device MD can be another device. For example, the memory device MD can be a nonvolatile random access memory (NVRAM), such as a flash memory, a ferroelectric random access memory (FeRAM), a phase change random access memory (PRAM), and a resistive random access memory (ReRAM).

[0087] In the above exemplary embodiment, three transistors, i.e. the read transistor T_{RD} , the write transistor T_{WT} , and the common transistor T_{CM} , are explained as switching elements, i.e. switches, for the memory device MD. The transistor is not limited to a specific transistor. For example, the transistor can be a metal oxide semiconductor field effect transistor or a bipolar transistor. Alternatively, a diode or a thyristor can be provided instead of the transistor as long as such an element is capable of switching the circuits of the memory device MD.

[0088] In the above exemplary embodiment, one read driver 40 and one write driver 50 are provided for one axon 20. However, the one read driver 40 and the one write driver 50 are not required to be provided for each axon 20 dedicatedly. In other words, the read driver 40 and the write driver 50 can be provided for multiple axons 20. That is to say, the number of the read drivers 40 and the write drivers 50 can be equal to or less than the number of the axons 20.

[0089] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

CLAIMS

1. A synapse memory comprising a plurality of synapse memory cells provided at cross points of a plurality of axon lines and a plurality of dendrite lines, wherein
each synapse memory cell comprises:
a memory device configured to store a weight value, the memory device being provided with a read terminal, a write terminal, and a common terminal, the read terminal being configured to receive a read signal to read the weight value stored in the memory device, the write terminal being configured to receive a write signal to write the weight value to the memory device, the common terminal being configured to output an output signal from the memory device having received the read signal or to input an input signal to the memory device having received the write signal;
a write transistor provided between the write terminal of the memory device and a write signal line configured to send the write signal; and
a common transistor provided between the common terminal of the memory device and one of the dendrite lines.
2. The synapse memory according to claim 1, wherein
each synapse memory cell further comprises a read transistor provided between the read terminal of the memory device and one of the plurality of axon lines.
3. The synapse memory according to claim 1, wherein
the memory device is a magnetoresistive random access memory (MRAM).
4. The synapse memory according to claim 1, wherein
a subgroup of the synapse memory cells is connected in common to one of the plurality of axon lines, and
a gate of the common transistor provided in each of the subgroup of the synapse memory cells is connected in common to a common control line configured to send a common transistor control signal.
5. The synapse memory according to claim 1, wherein
a subgroup of the synapse memory cells is connected in common to one of the plurality of dendrite lines,
and
a gate of the write transistor provided in each of the subgroup of the synapse memory cells is connected in common to one of a plurality of the write control lines.
6. The synapse memory according to claim 2, wherein

a subgroup of the synapse memory cells is connected in common to one of the plurality of dendrite lines, and

a gate of the read transistor provided in each of the subgroup of the synapse memory cells is connected in common to a read signal line configured to send a read transistor control signal.

7. The synapse memory according to claim 2, wherein

if the weight value stored in a part of the plurality of the synapse memory cells is to be read, each common transistor provided in the part of the plurality of the synapse memory cells is turned on and each common transistor provided in at least one of the other part of the plurality of the synapse memory cells is turned off.

8. The synapse memory according to claim 7, wherein

if the weight value stored in the part of the plurality of the synapse memory cells is to be read, each read transistor provided in the part of the plurality of the synapse memory cells is turned on and each write transistor provided in the part of the plurality of the synapse memory cells is turned off.

9. The synapse memory according to claim 2, wherein

if the weight value is to be written in a part of the plurality of the synapse memory cells, each common transistor provided in the part of the plurality of the synapse memory cells is turned on and each common transistor provided in at least one of the other part of the plurality of the synapse memory cells is turned off.

10. The synapse memory according to claim 9, wherein

if the weight value is to be written in the part of the plurality of the synapse memory cells, each read transistor provided in the part of the plurality of the synapse memory cells is turned off and each write transistor provided in the part of the plurality of the synapse memory cells is turned on.

11. A synapse memory comprising a plurality of synapse memory cells provided at cross points of a plurality of axon lines and a plurality of dendrite lines, wherein

each synapse memory cell comprises:

a memory device configured to store a weight value, the memory device being provided with a read terminal, a write terminal, and a common terminal, the read terminal being configured to receive a read signal to read the weight value stored in the memory device, the write terminal being configured to receive a write signal to write the weight value to the memory device, the common terminal being configured to output an output signal from the memory device having received the read signal or to input an input signal to the memory device having received the write signal; and

a switch configured to switch connection and disconnection between one of the plurality of dendrite lines and the common terminal of the memory device, and

if the weight value stored in a part of the plurality of the synapse memory cells is to be read, each switch provided in the part of the plurality of the synapse memory cells connects the one of the plurality of dendrite lines and the common terminal of the memory device, and each switch provided in at least one of the other part of the plurality of the synapse memory cells disconnects the one of the plurality of dendrite lines and the common terminal of the memory device.

12. The synapse memory according to claim 11, wherein the switch is a transistor.

13. A device comprising a synapse memory, wherein the synapse memory comprises a plurality of synapse memory cells provided at cross points of a plurality of axon lines and a plurality of dendrite lines, and

each synapse memory cell comprises:

a memory device configured to store a weight value, the memory device being provided with a read terminal, a write terminal, and a common terminal, the read terminal being configured to receive a read signal to read the weight value stored in the memory device, the write terminal being configured to receive a write signal to write the weight value to the memory device, the common terminal being configured to output an output signal from the memory device having received the read signal or to input an input signal to the memory device having received the write signal;

a write transistor provided between the write terminal of the memory device and a write signal line configured to send the write signal; and

a common transistor provided between the common terminal of the memory device and one of the plurality of dendrite lines.

14. A synapse memory comprising a plurality of synapse memory cells provided at cross points of a plurality of axon lines and a plurality of dendrite lines, wherein

each synapse memory cell comprises:

a memory device configured to store a weight value, the memory device being provided with a read terminal, a write terminal, and a common terminal, the read terminal being configured to receive a read signal to read the weight value stored in the memory device, the write terminal being configured to receive a write signal to write the weight value to the memory device, the common terminal being configured to output an output signal from the memory device having received the read signal or to input an input signal to the memory device having received the write signal;

a write transistor provided between the write terminal of the memory device and a write signal line configured to send the write signal;

a common transistor provided between the common terminal of the memory device and one of the plurality of dendrite lines; and

a read transistor provided between the read terminal of the memory device and one of the plurality of axon lines,

a first subgroup of the synapse memory cells is connected in common to one of the plurality of axon lines,
a second subgroup of the synapse memory cells is connected in common to one of the plurality of dendrite lines,

a gate of the common transistor provided in each of the first subgroup of the synapse memory cells is connected in common to a common control line configured to send a common transistor control signal,

a gate of the write transistor provided in each of the second subgroup of the synapse memory cells is connected in common to one of the write control lines, and

a gate of the read transistor provided in each of the second subgroup of the synapse memory cells is connected in common to a read control line configured to send a read transistor control signal.

15. A method for reading a weight value stored in a synapse memory, wherein

the synapse memory comprises a plurality of synapse memory cells provided at cross points of a plurality of axon lines and a plurality of dendrite lines,

each synapse memory cell comprises:

a memory device configured to store a weight value, the memory device being provided with a read terminal, a write terminal, and a common terminal, the read terminal being configured to receive a read signal to read the weight value stored in the memory device, the write terminal being configured to receive a write signal to write the weight value to the memory device, the common terminal being configured to output an output signal from the memory device having received the read signal or to input an input signal to the memory device having received the write signal;

a write transistor provided between the write terminal of the memory device and a write signal line configured to send the write signal;

a common transistor provided between the common terminal of the memory device and one of the plurality of dendrite lines; and

a read transistor provided between the read terminal of the memory device and one of the plurality of axon lines, and

the method comprises reading the weight value of a part of the plurality of the synapse memory cells in a state where the write transistor is turned off, the common transistor is turned on, and the read transistor is turned on.

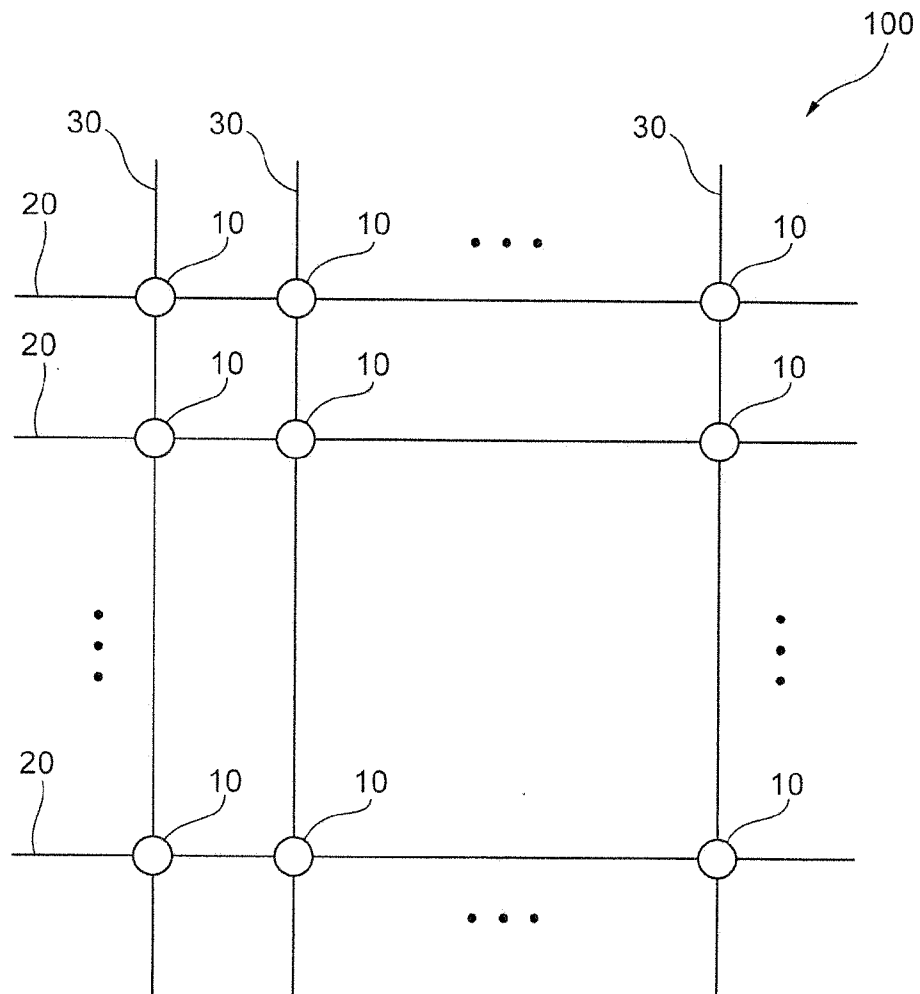


FIG. 1

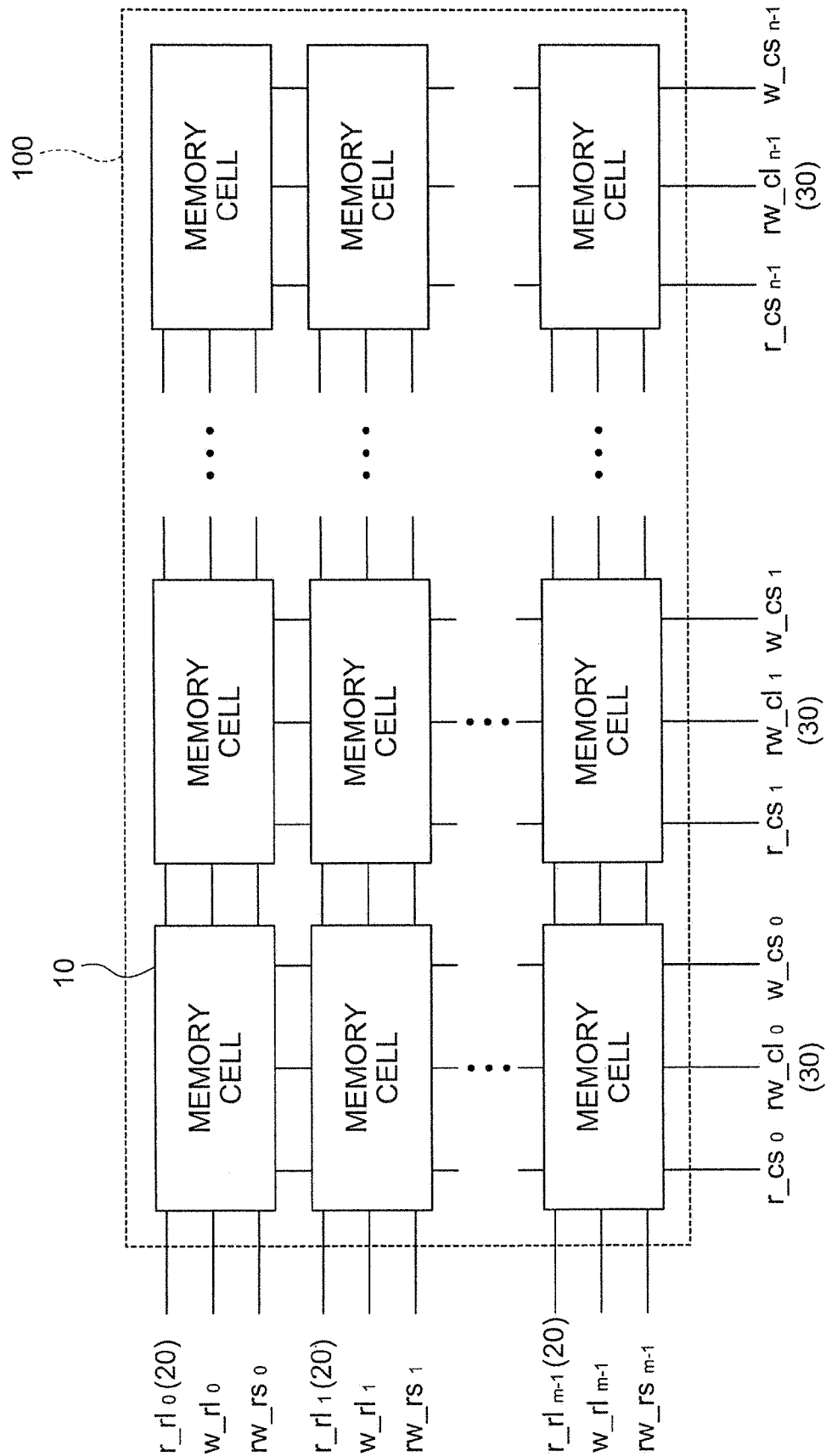


FIG. 2

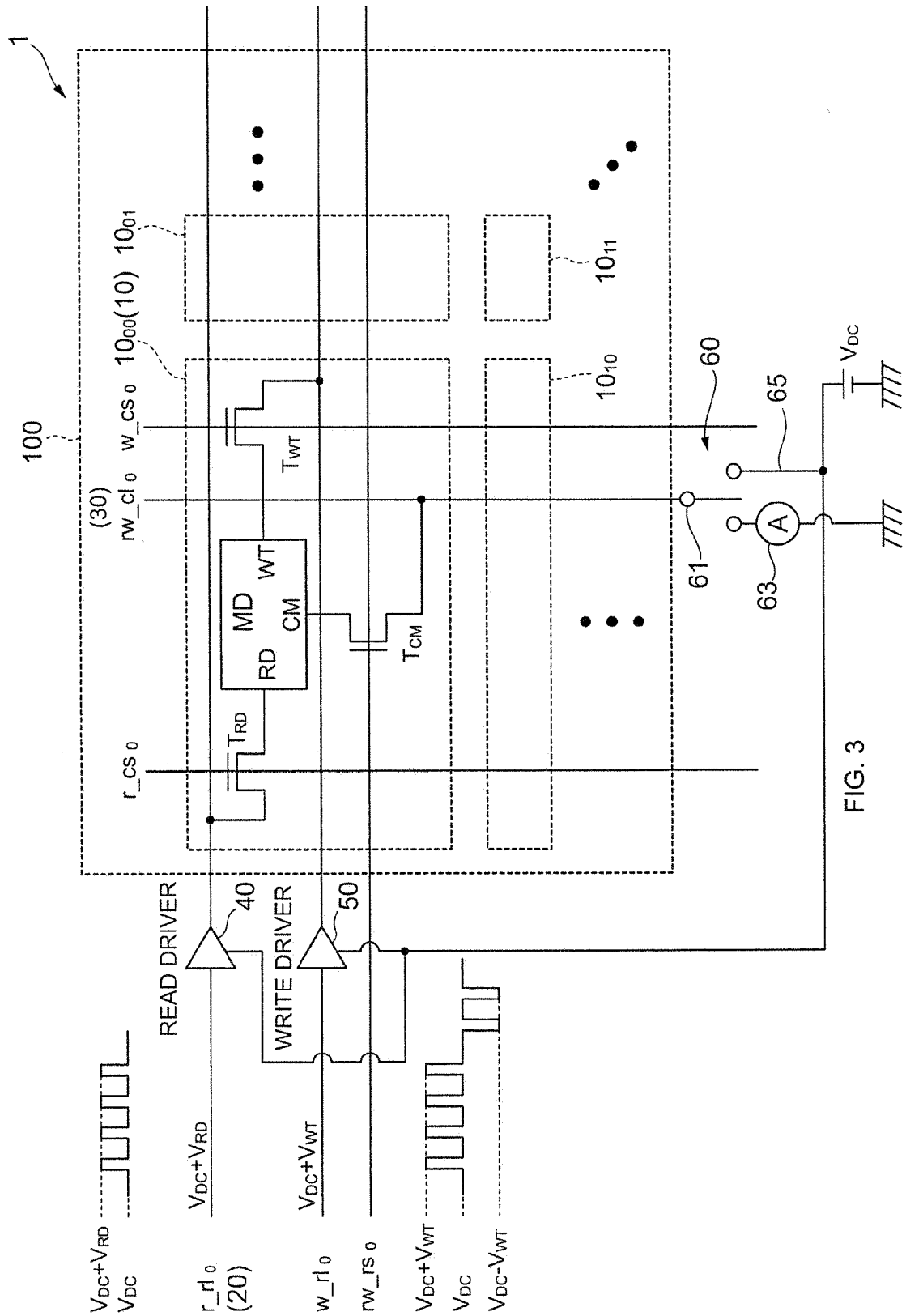
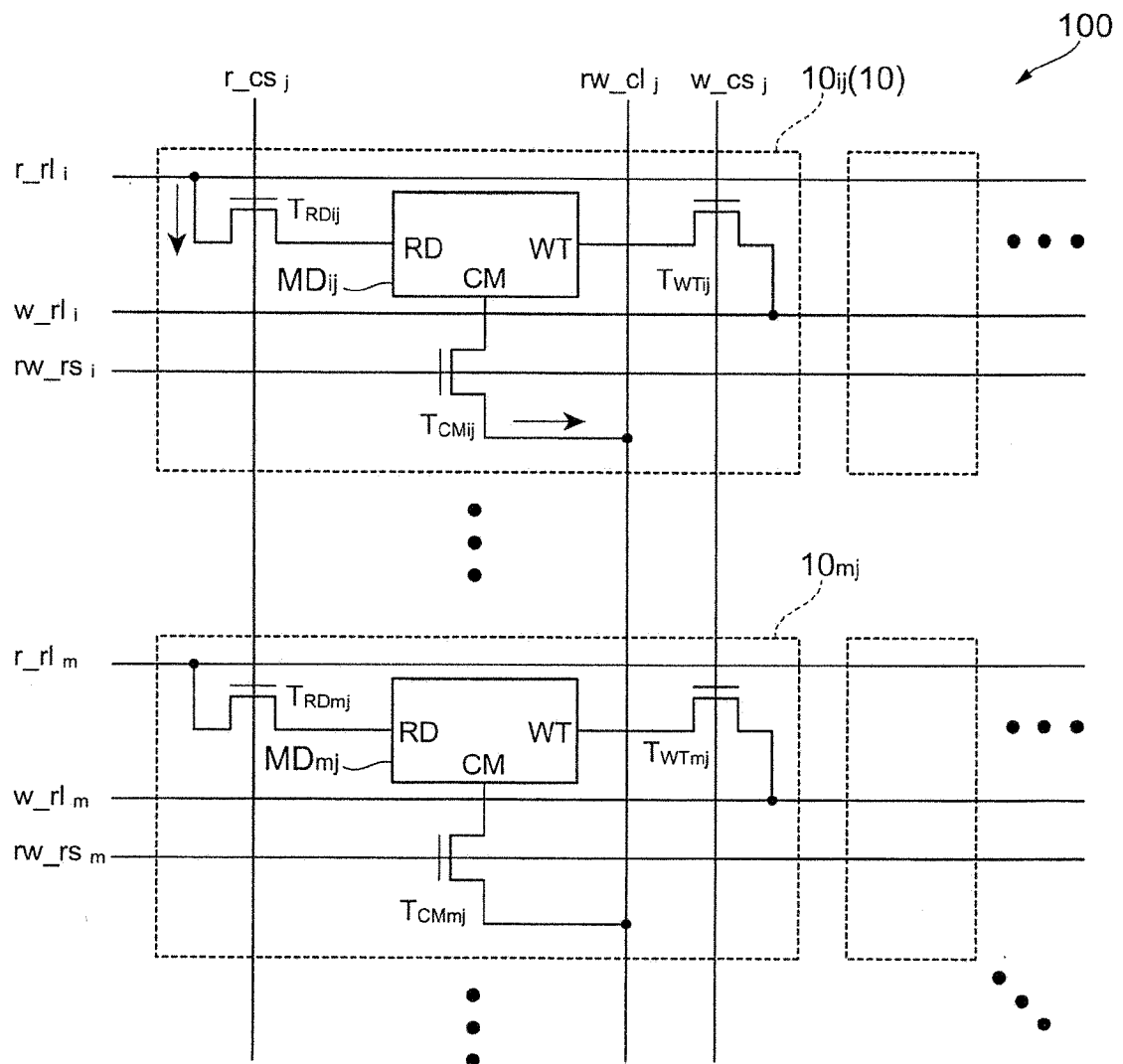
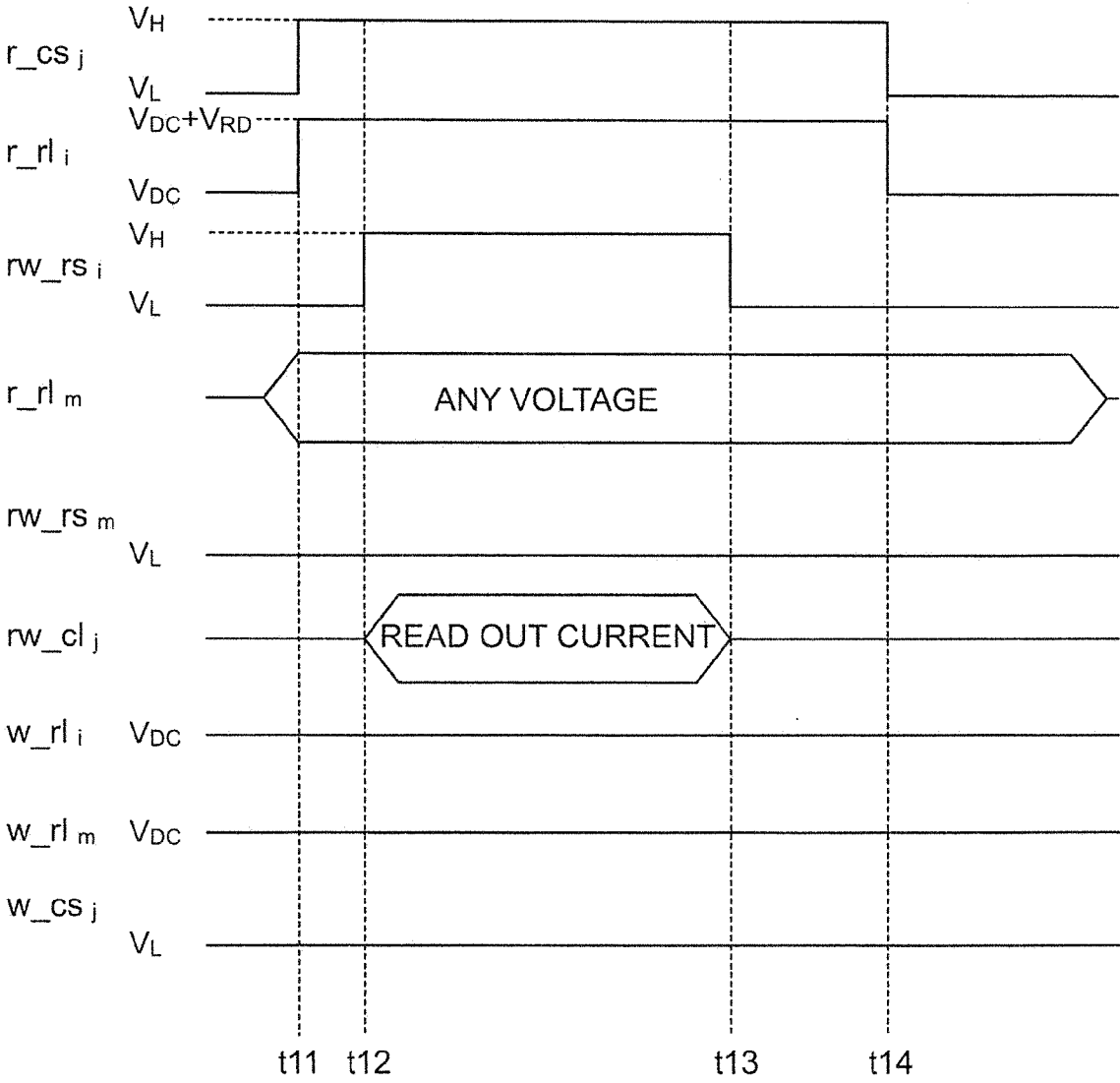


FIG. 3



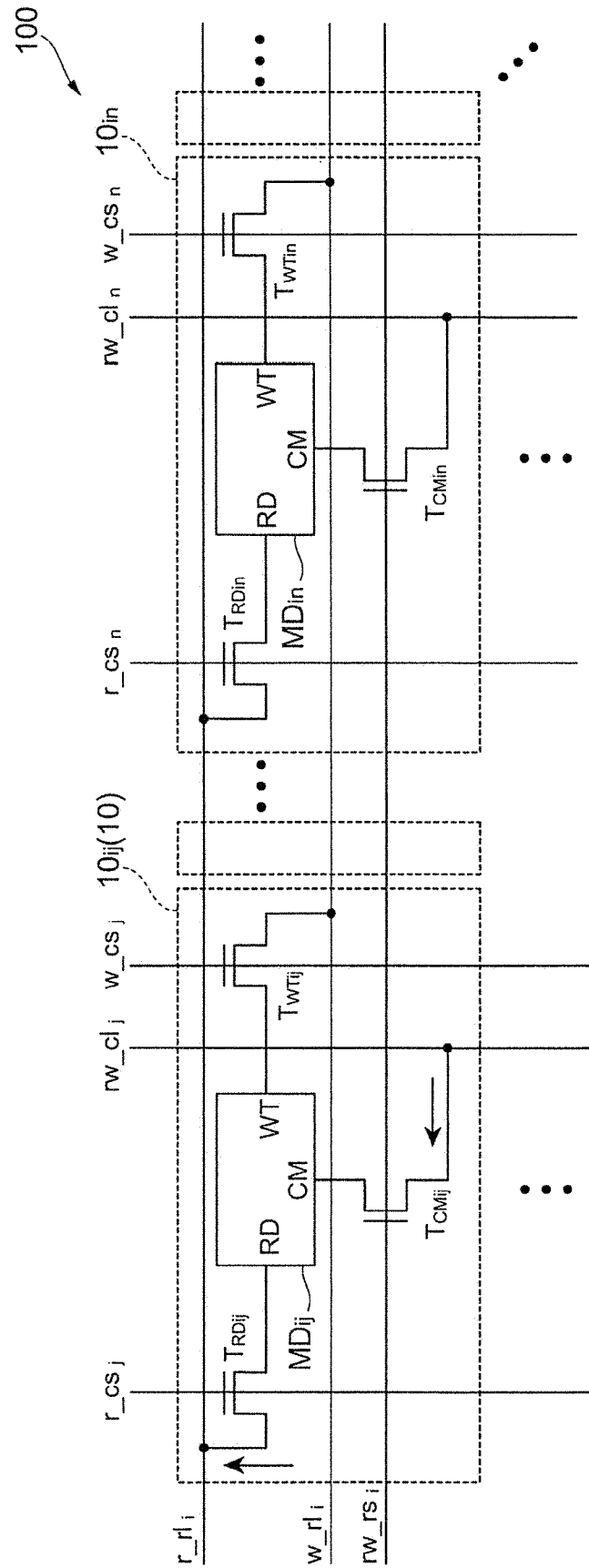
NORMAL DIRECTION READ

FIG. 4



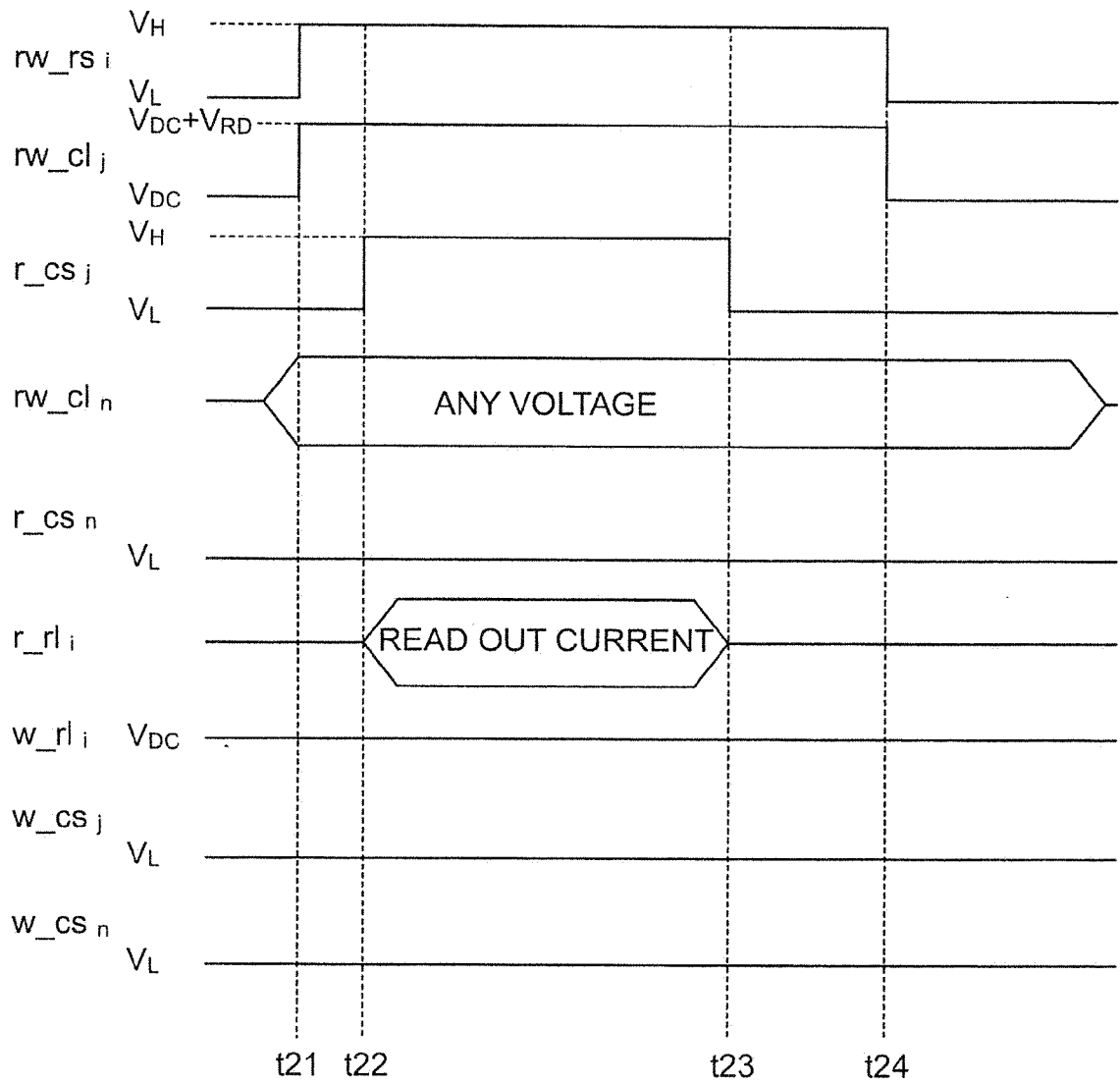
NORMAL DIRECTION READ

FIG. 5



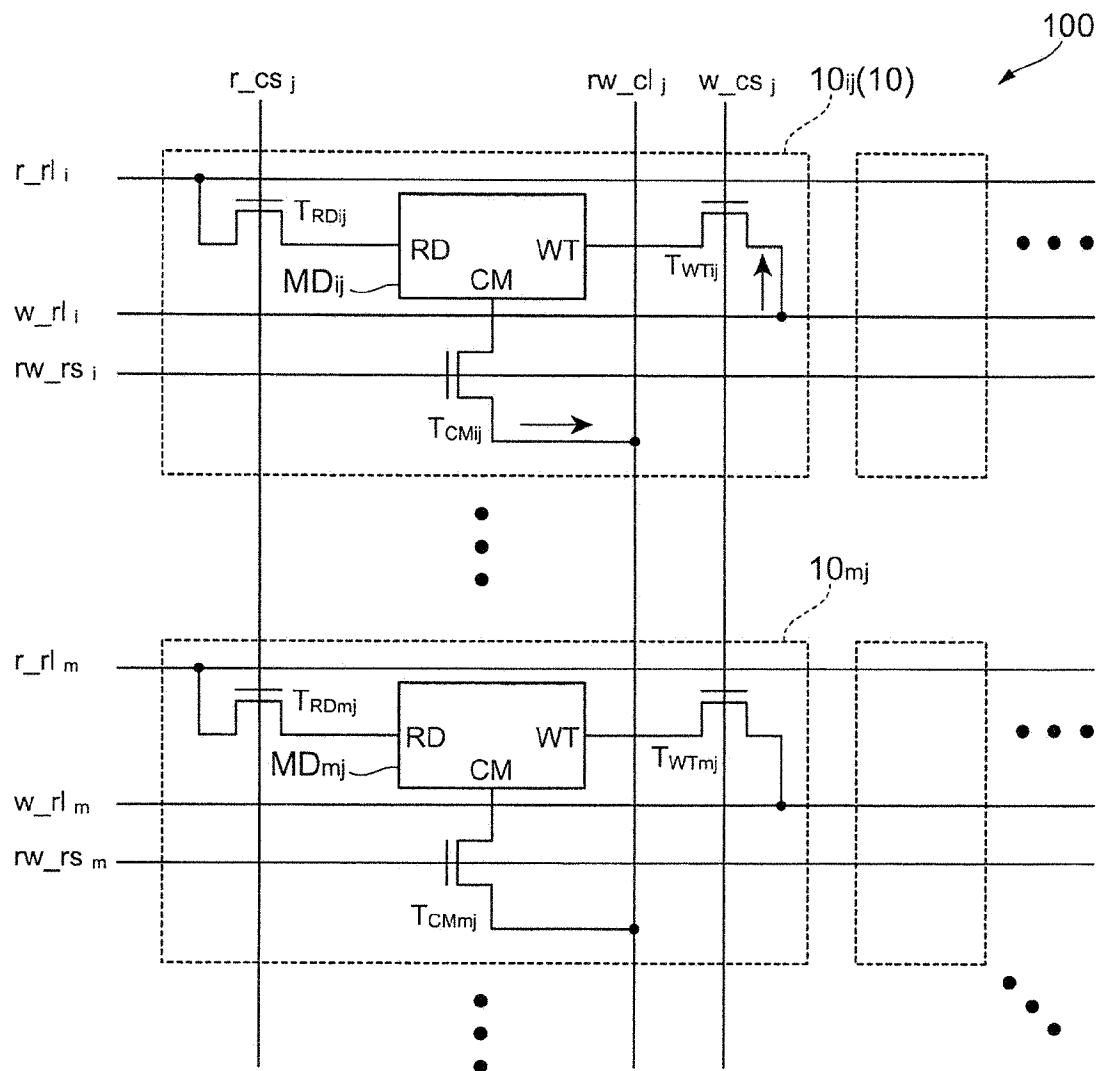
REVERSE DIRECTION READ

FIG. 6



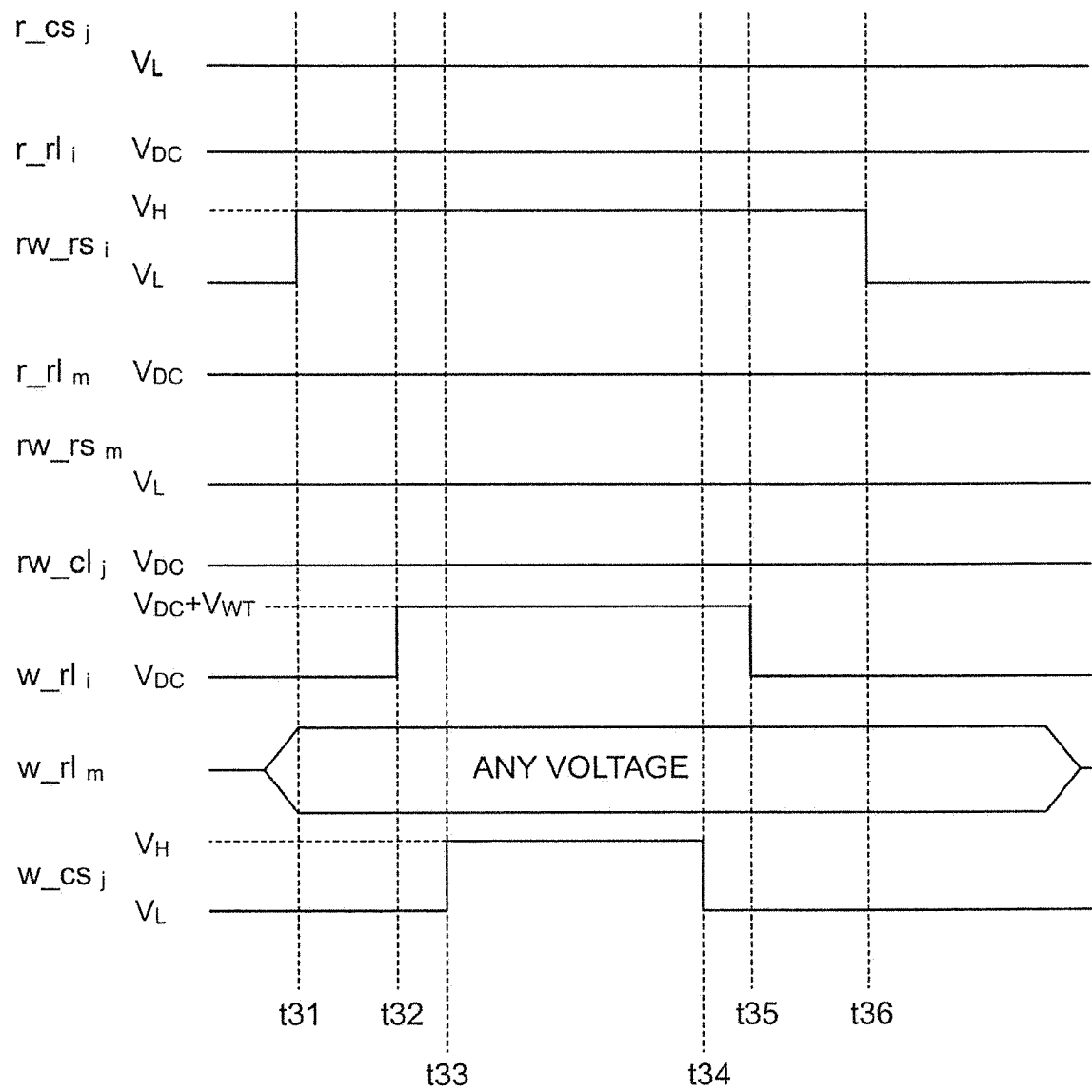
REVERSE DIRECTION READ

FIG. 7

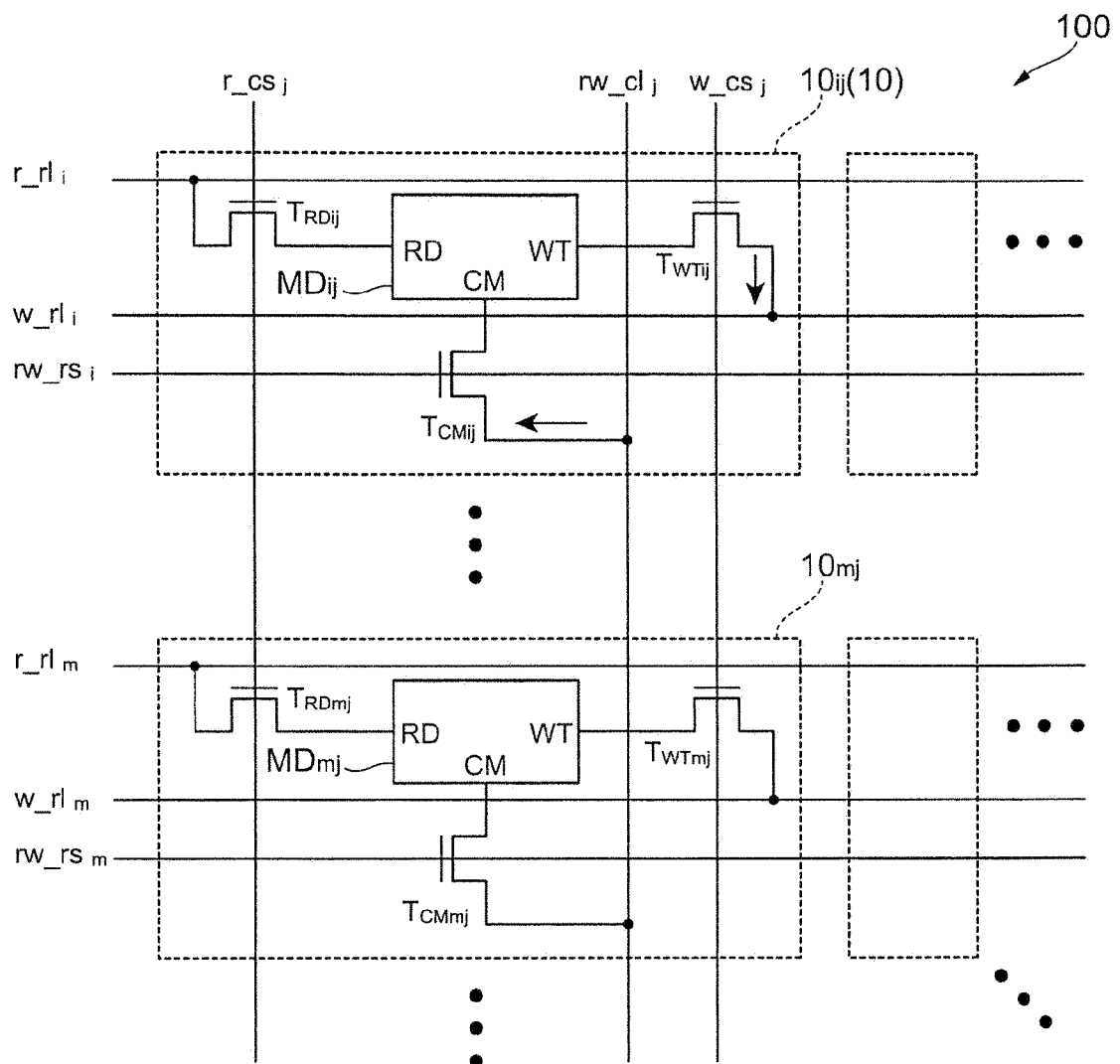


NORMAL INCREMENT WRITE

FIG. 8

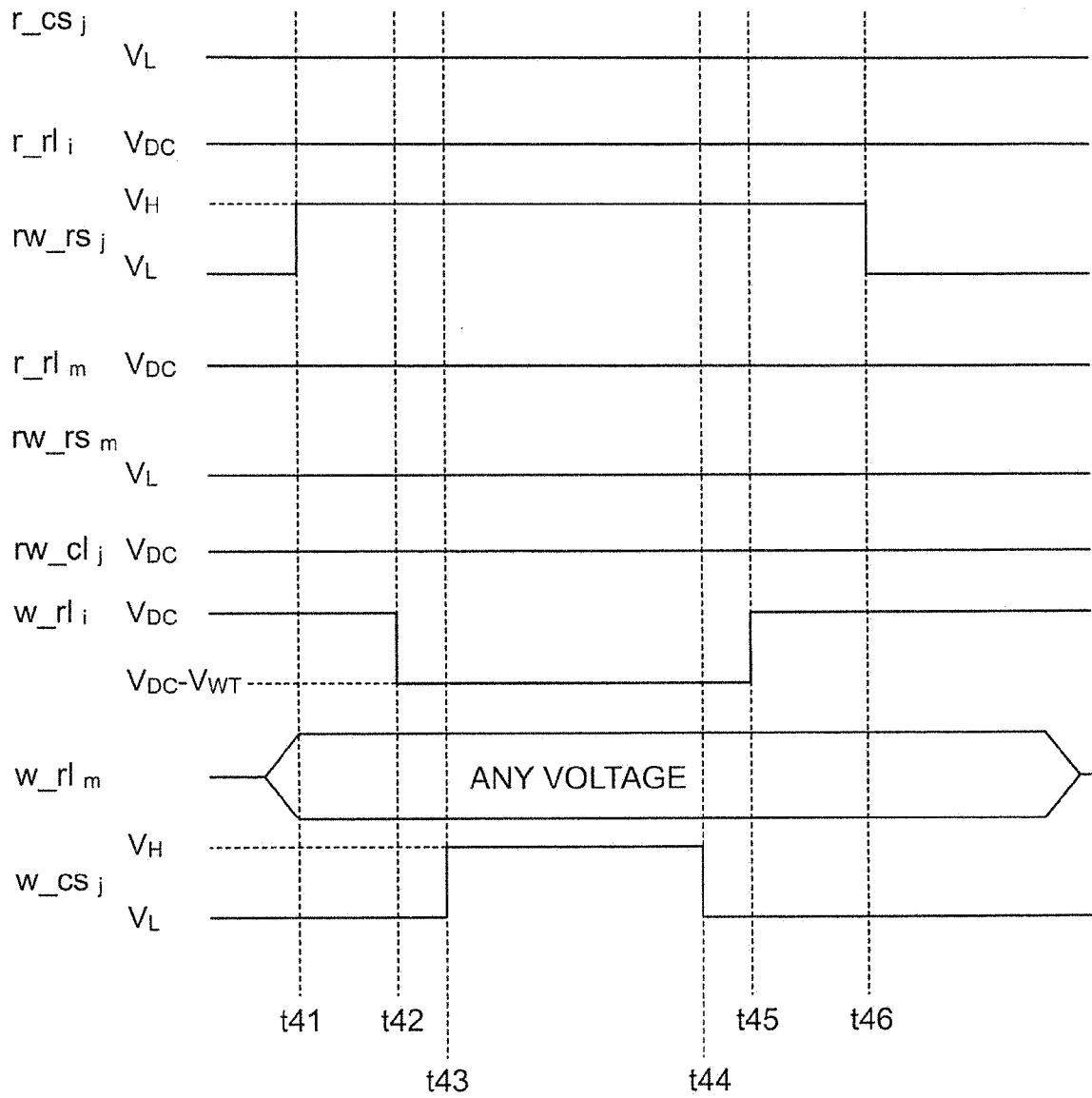


NORMAL INCREMENT WRITE
FIG. 9



NORMAL DECREMENT WRITE

FIG. 10



NORMAL DECREMENT WRITE

FIG. 11

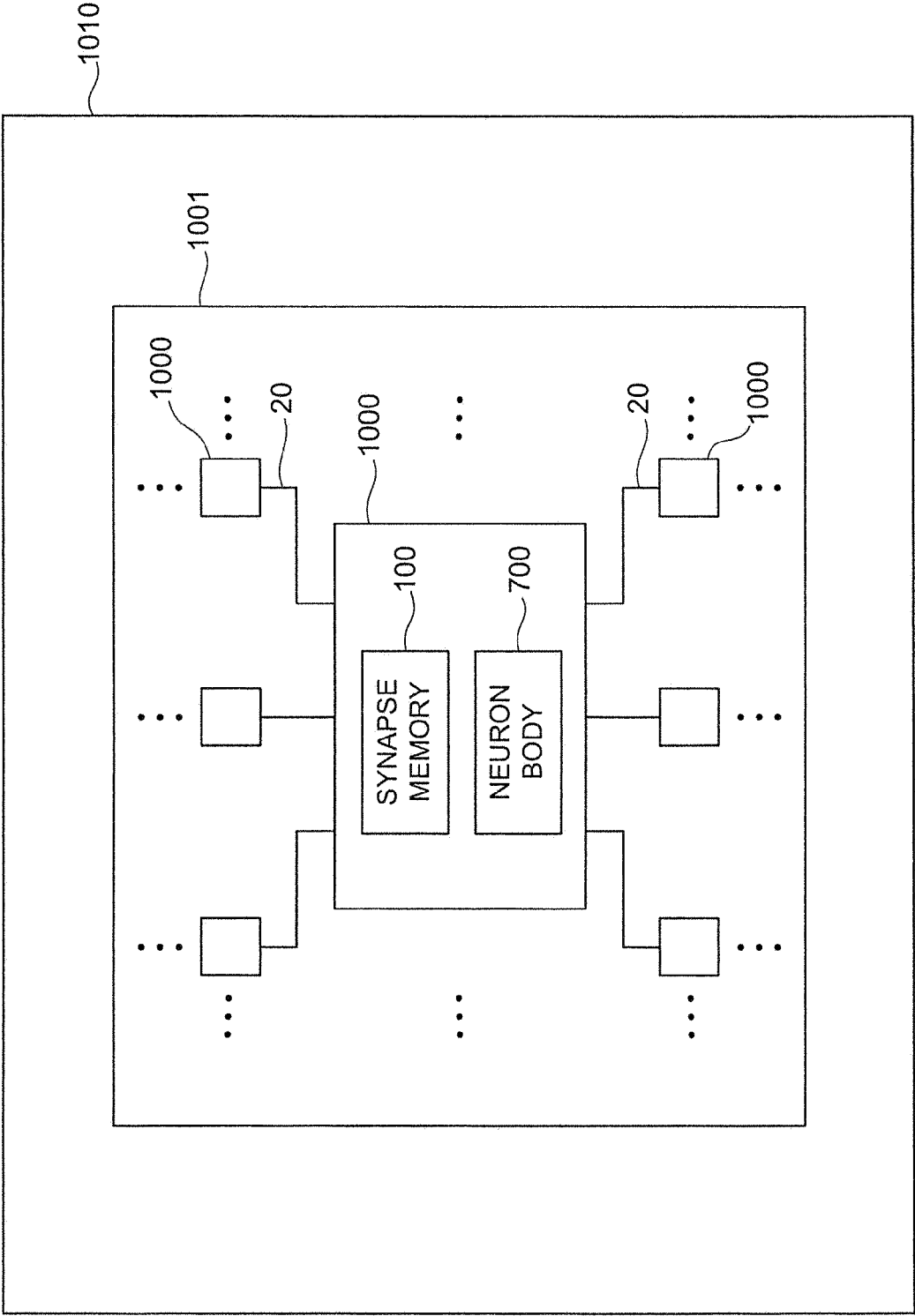
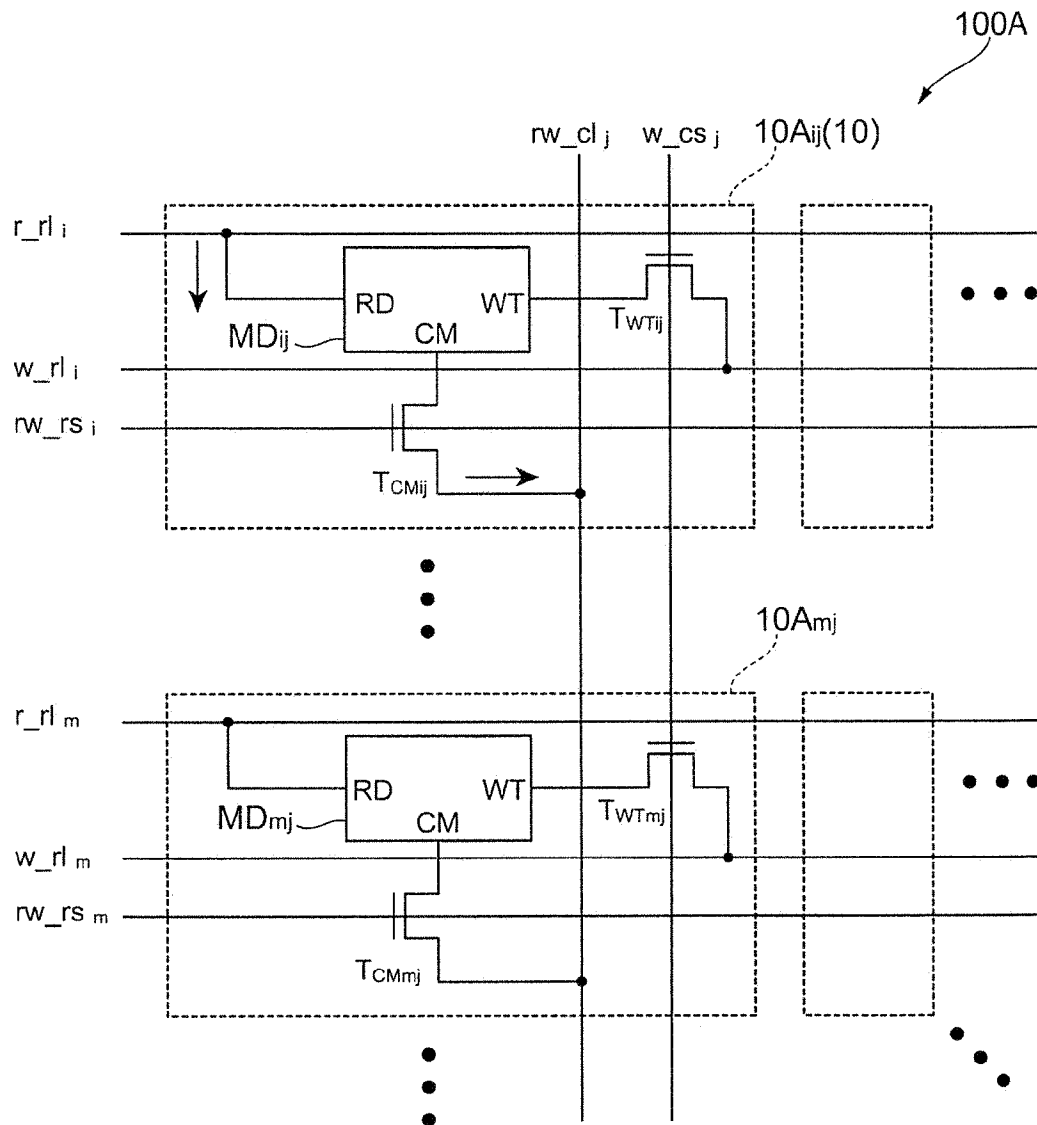
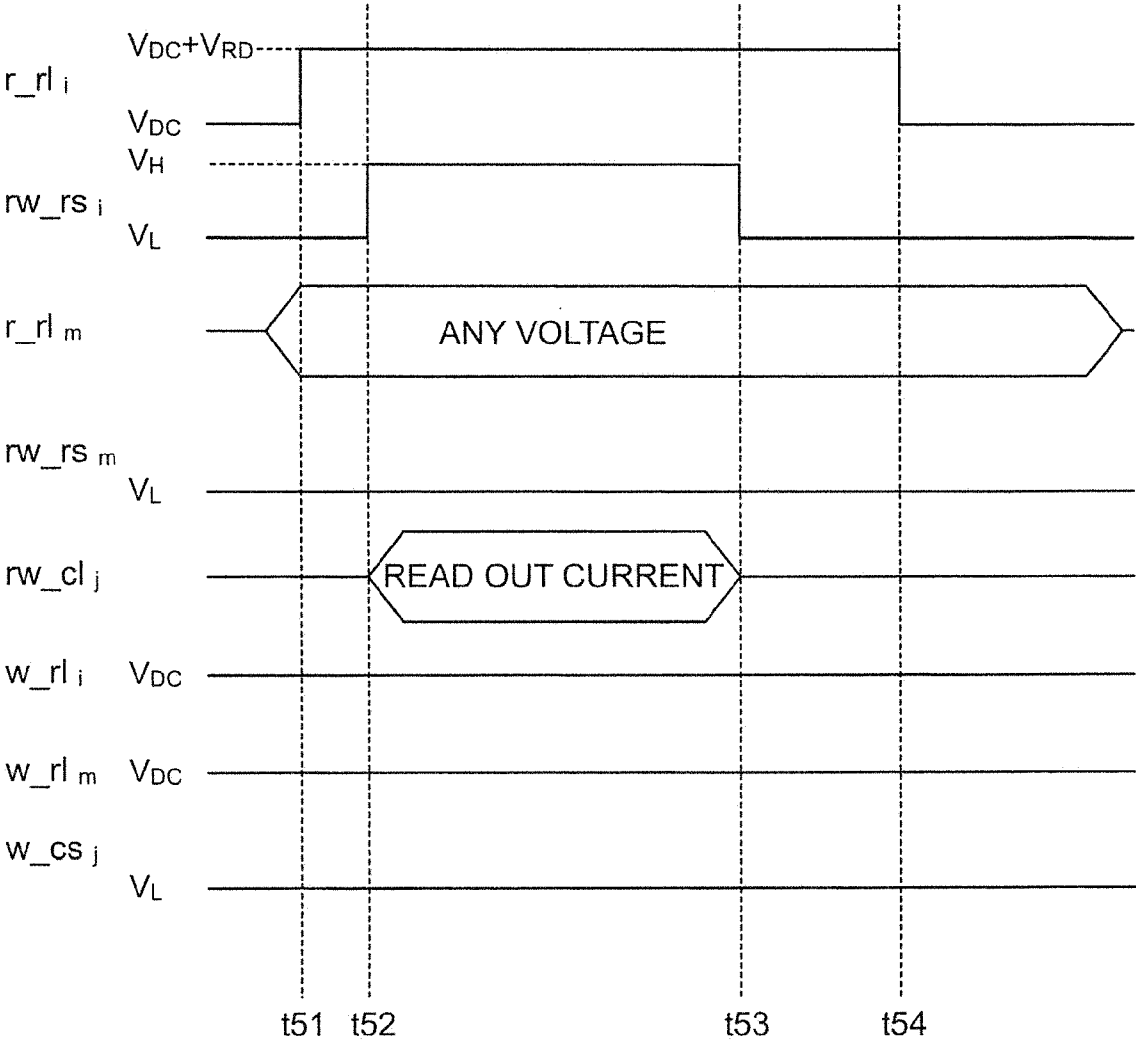


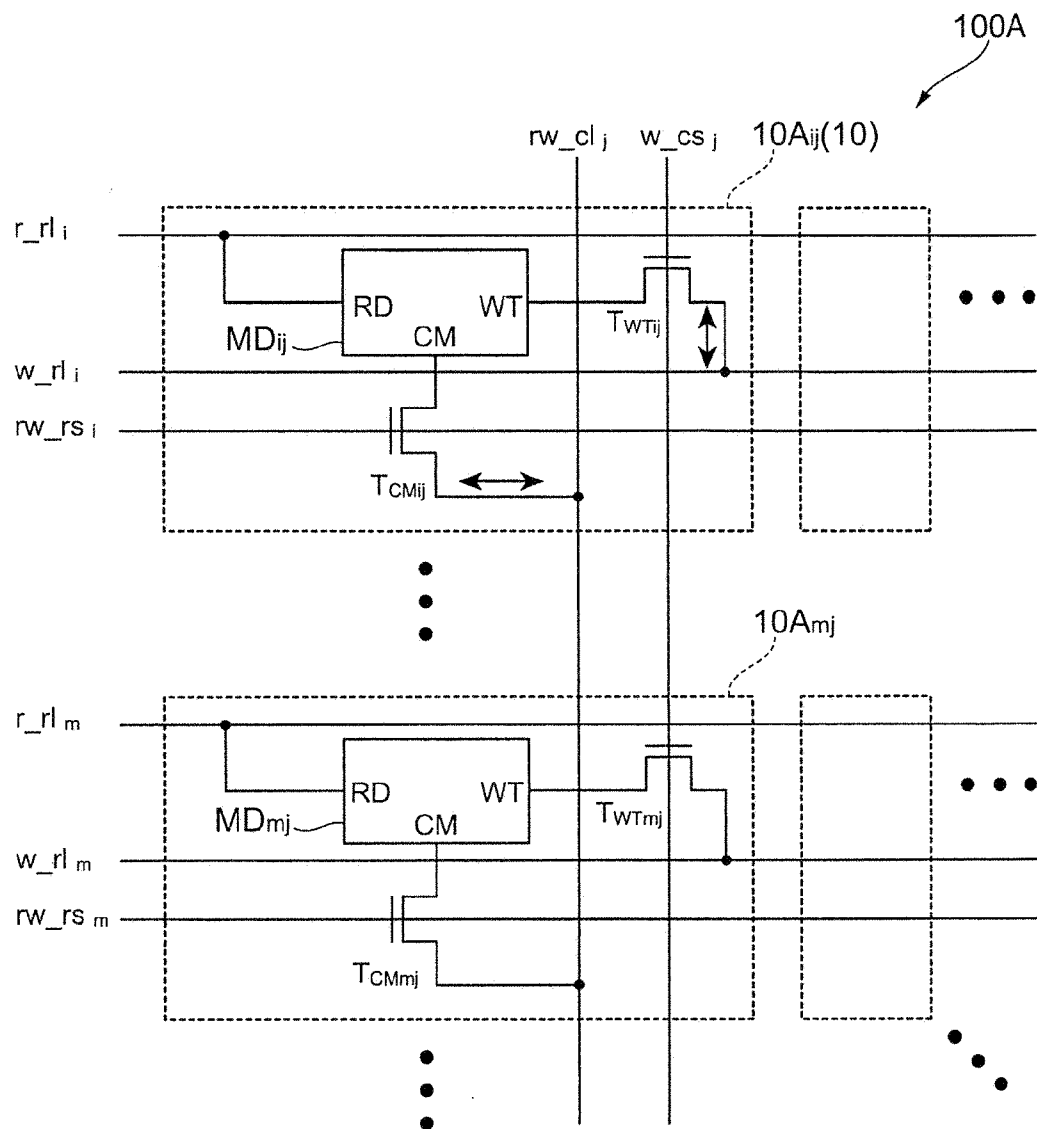
FIG. 12



NORMAL DIRECTION READ
FIG. 13

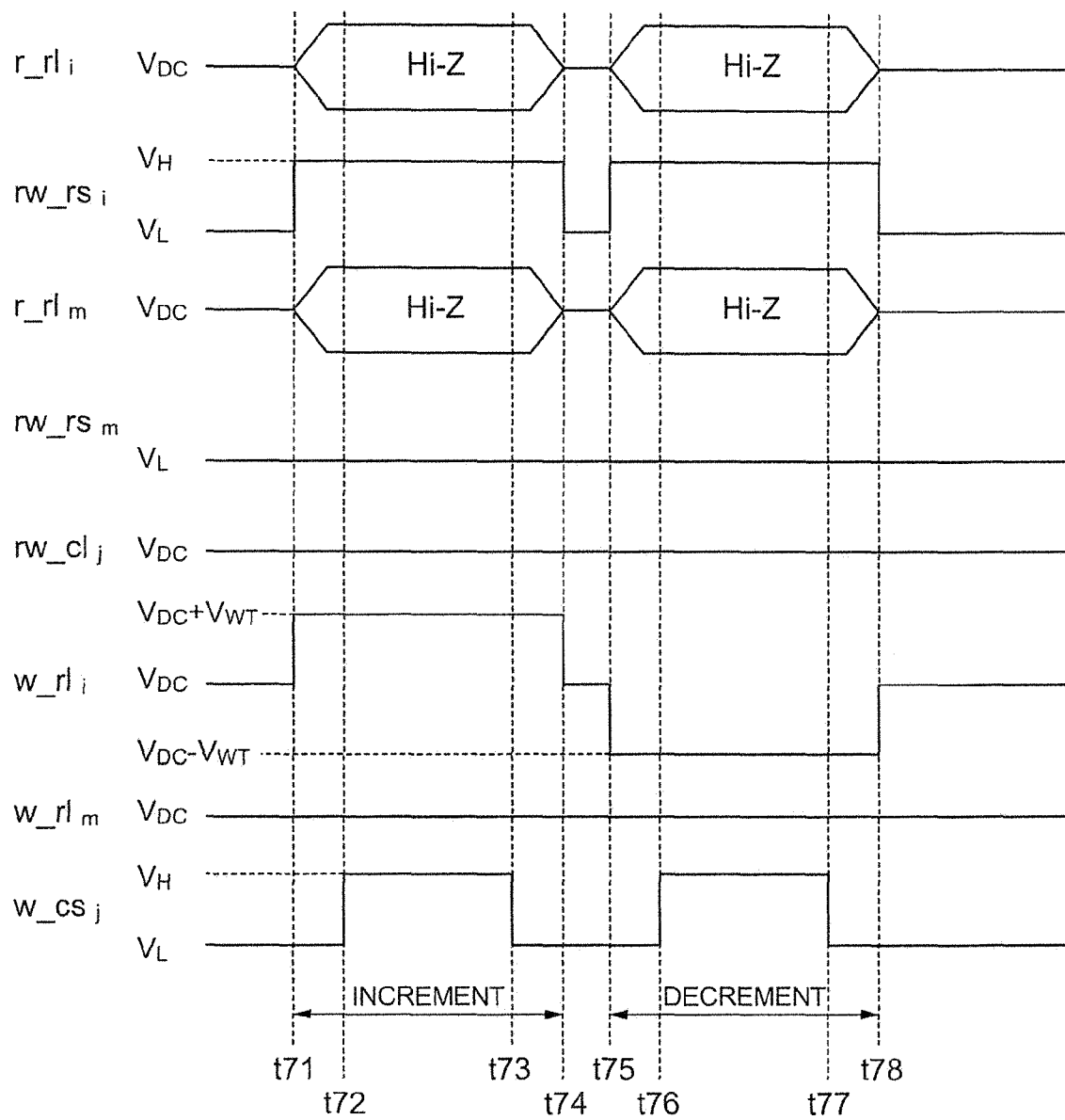


NORMAL DIRECTION READ
FIG. 14



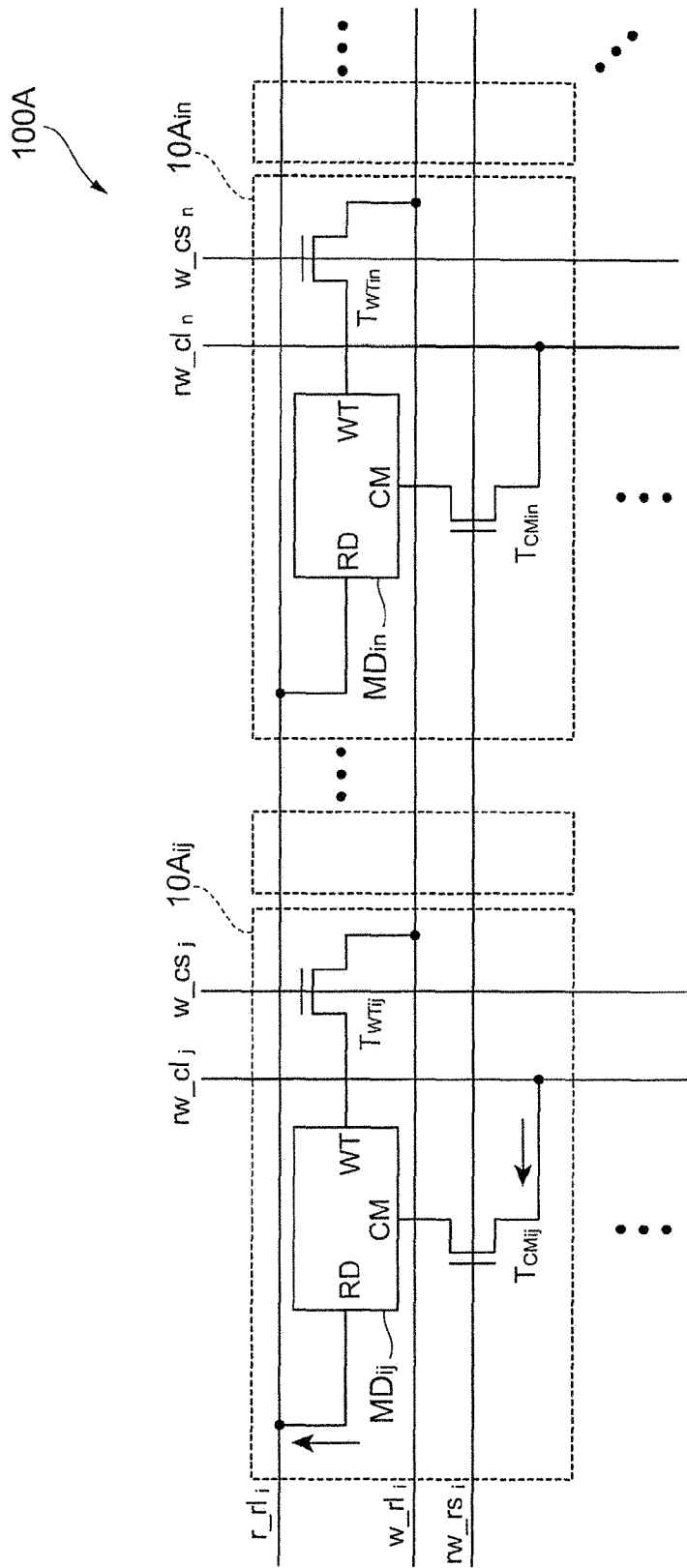
NORMAL WRITE

FIG. 15



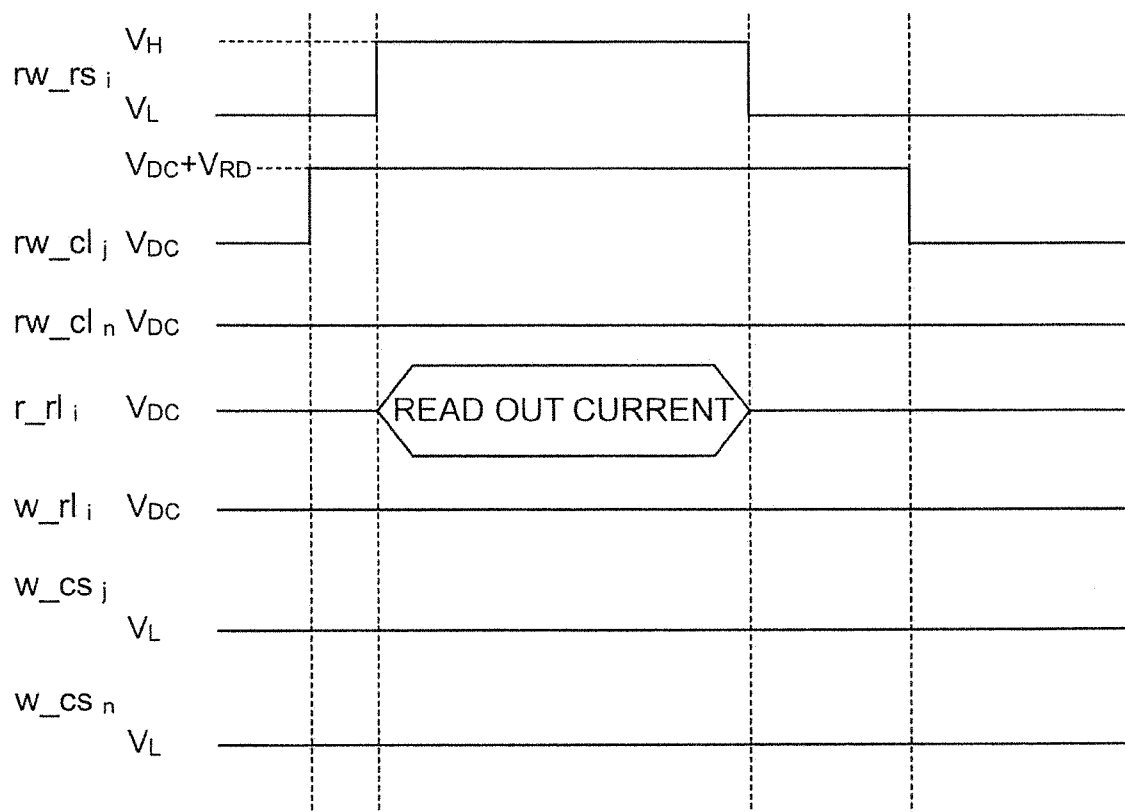
NORMAL WRITE

FIG. 16



REVERSE DIRECTION READ

FIG. 17



REVERSE DIRECTION READ

FIG. 18

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2019/050185

A. CLASSIFICATION OF SUBJECT MATTER

G06N 3/063(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI;EPODOC;CNKI;CNPAT: synapse, neuron, neuromorphic, axon, dendrite, memory, transistor, read, write, input, output

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2017185890 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 29 June 2017 (2017-06-29) description, paragraphs [0051]-[0052], figure 4	1-15
A	CN 107194462 A (TSINGHUA UNIVERSITY) 22 September 2017 (2017-09-22) the whole document	1-15
A	CN 104240753 A (SAMSUNG ELECTRONICS CO., LTD.) 24 December 2014 (2014-12-24) the whole document	1-15

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

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“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

06 April 2019

Date of mailing of the international search report

28 April 2019

Name and mailing address of the ISA/CN

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Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53961296

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/IB2019/050185

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2017185890	A1	29 June 2017	None			
CN	107194462	A	22 September 2017	None			
CN	104240753	A	24 December 2014	EP	2814036	A2	17 December 2014
				KR	20140144130	A	18 December 2014