US 20110147841A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2011/0147841 A1

(43) Pub. Date: Jun. 23, 2011

MORIKADO

(54) **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME**

(75) Inventor: **Mutsuo MORIKADO**, Yokohama-shi (JP)

(73) Assignee: **KABUSHIKI KAISHA TOSHIBA**, Minato-ku (JP)

(21) Appl. No.: **13/038,999**

(22) Filed: **Mar. 2, 2011**

Related U.S. Application Data

(63) Continuation of application No. 11/470,859, filed on Sep. 7, 2006, now Pat. No. 7,915,680.

(30) **Foreign Application Priority Data**

Sep. 7, 2005 (JP) 2005-259494

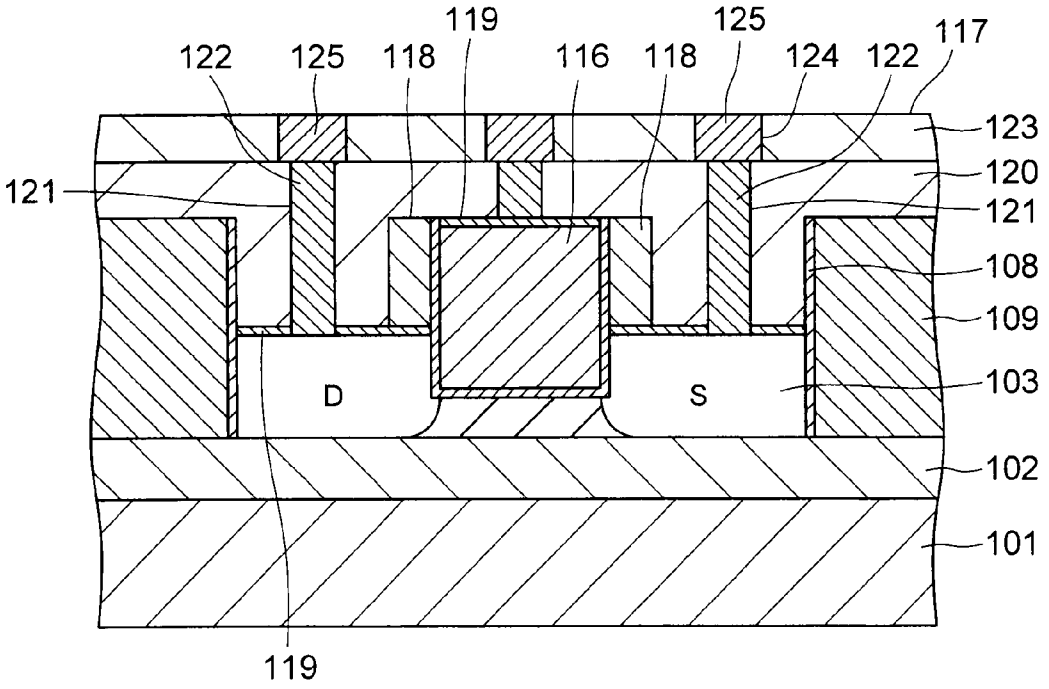
Publication Classification

(51) **Int. Cl.**
H01L 29/772 (2006.01)

(52) **U.S. Cl.** **257/348**; 257/E29.242

(57) **ABSTRACT**

A semiconductor device comprises: a channel region of a transistor formed in a predetermined region of silicon layer formed on insulation film; a gate electrode formed on the channel region via gate insulation film; and source/drain regions formed in the silicon layer thicker than said channel region located out of the channel region, wherein the transistor is a memory element constituting the channel region as a floating body cell.



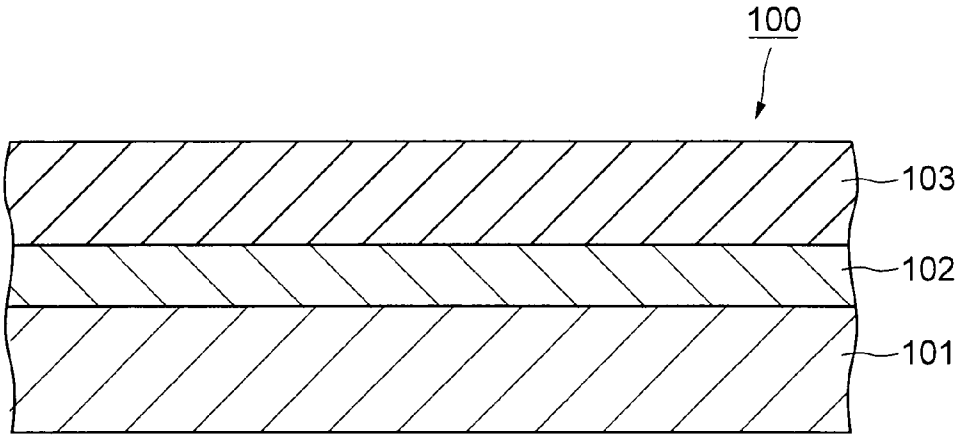


FIG.1A

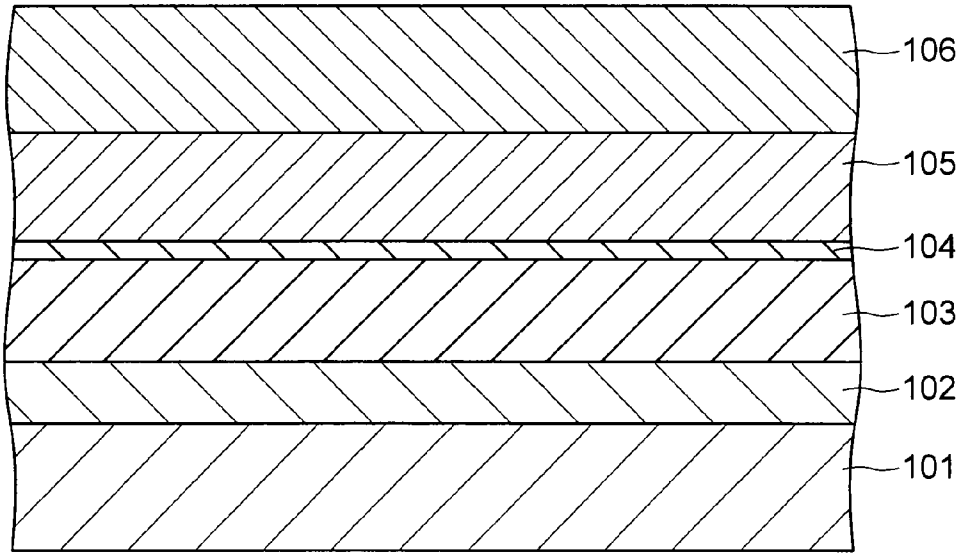


FIG.1B

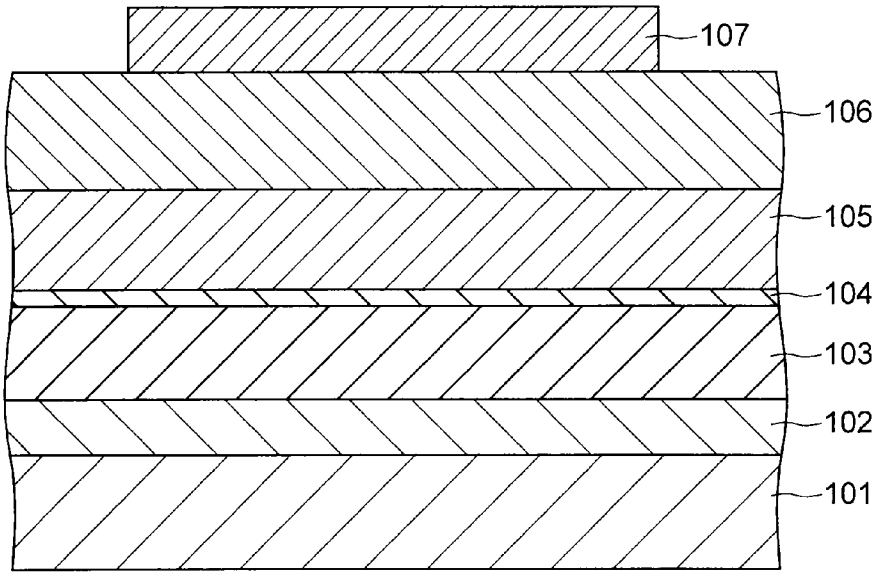


FIG.1C

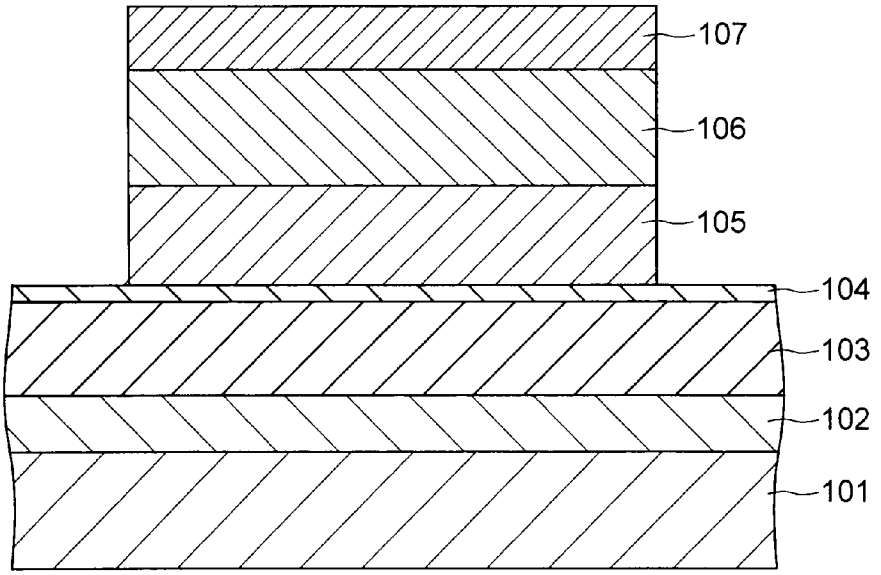


FIG.1D

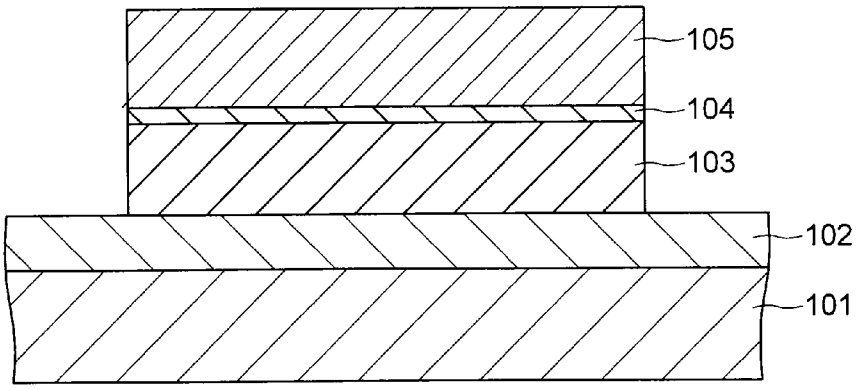


FIG.1E

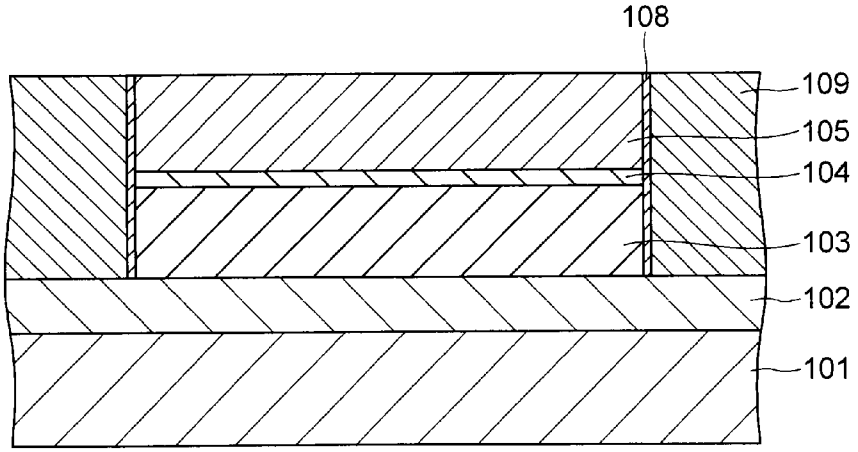


FIG.1F

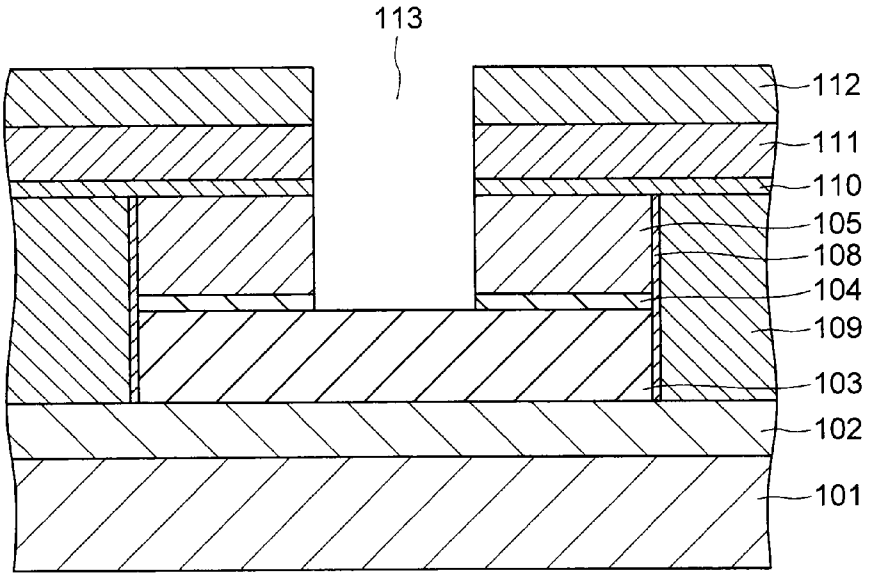

113
112
111
110
105
108
104
109
103
102
101

FIG.1G

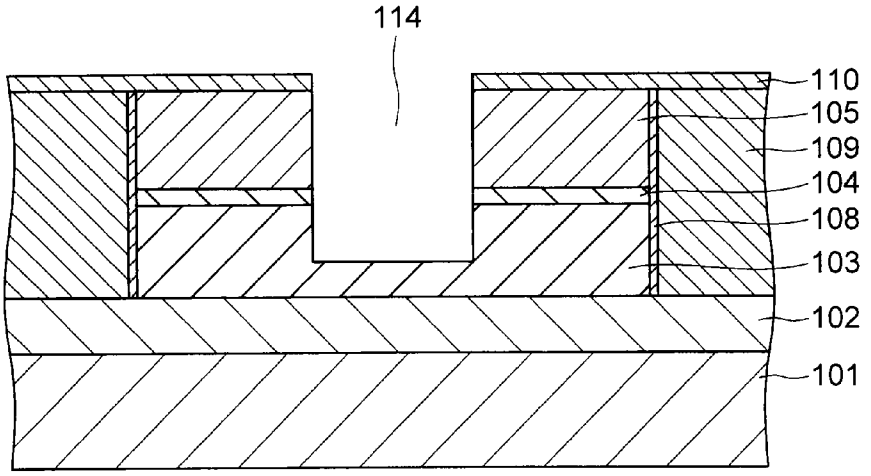

114
110
105
109
104
108
103
102
101

FIG.1H

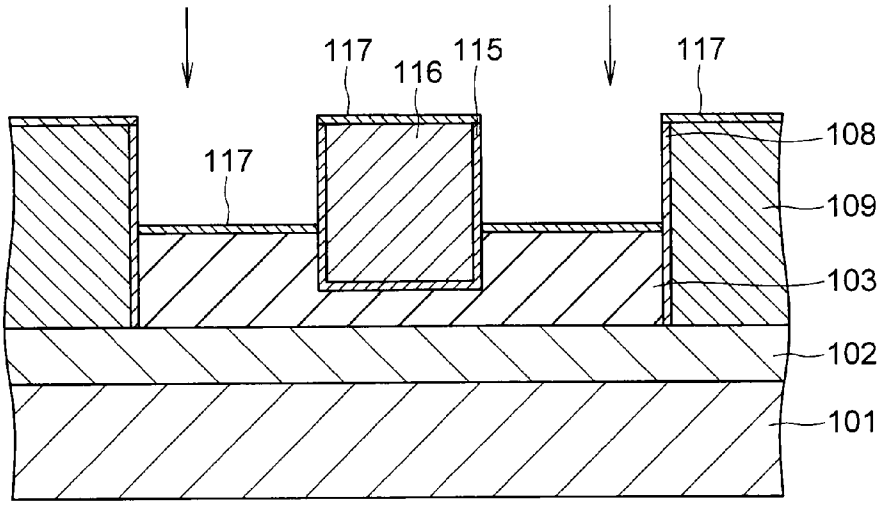

117
116
115
117
117
108
109
103
102
101

FIG.1 I

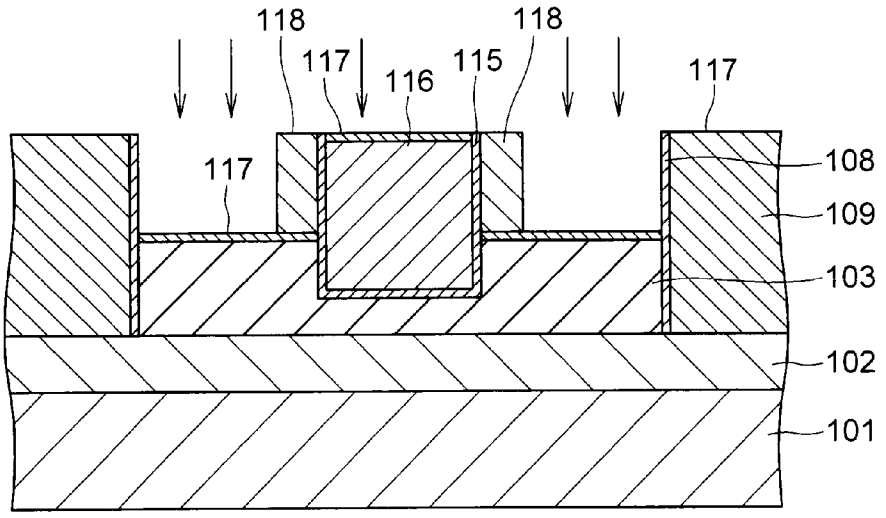

118
118
117
116
115
117
117
108
109
103
102
101

FIG.1J

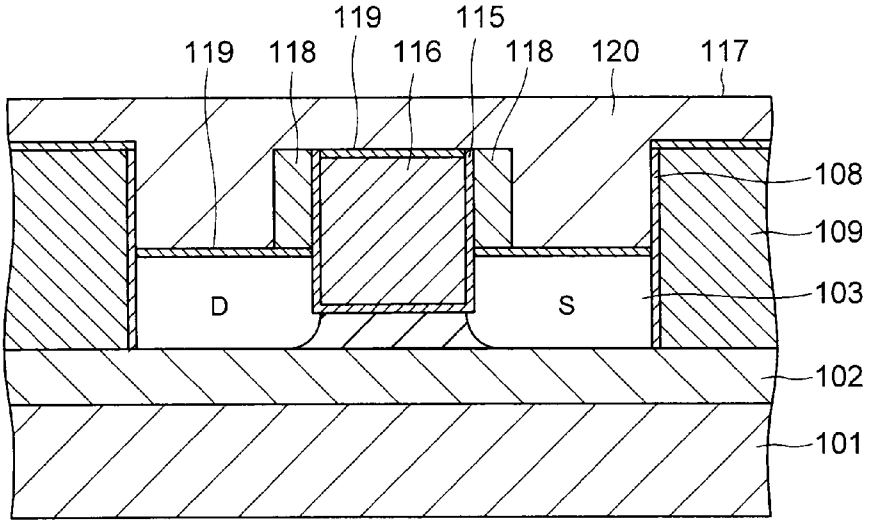

119
115
119
118
116
118
120
117
108
109
D
S
103
102
101

FIG.1K

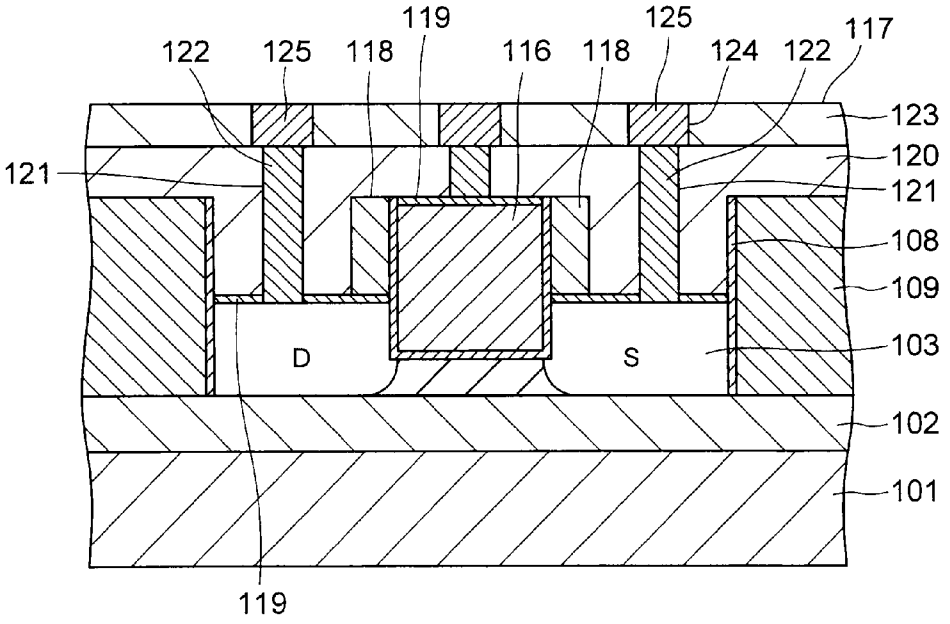

119
125
122
125
118
116
118
124
122
117
123
121
120
121
108
109
D
S
103
102
101
119

FIG.1L

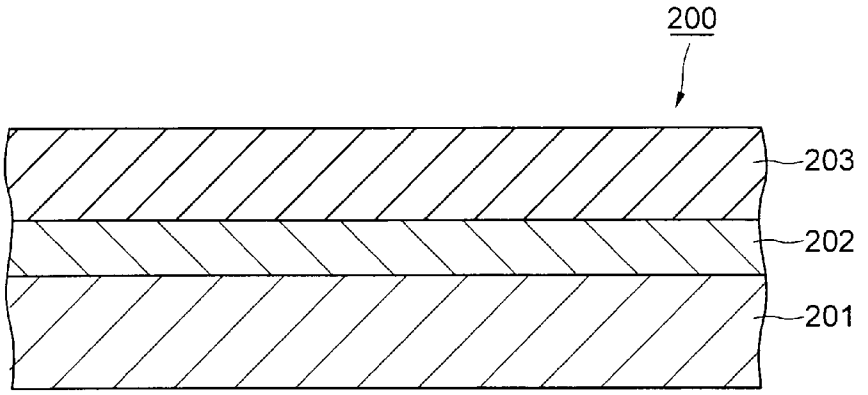


FIG.2A

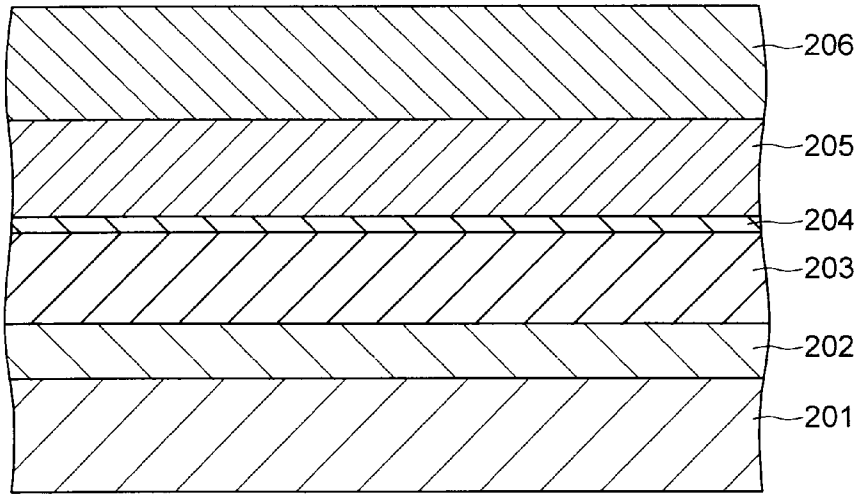


FIG.2B

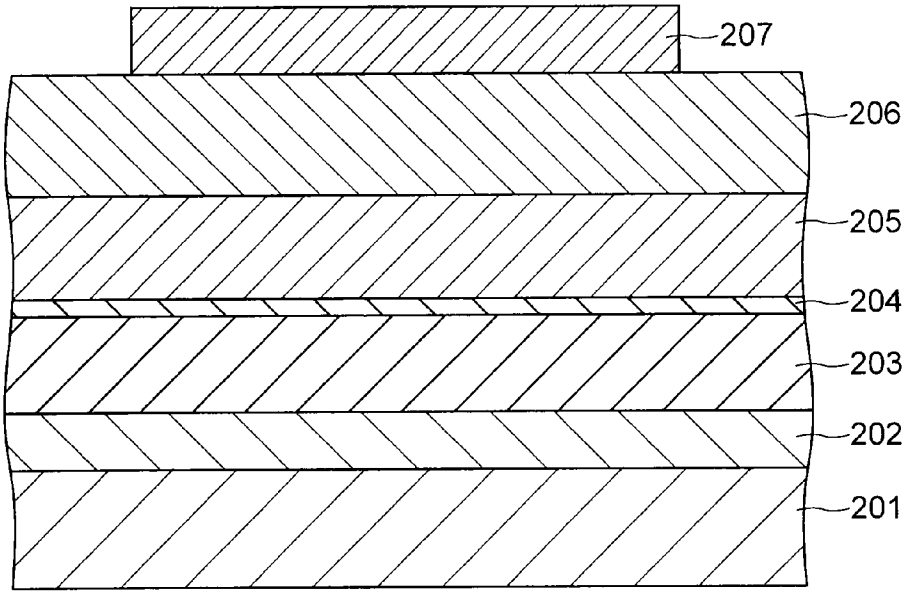


FIG.2C

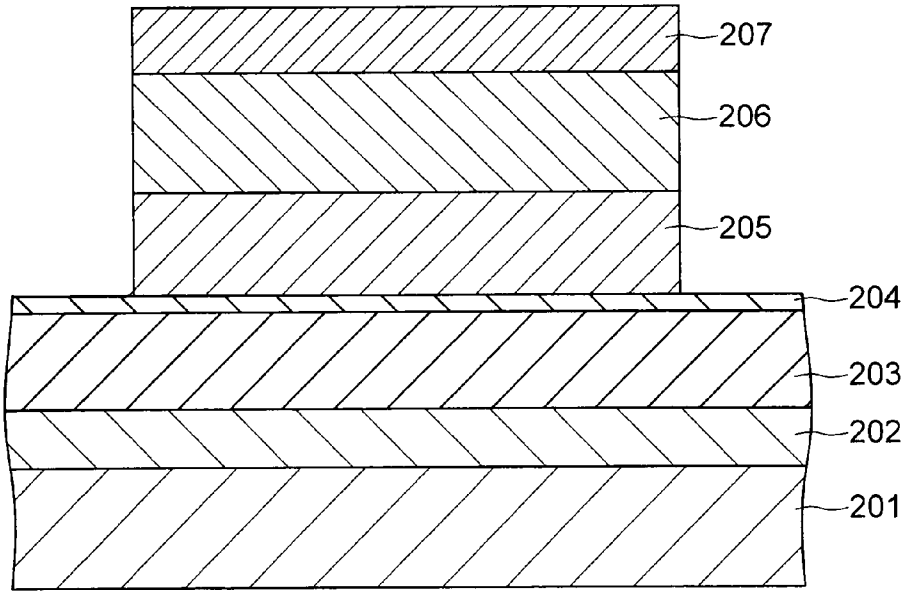


FIG.2D

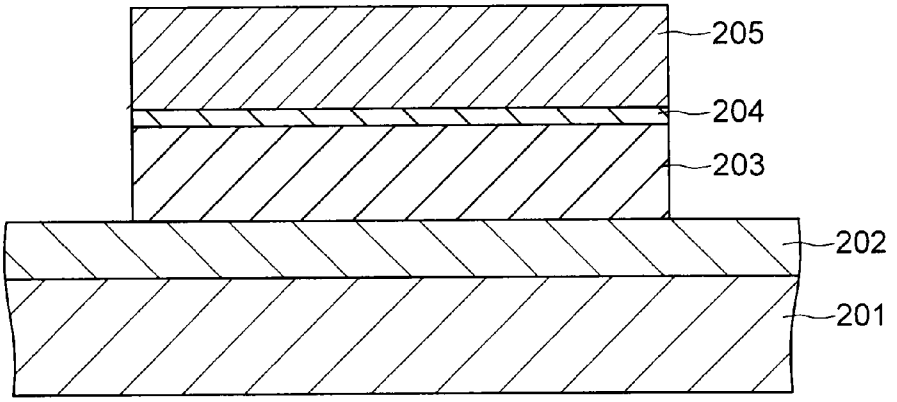


FIG.2E

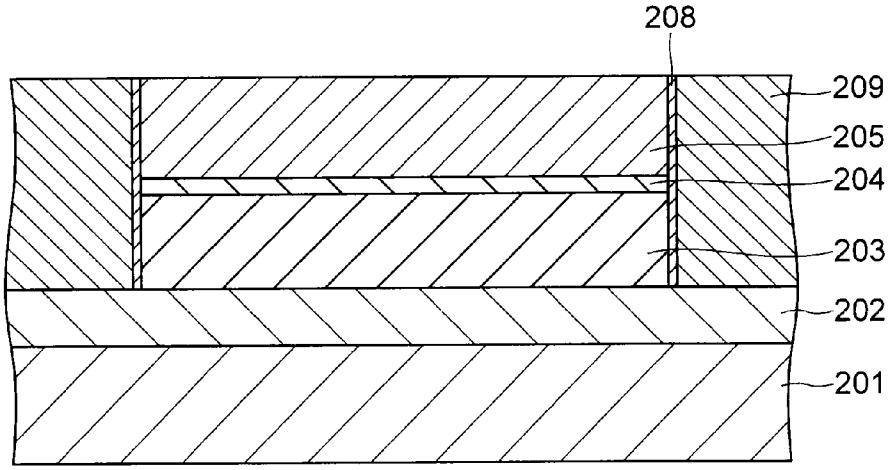


FIG.2F

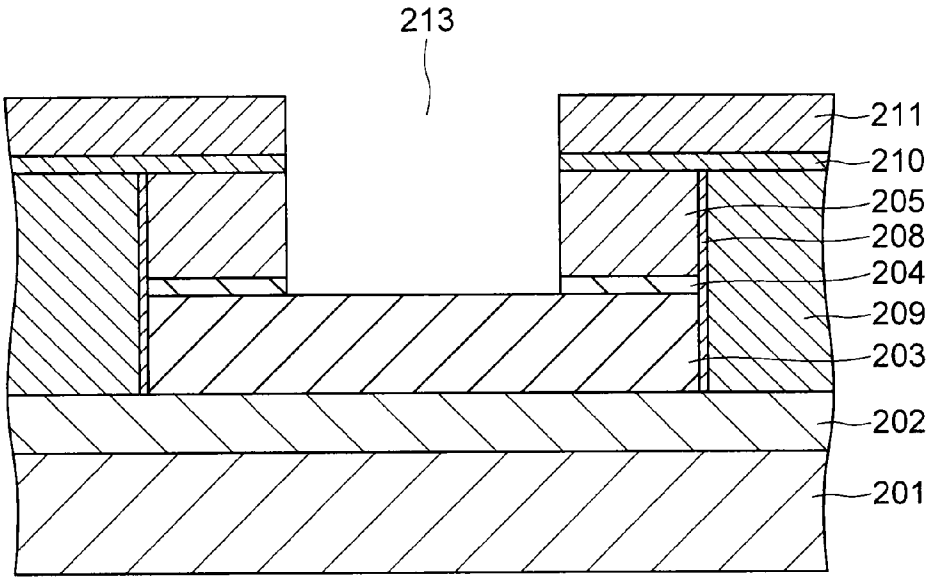

213
211
210
205
208
204
209
203
202
201

FIG.2G

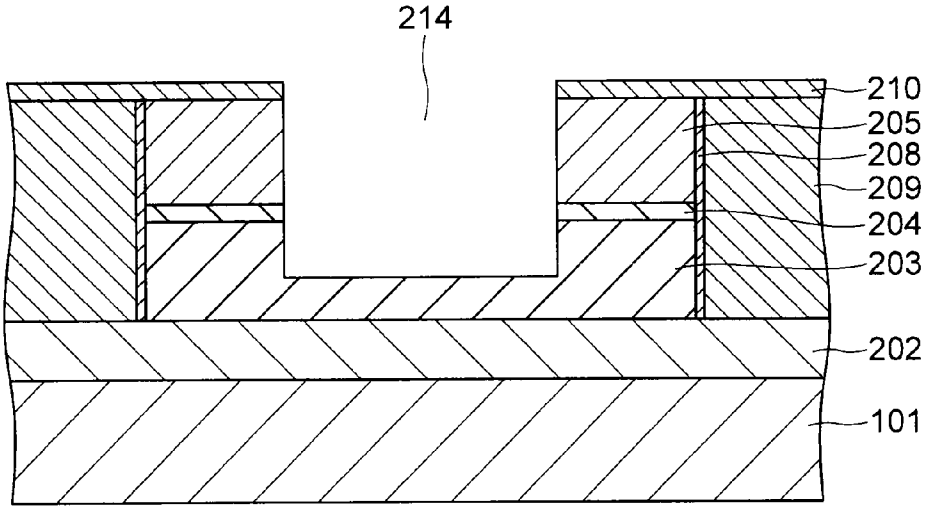

214
210
205
208
209
204
203
202
101

FIG.2H

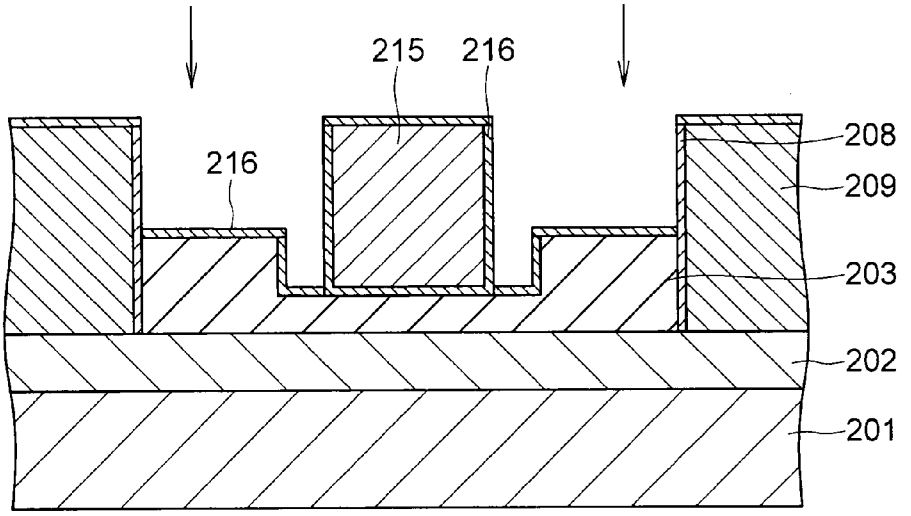

215
216
216
208
209
203
202
201

FIG.2 I

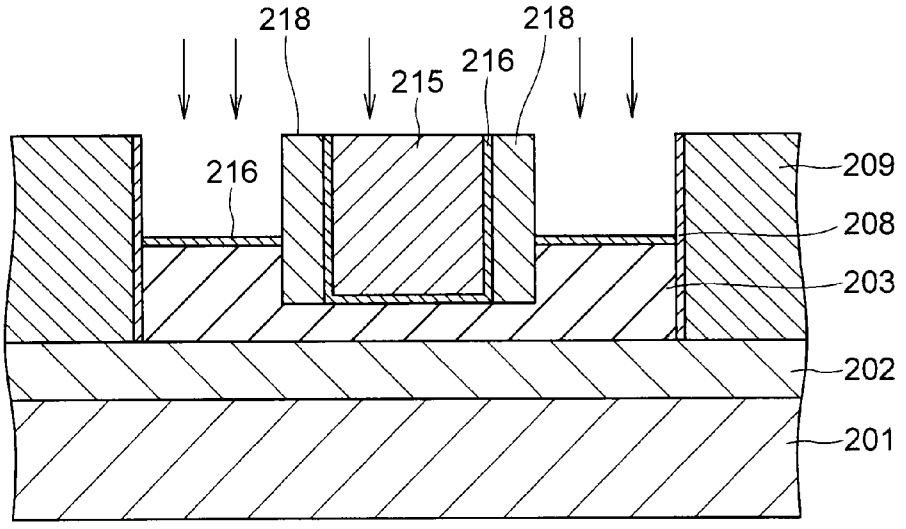

218
218
215
216
216
209
208
203
202
201

FIG.2J

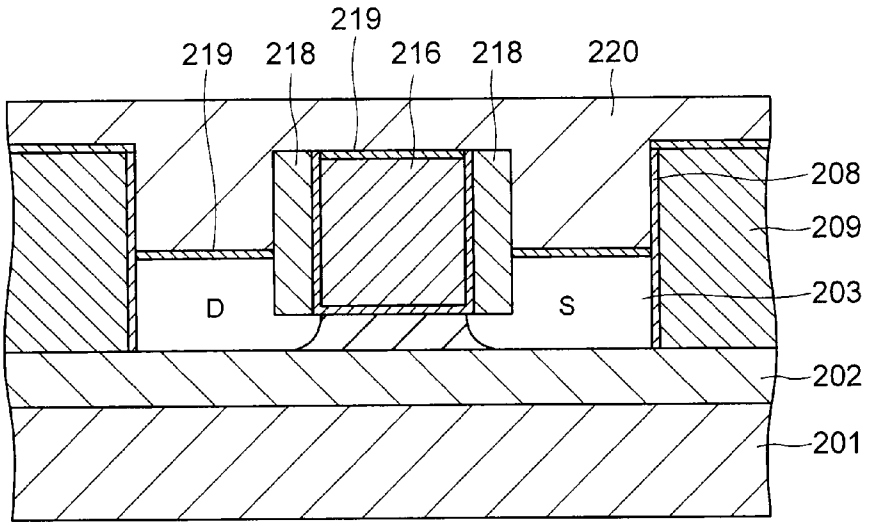

219
219
218
216
218
220
208
209
D
S
203
202
201

FIG.2K

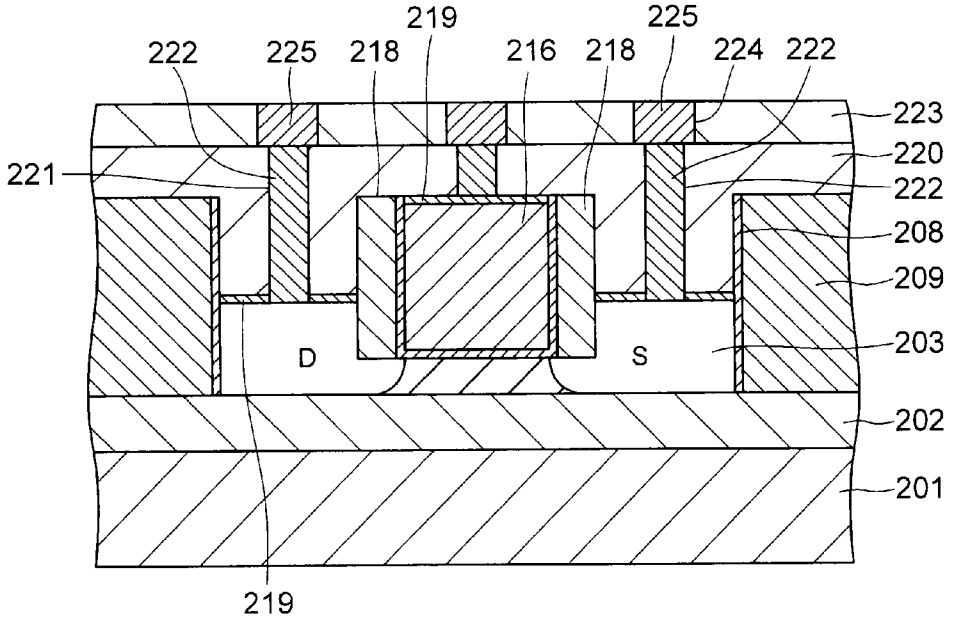

219
225
222
225
218
216
218
224
222
223
221
220
222
208
209
D
S
203
202
201
219

FIG.2L

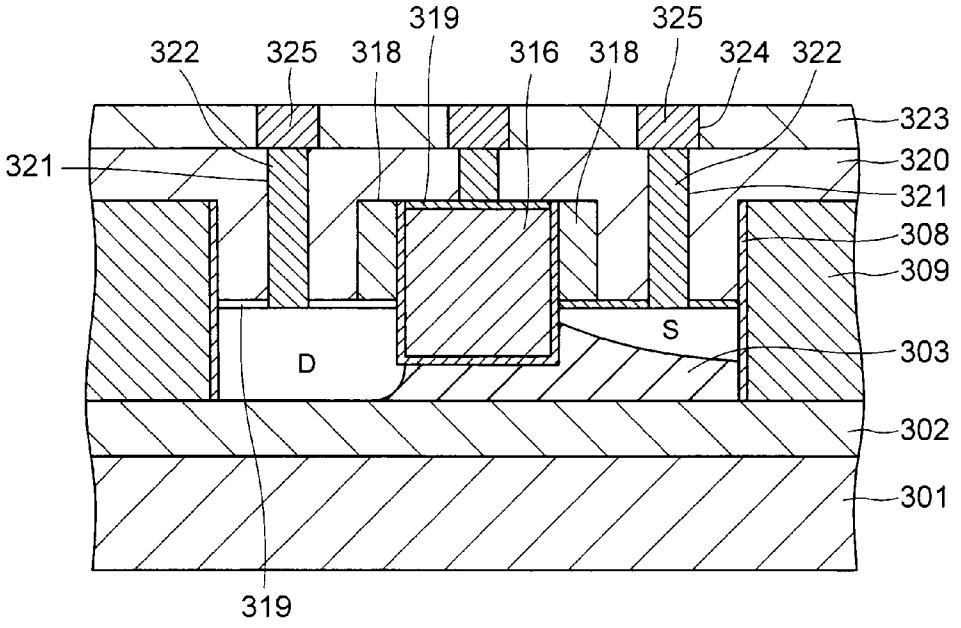

319
325
322
325
318
316
318
324
322
323
321
320
321
308
309
S
D
303
302
301
319

FIG.3

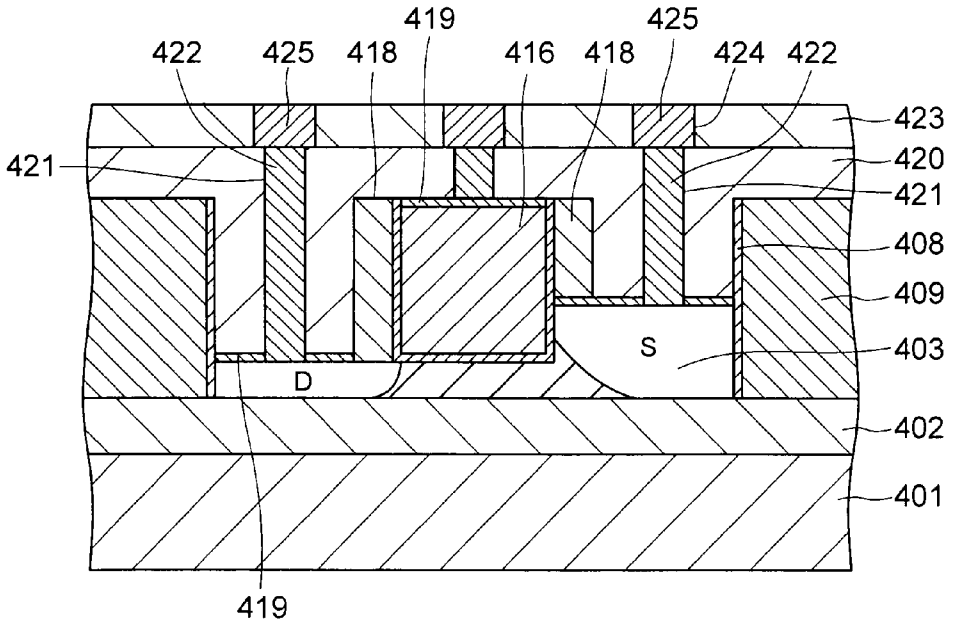

419
425
422
425
418
416
418
424
422
423
421
420
421
408
409
S
403
D
402
401
419

FIG.4

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation of and claims the benefit of priority under 35 U.S.C. §120 from U.S. Ser. No. 11/470,859 filed Sep. 7, 2006, and claims the benefit of priority under 35 U.S.C. §119 from Japanese Patent Application No. 2005-259494 filed Sep. 7, 2005; the entire contents of each of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to a semiconductor device and more particularly to a semiconductor memory device using a silicon on insulator (SOI) substrate. The present invention also relates to a manufacturing method of the semiconductor device.

[0003] The SOI substrate in which an insulation film (buried insulation film) is provided on a silicon substrate and a silicon layer is provided on the insulation film has been known in, for example, Japanese Patent Application Laid-Open Publication No. 2001-298171 and Japanese Patent Application Laid-Open Publication No. 5-257356 (1993).

[0004] A semiconductor memory device having a floating body cell (FBC) memory cell with a portion corresponding to a channel region of MOS transistor formed in the silicon layer on the buried insulation film of such an SOI substrate used as a floating body so as to accumulate electric charges has been developed.

[0005] In such a semiconductor memory device, the area of its memory cell can be extremely reduced because a capacitor may be eliminated, so that high integration can be achieved and accordingly the memory capacity per unit area can be increased.

[0006] In the FBC, as far as SOI film thickness concerned, as the degree of depleted condition is intensified to full depleted (FD) condition, namely, the thinner the SOI film be, the higher ΔVth which can serve as a criterion when detecting information accumulated in the memory cell may be increased. This ΔVth indicates a difference between Vth when "0" data is stored and Vth when "1" data is stored.

[0007] Because this FD condition is easier to be obtained as the thickness of the SOI film is decreased, the thickness of the SOI film is required to be decreased as much as possible from viewpoints of improvement (increase of ΔVth) of the performance of the memory cell of the FBC cell.

[0008] Furthermore, the BOX film which is buried oxide film is preferred to be as thin as possible in order to improve coupling between the body and a substrate electrode (hereinafter referred to a plate electrode) of the memory cell. Therefore, both of the buried oxide film and the SOI film thereon are preferred to be as thin as possible.

[0009] However, manufacturing of a SOI wafer with the BOX film set to less than 60 Angstrom in thickness and the SOI film set to less than 300 Angstrom in the SOI substrate requires highly accurate control of wafer manufacturing process, thereby leading to increase in wafer manufacturing cost, which is a large obstacle to achievement of an excellent FBC.

[0010] If the thickness of the SOI film is too small, when a contact is formed, not only electric short-circuit is likely to occur between the contact and plate potential but also contact resistance is increased, which is a problem to be solved. Although the SOI film can be thinned uniformly, if the SOI film is thinned to about 20 nm, the ΔVth is decreased, so that an intention of improving performance using a device under a fully depleted condition by thinning the SOI film is not achieved.

[0011] Additionally, if the BOX film is thinned extremely, diffusion capacitance increases so that sharing of process with a logic section, which is a large advantage of the FBC, becomes impossible.

SUMMARY OF THE INVENTION

[0012] According to a first aspect of the present invention, there is provided a semiconductor device comprising:

[0013] a channel region of a transistor formed in a predetermined region of silicon layer formed on insulation film;

[0014] a gate electrode formed on the channel region via gate insulation film; and

[0015] source/drain regions formed in the silicon layer thicker than said channel region located out of the channel region, wherein the transistor is a memory element constituting the channel region as a floating body cell.

[0016] According to a second aspect of the present invention, there is provided a semiconductor device comprising:

[0017] a channel region of transistor formed in a predetermined region of silicon layer formed on insulation film;

[0018] a gate electrode formed on the channel region via gate insulation film; and

[0019] a source region and a drain region formed in the silicon layer out of the channel region, said silicon layer having the same thickness of the channel region in the drain side while having thicker thickness than the channel region in the source side, wherein the transistor is a memory element constituting the channel region as a floating body cell.

[0020] According to a third aspect of the present invention, there is provided a method of manufacturing a semiconductor device, comprising:

[0021] forming stacked layers of a buried oxide film, a silicon film and silicon nitride film on a silicon substrate;

[0022] etching the nitride film to remain it for element region;

[0023] etching the silicon film and the buried oxide film to remain them for the element region;

[0024] filling an insulating film in a portion removed by the etching;

[0025] forming a trench in the silicon layer and the silicon nitride layer in the element region, the bottom of the trench being positioned in the thickness of the silicon film;

[0026] filling a gate material in the trench;

[0027] selectively removing the silicon nitride layer;

[0028] ion implanting to form source/drain regions; and

[0029] forming interconnections for leading out the source/drain and gate regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] FIGS. **1**A-**1**L are sectional views of a semiconductor device on respective steps showing a manufacturing method of the semiconductor device according to a first embodiment of the present invention;

[0031] FIGS. **2**A-**2**L are sectional views of a semiconductor device of respective steps showing a manufacturing method of the semiconductor device according to a second embodiment of the present invention;

[0032] FIG. **3** is a sectional view of the semiconductor device showing the structure of the semiconductor device according to a third embodiment of the present invention; and

[0033] FIG. **4** is a sectional view of a semiconductor device showing the structure of the semiconductor device according to a fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0034] Hereinafter, the embodiments of the present invention will be described in detail by taking a semiconductor memory device having a FBC memory cell as an example. Drawings shown below are not accurate representation of film thickness and the like but schematic ones.

(1) First Embodiment

[0035] An example of first manufacturing process for manufacturing a semiconductor device according to a first embodiment of the present invention will be described with reference to FIGS. **1**A-**1**L.

[0036] First, a SOI substrate **100** in which buried oxide film (BOX film) **102** in the thickness of 250 Angstrom is provided on a silicon semiconductor base material **101** and silicon film (SOI film) **103** in the thickness of 1500 Angstrom is formed thereon is prepared (FIG. **1**A).

[0037] Next, thermally-oxidized film **104** about 20 Angstrom thick is formed by heating the SOI substrate **100** in oxidation atmosphere and subsequently, SiN film **105** in the thickness of 1700 Angstrom is deposited and further, boro silicate glass (BSG) film **106** in the thickness of 3000 Angstrom is deposited (FIG. **1**B).

[0038] Next, resist pattern is formed for forming a device region of a desired pattern. That is, photo resist **107** is applied on its entire surface and the resist pattern is formed by patterning using photo lithography method. This pattern is a shape for keeping a portion corresponding to a device isolation expected region of a transistor to be formed later remained (FIG. **1**C).

[0039] The BSG film and SiN film are etched and removed using anisotropic etching method like RIE with employing the patterned resist **107** as masking material. As a consequence, the SOI film **103** and thermally-oxidized film **104** in the device isolation expected region are exposed outside (FIG. **1**D).

[0040] Subsequently, after the resist film **107** remained on the SOI substrate is removed, the SOI film **103** and the thermally-oxidized film **104** are etched using reactive ion etching (RIE) method with employing the BSG/BiN films **105**-**106** as masking materials. This etching depth is set to, for example, 1500 Angstrom. Therefore, the SOI film out of the device formation area is removed.

[0041] After this etching, reaction product at the time of etching is removed by washing and subsequently, the BSG film existing on the SiN film **105** is removed according to, for example, wet etching method (FIG. **1**E).

[0042] Then, thermally-oxidized film **108** is formed in the thickness of 40 Angstrom on the side face of the exposed SOI film **103** by thermal oxidation. The side portion of this thermally-oxide film is filled with TEOS film **109** because there is a trench with respect to a device formation area of an adjacent cell. Subsequently, according to CMP method (chemical mechanical polishing method) with the SiN film on the SOI used as stopper film, TEOS of a unnecessary portion is removed and flattened so as to form shallow trench isolation (STI). At this time, the remained film on the wafer of the SiN film is about 1500 Angstrom (FIG. **1**F).

[0043] Next, resist pattern in which only a cell portion is exposed is formed and after that, the resist is removed by ion-implantation of phosphor for plate electrode formation. SiN film **110** is deposited on the SOI wafer in the thickness of 200 Angstrom and next, BSG film **111** is deposited in the thickness of 1000 Angstrom (FIG. **1**(G)). Resist pattern **112** is formed such that the BSG film corresponding to a gate electrode is exposed and with this resist **112** used as masking material, the BSG/SiN **111**, **110**, the SiN film **105**, and the thermally-oxidized film **104** are etched up to the face of the SOI substrate **103** so as to form a trench **113** with the top face of the SOI **103** exposed outside (FIG. **1**G).

[0044] After the remained resist **112** is removed, a pattern in which the SOI portion expected to be formed into thin film is exposed is formed and by etching the exposed SOI film **103** according to the CDE method, a deeper trench **114** is formed so that the thickness of the SOI film **103** is adjusted to a desired thickness, for example, 400 Angstrom.

[0045] Next, the BSG film **111** remained on the SiN film **110** on the SOI substrate is removed by etching according to vacuum plasma method (VPC) and if necessary, ion implantation for Vt adjustment of Tr is carried out (FIG. **1**H).

[0046] Therefore, the thickness at a gate electrode formation expected location is reduced from the initially 1500 Angstrom to 400 Angstrom.

[0047] Next, thermally-oxidized film **115** is formed in the thickness of 60 Angstrom on the bottom and side wall of the trench **114** by thermal oxidation with this SOI **103** exposed and amorphous silicon doped with no impurity is deposited on the entire surface in the thickness of 2000 Angstrom so as to fill the trench **114**. Then, gate electrode **116** is formed according to damascene process for flattening using the CMP method.

[0048] Next, the SiN film **105** remained on the SOI substrate is removed using a chemical such as H_3PO_4 and oxide film **117** is formed on the surface of the SOI substrate **103** and the surface of the gate electrode **116** by post oxidation and ion implantation is carried out for doping for formation of desired diffusion layer. This ion implantation is carried out under a condition that dose of phosphor or boron is 3×10^{13} (hereinafter expressed as 3E13)/cm^2 and acceleration voltage is 10 keV (FIG. **1**I).

[0049] Next, layered film in the thickness of TEOS/SiN/TEOS 200/200/400 Angstrom are deposited on the entire surface of the SOI substrate and etching is carried out for leaving spacer **118** adjacent to the gate electrode **116** so as to expose the top face of the SOI substrate and polysilicon electrode. Then, phosphor or boron is ion-implanted into a desired region at a dose of 3E15/cm^2 or more at an acceleration voltage of 10 keV so that impurity is activated at high temperature for a short time according to RTA method (FIG. **1**J).

[0050] After activation is completed, the post oxidized film **117** is removed, cobalt (Co) is deposited on the entire surface of the SOI substrate and salicide film **119** is formed at a portion making direct contact with silicon by heat treatment. Excess cobalt at a portion in which no silicon exists is removed by etching.

[0051] After the salicide film is formed, SiN is deposited in the thickness of 200 Angstrom on the entire surface of wafer and next non-doped silicate glass (NSG) film **120**, which is silicate glass doped with no impurity, is deposited in the

thickness of 6000 Angstrom and then it is flattened according to the CMP method (FIG. **1**K).

[0052] Next, resist pattern for forming a contact between source/drain region and gate electrode is formed and the NSG film **120** is etched according to the RIE method until the top face of the SiN is exposed so as to form a contact hole **121** and remained resist is removed. Next, the SiN film exposed on the bottom of the contact hole **121** is removed by etching so that the top face of SOI/gate polysilicon is exposed within the contact hole **121** and then, three-layered film of Ti/TiN/W are deposited in the thickness of 100/200/3000 Angstrom respectively. Then, the Ti/TiN/W of other portion than the contact portion is removed according to the CMP method so that the Ti/TiN/W layered film **122** is left only inside the contact. Next, NSG film **123** about 3000 Angstrom is deposited and a channel **124** is formed at a portion corresponding to a wiring layer pattern and Cu is deposited therein by plating. Then, SL electrode **125** is formed by etching the Cu at an unnecessary portion according to the CMP method (FIG. **1**L).

[0053] After that, wiring metal layer and contact are formed using dual damascene process of executing these at the same time as filling a contact with metal (Cu) and finally, a semiconductor device is completed.

[0054] Because in the semiconductor device of this embodiment, the thickness of the SOI film at the channel portion is sufficiently small, FD state can be attained so as to increase ΔVth. This is particularly advantageous when this semiconductor device is used as a semiconductor device containing FBC cell.

[0055] Further, because according to the manufacturing process described above of this semiconductor device, when FBC memory cell is manufactured using a thick SOI substrate, the gate electrode of a memory cell is formed by using damascene process in which a channel is formed by reducing the film thickness of the SOI portion in a channel region until a desired thickness is reached before formation of gate insulation film and this channel
is filled with gate electrode material, stabilized thin SOI film having a high reliability can be obtained.

[0056] Further, because the thickness of the SOI film in other region than the channel region of the gate electrode bottom portion is a thickness which may be formed easily using current SOI wafer manufacturing technology, increase in manufacturing cost of the SOI wafer can be prevented.

[0057] Furthermore, because the SOI film thickness in other region than the channel region is sufficiently large, electric short-circuit between the contact and plate potential upon formation of a contact can be prevented easily.

[0058] FIGS. **2**A-**2**L are sectional views of a semiconductor device for explaining a second manufacturing process for manufacturing the semiconductor device according to the second embodiment of the present invention.

[0059] Here, SOI substrate in **200** which BOX film **202** in the thickness of 250 Angstrom and SOI film **203** in the thickness of 1500 Angstrom are provided on silicon substrate **201** like the first embodiment is used (FIG. **2**A).

[0060] Next, thermally-oxidized film **204** about 20 Angstrom is formed by heating the SOI substrate **200** in oxidation atmosphere and subsequently, SiN film **205** in the thickness of 1700 Angstrom is deposited and further, boron silicate glass (BSG) film **206** in the thickness of 3000 Angstrom is deposited (FIG. **2**B).

[0061] Next, resist pattern is formed for forming a device region of a desired pattern. That is, photo resist **207** is applied on its entire surface and the resist pattern is formed by patterning using photo lithography method. This pattern has a shape for keeping a portion corresponding to a device isolation expected region of a transistor to be formed later remained (FIG. **2**C).

[0062] The BSG film **206** and SiN film **205** are etched and removed according to anisotropic etching method like RIE by using this patterned resist **207** as masking material. As a consequence, the SOI film **203** and thermally-oxidized film **204** in the device isolation expected region are exposed outside (FIG. **2**D).

[0063] Subsequently, after the resist film **207** remained on the SOI substrate is removed, the SOI film **203** and the thermally-oxidized film **204** are etched according to reactive ion etching (RIE) method by using the BSG/BiN films **205**-**206** as masking materials. This etching depth is set to, for example, 1500 Angstrom. Therefore, the SOI film **203** out of the device formation area is removed.

[0064] After this etching, reaction product at the time of etching is removed by washing and subsequently, the BSG film **206** existing on the SiN film **205** is removed according to, for example, wet etching method (FIG. **2**E).

[0065] Then, thermally-oxidized film **208** is formed in the thickness of about 40 Angstrom on the side face of the exposed SOI film **203** by thermal oxidation. The side portion of this thermally-oxide film is filled with TEOS film **209** because there is a trench with respect to a device formation area of an adjacent cell. Subsequently, according to CMP method (chemical mechanical polishing method) with the SiN film on the SOI used as stopper film, TEOS of a unnecessary portion is removed and flattened so as to form shallow trench isolation (STI). At this time, the remained film on the wafer of the SiN film is about 1300 Angstrom (FIG. **2**F).

[0066] Next, resist pattern in which only a cell portion is exposed is formed and after that, the resist is removed by ion-implantation of phosphor for plate electrode formation. SiN film **210** is deposited on the SOI wafer in the thickness of 200 Angstrom.

[0067] Next, Resist pattern **212** is formed such that the BSG film corresponding to a gate electrode and a spacer adjacent to the gate is exposed and with this resist **212** used as masking material, the SiN film **210**, **205**, and the thermally-oxidized film **204** are etched up to the face of the SOI substrate so as to form a trench **213** with the top face of the SOI **203** exposed externally (FIG. **2**G).

[0068] After the remained resist **211** is removed, a pattern for exposing the SOI portion whose film is expected to be thinned is formed again and by etching the exposed SOI film **203** according to CDE method, a deeper trench **214** is formed so as to turn the thickness of the SOI film **203** to a desired thickness, for example, 400 Angstrom (FIG. **2**H). Therefore, the thickness at a gate electrode formation expected location is reduced from the initially 1500 Angstrom to 400 Angstrom (FIG. **2**H).

[0069] Next, by thermal oxidation with this SOI film exposed, thermally-oxidized film is formed in the thickness of 60 Angstrom on the bottom and side wall of the trench **214** and the trench **214** is filled with amorphous silicon doped with no impurity such that it is deposited in the thickness of 2000 Angstrom and then, damascene process is carried out for flattening using the CMP method. Further, by removing the SiN film remained on a portion on the source/drain of a portion formed by burying and the SOI substrate with chemical like H_3PO_4, gate electrode **215** is obtained. After ther-

mally-oxidized film **216** is formed on an exposed surface by thermal oxidation, ion implantation is carried out for doping for formation of desired diffusion layer. This ion implantation is carried out under a condition that dose of phosphor or boron is 3E13/cm^2 and acceleration voltage is 10 keV (FIG. **21**).

[0070] Next, TEOS/SiN/TEOS 200/200/400 Angstrom thick are deposited as layered film on the entire surface of the SOI substrate and etching is carried out for leaving spacer **218** adjacent to the gate electrode **215** within the trench **214** so as to expose oxide film **216** on the top face of the SOI substrate **203** and polysilicon electrode **215**. Then, phosphor or boron is ion-implanted into a desired region at a dose of 3E15/cm^2 or more at an acceleration voltage of 10 keV, so that impurity is activated at high temperature for a short time using RTA method (FIG. **2**J).

[0071] After activation is ended, the oxidized film **216** is removed, cobalt (Co) is deposited on the entire surface of the SOI substrate and salicide film **219** is formed at a portion making direct contact with silicon by heat treatment. Excess cobalt at a portion in which no silicon exists is removed by etching.

[0072] After the salicide film is formed, SiN is deposited in the thickness of 200 Angstrom on the entire surface of wafer and next non-doped silicate glass (NSG) film **120**, which is silicate glass doped with no impurity, is deposited in the thickness of 6000 Angstrom and then it is flattened using the CMP method (FIG. **2**K).

[0073] Next, resist pattern for forming a contact between source/drain region and gate electrode is formed and the NSG film **220** is etched using the RIE method until the top face of the SiN is exposed so as to form a contact hole **221** and remained resist is removed. Next, the SiN film exposed on the bottom of the contact hole **121** is removed by etching so that the top face of SOI/gate polysilicon is exposed within the contact hole **221** and then, three-layered film of Ti/TiN/W are deposited in the thickness of 100/200/3000 Angstrom respectively. Then, the Ti/TiN/W of other portion than the contact portion is removed using the CMP method so that the Ti/TiN/W stacked film **222** is left only inside the contact. Next, NSG film **223** about 3000 Angstrom is deposited and a channel **224** is formed at a portion corresponding to a wiring layer pattern and Cu is deposited therein by plating. Then, SL electrode **225** is formed by etching the Cu at an unnecessary portion using the CMP method.

[0074] After that, wiring metal layer and contact are formed using dual damascene process of executing these at the same time as filling a contact with metal (Cu) and finally, a semiconductor device is completed.

[0075] Because in the semiconductor device of this embodiment, the thickness of the SOI film at the channel portion is sufficiently small, FD state can be attained so as to increase ΔVth. This is particularly advantageous when this semiconductor device is used as a semiconductor device containing FBC cell.

[0076] Because according to this embodiment, the spacer is formed within the trench whose film thickness is reduced, the thin portion is expanded thereby obtaining a secure FD state.

[0077] Although in the examples of the above-described two manufacturing processes, the dimension of the channel in which the gate electrode is to be formed is based on a dimension specified by lithography, it is permissible to set a portion expected to be thinned of the SOI smaller than a portion specified by lithography by using the RIE method for etching to leave the side wall by depositing the BSG film preliminarily before the CDE process.

[0078] FIG. **3** is a sectional view of a semiconductor showing the structure of the semiconductor according to the third embodiment of the present invention.

[0079] The third embodiment will be described by comparing the structure of the first embodiment shown in FIG. **1**L. In FIG. **3**, reference numerals of the order from 300 are used and numbers of the order from 10 and from 1 correspond to those in FIG. **1**L.

[0080] Although the structure of FIG. **3** is almost the same as the first embodiment, a different point is the profile of drain region (D) and source region (S) formed in SOI film **303**. That is, although in FIG. **3**, the drain region (D) has completely the same profile as the first embodiment and is in contact with thin SOI film in a channel portion, the front end of the source region (S) is located on the surface of the SOI film on the side face of a gate electrode and its diffusion depth is shallow in entire source region.

[0081] To obtain such a structure, ion implantation condition for formation of diffusion layer described in FIG. **1**J is changed between the drain region and source region and for the source region, the dose and acceleration voltage are reduced as compared to the drain region, as 3E13/cm^2 and 10 keV.

[0082] Because with such a structure, coupling between the drain region and body region can be set larger than coupling between the source region and body region, deterioration of Vth is unlikely to occur even if the SOI in the channel region is thinned, thereby improving memory performance.

[0083] FIG. **4** is a sectional view of a semiconductor showing the structure of the semiconductor according to the fourth embodiment of the present invention.

[0084] The fourth embodiment will be described by comparing the structure of the first embodiment shown in FIG. **1**L. In FIG. **4**, reference numerals of the order from 400 are used and numbers of the order from 10 and from 1 correspond to those in FIG. **1**L.

[0085] Although the structure of FIG. **4** is almost the same as the first embodiment, a different point is that the thickness of the SOI film constituting the drain region is equal to the thickness of the channel portion.

[0086] Such a structure can be obtained by applying the manufacturing process described in the second embodiment. That is, an opening formed in the process of FIG. **2**G is expanded over entire channel portion and drain region to reduce thickness of the SOI film over the entire channel portion and drain region.

[0087] Although in this embodiment, as same as the embodiment shown in FIG. **3**, the drain region (D) is in contact with the channel portion just below the gate electrode, the front end of the source region (S) is located on the surface of the SOI film on the side face of the gate electrode. Such a difference in profile is obtained by adopting the method described about the structure of FIG. **3**.

[0088] Because in the semiconductor device of the fourth embodiment also, the coupling between the drain region and body region is set larger than the coupling between the source region and body region, deterioration of Vth is unlikely to occur even if the SOI is thinned in the channel region, thereby improving the memory performance.

[0089] Because in the semiconductor of the above-described embodiments, the SOI film of the channel portion is

thinned sufficiently while maintaining the thickness of the BOX oxide film, complete depletion action for writing data "0" and partial depletion action for writing data "1" are enabled so as to increase ΔVth. This is advantageous when this semiconductor device is used as a semiconductor memory device containing FBC cell.

[0090] Further, because the coupling capacity of the source side of the FBC can be increased, the ΔVth can be increased.

[0091] Because according to the present invention, the thickness of the SOI film in the channel portion of a transistor is set smaller than the thickness of the SOI film of the source/drain diffusion layer portion, an excellent transistor characteristic is secured and a semiconductor device easy to manufacture can be provided.

[0092] Such a semiconductor device is effective particularly if it is used as a memory device of the FBC memory cell.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

an insulating film formed on the semiconductor substrate, the insulating film including a flat upper surface;

a silicon layer formed on the flat upper surface of the insulating film, the silicon layer including a first portion having a first upper surface, a second portion having a second upper surface and a third portion having a third upper surface and located between the first and second portions, wherein a first thickness of the silicon layer between the first upper surface in the first portion of the silicon layer and the flat upper surface of the insulating film is same as a second thickness of the silicon layer between the second upper surface in the second portion of the silicon layer and the flat upper surface of the insulating film, and a third thickness of the silicon layer between the third upper surface in the third portion of the silicon layer and the flat upper surface of the insulating film is smaller than the first thickness of the silicon layer;

a gate electrode of a floating gate body cell, formed above the third upper surface in the third portion of the silicon layer, wherein the gate electrode includes a fourth upper surface and a first and a second side walls, the first side wall has a first facing portion facing to the first portion of the silicon layer, the second side wall has a second facing portion facing to the second portion of the silicon layer, and a height of the fourth upper surface of the gate electrode is higher than a height of the first upper surface in the first portion of the silicon layer relative to the flat upper surface of the insulating film;

a drain region formed in the first portion in the first side wall of the silicon layer, the drain region facing to whole of the first facing portion in the first side wall of the gate electrode; and

a source region formed in the second portion in the second side wall of the silicon layer, the source region facing to a part of the second facing portion in the second side wall of the gate electrode,

wherein the second facing portion of the gate electrode includes a lower portion which does not face to the source region.

2. The semiconductor device according to claim **1**, wherein the drain is formed from the first upper surface in the first portion of the silicon layer to a bottom portion in the first portion of the silicon layer.

3. The semiconductor device according to claim **1**, wherein the source region is formed at the second upper surface in the second portion of the silicon layer.

4. The semiconductor device according to claim **1**, wherein the third thickness in the third portion of the silicon layer is less than 400 Angstrom.

5. The semiconductor device according to claim **1**, wherein the first side wall between the fourth upper surface and the first upper surface is covered with a first spacer film, and the second side wall between the fourth upper surface and the second upper surface is covered with a second spacer film.

6. A semiconductor device comprising:

a semiconductor substrate;

an insulating film formed on the semiconductor substrate, the insulating film including a flat upper surface;

a silicon layer formed on the flat upper surface of the insulating film, the silicon layer including a first portion having a first upper surface, a second portion having a second upper surface and a third portion having a third upper surface and located between the first and second portions, wherein a first thickness of the silicon layer between the first upper surface in the first portion of the silicon layer and the flat upper surface of the insulating film is same as a second thickness of the silicon layer between the second upper surface in the second portion of the silicon layer and the flat upper surface of the insulating film, and a third thickness of the silicon layer between the third upper surface in the third portion of the silicon layer and the flat upper surface of the insulating film is smaller than the first thickness of the silicon layer;

a gate electrode of a floating gate body cell, formed above the third upper surface in the third portion of the silicon layer, wherein the gate electrode includes a fourth upper surface and a first and a second side walls, the first side wall has a first facing portion facing to the first portion of the silicon layer, the second side wall has a second facing portion facing to the second portion of the silicon layer, and a height of the fourth upper surface of the gate electrode is higher than a height of the first upper surface in the first portion of the silicon layer relative to the flat upper surface of the insulating film;

a drain region formed in the first portion of the silicon layer, wherein a fourth thickness of the drain region relative to the first upper surface is larger than a thickness of the first facing portion in the first side wall of the gate electrode; and

a source region formed in the second portion of the silicon layer, wherein a fifth thickness of the source region relative to the second upper surface is smaller than a thickness of the second facing portion in the second side wall of the gate electrode.

7. The semiconductor device according to claim **6**, wherein the drain region is formed from the first upper surface in the first portion of the silicon layer to a bottom portion in the first portion of the silicon layer.

8. The semiconductor device according to claim **6**, wherein the source region is formed at the second upper surface in the second portion of the silicon layer.

9. The semiconductor device according to claim **6**, wherein the third thickness in the third portion of the silicon layer is less than 400 Angstrom.

10. The semiconductor device according to claim **6**, wherein the first side wall between the fourth upper surface and the first upper surface is covered with a first spacer film, and the second side wall between the fourth upper surface and the second upper surface is covered with a second spacer film.

* * * * *