United States Patent

Jones

[15] **3,641,556**

[45] **Feb. 8, 1972**

[54] CHARACTER ADDRESSING SYSTEM

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[52] **U.S. Cl.** .....**340/324 A**, 315/18

[51] **Int. Cl.** **G06f 3/14**

[58] **Field of Search**.....340/324.1, 324 A; 315/18, 26, 315/19; 178/6.8, 7.5 SE

[56] **References Cited**

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[57] **ABSTRACT**

In a cathode-ray tube display, digital signals representative of characters to be generated are divided into two groups representing the two directions of deflection. A first group provides a linear region in which uniform deflection steps are generated for each signal increment, while a second group provides a nonlinear region in which varied deflection increments are generated for each signal increment. The nonuniform regions provide higher resolution in those areas where curves normally occur and less resolution in the remaining areas thus providing higher character resolution in specified positions on the same size matrix. The nonuniform deflection is obtained from associated decoders through a weighted addressing system which provides nonuniform current increments independent of the digital data input.

6 Claims, 7 Drawing Figures

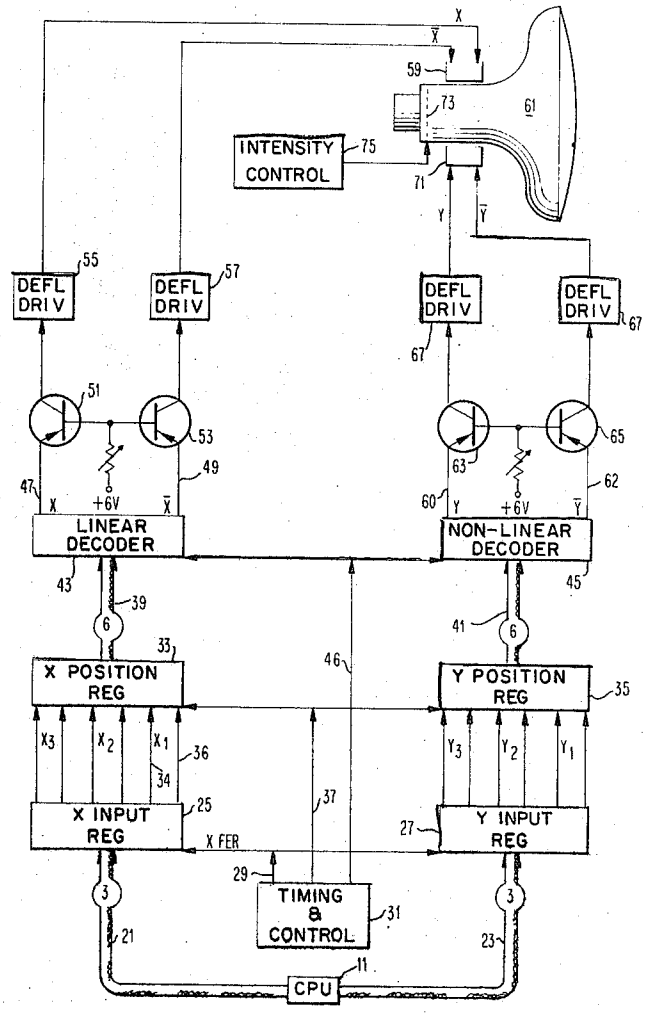

FIG. 1

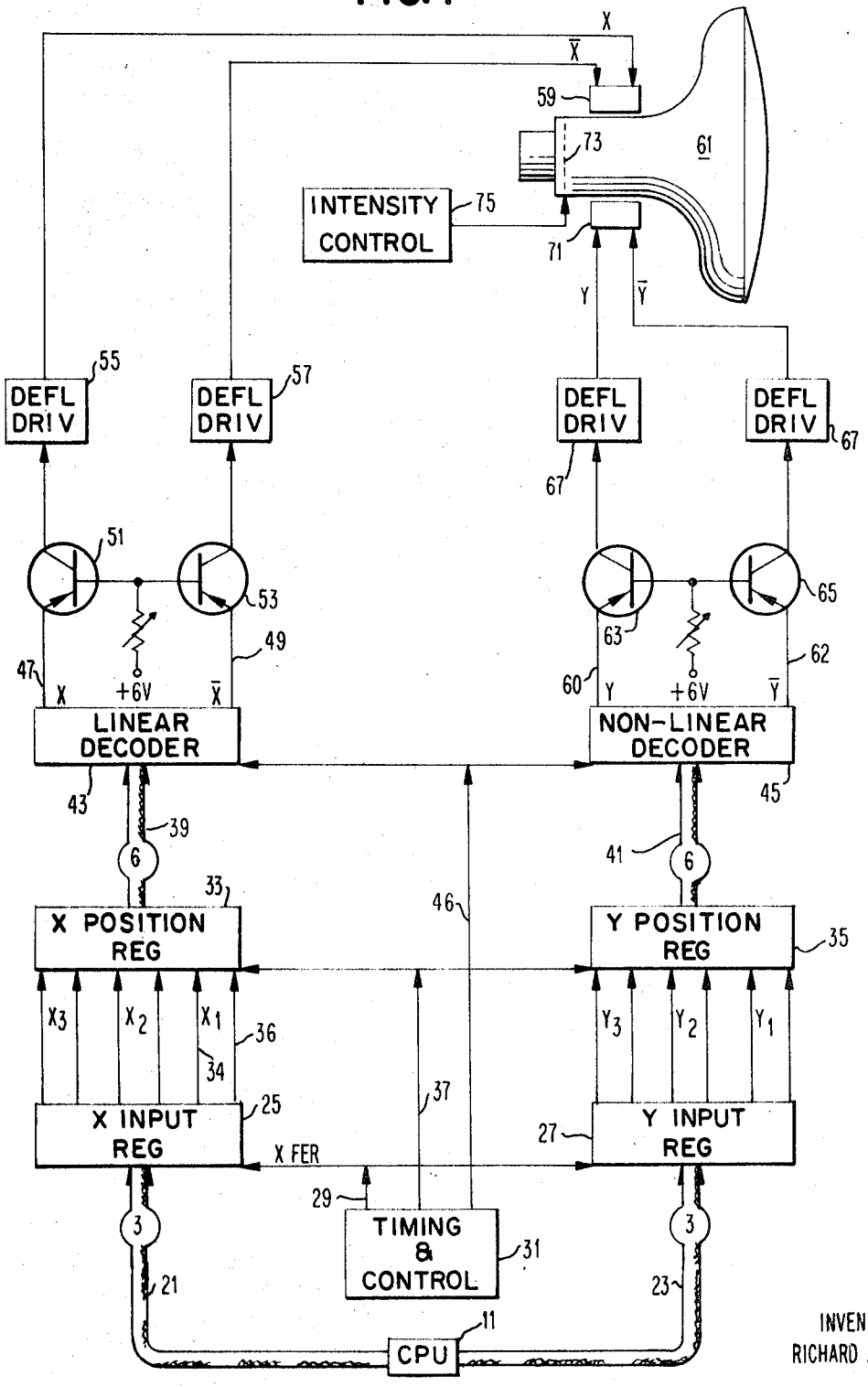

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FIG. 2a

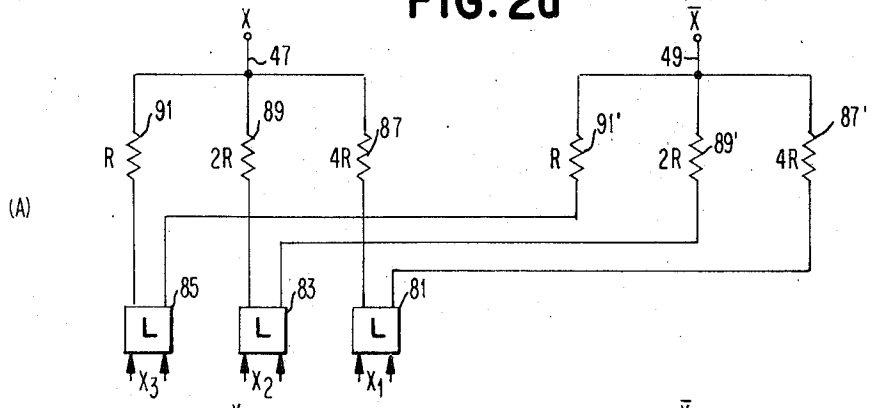

FIG. 2b

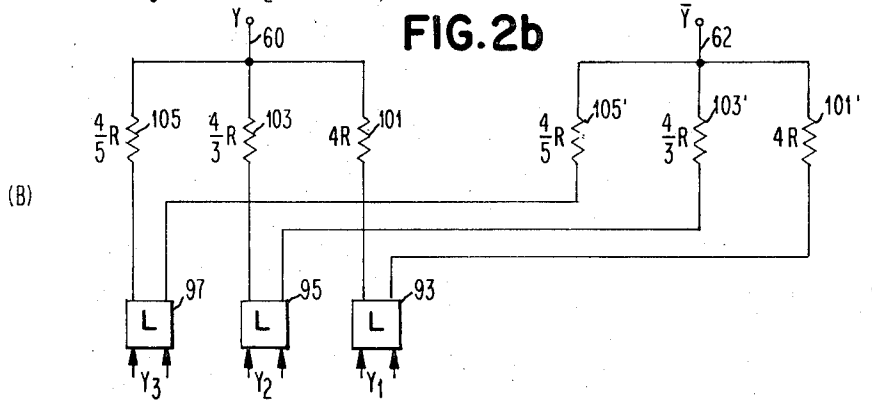

FIG. 3

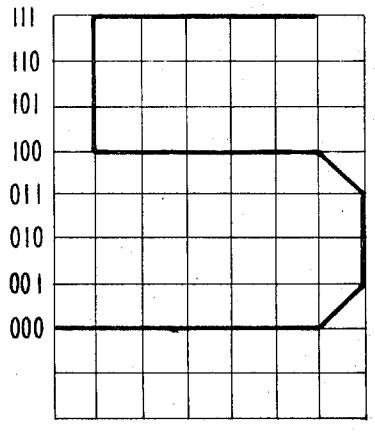

FIG. 3a

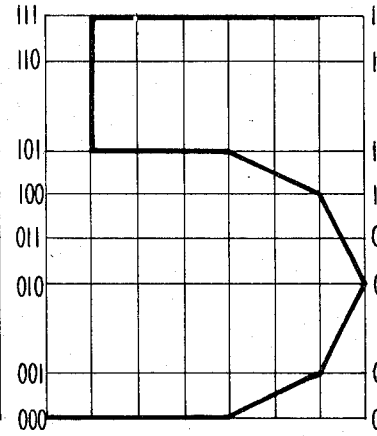

FIG. 3b

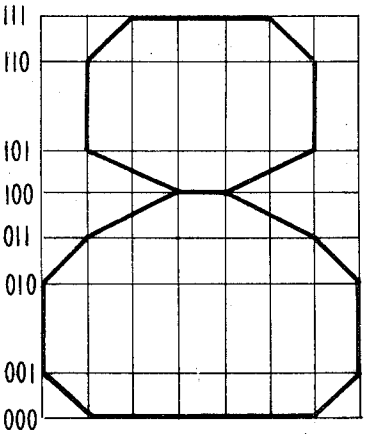

FIG. 3c

CHARACTER ADDRESSING SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a display device and more particularly to an improved character generator deflection system suitable for use with cathode-ray tubes for displaying the generated characters.

2. Description of the Prior Art

In known cathode-ray tube character generation systems, characters are normally generated on a linear coordinate matrix on the CRT screen either as a sequence of strokes or dots in which the size of the matrix determines the resolution. An example of a stroke character generator using a uniform rectangular matrix is shown in U.S. Pat. No. 3,334,304, "Asynchronous Character Generator for Successive Endpoint Definition," issued to R. J. Fournier et al., Aug. 1, 1967. However, where the size of the coordinate matrix is limited, uniform resolution in all areas of the character tends to produce an undesirable font, particularly in those areas where curves tend to occur. An analysis of stroke characters indicates that most end points occur at the extremities and center of the character such that increased resolution in this area will improve character quality. While improved resolution can normally be provided by increasing the size of the character matrix, this is undesirable because of added circuit complexity, flicker problems and storage capacity limitations. Where the video information is stored in a recirculating buffer, for example, an increase of the character matrix from 7×7 to 10×10 effectively more than doubles the storage requirements of the display. The present invention is directed to a means for increasing character resolution in a cathode-ray tube display without any added complexity in size or cost.

SUMMARY OF THE INVENTION

In one arrangement according to the invention, digital signals indicative of characters to be generated on a CRT display are decoded into analog signals suitable for deflecting the beam of the cathode-ray tube. Rather than generate the characters on a uniform coordinate grid, the present invention utilizes a linear deflection for one coordinate of the character (the horizontal), and a nonlinear deflection for the second coordinate of the character. This nonlinear deflection is obtained by weighting the individual decoded deflection signals such that smaller deflection units affording higher resolution are provided at those areas where the curved segments of most characters tend to occur. Those areas of the matrix not normally associated with curved characters utilize higher deflection units resulting in greater spacing without character degradation.

Accordingly, a primary object of the present invention is to provide an improved character generator circuit.

Another object of the present invention is to provide an improved deflection system for improving the resolution of specific character areas by modifying the deflection control to provide a nonuniform deflection in one of the character coordinates.

Another object of the present invention is to provide an improved character generator having a linear and nonlinear addressable grid system designed to improve the aesthetic appearance of characters.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 illustrates in block logical form a preferred embodiment of the present invention.

FIG. 2*a* illustrates in schematic form a binary weighted decoder shown in block form in FIG. 1.

FIG. 2*b* illustrates in schematic form a nonlinear weighted decoder shown in block form in FIG. 1.

FIG. 3 illustrates character display formats.

FIG. 3*a* illustrates a character generated by using the conventional addressable grid matrix.

FIGS. 3*b* and 3*c* illustrate characters generated in accordance with the addressable matrix of the present invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

Referring now to the drawings and more particularly to FIG. 1 thereof, binary coded signals are applied from a data source which might comprise, for example, a data processor such as Central Processing Unit 11 through input lines 21 and 23 to the X input register 25 and the Y input register 27, respectively. A data byte comprising six binary bits is used for each character stroke, three bits for the horizontal deflection and three bits for the vertical deflection. The preferred embodiment of the present invention utilizes an 8×8 character matrix which can be provided by three bits for each coordinate, each three-bit signal designating the end point of the vector. In response to a transfer signal on the line 29 from timing and control circuit 31, the contents of the X and Y input register are transferred through conductor pairs labeled X1, X2, X3 and Y1, Y2 and Y3, with X1 and Y1 representing the lowest order binary bits, to the X and Y Position Registers 33 and 35, respectively. The preferred embodiment of the instant invention is described as operating in double-ended, push-pull configuration such that each binary designation utilizes separate lines to represent the 1 and 0 states. The X and Y position registers 33 and 35 comprise count-up, countdown counters or registers which are incremented or decremented in accordance with the input signals applied from the associated input registers. A +X signal on line 34 will increment Position Register 33 by one, a −X signal on line 36 will decrement the counter by one. While various count-up, countdown counters are known in the art, one preferred embodiment is shown in U.S. Pat. No. 3,403,286 (IBM Docket Ki866009), "Digital Cathode Ray Deflection System" filed by F. R. Carlock et al., Dec. 27, 1966. Since the present invention is directed only to character generation, the initial positioning for each character has been omitted as unnecessary to an understanding of the present invention. However, either a separate deflection coil could be utilized to initially position the beam for character generation, or alternatively, the X and Y position registers 33 and 35 could be large enough to accommodate both the character position and individual stroke deflection signals.

In response to a transfer signal from timing and control circuit 31 on line 37, the contents of the X and Y Position Registers 33 and 35 are transferred through conductors 39 and 41 to their associated decoders 43 and 45, respectively. The horizontal decoder 43, as more fully described hereinafter, is a conventional binary weighted linear decoder in which uniform increments or decrements of current are provided for each positive of negative signal applied to the X position register 33. The vertical decoder 45 in the preferred embodiment of the instant invention is a nonlinear decoder in which the digital addresses, when decoded, generate nonuniform incremental steps to provide higher resolution in the upper, lower and center areas and lesser resolution in the noncritical intermediate area as more fully described hereinafter. In response to a control signal on line 46, the cumulative X signals on lines 47 and 49 from horizontal linear decoder 43 are transferred via lines 47 and 49 to their respective buffer transistors 51 and 53, respectively. Buffer transistors 51 and 53 function to isolate the decoder output from the associated deflection drive circuits 55 and 57, respectively. The output from the deflection drivers 55 and 57 are then applied to the horizontal yoke winding 59 of CRT 61. Likewise, the output from the vertical decoder 45 on lines 60 and 62 is applied through associated buffer transistors 63 and 65 and associated deflection drivers 67 and 69 to the vertical yoke winding 71 of CRT 61.

As the individual horizontal and vertical deflection signals are applied to the associated yoke windings 59 and 71 in the manner above described, the grid 73 is maintained unblanked by means of intensity control circuit 75. Intensity control cir-

cuits for maintaining a CRT beam in the unblanked condition during character generation are well known in the art such that a block showing is considered to constitute adequate description. However, one conventional method is to include an extra bit in the end point data for intensity control information.

Referring now to FIG. 2*a*, there is illustrated in block schematic form details of the horizontal linear decoder shown as block **43** in FIG. **1**. The decoder as shown is a double-ended decoder operating on three bits ranging from the lowest order bit **X1** through **X2** and **X3**. Since the decoder operates in a push-pull fashion, a latch register comprising latch circuits **81**, **83** and **85** is employed, each stage having binary 1 and 0 outputs, the respective outputs of which in turn are connected to binary weighted resistors **87**, **89** and **91** and **87'**, **89'** and **91'**. Latch circuits are well-known components in a data processor, are similar to flip-flops or triggers except for timing considerations related to reversal of state. For a detailed description of latch registers and latch circuits, reference is made to U.S. Pat. No. 3,115,574 to G. T. Paul et al., entitled "High Speed Multiplier," FIGS. **33–35** and related description. The values of **4R**, **2R** and **R** are merely relative to reflect the binary weighting of each binary bit in proportion to its place value. Actual values would vary according to the deflection system employed, the character size, etc., and such values represent mere design considerations known to those skilled in the art. The outputs on lines **47** and **49**, representing the cumulative horizontal deflection signals, are connected to the buffer transistors **51** and **53** as shown in FIG. **1**. As shown in the grid arrangements of FIG. **3**, the horizontal decoders provide uniform horizontal deflection increments for each input signal permutation. Since the characters or character segments may be generated either from left to right or right to left, depending on the specific character configuration, the decoder **43** responds to the output from the X position register **33** (Fig. **1**) which may be incremented or decremented in single steps heretofore described.

Referring now to FIG. 2*b*, the nonlinear vertical decoder **45** utilized in the preferred embodiment of the invention is shown in block schematic form. The three-bit coded signals for each character segment are applied to the appropriate latch register stages **93**, **95** or **97**, the individual outputs of which are connected to resistors **101**, **103** and **105** and **101'**, **103'** and **105'**. However, instead of being binary weighted as in the horizontal deflection, the vertical decoder stages are weighted in a ratio of 1:3:5 to reflect the expansion factor of 1 which has been added to the weighting values corresponding to the binary place values of 2 and 4. The weighting value corresponding to the place value of 1 has not been expanded. For purposes of comparison, the low order bit of decoder **45** is also designated as **4R**, the next more significant bit as **4/3 R**, and the most significant bit **4/5 R**. The relative ratio of the currents for the eight possible input combinations to the decoder is shown in decreasing binary increments in the table below, the tabulated coded values corresponding to those shown in Figures 3*b* and 3*c*.

TABLE 1

Y3	Y2	Y1	I
1	1	1	2¼ I
1	1	0	2 I
1	0	1	1½ I
1	0	0	1¼ I
0	1	1	1 I
0	1	0	184 I
0	0	1	¼ I
0	0	0	0

It should be noted that the values for current indicated in the table above are relative, the actual values again being determined by various design considerations associated with the specific cathode-ray tube display. The outputs from nonlinear decoder **45** are applied through associated conductors **60** and **62** to the vertical winding **71** of the magnetic yoke.

Referring now to FIG. **3**, there is illustrated a sequence of characters including one generated by the conventional rectangular grid and several characters generated in accordance with the preferred embodiment of the present invention, all characters being generated on an 8×8 matrix. Referring initially to FIG. 3*a*, the character **5** is shown on an 8×8 coordinate matrix, eight segments representing the maximum resolution which can be achieved from a three-bit by three-bit word. The numeral "5" has been selected as exemplary of problems associated with the conventional coordinate grid matrix. As shown thereon, and particularly at the normally curved center and lower portions of the figure, the limited resolution provides a very poor image quality such that the numeral "5" cannot be readily distinguished from the letter "S." Further, purely from a human factors standpoint, the appearance of the character is undesirable. One way and the conventional way of improving image quality is to increase the resolution of the available grid from 8×8 to some higher number depending on the degree of resolution desired. However, this requires a larger word size, and the entire system including the input registers, the position registers, decoders, buffer and even the data processor transmitting the data bytes would all necessarily be larger to accommodate the larger word such that this solution from an economic standpoint is impractical.

A practical solution for improving character quality is provided by the instant invention. The drawings of FIG. **3** are not intended to indicate a precise character size, but are enlarged and exaggerated to identify the problem. However, the relative proportions correspond to characters generated by the instant invention. Referring to FIGS. 3*b* and 3*c*, there are shown several characters generated on a variation of an 8×8 matrix utilizing the principles of the instant invention. It will be noted that the upper lines of the matrix (**111, 110**), the lower lines (**000,001**) each have areas of fine resolution and that a series of fine resolution lines are shown in the center portion (**010, 011, 100, 101**). However, both the intermediate lower (**001** to **010**) and intermediate upper (**101** to **110**) sections provide a relatively gross resolution in this area. However, it is apparent from FIGS. 3*b* and 3*c* that gross resolution in this area does not constitute a problem but from an aesthetic standpoint, actually enhances the character appearance. Thus it is seen that although the digital data input is not increased, improved overall resolution is achieved by using grossly resolved data in noncritical areas and finely resolved data in critical areas. The corresponding vertical addresses of each unit of deflection are shown in FIGS. 3*b* and 3*c* and the image quality, as readily apparent, is substantially enhanced over that provided by the conventional square address matrix of FIG. 3*a*.

While the advantages of improved character quality may not be readily apparent from the exaggerated drawings of FIG. **3**, they are apparent in a display system when it is recognized that in actual size where up to 960 characters may be displayed on a cathode-ray tube screen of approximately 14 inches. The invention affords improved image quality with no required change in input data and minimum change from the conventional square grid matrix.

While the invention has been shown and described with reference to a specific embodiment, it is apparent that other modifications to either or both deflection systems to alter character appearance are encompassed within the teaching of the subject invention, and that while the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. In a cathode-ray tube character generator, the combination comprising:

a cathode-ray tube having beam deflection means and intensity control means;

a source of video data representative of characters to be displayed;

said video data being applied for each stroke of said character, first and second decoder means for converting said video data into deflection signals;

said first decoder means being adapted to produce uniformly weighted linear signals;

said second decoder producing a nonuniformly weighted incremental signals, and

means connecting said uniformly weighted and said nonuniformly weighted signals to said beam deflection means to produce linear deflection signals in one direction and nonlinear deflection in the orthogonal direction whereby the resolution of the generated characters is substantially improved.

2. Apparatus of the type claimed in claim 1 wherein the output of said first decoder means has a plurality of regions within its output range, said regions including areas of high resolution and low resolution.

3. Apparatus of the type claimed in claim 2 wherein said areas of high resolution include the upper, lower and medial regions of said characters.

4. A method for decoding digital signals each having a plurality of groups representing coordinates of display stroke end points of a character to be displayed with increased resolution, comprising the steps of:

1. weighting a first binary data bit of a first digital signal group by a first value corresponding to the binary place value of said first binary data bit to provide a first analog signal;

2. weighting a next more significant binary bit of said first digital signal group by a second value corresponding to the binary place value of said next more significant binary data bit plus an expansion factor to provide a second analog signal;

3. weighting a second more significant binary data bit of said first digital signal group by a third value corresponding to the binary place value of said second more significant binary data bit plus said expansion factor to provide a third analog signal;

4. summing said first, second and third analog signals to provide a first coordinate of a display stroke end point.

5. The method of claim 4 further comprising the steps of:

5. weighting each binary data bit of a second digital signal group by values corresponding to the binary place values of each of said binary data bits of said second digital signal group to provide analog signals;

6. summing said analog signals to provide a second coordinate of said display stroke end point.

6. The method of claim 5 further comprising the steps of:

7. repeating Steps 1 through 6 for each digital signal representing a display stroke end point of a character to be displayed whereby said character has a high resolution concentrated in upper, medial, and lower regions, and has a lower resolution between said upper and said medial and between said medial and said lower regions.

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