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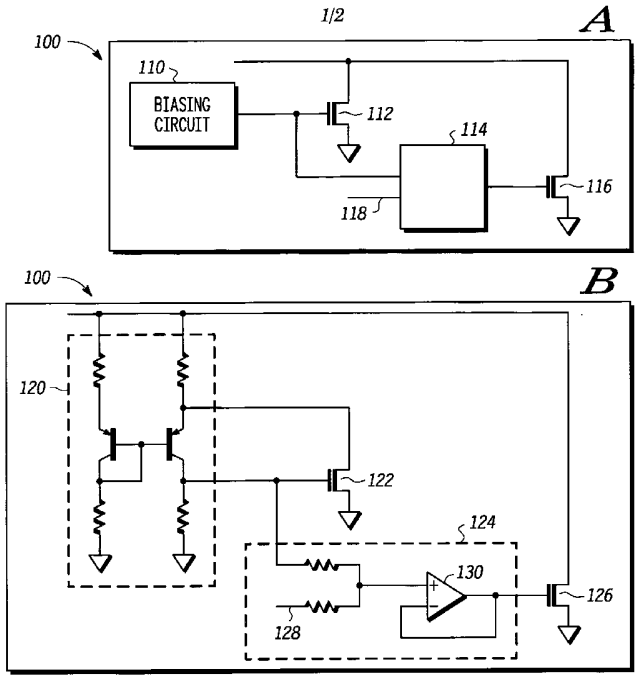
(54) Title: METHOD AND APPARATUS FOR DOHERTY AMPLIFIER BIASING




(57) Abstract: Apparatus and methods are described for biasing amplifiers with multiple outputs. A semiconductor die (100) may include a reference Field Effect Transistor (FET) (112) integrated on the semiconductor die and coupled to an amplifier (116) integrated on the semiconductor die. A voltage offset circuit (114) may also be integrated on the semiconductor die (100) for determining the voltage needed to operate the amplifier (116).

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# METHOD AND APPARATUS FOR DOHERTY AMPLIFIER BIASING

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The invention relates generally to the field of amplification circuits, more particularly, to automatic biasing of amplifiers.

### 2. Discussion of the Related Art

In a power amplifier, the direct current (DC), or quiescent current biasing point is a critical design parameter. The quiescent current has significant effects on the characteristics and performance, *e.g.*, linearity, signal distortion, power efficiency, *etc.*, of the amplifier. The optimal DC biasing point of a transistor in an amplifier depends on the application of the amplifier and the characteristics of the transistor, which are affected by environmental surroundings such as temperature variations, process variations, and the like.

An example of a power amplifier is the Doherty Amplifier. The Doherty topology has been used widely in sophisticated and high power application. Traditionally, a Doherty amplifier includes a plurality of peaking amplifiers in which each peaking amplifier requires a different bias level. However, the quiescent conditions of these peaking amplifiers are not easily measurable. Further, amplifier devices are known to have varying characteristics that make it difficult to preset all stages to a predetermined value.

Current methods for biasing these peaking amplifiers employ an off-chip bias that is factory set for each peaking amplifier. Similarly, for configurations such as radio-frequency integrated circuits (RFIC) in a Doherty amplifier configuration, two integrated circuits are needed to bias both the carrier amplifier devices and the peaking amplifier devices. In this

configuration, at least one of the integrated circuits is an off-chip, factory bias set. However, for amplifier architectures with multiple output stages, this method becomes inefficient and expensive.

The referenced shortcomings are not intended to be exhaustive, but rather are among many that tend to impair the effectiveness of previously known techniques concerning biasing for amplifier architecture; however, those mentioned here are sufficient to demonstrate that the methodologies appearing in the art have not been altogether satisfactory and that a significant need exists for the techniques described and claimed in this disclosure.

## BRIEF DESCRIPTION OF THE DRAWINGS

The drawings accompanying and forming part of this specification are included to depict certain aspects of the invention. The invention may be better understood by reference to one or more of these drawings in combination with the description presented herein. Identical or similar elements use the same element number. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale.

**FIG. 1A** is a block diagram of a die including a biasing circuit and a peaking amplifier, in accordance with an embodiment of the present invention.

**FIG. 1B** is a circuit diagram of an on-chip biasing circuit coupled to a peaking amplifier, in accordance with an embodiment of the present invention.

FIG. 2 is a circuit diagram of an on-chip biasing circuit for a RFIC amplifier, in accordance with an embodiment of the present invention.

**FIG. 3** is a graph showing the gain of Doherty amplifier relative to the input power, in accordance with an embodiment of the present invention.

**FIG. 4** is a graph showing the phase of a Doherty amplifier relative to the input power, in accordance with an embodiment of the present invention.

## DETAILED DESCRIPTION

Shortcomings of conventional biasing of amplifier architectures are addressed by the techniques of this disclosure. In particular, the techniques of this disclosure provide an on-chip, automatic biasing circuitry coupled to an amplifier. An amplifier architecture, having multi-parallel output stage amplifiers, using the techniques of this disclosure is more efficient, much more robust, and is cost-effective when compared to today's off-chip, factory biasing methods.

In general, the present invention provides an on-chip, automatic self-biasing scheme for power amplifiers. In one embodiment of the invention, a semiconductor die may include at least one amplifier, bias circuitry coupled to the at least one amplifier, voltage offset circuitry coupled to the bias circuitry, where the bias circuitry and voltage offset circuitry are adapted to bias the at least one amplifier.

In accordance to one embodiment of the invention, a method for biasing an amplifier includes providing a semiconductor having an amplifier, a bias circuit for tracking device parameters of the amplifier, and a voltage offset circuit, the voltage offset circuit for determining where the amplifier will operate and for calculating a biasing voltage for the amplifier based on the device parameters.

In accordance to another embodiment of the invention, a method includes providing a semiconductor die having a first and second amplifier, a biasing circuit for providing a reference voltage to the second amplifier, and a voltage offset circuit, the voltage offset circuit for providing a reference voltage to the first amplifier and for automatically biasing the first amplifier proportionally to the second amplifier.

These and other features and embodiments of the invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating various embodiments of the invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many substitutions, modifications, additions and/or rearrangements may be made within the scope of the invention without departing from the spirit thereof, and the invention includes all such substitutions, modifications, additions and/or rearrangements.

According to one embodiment of the present disclosure, a biasing circuit is provided to bias a peaking amplifier, where the biasing circuit is fabricated on the same die as the peaking amplifier, as illustrated in FIG. 1A. Die 100 may include a reference FET 112 coupled to a peaking amplifier transistor 116. During the operation of the amplifier on die 100, variations such as the die temperature may cause device characteristics of the peaking amplifier transistor 116 to vary. The reference FET 112, having been fabricated on the same

die as transistor 116, automatically tracks variations in device parameters such as the threshold voltage ($V_{th}$) or the transconductance ($g_m$) of the peaking amplifier transistor 116. Accordingly, in one embodiment of the present disclosure, biasing of the peaking amplifier transistor is based on the quiescent conditions of reference FET 112. Furthermore, the method includes dynamically adjusting the offset voltage circuitry 114 based on die temperature, process variations, or load conditions.

In particular, gate voltage of the peaking amplifier transistor 116 is set based on the gate voltage of the reference FET 112. Biasing circuit 110 is coupled to the gate terminal of the reference FET 112 such that the reference FET 112 is biased to a desired current density. For example, reference FET 112 operates in an ON mode in response to gate voltage $V_g$ greater than a threshold voltage $V_{th}$. The gate voltage of the reference FET 112 is also coupled to a voltage offset circuitry 114. The voltage offset circuitry 114 is adapted to determine the drive level at which the peaking amplifier transistor will be turned to an ON mode and operate in a Doherty mode. As such, the voltage offset circuitry 114 couples to the gate terminal of the peaking amplifier transistor 116. In one embodiment, the voltage offset circuitry 114 uses the gate voltage of the reference FET 112 minus an offset voltage 118 to determine the operation mode of the peaking amplifier transistor 116. The offset voltage 118 is set to a predetermined value corresponding to a gate voltage that would have the peaking amplifier transistor 116 operate in an ON mode at a predetermined input voltage drive level. Alternatively, the offset voltage 118 may also be adjusted to account for different operating conditions (for example, single carrier or multi-carrier applications).

As shown in FIG. 1A, biasing circuit 110, reference FET 112, voltage offset circuits 114, and peaking amplifier transistor 116 are all integrated on the same semiconductor die 100.

Different circuit implementation is adapted to provide an automatic, on-chip biasing of the peaking amplifier transistors. According to one embodiment of the invention, biasing circuit 120 may include, but is not limited to, a current mirror adapted to bias reference FET 122 to a particular current density, as illustrated in FIG. 1B. The gate voltage of reference FET 122 is used to determine the gate voltage of the peaking amplifier transistor 126. Accordingly, voltage offset circuitry 124 includes two parallel resistors coupled to a buffer to determine a gate voltage for the peaking amplifier transistor 126 using offset voltage 128 and $V_g$ of the reference FET 122. In one embodiment, a voltage divider is used to calculate and determine the gate voltage for the peaking amplifier transistor 126. Additionally, the voltage offset circuitry may include feedback amplifier 130 to select the gate voltage for the peaking amplifier transistor 126. In one embodiment, if the device parameters of the peaking amplifier transistor have changed, the gate voltage needed for the peaking amplifier transistor to operate in an ON mode may need to be changed. Accordingly, amplifier 126is provided with a bias voltage determined from the reference FET 122 and voltage offset circuitry 124. Similarly, if the peaking amplifier transistor 126 is operating in the correct mode, feedback amplifier 130 on die 100 continues to be provide the same gate voltage to peaking amplifier transistor 126, as illustrated by a feedback loop to the amplifier.

Once again, as shown in FIG. 1B, biasing circuit 120, reference FET 122, voltage offset circuitry 124, and peaking amplifier transistor 126 are all integrated on the same semiconductor die 100.

Additionally, other circuit components may be used to implement the on-chip, self-biasing of the peaking amplifier transistor. In one embodiment, the reference FET 112 includes a bias FET. In another embodiment, the reference FET 112 includes, but is not limited to, a carrier amplifier. The carrier amplifier may be part of an amplifier circuitry,

such as a multi-chip combined linear power amplifier (CLPA) multiple output amplifier.

## EXAMPLES

Specific embodiments of the invention will now be further described by the following, nonlimiting examples which will serve to illustrate in some detail various features. The following examples are included to facilitate an understanding of ways in which the invention may be practiced. It should be appreciated that the examples which follow represent embodiments discovered to function well in the practice of the invention, and thus can be considered to constitute preferred modes for the practice of the invention. However, it should be appreciated that many changes can be made in the exemplary embodiments which are disclosed while still obtaining like or similar result without departing from the spirit and scope of the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

### Example 1

FIG. 2 illustrates a portion of a Doherty amplifier configuration utilizing an RFIC. Particularly, die 200 includes a self-bias FET 202 integrated thereof, with inputs 204 and 205. Die 200 may also include a carrier amplifier transistor 206 with input circuit 212 that is matched to the input power source 210 and coupled to output 207. Further, die 200 may include a peaking amplifier transistor 208 with input circuit 216 that is matched to the input power source 214 and coupled to output 209. In one embodiment, outputs 207 and 209 couple to loads of the respective amplifiers 206 and 208, in which the loads are external to die 200. In an integrated amplifier configuration for Doherty amplifiers, the characteristics of the peaking amplifier transistor and the carrier amplifier transistor would typically be similar. As such, the bias for the peaking amplifier transistor 208 is proportional to the bias for the carrier amplifier transistor 206. The gate voltage of the self-bias FET 202 is coupled to the gate

terminal of the carrier amplifier transistor 206. To insure the bias for the peaking amplifier transistor 208 is proportional to the bias of the carrier amplifier transistor 206, the gate voltage to the carrier amplifier transistor is coupled to a resistor divider, the resistor divider network including resistors 218 and 220. The voltage from the network divider is provided to the gate terminal of peaking amplifier transistor 208.

As illustrated in FIG. 2, the self-bias FET 202, carrier amplifier transistor 206, peak amplifier 208, input circuits 212 and 216, and the resistor divider network including resistors 218 and 220 are all integrated on the same semiconductor die 200.

**Example 2**

FIG. 3 and FIG. 4 illustrate the results of automatic biasing of a peaking amplifier transistor in a Doherty amplifier configuration, in which a reference FET is on the same die with the amplifier. Particularly, FIG. 3 illustrates the gain (dB) of the Doherty amplifier relative to the input power (dBm) and a corresponding compensation for variations in device parameters during operation of the amplifier. The highest gain observed was for graph line 302 which at approximately 23 dBm, the gain was about 18.7 dB for a gate voltage of 2.5 Volts (V) for the peaking amplifier transistor. At a gate voltage of 2 V, the maximum gain was observed at an input power of about 24 dBm, illustrated by graph line 306. For a gate input voltage of 2.3 V, the maximum gain of the peaking amplifier transistor was observed at an input power of 22 dBm, as illustrated by graph line 304.

Similarly, FIG. 4 illustrates the phases (in degrees) of the Doherty amplifier relative to the input power and a corresponding compensation for variations in device parameters during operation of the amplifier. Graph line 402 refers to a gate voltage of 2.5 V applied to the gate

terminal of a peaking amplifier transistor. Graph line 406 refers to a gate voltage of 2 V and graph line 404 refers to a gate voltage of 2.3 V applied to the gate terminal of a peaking amplifier transistor.

All the disclosed embodiments of the invention disclosed herein can be made and used without undue experimentation in light of the disclosure. It will be manifest that various substitutions, modifications, additions and/or rearrangements of the features of the invention may be made without deviating from the spirit and/or scope of the underlying inventive concept. It is deemed that the spirit and/or scope of the underlying inventive concept as defined by the appended claims and their equivalents cover all such substitutions, modifications, additions and/or rearrangements.

## CLAIMS

What is claimed is:

1. An amplifier circuit, comprising:

a semiconductor die (100);

a Doherty amplifier integrated on the semiconductor die, the Doherty amplifier including a peaking amplifier (116) and a carrier amplifier (112) coupled to the peaking amplifier;

a bias circuit (110) integrated on the semiconductor die and coupled to the Doherty amplifier; and

a voltage offset circuit (114) integrated on the semiconductor die and coupled to the bias circuit and to the Doherty amplifier, the voltage offset circuit and the bias circuit together biasing the Doherty amplifier.

2. The amplifier circuit of claim 1, the bias circuit (110) comprising a Field Effect Transistor.

3. The amplifier circuit of claim 1, the voltage offset circuit (114) determining a drive level at which the peaking amplifier is turned to an ON mode.

4. The amplifier circuit of claim 1, further comprising a resistor divider network (218, 220) integrated on the semiconductor die (200) and coupled to the carrier amplifier (206), the resistor divider network biasing the peaking amplifier (208).

5. An amplifier circuit, comprising:

a semiconductor die (200);

at least one amplifier (202, 206, 208) integrated on the semiconductor die;

a bias circuit (212) integrated on the semiconductor die and coupled to the at least one amplifier; and

a voltage offset circuit (216) integrated on the semiconductor die and coupled to the bias circuit and to the at least one amplifier, the voltage offset circuit and the bias circuit together biasing the at least one amplifier.

6. The amplifier circuit of claim 5, the at least one amplifier comprising a peaking amplifier (208).

7. The amplifier circuit of claim 6, the at least one amplifier comprising a carrier amplifier (206) coupled to the peaking amplifier (208).

8. The amplifier circuit of claim 5, the bias circuit (212) comprising a Field Effect Transistor.

9. The amplifier circuit of claim 5, the voltage offset circuit (216) determining a drive level at which the at least one amplifier is turned to an ON mode.

10. The amplifier circuit of claim 9, the ON mode comprises operating in a Doherty amplifier configuration.

11. The amplifier circuit of claim 5, the at least one amplifier comprising a peaking amplifier (208) coupled to a carrier amplifier (206) via the voltage offset circuit (216).

12. The amplifier circuit of claim 11, the bias circuit (212) being coupled to the carrier amplifier (206).

13. The amplifier circuit of claim 11, further comprising a resistor divide network (218, 220) integrated on the semiconductor die and coupled to the carrier amplifier (206), the resistor divider network for biasing the peaking amplifier (208).

14. The amplifier circuit of claim 5, the at least one amplifier comprising a Doherty amplifier.

15. A method, comprising:

providing a semiconductor die (100) having an amplifier (116) integrated on the semiconductor die, a bias circuit (110) integrated on the semiconductor die, and a voltage offset circuit (114) integrated on the semiconductor die;

operating the bias circuit to track device parameters of the amplifier; and

operating the bias circuit and the voltage offset circuit to bias the amplifier based on tracked changes to the device parameters of the amplifier.

16. The method of claim 15, the amplifier (116) comprising a peak amplifier.

17. The method of claim 15, the amplifier comprising a carrier amplifier (112).

18. The method of claim 15, the bias circuit comprising a Field Effect Transistor.

19. The method of claim 15, the step of tracking device parameters comprising tracking a threshold voltage and transconductance of the amplifier.

20. The method of claim 15, further comprising setting the voltage offset circuitry to a fixed voltage.

21. The method of claim 15, further comprising dynamically adjusting the offset voltage circuitry based on die temperature, process variations, or on load conditions on the at least one amplifier.

22. A method, comprising:

providing a semiconductor die (100) having a first and second amplifier integrated on the semiconductor die, a bias circuit (120) integrated on the semiconductor die, and a voltage offset circuit (124) integrated on the semiconductor die;

operating the bias circuit (120) to provide a reference voltage to the second amplifier (122); and

operating the voltage offset circuit (124) to automatically bias the first amplifier (126) proportional to the reference voltage of the second amplifier (122).

23. The method of claim 22, the first amplifier (126) comprising a peaking amplifier and the second amplifier (122) comprising a carrier amplifier.

24. The method of claim 22, the voltage offset circuit (124) comprising a resistor divider network.

FIG. 1A

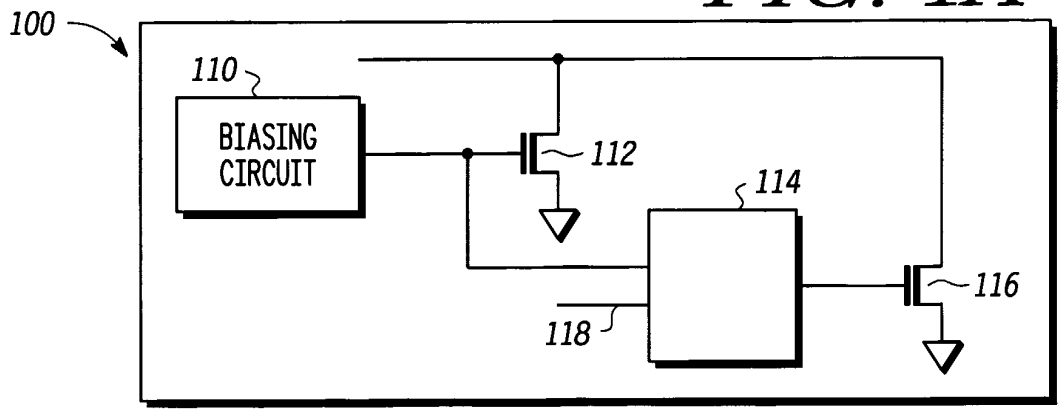



FIG. 1B

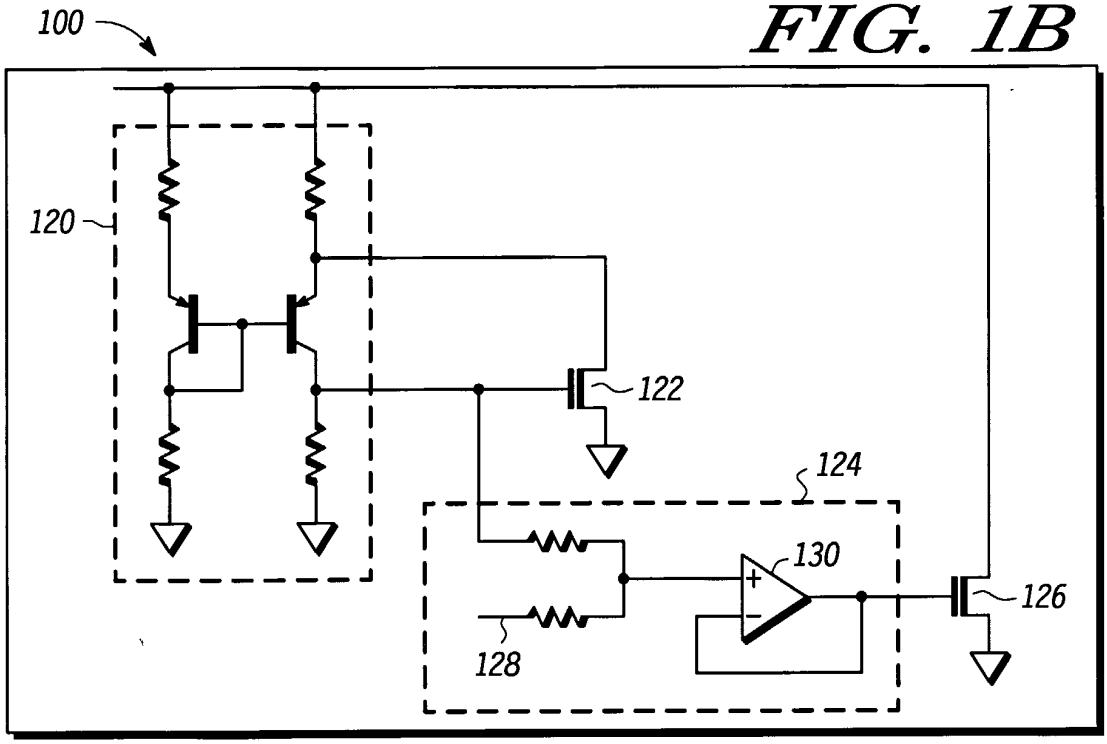
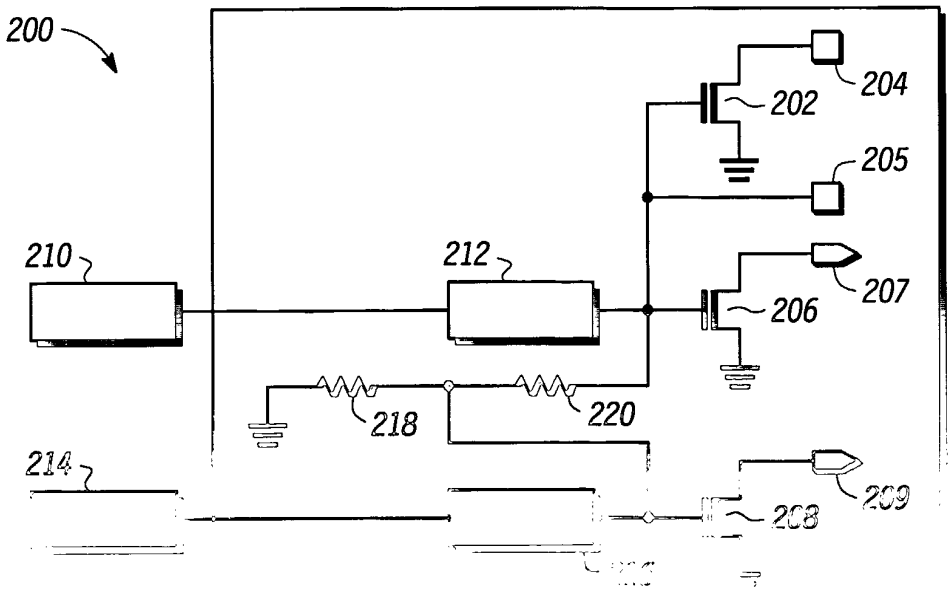



FIG. 2



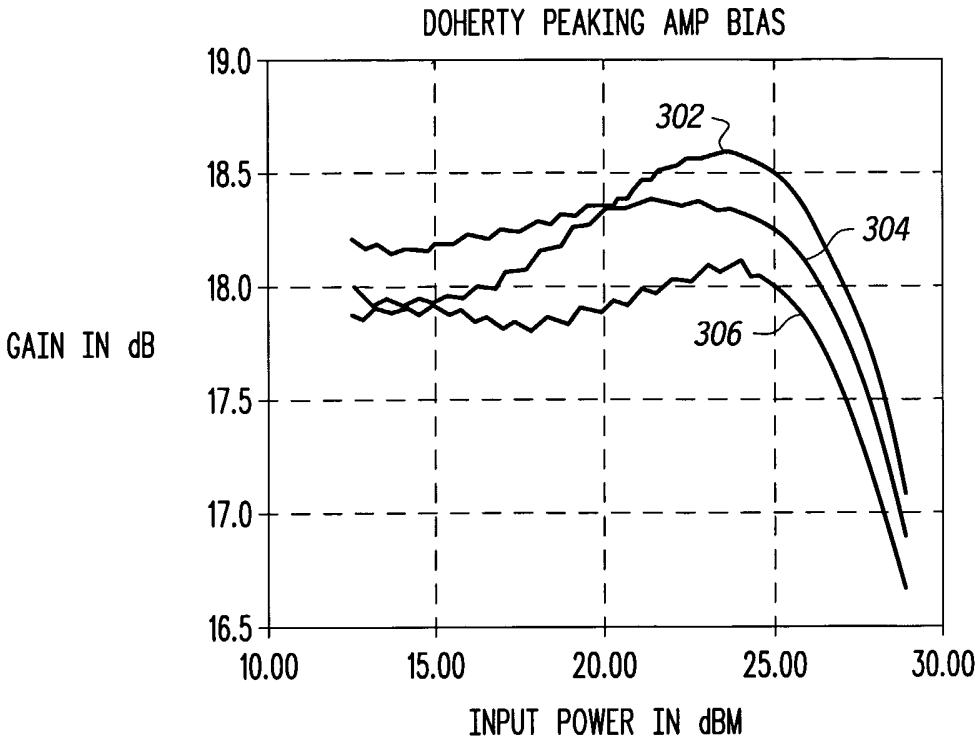

DOHERTY PEAKING AMP BIAS
GAIN IN dB
19.0
18.5
18.0
17.5
17.0
16.5
10.00
15.00
20.00
25.00
30.00
INPUT POWER IN dBM
302
304
306

FIG. 3

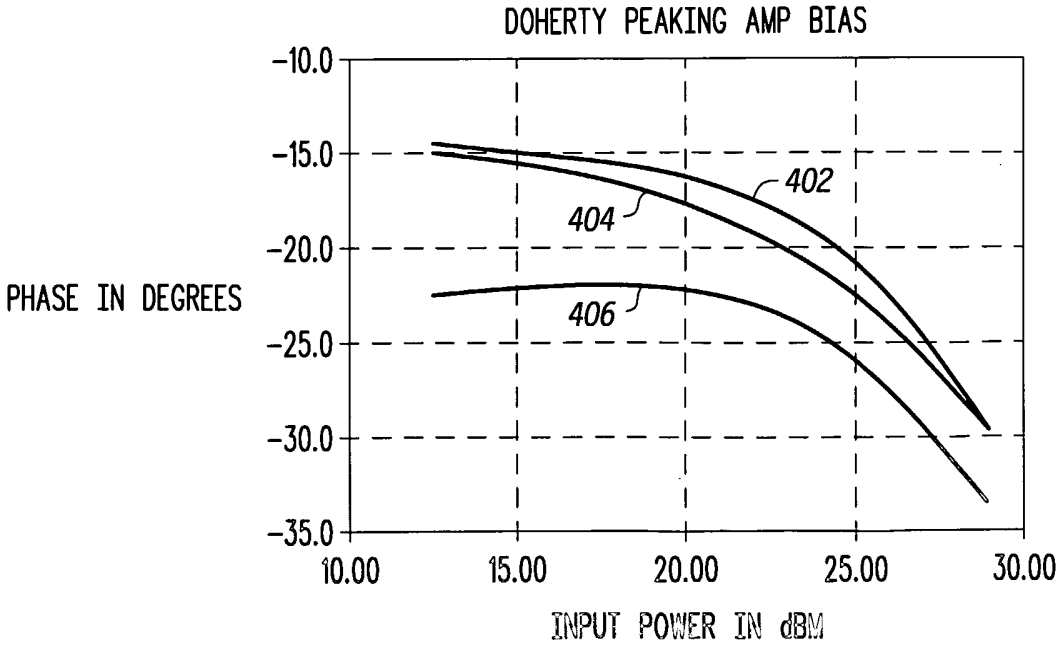

DOHERTY PEAKING AMP BIAS
PHASE IN DEGREES
-10.0
-15.0
-20.0
-25.0
-30.0
-35.0
10.00
15.00
20.00
25.00
30.00
INPUT POWER IN dBM
402
404
406

FIG. 4

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/02494

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H03F 3/04
US CL : 330/307,296
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 330/307,296 330/9/124R,295,84

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X,P | US 6,731,173 B1 (Thompson) 04 May 2004, see entire document. | 1-24 |
| A | US 6,262,629 B1 (Stengel et al.) 17 July 2001. | 1-24 |
| A | US 5,757,229 A (Mitzlaff) 26 May 1998. | 1-24 |
| A | US 4,074,181 A (Crowle) 14 February 1978. | 1-24 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 22 July 2005 (22.07.2005) | 10 AUG 2005 |
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# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/02494

Continuation of B. FIELDS SEARCHED Item 3:
IEEE XPLORE
amplifier, biasing, bias, offset, integrated