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(54) **COMMON BALL-LIMITING METALLURGY FOR I/O SITES**

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Publication Classification

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(52) **U.S. Cl.** **438/613**

(57) **ABSTRACT**

A process is described for forming a common input-output (I/O) site that is suitable for both wire-bond and solder bump flip chip connections, such as controlled-collapse chip connections (C4). The present invention is particularly suited to semiconductor chips that use copper as the interconnection material, in which the soft dielectrics used in manufacturing such chips are susceptible to damage due to bonding forces. The present invention reduces the risk of damage by providing site having a noble metal on the top surface of the pad, while providing a diffusion barrier to maintain the high conductivity of the metal interconnects. Process steps for forming an I/O site within a substrate are reduced by providing a method for selectively depositing metal layers in a feature formed in the substrate. Since the I/O sites of the present invention may be used for either wire-bond or solder bump connections, this provides increased flexibility for chip interconnection options, while also reducing process costs.

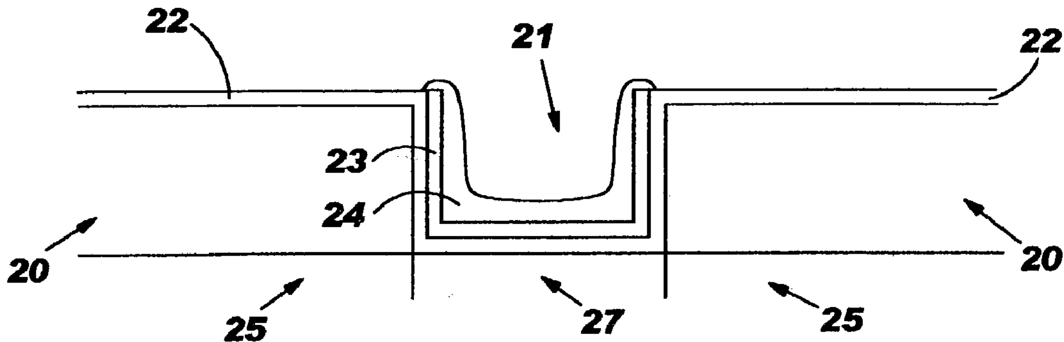


FIG. 1A
(PRIOR ART)

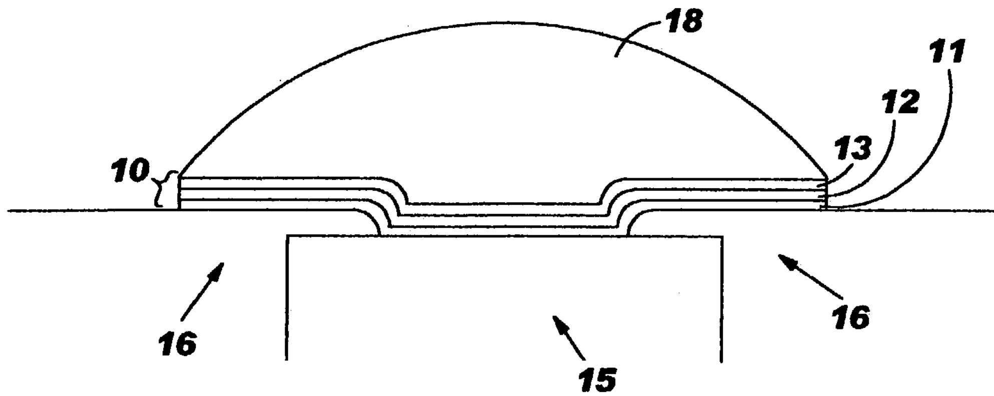


FIG. 1B
(PRIOR ART)

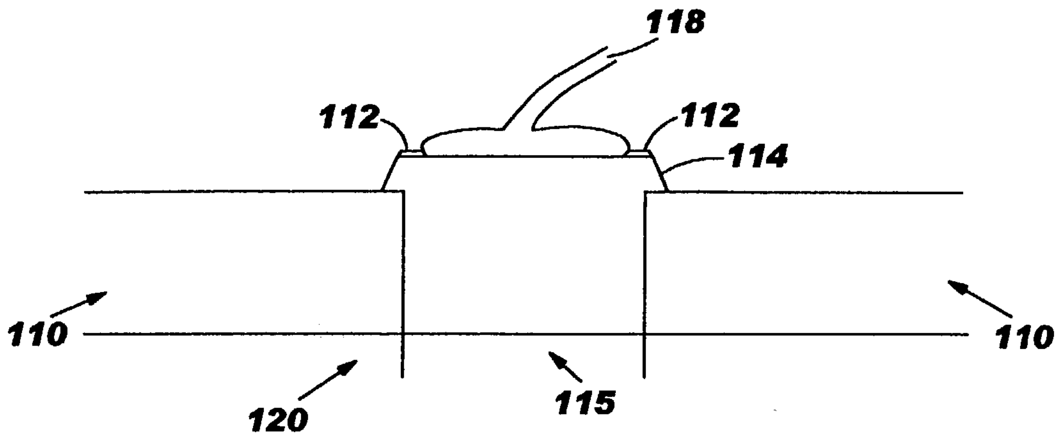


FIG. 2A

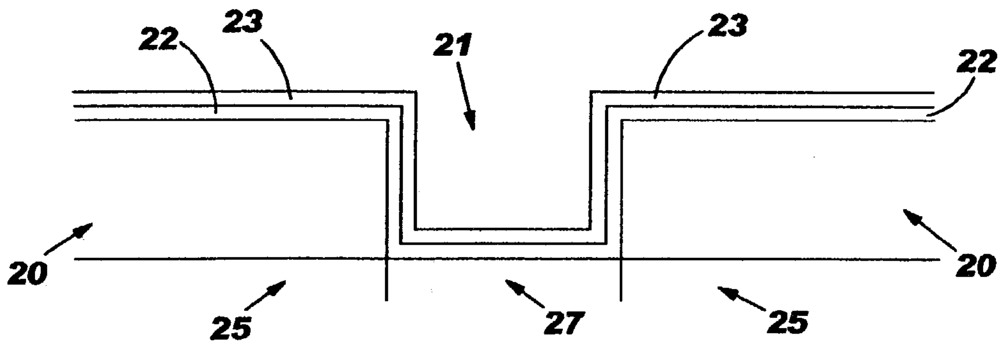


FIG. 2B

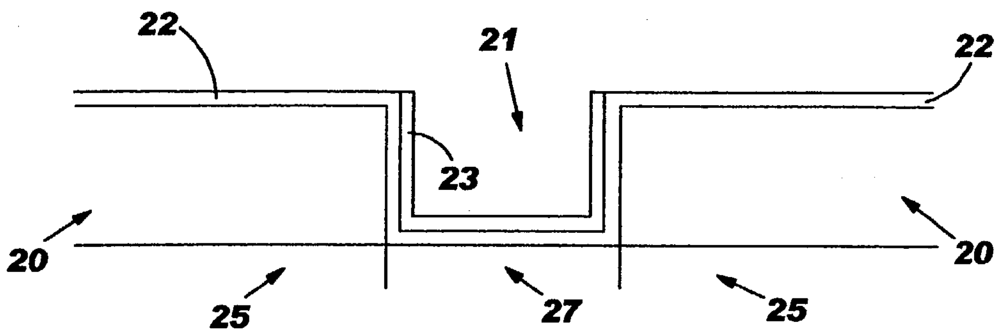


FIG. 2C

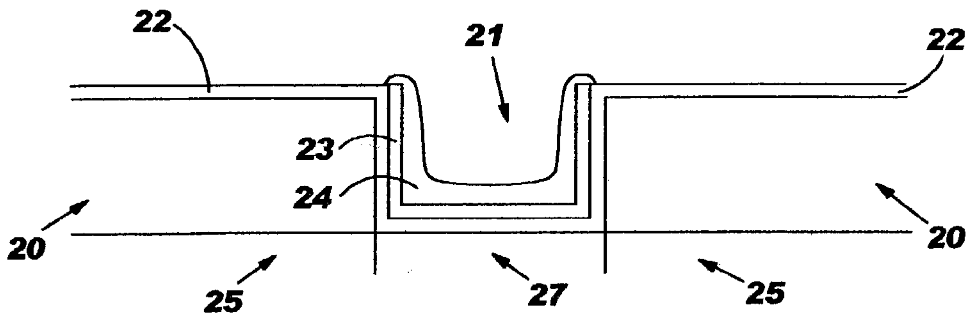


FIG. 2D

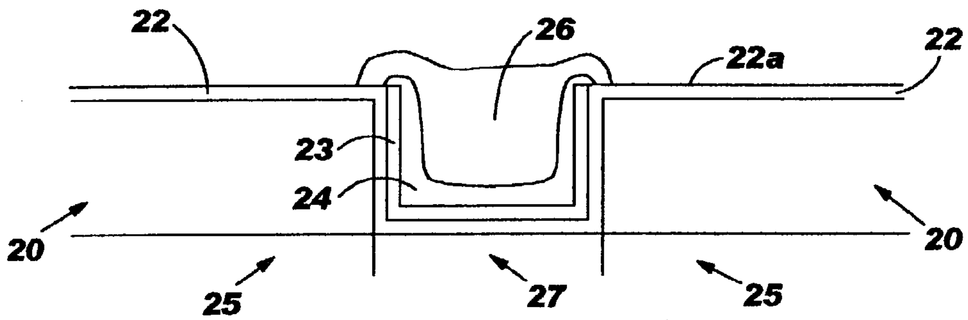


FIG. 3A

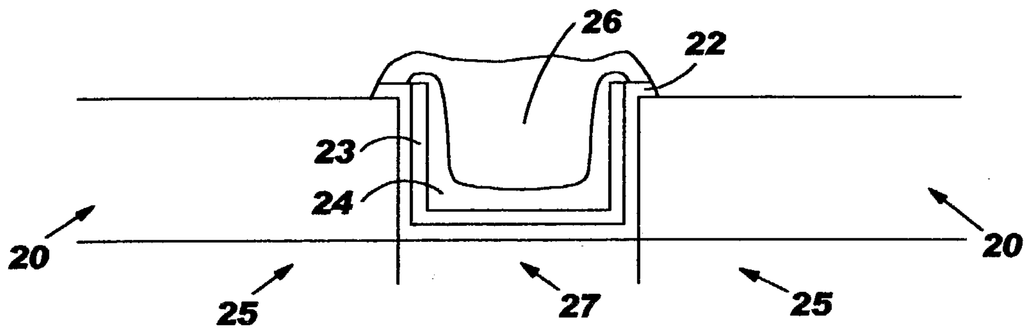


FIG. 3B

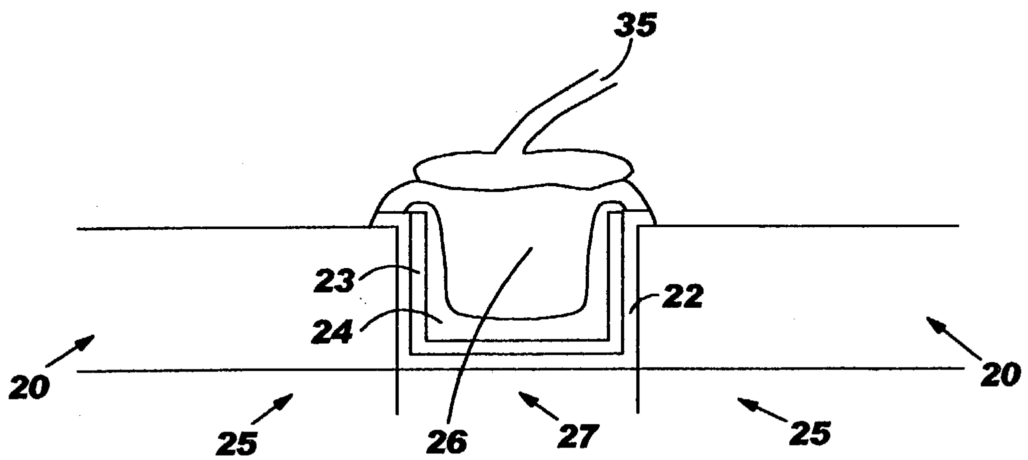


FIG. 4A

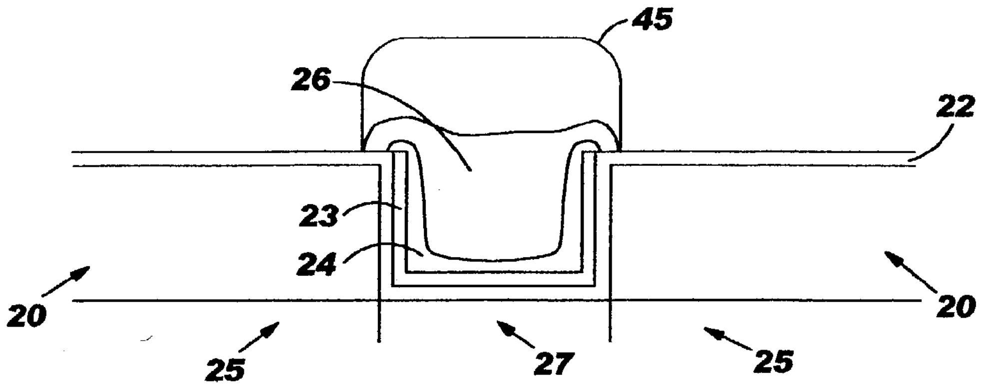


FIG. 4B

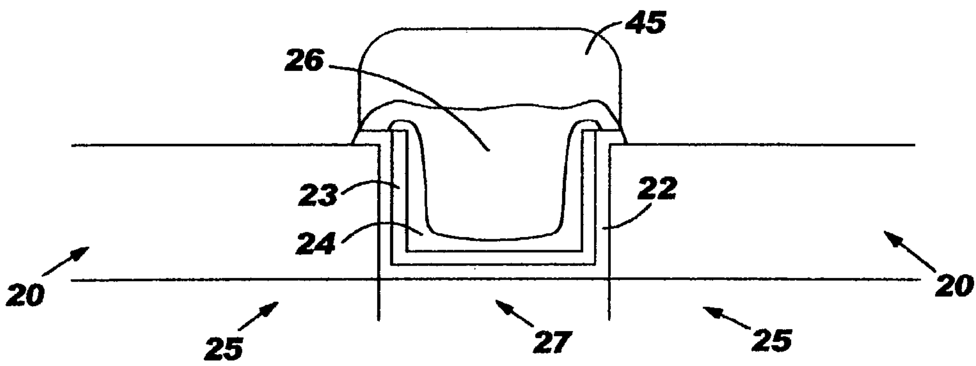


FIG. 4C

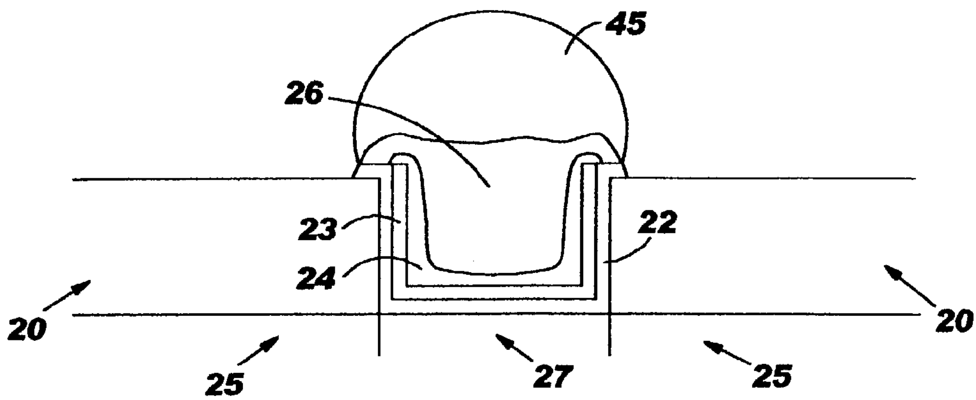


FIG. 5A

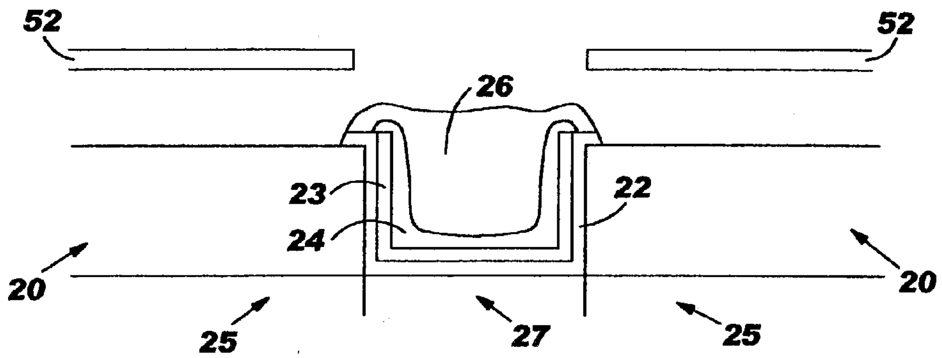


FIG. 5B

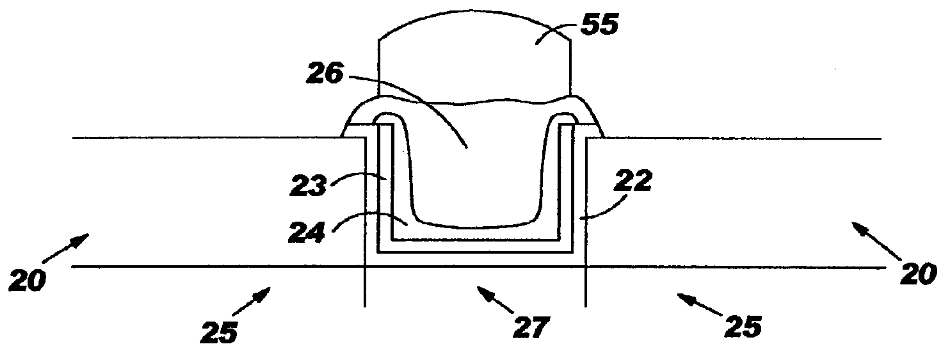
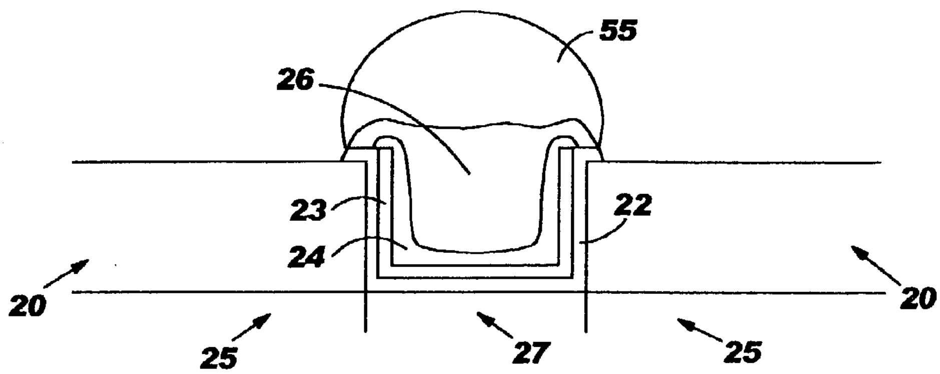


FIG. 5C



COMMON BALL-LIMITING METALLURGY FOR I/O SITES

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor processing, and more particularly to a process for fabricating a common ball-limiting metallurgy for input/output (I/O) sites used in packaging integrated circuit (IC) chips.

BACKGROUND OF THE INVENTION

[0002] In the fabrication of semiconductor devices, metal lines are often embedded in dielectric layers in a multilevel structure, particularly in the latter stage ("back end of the line" or "BEOL") of the fabrication process. The final layer containing metal lines (sometimes referred to in the art as the terminal via or TV layer) will have metal pads fabricated in contact with the metal lines, in a process sometimes referred to as "far back end of the line", or "far BEOL". The pads and lines together provide interconnects from the chip to other system components. The majority of IC chips use aluminum (Al) to form the interconnects, but more recently copper (Cu) is used.

[0003] Some advantages of using Cu rather than Al to form interconnects include higher conductivity (with lower resistance), lower capacitive load, lower power consumption, less crosstalk, fewer metal layers and fewer potential manufacturing steps. However, the disadvantages of using Cu include increased difficulty of depositing thin layers of Cu, potential for contamination of the Cu by underlying silicon thereby lowering performance, migration of Cu between lines, thereby increasing the risk of electrical shorts, and a mismatch in thermal expansion between the substrate and the Cu pads and lines. In order to take full advantage of Cu interconnects, methods of forming Cu interconnects must attempt to overcome these disadvantages of using copper.

[0004] Depending on the application, a variety of techniques are used to provide connections between a chip and other components, such as another level of interconnect. Common connections include wire bond and solder bumps.

[0005] Wire bonding is well-known in the art and used in the majority of IC chips, but disadvantages include a limited density of interconnect sites and, particularly during chip functional testing, there is the possibility of mechanical damage to the chip at the site of the bond. A typical example of a wire bond is illustrated in **FIG. 1B**. In this prior art example, a substrate **120** has a metal line **115** embedded. The metal line could be aluminum or copper. A metal pad **114**, often composed of aluminum (Al) is formed over the metal line **115**, supported by a dielectric **110**. Typically, the aluminum pad will have an oxide layer **112** which forms readily over the surface because of the reactivity of aluminum. A wire **118**, often gold (Au), will be bonded to the pad using techniques known in the art, such as thermosonic bonding. One problem in forming wire bonds between gold and aluminum is that gold forms intermetallics with aluminum that can reduce the reliability of the bond.

[0006] Another problem with current integrated circuits, particularly those using Cu metallization, is that the low-k dielectrics employed are soft and sensitive to damage by pressure. Circuit testing is performed by pushing a set of test probes against critical conductive points on the top layer. The surface oxide must be broken through (often by a technique known as "scrubbing") in order to form a good contact between the test probe and the pad metal. Therefore, particularly in the case of soft low-k dielectrics, the chip is subjected to potential mechanical damage. It would therefore be desirable to form an I/O pad that does not require scrubbing to provide low contact resistance with test probes.

[0007] Solder bump technology (known as flip chip technology in the art) potentially provides higher density and higher performance, but suffers from greater difficulty compared to wire bonding for rework and testing. An example of solder bump technology is controlled-collapse chip connection (C4) in which solder bumps are provided on both the chip and the interconnection substrate, and the connection is made by aligning the solder bumps of the chip and substrate and reflowing the solder to make the connections. The solder bumps are formed by depositing solder on a ball-limiting metallurgy (BLM) as illustrated in **FIG. 1A**. A metal feature **15**, which could be aluminum or copper, is formed in a substrate **16**. To prevent the solder from diffusing into the metal feature **15**, a multi-layer film of metal **10** is formed as a cap over the metal feature, and then the solder is formed onto the top of the multilayer cap **10** which may initially extend beyond the cap onto the oxide surface. The ball-limiting metallurgy **10** is formed using multiple layers of metals, such as layer **11** including chromium, layer **12** including copper, and layer **13** including gold. The solder ball **18** is formed by initially depositing solder (a typical solder is 95% lead and 5% tin), using a process such as evaporation through a mask, which overlays the pad and a portion of the surface of the substrate **16**. The solder used for attaching flip chips to interconnection substrates has a relatively high melting point so that when the module containing the flip chip is assembled in subsequent packaging, other lower-melting point solders may be flowed without remelting of the flip chip solder connections. The ball **18** is then formed by heating the solder, which reflows into a ball, limited by the dimension of the BLM because of surface tension.

[0008] In view of the foregoing discussion, there is a need to provide an I/O site that can take advantage of copper metallization without degrading performance, reduce process steps and increase flexibility in preparing I/O sites.

SUMMARY OF THE INVENTION

[0009] The present invention addresses the above-described need by providing a process for fabricating a ball-limiting metallurgy (BLM) that can be used as a common site for both wire bond and controlled-collapse chip connection (C4) wafers.

[0010] This invention solves the problem of contamination of the metal lines by providing a diffusion barrier layer between the line and the I/O pad, and by providing a first recessed layer of metal within a feature formed in within a substrate upon which the I/O site of the present invention is formed.

[0011] This invention also solves the problem of damage to the chip caused by the forces of probing and/or wire bonding by providing a top layer of noble metal on the I/O site, which eliminates the presence of an oxide layer and

requires less bonding force, and, in the case of gold wire bonding, no intermetallics are formed.

[0012] This invention has the advantage of reducing the number of process steps used to form an I/O site, and provides a flexible site that can be a common site for either a wire bond or a BLM, thereby reducing overall processing costs.

[0013] In accordance with one aspect of the invention, an input-output structure in a feature formed in a substrate, the substrate having a top surface, the feature having feature sidewalls and a feature bottom, the feature bottom formed over an electrically conductive material, the structure comprising:

[0014] a barrier layer covering the feature sidewalls and feature bottom, the barrier layer having a barrier bottom and barrier sidewalls;

[0015] a seed layer of metal having a seed bottom and seed sidewalls covering at least said barrier bottom; and

[0016] a first metal layer covering at least said seed bottom and having a recess formed therein, so that a top surface of said first metal layer is lower than the top surface of the substrate; and

[0017] a second metal layer covering said first metal layer.

[0018] In accordance with another aspect of the present invention, an input-output site is formed in a feature in a substrate, the substrate having a top surface, the feature having feature sidewalls and a feature bottom, the feature bottom formed over an electrically conductive material, the method comprising the steps of:

[0019] depositing a barrier layer covering the top surface of the substrate, the feature sidewalls and the feature bottom, so that the barrier layer has a barrier bottom and barrier sidewalls;

[0020] depositing a seed layer of metal covering the surface of said barrier layer;

[0021] selectively removing said seed layer from at least the top surface so that the seed layer is reduced to a portion of the seed layer on at least said barrier bottom;

[0022] electroplating a first metal layer using said portion of said seed layer, so that said first metal layer has a recess formed therein and so that a top surface of said first metal layer is lower than the top surface of the substrate; and

[0023] electroplating a second metal layer, so that said second metal layer covers said first metal layer.

[0024] The novel features believed to be characteristic of this invention are set forth in the appended claims. The invention itself, however, as well as other objects and advantages thereof, may be best understood by reference to the following detailed description of an illustrated preferred embodiment to be read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] **FIG. 1A** illustrates a prior art BLM for a C4 site.

[0026] **FIG. 1B** illustrates a prior art wire bond site.

[0027] **FIG. 2A** illustrates the starting structure for the present invention at the last level build prior to packaging, showing the top level conductive layer overlain by a dielectric substrate having a bucket feature, a barrier layer, and a seed layer.

[0028] **FIG. 2B** illustrates the structure following removal of the seed layer from the top surface of the structure shown **FIG. 2A**, leaving a portion of the seed layer within the bucket feature.

[0029] **FIG. 2C** illustrates the structure following electroplating of a first metal layer onto the structure of **FIG. 2B**.

[0030] **FIG. 2D** illustrates the structure following electroplating of a second metal layer onto the structure of **FIG. 2C**.

[0031] **FIG. 3A** illustrates the structure following selective removal of the barrier layer from **FIG. 2D** to form a wirebond site.

[0032] **FIG. 3B** illustrates the structure after bonding of a wire to the wirebond site of **FIG. 3A**.

[0033] **FIG. 4A** illustrates the structure following the step of plating solder upon the structure of **FIG. 2D**.

[0034] **FIG. 4B** illustrates the structure following selective removal of the barrier layer from the structure of **FIG. 4A**.

[0035] **FIG. 4C** illustrates the C4 structure following reflow of the plated solder in **FIG. 4B**.

[0036] **FIG. 5A** illustrates the step of evaporating solder using a mask onto the structure of **FIG. 3A**.

[0037] **FIG. 5B** illustrates the structure following evaporation of solder as illustrated in **FIG. 5A**.

[0038] **FIG. 5C** illustrates the C4 structure following reflow of the evaporated solder from **FIG. 5B**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0039] In the following descriptions of the preferred embodiments of the invention, steps in the formation of the last level build to form a common ball-limiting metallurgy (BLM) structure prior to packaging will be detailed. It will be appreciated that this is intended as an example only, and that the invention may be practiced with a variety of substrates and metals.

[0040] As shown in **FIG. 2A, a** dielectric layer **20** has a feature **21** formed therein, at the desired location of a metal pad. The dielectric layer **20** is comprised of at least one dielectric material, but is preferably comprised of a stack of dielectric layers such as silicon nitride (SiNx) and silicon dioxide (SiO2). The feature **21** is formed over a conductive feature **27**, typically a metal such as aluminum (Al) or copper (Cu), formed in a dielectric substrate **25**. In the case of conductive feature **27** formed using Cu, the substrate **25** is preferably a low-k dielectric. A layer **22** of liner material may be deposited on the entire surface of the substrate **20**, including the sidewalls and bottom of feature **21**. The liner **22** serves as a diffusion barrier and an adhesion promoter. In addition, the liner **22** in accordance with the present invention is electrically conductive. In the case where Cu is to be plated, this liner material is preferably a combination of

tantalum (Ta) and tantalum nitride (TaN), preferably with TaN in contact with the dielectric layer **20** and the top surface of the conductive feature **27**. A seed layer **23** of metal is deposited over the surface of the liner/barrier layer **22**, using deposition methods known in the art, such as by chemical vapor deposition (CVD), or preferably by physical vapor deposition (PVD). The seed layer **23** is typically thin, for example, on the order of about 1000 Å. The seed layer is preferably Cu, which has good adhesion to TaN/Ta.

[**0041**] The seed layer **23** is then selectively removed from at least the top surface of the liner **22**, preferably using chemical-mechanical polishing (CMP), leaving a portion of the seed layer **23** on at least the bottom of the feature **21** and typically also remaining on the sidewalls of feature **21**, resulting in the structure shown in **FIG. 2B**. Although the resulting seed layer **23** shown in **FIG. 2B** is flush with the top surface of the barrier layer **22**, seed layer **23** could be partially removed from the sidewalls of the feature **21**.

[**0042**] A first electroplated layer **24** is formed using the seed layer **23** and applying a current to the barrier layer **22**, resulting in the structure illustrated in **FIG. 2C**. Before layer **24** is formed, the surface of the seed layer **23** must be clean. This can be accomplished by cleaning methods such as brush cleaning, wet cleaning, or wet cleaning with ultrasonics as known in the art. Suitable materials for the first electroplated layer **24** include platinum (Pt), gold (Au), copper (Cu), silver (Ag), solder, or nickel (Ni). In the case where the conductive feature **27** is Cu, the material selected to electroplate layer **24** is preferably selected to act as an additional diffusion barrier, for example Ni. During plating, layer **24** will nucleate only on the seed layer **23** and will not plate on the barrier layer **22**.

[**0043**] A second electroplated layer **26** is formed over the first electroplated layer **24**, which will serve as the pad for the common I/O site. Layer **26** is preferably a noble metal, such as Au. Once again, current is applied to the conductive barrier layer **22** during the electroplating process, which is preferably performed while the Ni layer **24** is still wet after the Ni bath has been rinsed. The thickness of layer **26** can be varied according to the desired application, and may extend above the top surface **22***a* as shown in **FIG.** 2D, but could be formed to be flush with or recessed below the top surface **22***a*. Layer **24**, preferably Ni, acts as a barrier layer between the seed layer **23**, which is preferably Cu, and layer **26**, which is preferably Au. The structure illustrated in **FIG. 2D** in accordance with the present invention is suitable for use as a common I/O site, for example, for either wirebond or C4 sites, which results in cost savings and flexibility. Examples of embodiments of the present invention for wirebond and C4 sites are described below.

[**0044**] First Embodiment: Wirebond Pad

[**0045**] An embodiment of the present invention for use as a wirebond I/O site may be formed starting with the structure in **FIG. 2D**. The barrier layer **22** is selectively removed from portions of the top surface not covered by plated layer **26**, which is preferably Au. This can be performed by a selective polishing method as known in the art, or by a wet etch, such as HF/Nitric acid.

[**0046**] Following the selective removal of the barrier layer **22**, an optional scratch protection layer (not shown) may be deposited over the entire surface. A typical scratch protection layer known in the art is polyimide.

[**0047**] A wire **35**, preferably Au, may now be bonded to the pad layer **26** as shown in **FIG. 3B**. The wire **35**, which is also preferably Au, is bonded to the pad **26** using standard techniques known in the art, such as thermosonic bonding, ultrasonic bonding, or thermocompression bonding. The pad layer **26** formed in accordance with the present invention has the advantage over prior art in that lower force is required to provide a bond, since both the wire **35** and the pad **26** may be Au. During the testing of integrated circuits, prior art aluminum pads require a sufficiently large surface so that a test probe can scrub the surface of the pad in order to break through the aluminum oxide layer that normally forms on the surface of the aluminum. Unlike prior art aluminum pads, the pad **26** formed from Au in accordance with the present invention will have a surface that is free of oxide because gold is a noble metal. Because scrubbing during testing is not required, the wirebond pad **26** formed in accordance with the present invention can be smaller than prior art pads, which can result in an increased density of I/O sites.

[**0048**] Second Embodiment: C4 Site with Plated Solder

[**0049**] The structure of **FIG. 2D** can also be used as the starting structure for an embodiment of the present invention for use as a C4 site in which the solder bump is formed by plating.

[**0050**] In this embodiment, a third layer **45** is electroplated onto layer **26** by applying current to the conductive barrier layer **22** as shown in **FIG. 4A**. Again, the barrier layer **22** is preferably a combination of Ta and TaN. The material used to form layer **45** is a solder, preferably 97% lead (Pb) and 3% tin (Sn), but many other suitable varieties of solder may be used as known in the art.

[**0051**] Next, the conductive barrier layer **22** is selectively removed, preferably by a wet etch technique as known in the art, leaving the solder layer **45** as shown in **FIG. 4B**.

[**0052**] Finally, the solder is re-flowed to form the C4 solder bump **45** as shown in **FIG.** 4C, using standard techniques as known in the art.

[**0053**] Third Embodiment: C4 Site with Evaporated Solder

[**0054**] As an alternative embodiment of the present invention, a C4 solder bump may be formed starting with the structure of **FIG. 3A** in which the barrier layer **22** of **FIG. 2D** has been selectively removed. A mask **52** is held in a fixture over the surface of the substrate as shown in **FIG. 5A**. The mask material is any suitable material known in the art used for evaporation of solder, and is preferably molybdenum (Mo). The evaporation of a solder is well-known in the art, and any suitable solder may be used, but is preferably a mixture of 97% Pb and 3% Sn.

[**0055**] After evaporation, the mask **52** is removed, leaving evaporated layers **55** of Pb and Sn on the pad layer **26** as shown in **FIG. 5B**.

[**0056**] Next, the solder is reflowed to form the C4 solder bump **55** shown in **FIG. 5C**.

[**0057**] In summary, the common BLM structures formed in accordance with the present invention allows the use of noble metals to form I/O pads that reduce costs by simplifying process steps and also allow an increase in I/O site density due to smaller pad sizes.

[**0058**] While the invention has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and variations will be apparent to those skilled in the art.

Accordingly, the invention is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the invention and the following claims.

We claim:

1. An input-output structure in a feature formed in a substrate, the substrate having a top surface, the feature having feature sidewalls and a feature bottom, the feature bottom formed over an electrically conductive material, the structure comprising:

a barrier layer covering the feature sidewalls and feature bottom, the barrier layer having a barrier bottom and barrier sidewalls;

a seed layer of metal having a seed bottom and seed sidewalls covering at least said barrier bottom; and

a first metal layer covering at least said seed bottom and having a recess formed therein, so that a top surface of said first metal layer is lower than the top surface of the substrate; and

a second metal layer covering said first metal layer.

2. The input-output structure of claim 1 wherein said second metal layer comprises a noble metal.

3. The input-output structure of claim 2 wherein the noble metal is selected from the group consisting of gold, platinum, and palladium.

4. The input-output structure of claim 1 wherein said second metal layer comprises gold.

5. The input-output structure of claim 1 wherein said seed layer comprises copper.

6. The input-output structure of claim 1 wherein said first metal layer comprises an electroplatable material.

7. The input-output structure of claim 6 wherein the electroplatable material is selected from the group consisting of copper, platinum, nickel, gold, silver, and solder.

8. The input-output structure of claim 1 wherein said first metal layer comprises nickel.

9. The input-output structure of claim 1 wherein said barrier layer comprises tantalum and tantalum nitride.

10. The input-output structure of claim 9 wherein the tantalum nitride is in contact with the substrate.

11. The input-output structure of claim 1 further comprising a wire bonded to said second metal layer.

12. The input-output structure of claim 11 wherein said wire and said second metal layer comprise gold.

13. The input-output structure of claim 1 further comprising a solder ball connected to said second metal layer.

14. A method of forming a ball-limiting metallurgy structure for an input-output site in a feature formed in a substrate, the substrate having a top surface, the feature having feature sidewalls and a feature bottom, the feature bottom formed over an electrically conductive material, the method comprising the steps of:

depositing a barrier layer covering the top surface of the substrate, the feature sidewalls and the feature bottom, so that the barrier layer has a barrier bottom and barrier sidewalls;

depositing a seed layer of metal covering the surface of said barrier layer;

selectively removing said seed layer from at least the top surface so that the seed layer is reduced to a portion of the seed layer on at least said barrier bottom;

electroplating a first metal layer using said portion of said seed layer, so that said first metal layer has a recess formed therein and so that a top surface of said first metal layer is lower than the top surface of the substrate; and

electroplating a second metal layer, so that said second metal layer covers said first metal layer.

15. The method of claim 14 wherein the step of depositing a seed layer comprises physical vapor deposition or chemical vapor deposition.

16. The method of claim 14 wherein the step of depositing a seed layer comprises chemical vapor deposition.

17. The method of claim 14 wherein the step of selectively removing said seed layer comprises chemical-mechanical polishing (CMP).

18. The method of claim 14 wherein the steps of electroplating said first metal layer and said second metal layer includes applying a current to said barrier layer.

19. The method of claim 14 wherein said second metal layer comprises a noble metal.

20. The method of claim 19 wherein the noble metal is selected from the group consisting of gold, platinum, and palladium.

21. The method of claim 14 wherein said second metal layer comprises gold.

22. The method of claim 14 wherein said seed layer comprises copper.

23. The method of claim 14 wherein said first metal layer comprises an electroplatable material.

24. The method of claim 23 wherein the electroplatable material is selected from the group consisting of copper, platinum, nickel, gold, silver, and solder.

25. The method of claim 14 wherein said first metal layer comprises nickel.

26. The method of claim 14 wherein said barrier layer comprises tantalum and tantalum nitride.

27. The method of claim 26 wherein the tantalum nitride is in contact with the substrate.

28. The method of claim 14 further comprising the step of bonding a wire to said second metal layer.

29. The method of claim 28 wherein said wire and said second metal layer comprise gold.

30. The method of claim 28 wherein said step of bonding a wire is selected from the group consisting of thermosonic bonding, ultrasonic bonding, and thermocompression bonding.

31. The method of claim 14 further comprising the step of forming a solder ball connected to said second metal layer.

32. The method of claim 31 wherein the step of forming a solder ball comprises plating.

33. The method of claim 31 wherein the step of forming a solder ball comprises evaporation.

* * * * *