

[54] **INPUT/OUTPUT MULTIPLEX CONTROL SYSTEM**

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[51] Int. Cl.....**H04g 9/00, H04g 11/00**

[58] Field of Search.....**340/152, 153, 147 LP**

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[57] **ABSTRACT**

An input and output control system is disclosed including at least one channel and input-output devices which are connected by a set of interconnecting lines which include a data input bus adapted to transfer data from said input-output devices to said channel and a data output bus adapted to transfer data from said channel to said input-output devices. An improved system of a bus type connection system is defined in which connection of one channel and a plurality of input-output devices is attained by said set of interconnecting lines and said input-output devices utilize one interconnecting line in time-divisional manner, said improved system being adapted to select one from among said several input-output devices said one having a request to be coupled with the channel. According to the improved system, it is therefore possible that the several input-output devices to be connected to the channel can impart the connecting requirement to the channel unit by utilizing the data input bus without providing signaling lines provided inherently on each of said devices, and that designation of any input-output device to be coupled can be attained by utilizing the data output bus without providing lines for designating connection of a required input-output device on the channel.

2 Claims, 5 Drawing Figures

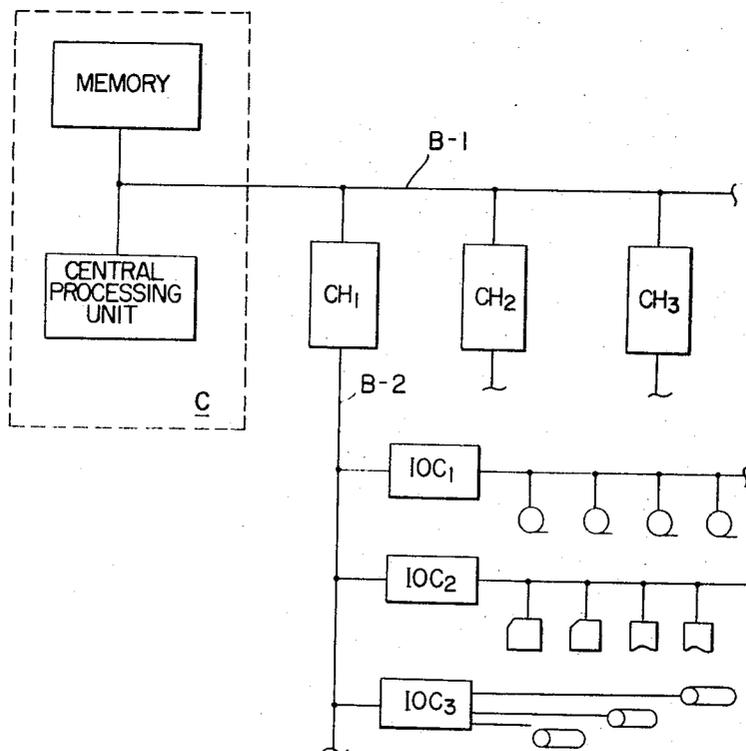
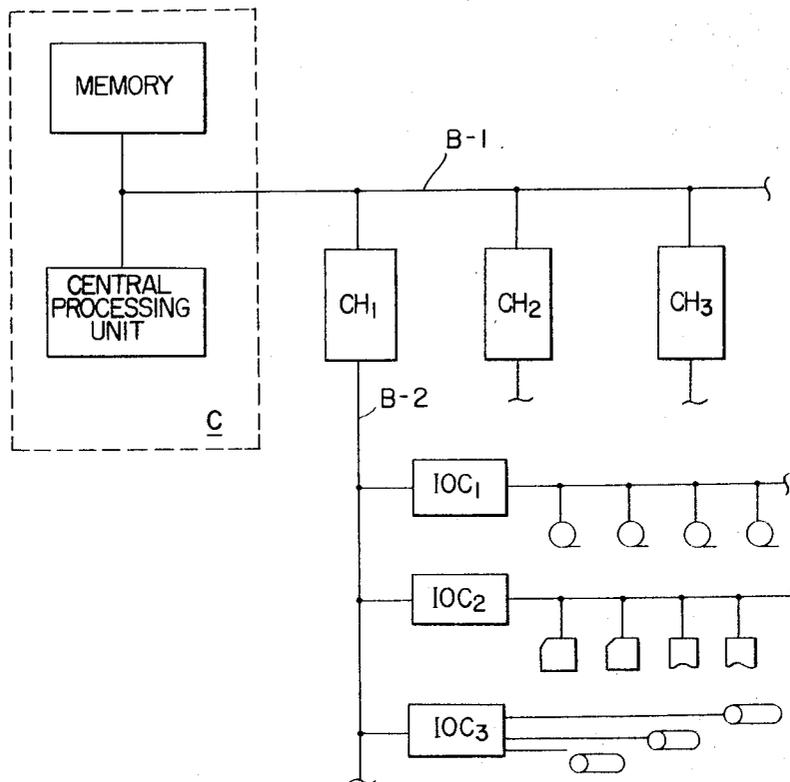


FIG. 1



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FIG. 2

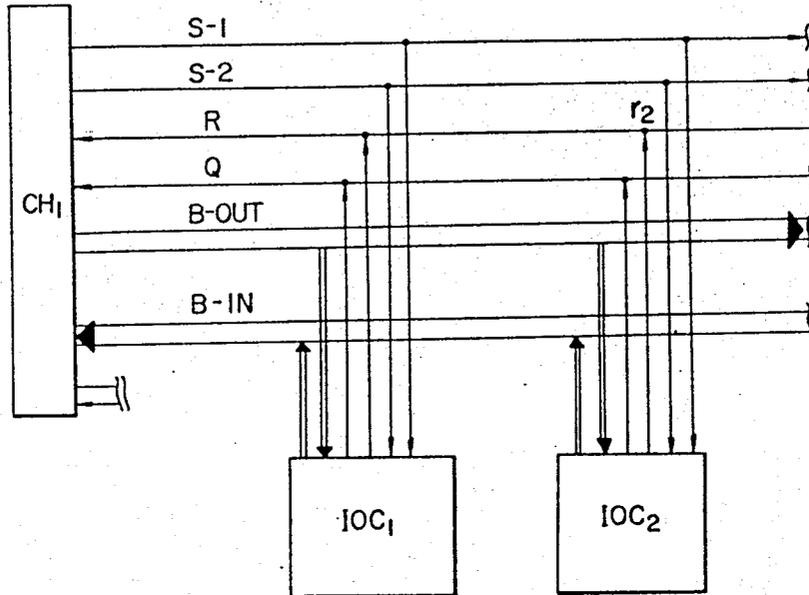
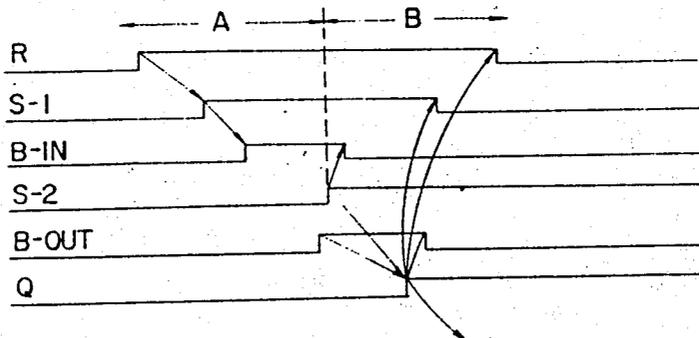


FIG. 3

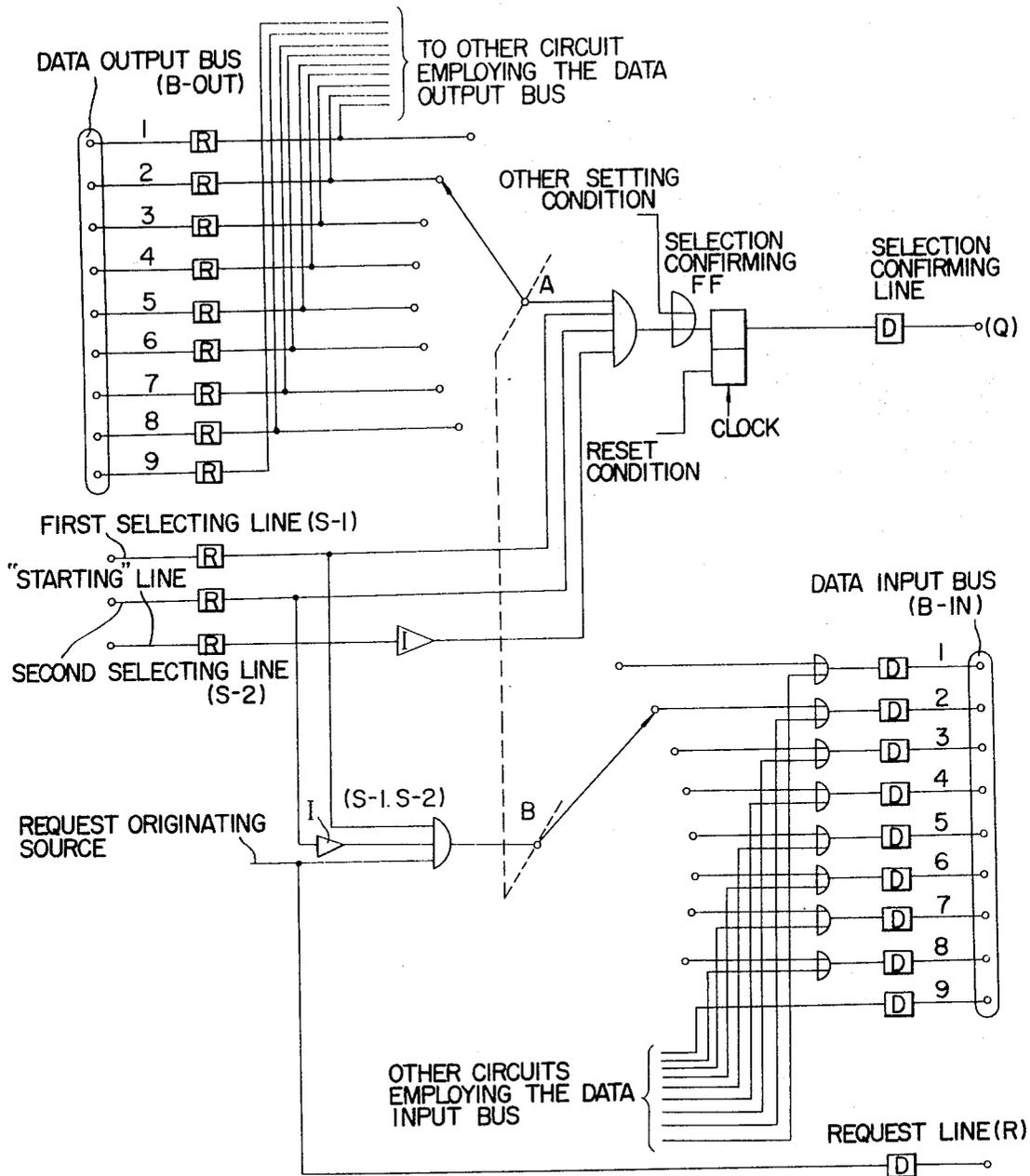


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FIG. 4

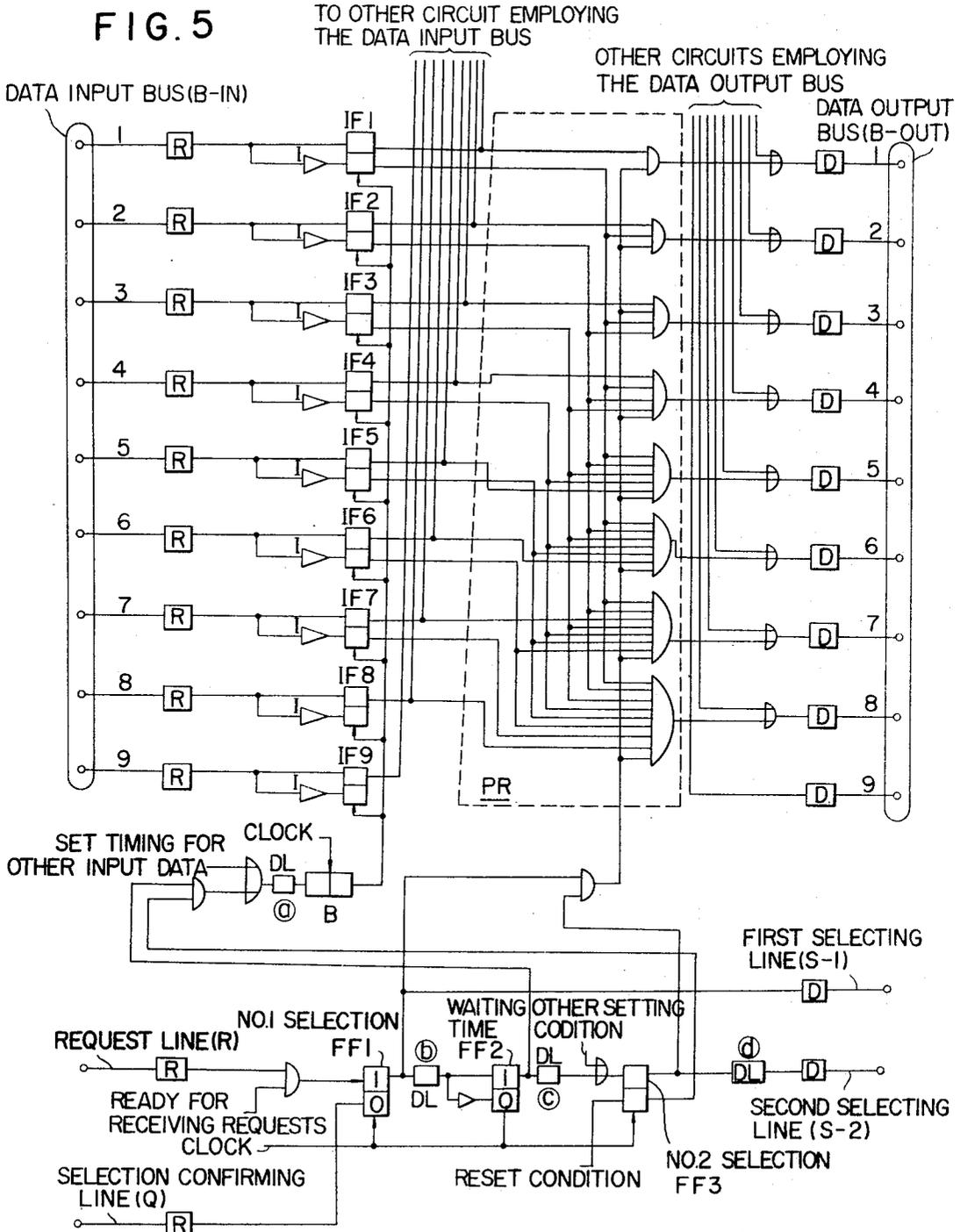


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INPUT/OUTPUT MULTIPLEX CONTROL SYSTEM

BACKGROUND OF THE INVENTION

This invention relates generally to the field of input and output devices to be employed for an electronic computer, and more particularly to a control system of the input and output devices for an electronic computer which is widely used for arithmetic operation, data processing, and for data transferring operation. More specifically, the invention is directed toward providing a novel type of a control system for the input and output devices, which is simple in construction and highly reliable in operation.

The input and output devices (hereinafter called I/O) are capable of issuing at random a request for transmitting information to memories in a central computer (the inlet and outlet of the memories are called channels), and at the memories (or channels) of the central computer, it is impossible to predict the occurrence of the requests from the I/O's. Conventional input and output control systems are divided into two types. One is a system in which a channel unit scans I/O devices one by one, discriminates which I/O device requires a data transfer and finishes the data transfer thereto, thereafter it begins again to scan the following I/O device. The other is a system in which a channel unit sends a signal for connection-permission to I/O devices, each of which relays said signal and transmits it to the following I/O device unless a data transfer is required by itself. In the former there is a defect in that when a channel unit scans I/O devices, it spends time, and accordingly, the rate of data transfer becomes small and sometimes a data is lost. In the latter there is a disadvantage that since I/O device relays a signal for connection-permission from a channel unit, normal operation of the following I/O device is prevented in case when a relay circuit does not operate.

The size and capacity of electronic computers are constantly yearly growing larger, and the number of I/O's connected in the computer system is constantly increasing. This also results in an increased number of the requests for transmitting information issued from the I/O's, and processing of the thus increasing requests is not an easy task.

Since a single memory (or a channel thereof) can be connected with one I/O or operational instrument at one time, if so many requests are desired to be processed at one time, priority must be determined with respect to these requests by means of a priority circuit so that only one I/O is allowed to be connected at one time with a memory (or a channel) of the central computer.

Furthermore, for the purpose of connecting the memories in the central computer station with each of the I/O's, there are provided a plurality of channels (the connection of the channels with the memories are completed only for a time period (time slot) allocated to each of the channels), each of which is in ordinary case connected with a priority circuit and a plurality of I/O control devices (hereinafter called IOC) which are directly connected to a common channel through respective data buses. Each of the IOC is further connected with a plurality of actual I/O's such as magnetic tapes, magnetic discs, magnetic drums, line printers, or the like, all of these and the above described connections constituting a series concatenated control system.

However, even with the series concatenated control system, the number of IOC's connected with one channel is still large, and to obtain proper connection of IOC's with a channel was not easy. A problem of "scanning in view of priority" here occurs. The present invention contemplates overcoming difficulties accompanying this problem.

When a plurality of IOC's are connected, in series concatenation, with one inlet (one channel) of a memory in an electronic computer, a requirement for the channel is that one of the IOC's having a request be first selected, and the required services be thereafter rendered. One of the conventional practices following the above described principle is disclosed in the specification of our copending U. S. Patent application Ser. No. 357,383, filed Feb. 6, 1964, now U.S. Pat. No.

3,303,476 and in such practice, the scanning is performed through a selecting line emanated from a channel and passing each of the IOC's consecutively, and a request line functioning to inform the channel of the existence of a request in any of the IOC's. A signal sent out over the selecting line is received once in a receiving circuit in each of the IOC's and passed into a judging circuit provide therein. The output signal from the judging circuit is then sent out onto the next IOC through a driver energized from the power source located in the first IOC.

Each of the IOC's, upon reception of the selecting signal, retransmits the signal to the next succeeding IOC if the first IOC has no request, but suspends the retransmission if the first IOC has any request and receives subsequent services from the channel. (see the above cited Patent application, FIG. 1, 1632, 1637, and 1639).

However, this kind of control system has the following drawbacks.

1. Since the selecting signal is received once in an IOC, judged therein, and sent out to the subsequent IOC through a driver energized from a power source in the former IOC, the power source in such IOC should have a provision allowing the driver to operate even if the power switch of the IOC is turned off.
2. Since the transmission of the selecting signal requires a considerably long time, another signal line is required for shortening an entailing transient of the signal.
3. For the purpose of imparting variability to the priority setting and also for the purpose of the above described reason, a return line returning to the channel is required for each of the signal lines.

SUMMARY OF THE INVENTION

Therefore, the principal object of the present invention is to overcome the above described drawbacks of the conventional I/O control systems.

Another object of the invention is to provide a novel I/O control system wherein the connection of the IOC's and the channel is carried out utilizing the data input and output buses inherently provided for these circuits.

Still another object of the invention is to provide a novel I/O control system whereby the number of the signal lines required between the channel and the IOC's is substantially reduced.

A further object of the invention is to provide a novel I/O control system wherein the setting of the priority for each of the IOC's can be arbitrarily determined.

An additional object of the invention is to provide a novel I/O control system wherein the conventional driver operated from a power source in each IOC can be eliminated.

These and other objects of the present invention are achieved by a novel I/O control system which comprises a data transmitting input bus and a data transmitting output bus provided between a channel in a central computer and each of the I/O's, means for informing the channel of the existence of a request in any one of the I/O's through the data input bus, a priority determining circuit which allows to pass a request from a higher priority I/O to the data output bus, and means for informing the I/O having the request of the decision in the priority circuit.

The invention will be more clearly understood from the following detailed description when read in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

In the drawing:

FIG. 1 is a diagram schematically showing an electronic computer system which is related with an I/O control system according to the present invention;

FIG. 2 is another diagram schematically showing a principal part of the I/O control system according to the invention;

FIG. 3 is a diagram showing time relation of the operations of the important parts of the I/O control system according to the invention; and

FIGS. 4 and 5 are block diagrams showing an example of the I/O control system according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

In one type of an electronic computer system as shown in FIG. 1, a central computer C is provided with a memory unit MU and a central processing unit CPU, which are connected in parallel through one input and output data bus B-1 to three channels CH1, CH2, and CH3. The number of the channels may be any desired number instead of the above indicated three. The channel CH1 is connected through an input and output data bus B-2 with three input-output control devices IOC1, IOC2, and IOC3, and the IOC1 is further connected with, for instance four magnetic tapes, the IOC2 is connected with, for instance, a card machine and a line-printer, and the IOC3 is connected with three magnetic drums. However, these connection and the numbers of the equipments are exemplary and may be changed in any suitable manner.

The present invention concerns a circuit connected between the CH1 and IOC1, IOC2, IOC3, and so on, and in FIG. 2, these circuits will be more fully illustrated. In FIG. 2, CH1 corresponds to one channel, and from the channel CH1, a first selecting line S-1, a second selecting line S-2, a data output bus B-OUT (consisting of 8 data lines and one check line), and other not shown lines are led out and connected with each of the IOC's. Furthermore, from each of the IOC's (consisting of IOC1, IOC2, IOC3, . . .), a request line R, a selection confirming line Q, a data input bus B-IN (consisting of 8 data lines and a check line), and not indicated lines are led to the channel CH1. The request line R is employed for reporting to the channel CH1 whether any one of the IOC's has or has not a request for transmitting data to CH1, and requests from respective IOC's, for instance, $r1$ from IOC1 and $r2$ from IOC2 logically added therein as $(r1 + r2)$, the sum being sent to the channel CH1.

The selection confirming line Q is employed for reporting to the channel CH1 that the selection of IOC's or I/O's connected to each of the IOC's has been positively carried out.

The data output bus B-OUT is a bus through which data or any other information is transmitted from the channel CH1 to each of the IOC's, and is connected to each of the IOC's in a branched-off manner from a common cable. This type of connection was described as "series concatenated" in the forward part of this description.

The data input bus B-IN is employed for transmitting data or any other information from the IOC's to the channel CH1, and branched lines led from each of the IOC's are connected to a common cable. This connection is also the type described as "series concatenated."

In an ordinary practice such as that described in our copending patent application mentioned above and also in the present invention, the number of IOC's connected to one channel, for instance, CH1 is restricted within eight in consideration of the transmitting time in the cable, and time limitations in the driver and receiver circuits, and also of the convenience in operation. In the present invention, maximum number of eight IOC's are connected to the channel through the common cable, and each of the eight data lines of input bus B-IN and output bus line B-OUT are assigned to the eight IOC's for the selecting purposes so that each IOC is uniquely specified.

FIG. 3 illustrates waveforms of signals (corresponding to a logic "1") in the interconnecting lines between the channel and the IOC's, such as a request line R, a first selecting line S-1, a second selecting line S-2, a data input bus B-IN, a data output bus B-OUT, and a selection confirming line Q. As indicated in FIG. 3, the selecting operation is divided into two stages A and B. The first selecting line S-1 and the second selecting line S-2 respectively directs initiation of the first stage A and the second stage B of the selection operation.

To be more particular, in the first stage A, the existence of requisition in any of the IOC's is informed to the channel through the data input bus B-IN, and in the second stage B, the channel indicates to anyone of the IOC's to receive a service thereof employing the data output bus B-OUT. As described above, since each of the IOC's is assigned a corresponding data line within eight data lines of the input and output buses, in the first stage A, anyone of the IOC's having request issues a request signal through the corresponding data line in the input data bus B-IN, and in the second stage, each of the IOC's can judge whether the request has been received or not. The reception of the requests in the channel is carried out by the priority determining circuit.

Although it is not shown in FIG. 2, the priority determining circuit is connected with the data input bus B-IN within the channel CH1, and the thus determined results are sent out through the data output bus B-OUT. More detailed description for the priority determining circuit will be presented with reference to FIG. 5 in a latter part of this specification.

Referring next to FIG. 2, the operation of the whole circuit will be explained. A process-requiring signal from each of the IOC's having a request is sent out through the request line R in the form of a logic sum, and the requiring signal is thereafter received by the channel CH1. If the channel CH1 is in a condition allowing processing of such requisition, the channel sends out a signal through the first selecting line S-1. When each of the IOC's receives this signal, the IOC having a request sends out a signal through a data line corresponding to the IOC. The channel investigates all of the data lines in the data input bus B-IN at a time when, in consideration of the transmission period in the cable and delay times in the driver and receiver, all of the requests from the IOC's are considered as having arrived. The channel upon finding such requests, sends out a signal through a data line in the data output bus B-OUT corresponding to the highest priority IOC among those having requests and, at the same time, sends out another signal on the selecting line S-2. Each of the IOC's, upon finding this signal sent out on S-2, stops sending out the signal through the above described data line of the data input bus B-IN, and simultaneously investigates its own data line in the data output bus B-OUT for a signal sent out of the channel. When the IOC finds out the signal sent out from the channel in the corresponding data line allocated to the IOC in the data output bus B-OUT, the IOC sends back a selection confirming signal Q on the selection confirming line, and then after sending back an address signal for the I/O, data or commanding signals are transmitted or received.

Above description concerns the case where an IOC having a request issues a requisition signal to the channel. Next, the operation of the circuit when the channel demands a connection with the an IOC will be described briefly although this has not much importance in the explanation of the present invention.

In FIG. 4, there is illustrated an exemplary constitution of the scanning circuit and related portions thereto included in each of the IOC's. Two switches A and B are interlinked each other and each of the switches A and B is connected with one data line of the output and the input buses allocated to the IOC, respectively. For example, if the second data line is allocated to the IOC, the switches A and B must be connected to the second data line of output bus and input bus, respectively. The connection of the two switches may be made by manual operation. An important requirement is that the switch position must be different for each of the IOC's.

When a request occurs in one of the IOC's, the request is sent through the data input bus B-IN gated by the logical condition $(S-1 \cdot S-2)$ where \cdot means logical AND of two signals. The channel, after investigating the input bus and deciding which IOC to be selected, sends out a signal through the data line assigned to the IOC on the B-OUT. IOC's investigate the assigned data line in the data output bus B-OUT, and if the signal was found to be logic "1", the selection-confirming Flip-flop FF is set under the logical condition of $(S-1 \cdot S-2 \cdot \overline{\text{start}})$, and a selection confirming signal is sent out to the chan-

nel. As described before, one line in these data input and output buses is employed for transmitting a check bit, and is not used for selection in this example. However, it would be easily understood that this line can also be used for selection if it is desired. FIG. 5 illustrates a timing signal generating circuit and a priority determining circuit in accordance with the present invention, both included in the channel.

When the channel is at a condition ready for receiving a request from IOC's, a first selection flip-flop FF1 is set upon arrival of a request from an IOC (over the request line R). Then, at the next clock signal, a waiting flip-flop FF2 is set. This waiting flip-flop is provided for establishing an waiting time during which all of the requests from the IOC's are allowed to arrive the channel, and a monostable multivibrator or a delay circuit may also employed instead of the waiting flip-flop FF2.

Under a condition where the waiting flip-flop FF2 is set and a second selection flip-flop FF3 is not set, the clock gates of all of the bus line flip-flops 1F1 through 1F9 are opened, and by the next clock signal the data in all of the data lines included in the input data bus B-IN (in this case, the requests from all of the IOC's) are set in the bus line flip-flops 1F1 through 1F9, and at the same time the second selection flip-flop FF3 is thereby set.

Upon setting of the second selection flip-flop FF3, the data set in all of the bus line flip-flops 1F1 through 1F8 are passed into the priority determining circuit PR and only one of the data lines is selected out of B-OUT and a signal is sent out on it. The priority determining circuit PR is shown to be connected so that the priority is determined in an order of 1F1 > 1F2 > 1F3 > 1F4 > . . . > 1F8. However, it is apparent that the connection of the priority circuit PR may be determined to adapt to any other order, or the circuit PR may be so arranged that the priority order can be changed at will. When a signal on a data line is sent out through the output bus B-OUT to a selected IOC, the second selecting signal is also sent out to the IOC simultaneously through the second selecting line S-2.

Furthermore, a circuit symbol "R" indicated in FIGS. 4 and 5 designates a receiver circuit which creates an output of logic "1" each time when the input over a cable is logic "1". Another circuit symbol "D" represents a driver circuit which delivers an output of logic "1" each time the input of the circuit is logic "1". Another circuit symbol "I" represents an inverter, "B" represents a blocking-oscillator which furnishes a clock signal to the bus line flip-flops 1F1 through 1F9, and "DL" designates a delay circuit which produces a delayed output "1" for an input of logic "1". Among the delay circuits "DL", "DL" a, b, c are employed for avoiding the racing of these circuits, and "DL" d is provided for sending out the second selecting signal after all the information is established for selecting IOC's connected with the output bus B-OUT.

Furthermore, the exemplary circuit shown in FIGS. 4 and 5 was found to operate satisfactorily with a sequential clock-pulse of 2 Mc/s.

We claim:

1. An apparatus for controlling input-output devices for an electronic computer system including at least one channel unit and a plurality of input-output devices, which apparatus comprises: a set of interconnecting lines for connecting said channel unit with said input-output devices so as to form a bus

system, said interconnecting lines including a data input bus connected to transfer data from one of said input-output devices to said channel unit; a data output bus connected to transfer data from said channel unit to said one of said input-output devices; and sequence control lines for controlling information transmission through the input-output buses, said channel unit comprising a first selection signal sending circuit to instruct each input-output device to send a request to the input bus in order to select one input-output device requiring to be connected with the channel unit from among the several input-output devices; a priority determining circuit to read out said request transmitted through the input bus thereby to determine the highest priority input-output device; a circuit for sending out the output of said priority determining circuit into the output bus, a second selection signal sending circuit for instructing each input-output device to read out the signal passing through said output bus; and wherein each of said input-output devices comprises a circuit for sending out a signal to a predetermined data line of the input bus in response to the first selection signal from the channel unit and a circuit adapted to read out the output bus line to determine whether said input-output device is selected or not, whereby said one set of interconnecting lines are time-divisionally and commonly used for the input-output devices and for only a time period when data transfer is carried out between one input-output device and the channel unit.

2. An apparatus for controlling input-output devices for an electronic computer system including at least one channel unit and a plurality of input-output devices, which apparatus comprises: a set of interconnecting lines for connecting said channel unit with said input-output devices so as to form a bus system, said interconnecting lines including a data input bus connected to transfer data from one of said input-output devices to said channel unit; a data output bus connected to transfer data from said channel unit to one of said input-output devices; and sequence control lines for controlling information transmission through the input-output buses, said channel unit comprising a first selection signal sending circuit to instruct each input-output device to send a request to the input bus in order to select one input-output device requiring to be connected with the channel unit from among said input-output devices; a priority determining circuit to read out said request transmitted through the input bus thereby to determine the highest priority input-output device, said priority determining circuits sending out a signal to a data line on the data output bus, said data line corresponding respectively to said plural input-output devices; a second selection signal sending circuit for instructing each input-output device to read out the signal passing through said output bus; and wherein each of said input-output devices comprises a circuit for sending out a signal to a data line of the data input bus in response to the first selection signal from the channel unit said data line being predetermined in correspondence with a respective one of said input-output devices and a circuit adapted to read out the output bus line to determine whether said input-output device is selected or not, whereby said one set of interconnecting lines are time-divisionally and commonly used for the input-output devices and for only a time period when data transfer is carried out between one input-output device and the channel unit.

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