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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :		(11) International Publication Number:
H04Q 1/453, H04L 27/30, 27/14 H03K 5/153	A1	WO 93/01687
		(43) International Publication Date: 21 January 1993 (21.01.93)

(21) International Application Number: PCT/NL92/00115

(22) International Filing Date: 1 July 1992 (01.07.92)

(30) Priority data:
91201679.7 1 July 1991 (01.07.91) EP
(34) Countries for which the regional or international application was filed: NL et al.

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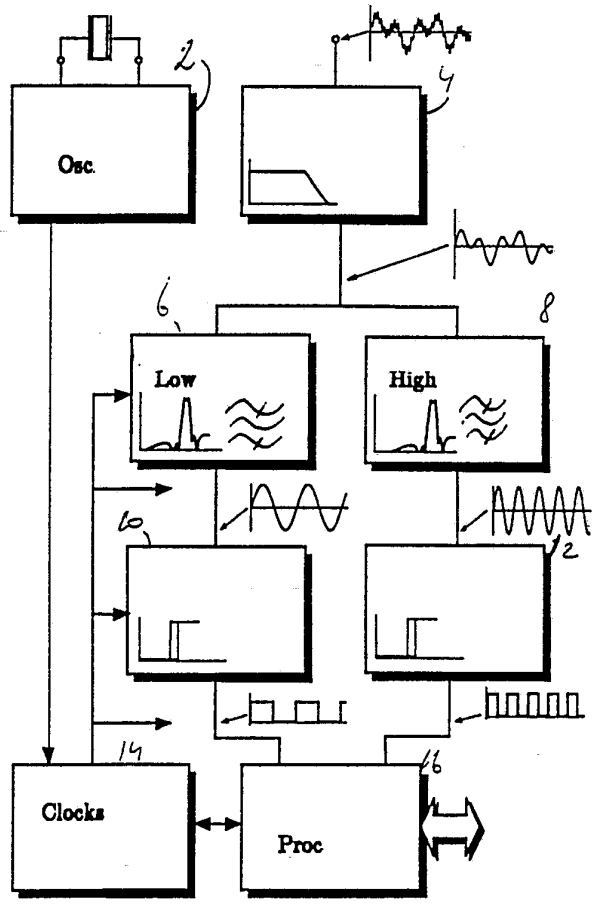
(81) Designated States: JP, KR, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LU, MC, NL, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
In English translation (filed in Dutch).

(54) Title: TONE RECEIVER COMPRISING A SWITCH CAPACITOR ZERO CROSSING DETECTOR

(57) Abstract

Tone receiver comprising a switched capacitor zero crossing detector (10). The zero crossing detector is arranged for compensating the input offset voltage by causing during a first capacitor switching phase this offset voltage to be present across a capacitor (34) which is connected in parallel with the input of the comparator. At the same time it appears that with this operation any DC voltage component in the input signal can be blocked. With the aid of a voltage step source (46) a voltage step is realised on the input capacitor (34), which step functions as a threshold in the comparator phase. Once the threshold voltage has been exceeded, the comparator is reversed and the processor changes the control of the voltage step source, so that this source produces a threshold voltage of opposite sign. This achieves an effect of hysteresis which counteracts the constant reversing of the comparator.



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Tone receiver comprising a switch capacitor zero crossing detector.

The invention relates to a tone receiver comprising a zero crossing detector which includes an amplifier circuit that has an inverting input and a non-inverting input. Such receivers are known, for example, from the article entitled "A monolithic dual tone multifrequency receiver" in IEEE Journal of Solid State Circuits, Vol. SC-14, No. 6, December 1979. These tone receivers may be used in telephone sets for detecting tone signals customary in telephony, such as DTMF signals (Dual Tone Multi Frequency).

Amplifier circuits having an inverting and a non-inverting input have the property of being capable of presenting an offset voltage *i.e.* it is possible that a voltage unequal to zero occurs at the output if there is a zero voltage difference between the two inputs. This offset voltage has a detrimental effect on the operation of the zero crossing detector, because the zero level of the amplifier/comparator input now no longer has a symmetrical position between the positive and negative input threshold voltages to be set. This may have the effect that the amplifier circuit acting as a comparator is energized by small interference signals which are smaller than the set threshold value.

It is an object of the invention to provide a tone receiver of the type mentioned in the opening paragraph, in which the offset voltage is compensated, so that the detrimental effect of the offset voltage is eliminated.

According to the invention, the tone receiver is characterized in that the zero crossing detector includes:

* an amplifier circuit used as an amplifier and as a comparator and having an inverting input and a non-inverting input, the non-inverting input being coupled to a reference voltage source, and including a feedback loop between the output and the inverting input which loop includes a first on/off switch,
* a first capacitor between the two inputs,
* a second capacitor between the signal input of the tone receiver

and the inverting input of the amplifier,

* a second on/off switch connected in series with the second capacitor,
* and a control circuit which opens and closes the two on/off switches in phase opposition.

In a first control phase of the two switches, the first switch is closed (*i.e.* conductive), and the second switch is open. Consequently, the second capacitor is not connected to the amplifier and the output of the amplifier is connected directly to the inverting input. This results in the fact that the first capacitor is charged to the offset voltage. In the second control phase of the switches, the first switch is open and the second switch is closed. The original charge of the first capacitor is now divided between the first and the second capacitor. These phases are repeated, so that the second capacitor will eventually be charged to the offset voltage. In this situation and in the event of a lacking input signal on the zero crossing detector, the offset voltage will be present on both inputs *i.e.* the actual offset voltage on the non-inverting input and the voltage across the second capacitor having the same magnitude on the inverting input. The result of this is that with a zero voltage input signal the output voltage is also zero.

An additional advantage of said measures is that also any DC voltage component present in the input signal is blocked. Such a component may have the same disturbing effect as the offset voltage.

An embodiment of the tone receiver according to the invention is characterized in that the tone receiver comprises:

* a third capacitor connected on one side *via* a third on/off switch to the non-inverting input of the amplifier circuit,
* connected to the other side of the third capacitor a threshold voltage source for producing a threshold voltage signal which consists of a fixed step size,
* and a fourth on/off switch, one side of which is connected to the junction of the third capacitor and the third on/off switch and the other side of which is connected to the reference voltage source,
* which third and fourth switches are opened and closed in phase with the second switch and the first switch respectively, by the

control circuit.

These measures achieve that the zero crossing detector can produce a threshold voltage, so that minor interference signals such as noise do not activate the detector. This threshold voltage presents hysteresis *i.e.* once the detector has been activated in reaction to, for example, an upward transgression of a positive threshold voltage, the threshold voltage is then rendered negative and *vice versa*. This is advantageous in that a signal varying around the threshold voltage will not constantly reverse the zero crossing detector.

Because the threshold voltage generator constantly generates voltage steps, the series combination of the first, the second and the third capacitor is charged. The first and third capacitors are also constantly discharged (the former because it is constantly connected to the output of the amplifier by the first switch and the latter because it is constantly connected to the reference voltage by the fourth switch). The second capacitor, however, is not constantly discharged and it is conceivable that as a result the proper operation of the zero crossing detector is affected detrimentally. In order to avoid this situation the tone receiver according to a further embodiment of the invention is characterized, in that the threshold voltage source in the tone receiver comprises means for producing within a switch-on interval of the second switch after said threshold voltage step a voltage step of equal magnitude and opposite polarity. The equally large voltage step of opposite polarity will now discharge the third capacitor by the same charge as the one it had been charged with.

The invention will be further explained with reference to the drawing Figures, in which:

Fig. 1 shows a block diagram of a tone receiver according to the invention;

Fig. 2 shows a zero crossing detector to be used in a tone receiver according to the invention.

The tone receiver as shown in Fig. 1 may be used in a telephone set. The incoming signal is then applied to an anti-aliasing filter 4. The function of this filter is to reject the mixing frequencies developing during signal sampling. The output of this filter is connected to two filters 6 and 8 for band splitting and rejecting undesired signals. In the DTMF mode the two filters operate at fixed bandpass frequencies; in the

signalling tone mode one of these filters is switched off. The other filter is then adjustable in a number of frequency bands the range of which being situated between 80 Hz and 3400 Hz. The output signal of the filters 6 and 8 are applied to zero crossing detectors 10 and 12. These detectors will be described in detail with reference to Fig. 2. The output signal of each of the zero crossing detectors is applied to a digital processor 16 which further evaluates signals and controls the various circuit elements including the zero crossing detector. Each of the blocks shown in Fig. 1 is supplied with clock signals derived from a crystal oscillator 2 with a frequency of, for example, 3.58 MHz. The exact frequency and phase of the clock signals are produced in divider and control circuit 14. At the inputs of the various blocks in the drawing Figure there is shown diagrammatically which signal form is applied to each block.

Drawing Fig. 2 shows in more detail a zero crossing detector such as, the detector 10 shown in Fig. 1. This zero crossing detector comprises an amplifier circuit 20 acting as an amplifier-cum-comparator and having an inverting input 22 and a non-inverting input 24. This non-inverting input 24 is connected by means of a switch 58 to a reference source 26 (not shown in the drawing Figure). The amplifier circuit further includes a feedback loop 28 which includes a switch 32; this feedback loop is situated between the output 30 of the amplifier and the inverting input 22. A series combination of a capacitor 36 and a switch 40 is situated between the signal input 38 of the zero crossing detector and the inverting input 22.

The non-inverting input 24 is also connected to a threshold voltage source 46 *via* a switch 44 and a capacitor 42. A further switch 48 is inserted between the reference voltage 26 and the junction of capacitor 42 and switch 44. The threshold voltage source 46 comprises a parallel combination of a current source 50, on the one hand, and a series combination of a current source 52 and a switch 54, on the other. These two current sources apply their current to a forward biased diode 56.

The switches in this zero crossing detector are preferably arranged as complementary CMOS gates known *per se*. The advantage of CMOS transistors is that in the open state (non-conductive) they present a very high resistance between drain and source, whereas the control electrode, as a result of its capacitive coupling to the drain-source path, hardly draws a charge from the elements driving the control electrode.

For the elucidation of the operation of the zero crossing detector it is assumed that the non-inverting input is connected to a fixed voltage *i.e. via* switch 58

and reference 26. The switches of the zero crossing detector are driven with a frequency that is high relative to the signals to be received, for example, several hundred kHz. In a first phase of the operating interval of the zero crossing detector a number of switches is closed (*i.e.* conductive); these switches are symbolically denoted by "e" (even) in the drawing Figure, whereas the other switches are denoted by "o" (odd). Even switches are in phase opposition to the odd switches *i.e.* one type of switches is open, whereas the other type is closed and *vice versa*. Only switch 54 is not of the control type described hereinbefore, as will be explained hereinafter.

The operation of the zero crossing detector as an offset voltage compensation circuit is as follows:

In a first phase of the operation of the detector switch 58 is closed and the non-inverting input 24 is connected to reference 26 *via* switch 58. The offset at the input is symbolically represented by means of a voltage source 60. In this phase also switch 32 is closed, so that the inverting input 22 is connected to output 30. Since a feedback differential amplifier always tries to drive the two inputs to the same voltage, the offset voltage will now be present across capacitor 34. In the next phase switch 32 is open and the switches 44 and 40 are closed. The charge of capacitor 34 will now partly flow to capacitor 36 which is charged as a result. In the next phase capacitor 34 is charged again to the offset voltage after which, in a next phase, again part of this offset voltage flows to capacitor 36. This process is continued until the whole offset voltage is present across capacitor 36. Assuming that no input signal is present on input 38, the side of capacitor 36 connected to the inverting input has been brought to the level of the offset voltage, and so has the inverting input. Because this is also the case with the non-inverting input, there is no longer a voltage difference between the two inputs and neither is there an offset effect any longer.

For recognizing that the zero crossing detector also blocks any DC component V_{DC} present in the input signal, it is again assumed that input 24 is connected to reference. With an open switch 32 and a closed switch 40 the capacitors 36 and 34 are charged by V_{DC}. In the next phase the two switches are reversed, so that the charge of capacitor 34 is nulled; the charge of capacitor 36 is maintained. In the next phase V_{DC} again charges the two capacitors, after which the capacitor 34 is discharged. This is continued until the complete V_{DC} is present across capacitor 36, which means that the DC component in the input signal is blocked.

The zero crossing detector according to the invention is arranged for producing a threshold voltage which, in addition, is reversed to a value of opposite sign once the input signal has exceeded the threshold voltage. This effect of hysteresis avoids that the detector is constantly reversed by a signal that remains in the neighbourhood of the threshold voltage for some time. The threshold voltage is produced as follows:

During the even phase (thus when switches 44 and 40 are closed), switch 54 is either being opened or closed. In either case the current flowing through diode 56 will vary by a step size, so that the voltage present across the diode will also present a (small) step. This voltage step is transferred to capacitor 34 by capacitor 42. Capacitor 34 is considerably smaller than either of the two capacitors 42 and 36. This means that substantially the whole voltage step is present across capacitor 34. For reversing the amplifier 20 acting as a comparator, the input voltage is to exceed this voltage present across capacitor 34. This procedure thus creates the threshold voltage.

Once the comparator has reversed, this is detected by the digital processor (see Fig. 1) connected to the zero crossing detector. This processor controls, for example, the operation of switch 54. It is assumed that, initially, a positive threshold voltage had been set. If the threshold is exceeded by the input signal, the detector is reversed. This is detected by the processor which, in response, controls switch 54 so that this switch is closed at the beginning of the "even" period. Shortly after the beginning of this period, switch 54 is opened, so that threshold voltage source 46 produces a negative current step, thus also voltage step. This negative voltage step becomes present across capacitor 34 in above fashion, so that the input signal is to have a more negative value for reversing the comparator. This procedure thus creates the negative threshold voltage.

It is advantageous to have the current step of threshold voltage source 46 effected again in reverse order just before the end of the even period. As a result, all capacitors allowing the current step to pass through, are now discharged by an opposite current step. This avoids that, particularly capacitor 36, which is not discharged during the entire operation cycle of the zero crossing detector, is charged to an unacceptably high voltage value.

CLAIMS:

1. Tone receiver comprising at least one zero crossing detector (10), this zero crossing detector including:

* an amplifier circuit (20) used as an amplifier and as a comparator and having an inverting input (22) and a non-inverting input (24), the non-inverting input being coupled to a reference voltage source (26), and including a feedback loop (28) between the output (30) and the inverting input (22) which loop includes a first on/off switch (32),
* a first capacitor (34) between the two inputs (22, 24),
* a second capacitor (36) between the signal input (38) of the tone receiver and the inverting input (22) of the amplifier (20),
* a second on/off switch (40) connected in series with the second capacitor (36),
* and a control circuit (14, 16) which opens and closes the two on/off switches (32, 40) in phase opposition.

2. Tone receiver as claimed in Claim 1, comprising:

* a third capacitor (42) connected on one side *via* a third on/off switch (44) to the non-inverting input (24) of the amplifier circuit (20),
* connected to the other side of the third capacitor (42) a threshold voltage source (46) for producing a threshold voltage signal which consists of a fixed step size,
* and a fourth on/off switch (48), one side of which is connected to the junction of the third capacitor (42) and the third on/off switch (44) and the other side of which is connected to the reference voltage source (26),
* which third and fourth switches (44, 48) are opened and closed in phase with the second switch (40) and the first switch (32)

respectively, by the control circuit (14, 16).

3. Tone receiver as claimed in Claim 2, wherein the tone receiver comprises means (14, 16) for producing within a switch-on interval of the second switch (40) following said threshold voltage step a further voltage step of equal magnitude and opposite polarity.

4. Tone receiver as claimed in Claim 1, wherein the first capacitor (34) is formed by the parasitic capacitance of the input stage of the amplifier circuit (20).

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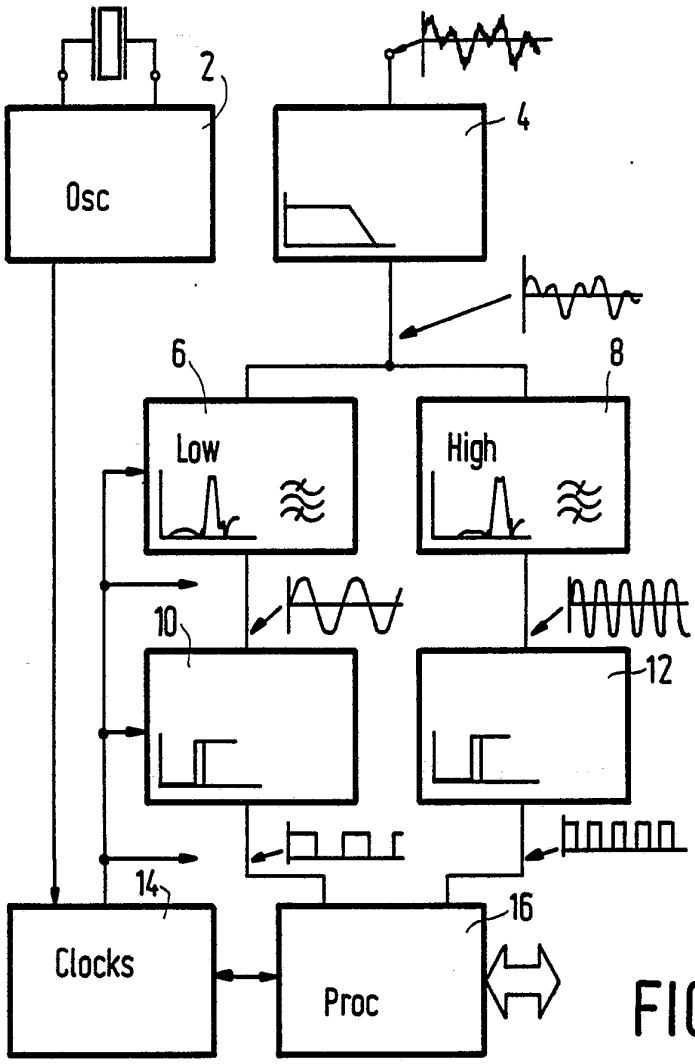
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FIG.1

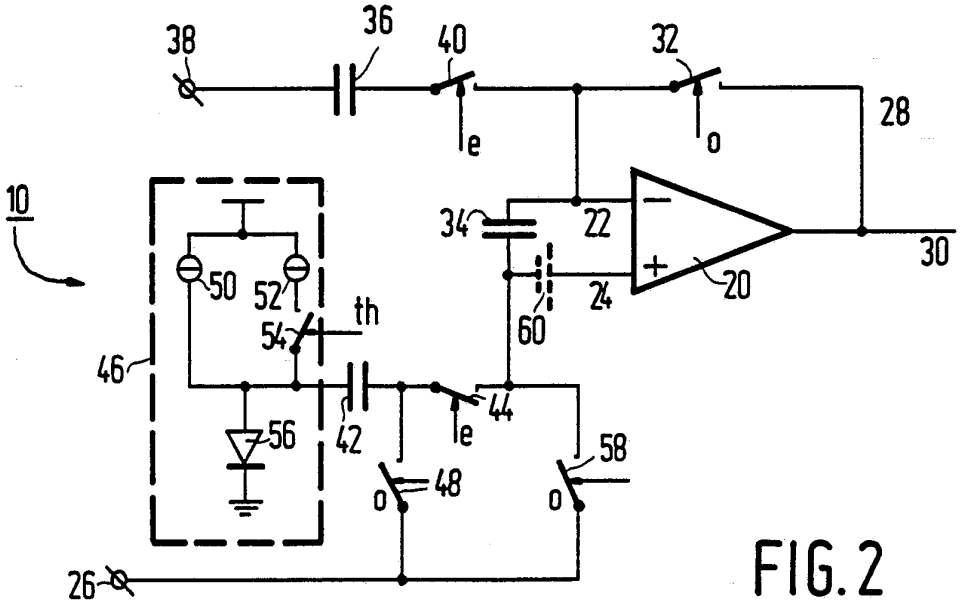
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FIG.2

INTERNATIONAL SEARCH REPORT

International Application No PCT/NL 92/00115

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H04Q1/453; H04L27/30; H04L27/14; H03K5/153

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H04Q ; H04L ; H03K

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE vol. 25, 11 February 1982, NEW YORK, USA page 212 FLEISHER ET AL. 'A single chip Dual-Tone and Dial-Pulse Signaling Receiver' see the whole document	1-4
A	EP,A,0 008 220 (ROLM CORPORATION) 20 February 1980 see abstract; figure 1	1-3
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 305 (E-363)(2028) 3 December 1985 & JP,A,60 142 613 (FUJITSU K.K.) 27 July 1985 see abstract	1-2

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
09 NOVEMBER 1992	16. 11. 92
International Searching Authority	**Signature of Authorized Officer**
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III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 11, no. 187 (E-516)(2634) 16 June 1987 & JP,A,62 15 918 (NEC CORP) 24 January 1987 see abstract ---	1-3
A	ELEKTRONIK vol. 39, no. 5, 2 March 1990, MUNCHEN, DE pages 100 - 110 , XP100469 WALTER J. ET AL 'Integrierbare Funktionblöcke und Systeme. see Teil 5: Analog- Komparatoren' -----	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. NL 9200115 SA 63176

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-0008220	20-02-80	US-A- 4191862	04-03-80