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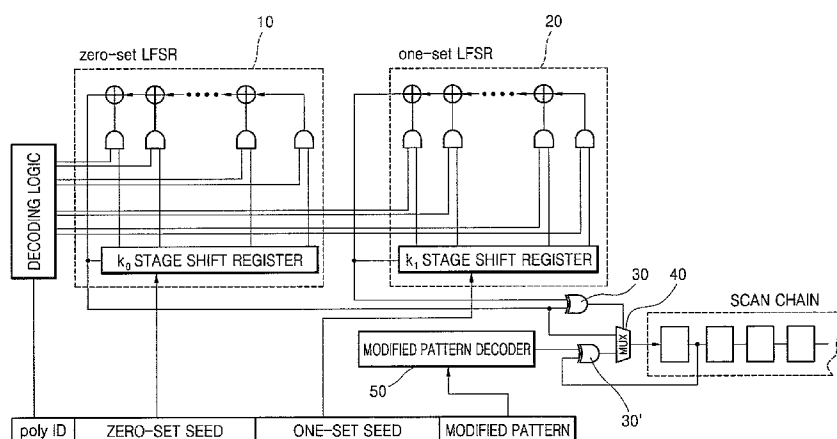
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[Continued on next page]

(54) Title: LOW POWER DETERMINISTIC BIST USING SPLIT LFSR



(57) Abstract: A technique of dividing a linear feedback shift register (LFSR) into LFSRs in order to reduce power consumption by reducing the number of transitions in a deterministic built-in self test (BIST) for testing a semiconductor device is provided. The deterministic BIST technique of testing the semiconductor device by applying test patterns to a scan chain of the semiconductor device includes: dividing a test cube generated by automatic test pattern generation (ATPG) into a zero-set cube and a one-set cube; generating test patterns by combining test patterns generated by the zero-set cube and the one-set cube; and comparing two generated test pattern values, and if the two test pattern values are the same, providing the generated test pattern value to an input of the scan chain, and otherwise, i.e. if the two test pattern values are different, providing the previous scan chain input value to an input of the scan chain.

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LOW POWER DETERMINISTIC BIST USING SPLIT LFSR

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TECHNICAL FIELD

The present invention relates to a technique of splitting a linear feedback shift register (LFSR) so as to reduce power consumption by reducing number of transitions in a deterministic built-in self test (BIST) for testing a semiconductor device.

10

BACKGROUND ART

A built-in self test (BIST) is a logic test for determining whether a circuit is defective. The BIST is a typical technique used in a design for testability (DFT) substituting for expensive automated test equipment (ATE) and allows at-speed testing. However, since correlation of test patterns that are applied in a test mode is very low as compared with those in a normal functional mode, a large amount of heat is generated due to an excessive number of transitions. Since heat damages circuits, power concerns are one of the most important considerations in the test mode. In case of the BIST in which deterministic test patterns are applied in order to detect defects, which are hardly found by using random patterns, unnecessary switching operations are performed since X values (disregarding bits) of the test pattern are filled with random patterns, and therefore power concerns become further serious.

In the past, a method using double LFSR reseeding has been suggested as a method of reducing power consumption when a deterministic pattern is applied to detect defects. According to the method of using double LFSR reseeding, a main-LFSR generates test patterns by using an existing LFSR reseeding, and an additional sub-LFSR generates a mask pattern. Final patterns are generated by performing an OR operation or an AND operation with the two LFSR patterns. Accordingly, the number of transitions of the patterns that are finally applied to a scan operation can be reduced. However, in this method, an additional LFSR and an additional seed value for generating the mask pattern has to be stored, and the number of transitions of the patterns is reduced by only about 25 %.

A method of using a hold cube has also been suggested and according to this method, each test cube is divided into several blocks, and a hold flag is allocated to each

of the blocks. When the hold flag of a block is 1, a scan input in the corresponding block maintains the last value generated in the previous block. However, in this method, an additional storage space for storing the hold cube is needed and additional hardware for a hold flag shift register is necessary.

5 A low power test method using a scan slice overlapping has been suggested however, a test pattern is divided into several overlapping slice sets, and accordingly transitions do not occur in an overlapping block. However, in this case, since a change of the number of overlapping blocks is high, deviations of a reduction of the number of switching operations increases.

10 DETAILED DESCRIPTION OF THE INVENTION

TECHNICAL PROBLEM

The present invention provides a new linear feedback shift register (LFSR) reseeding method using split LFSRs capable of reducing the number of transitions in a scan chain by researching a structure capable of generating low power patterns even when deterministic patterns are applied, in relation with a scan operation in which power is largely consumed.

15 The present invention also provides a low power and deterministic built-in self test (BIST) method of testing a semiconductor device capable of reducing power consumption by reducing the number of transitions in a scan chain by dividing the LFSR into two LFSRs and using the two LFSRs and a device therefor.

TECHNICAL SOLUTION

25 According to an aspect of the present invention, there is provided a deterministic built-in self test (BIST) method of testing a semiconductor device by applying a test pattern in a scan chain of the semiconductor device, the method comprising: dividing a test cube generated by automatic test pattern generation (ATPG) into a zero-set cube and a one-set cube; generating test patterns by combining test patterns generated by the zero-set cube and the one-set cube; and comparing two generated test pattern values, and
30 if the two test pattern values are the same, providing the generated test pattern value to an input of the scan chain, and otherwise, i.e. if the two test pattern values are different, providing the previous scan chain input value to an input of the scan chain.

The method may further comprise initially removing defects by applying pseudo-r

andom patterns to the scan chain before dividing the test cube.

When the test pattern values generated in the generating of the test patterns are different from each other, the previous scan chain input value is inverted and applied to the scan chain.

5 The above-described method can be implemented as a computer readable program, and thus a computer readable recording medium having embodied thereon the computer program is also within the scope of the present invention.

According to another aspect of the present invention, there is provided a low power and deterministic built-in self test (BIST) device for testing a semiconductor device by
10 applying a test pattern in a scan chain of the semiconductor device, the device comprising: a first unit dividing a test cube generated by automatic test pattern generation (ATPG) into a zero-set cube and a one-set cube;
a second unit generating test patterns by combining test patterns generated by the zero-set cube and the one-set cube; and a third unit comparing two generated test pattern values and, if the two test pattern values are the same, providing the generated test pattern value to an input of the scan chain, and otherwise, i.e. if the two test pattern values are different, providing the previous scan chain input value to an input of the scan chain.
15

The first unit may include a linear feedback shift register (LFSR) for the zero-set cube and an LFSR for the one-set cube.
20

The third unit may include a selecting unit inputting the generated test pattern value as an input of the scan chain when the test pattern values are the same, and inputting the previous scan chain input value as an input of the scan chain when the test pattern values are different from each other.

25 In the BIST method according to an embodiment of the present invention and the device therefor, two split LFSRs are used to generate test patterns. Each LFSR generates a zero-set cube which is constructed by bits of 0 in the original test cube and a one-set cube which is constructed by 1 bits in the original test cube, respectively. Accordingly, the 1 bits generated in the LFSR for the zero-set cube and the bits of 0 generated in the LFSR for the one-set cube have X values (don't care bits). The X values allow
30 the final input values to be maintained, thereby reducing the number of transitions in the scan chain. As the experiment result of applying the present invention to the ISCAS

circuits, the BIST according to an embodiment of the present invention can reduce the switching operations in the scan chain by 50 %.

ADVANTAGEOUS EFFECTS

5 According to an embodiment of the present invention, when a circuit is tested by applying a deterministic pattern using the BIST technique, power consumption due to the applied patterns is low, and therefore, a safe and low power test can be performed on the circuit. In addition, since it is possible to supply one module, which is combined with software for automatically generating the structure according to an embodiment of the present invention, in CAD related fields, an economic effect due to single item can be achieved. It is possible to create profits due to the technology transfer such as insertion of the corresponding algorithm into the existing BIST generation tool.

DESCRIPTION OF THE DRAWINGS

15 FIG. 1 is a schematic view illustrating a built-in self test (BIST) device;
 FIG. 2 illustrates an algorithm source for generating low power patterns and modified patterns; and
 FIG. 3 illustrates a flowchart of an encoding method according to an embodiment of the present invention.

20

BEST MODE

A built-in self test (BIST) structure using split linear feedback shift registers (LFSRs)

25 Hereinafter, the BIST structure for applying the aforementioned low power and deterministic patterns will be described. In FIG. 1, a hardware architecture according to an embodiment of the present invention is illustrated. By comparing the hardware architecture with an existing reseeding hardware structure, two XOR logic gates 30 and 30', a multiplexer (MUX) 40, and a modified pattern decoder 50 are additionally used for the hardware architecture. In addition, in the present invention, an LFSR is divided into an LFSR 10 for a zero-set cube and an LFSR 20 for a one-set cube. The split test cube has a less number of specific bits than an original test cube. Accordingly, the length of each LFSR is less than that of an existing LFSR. Accordingly, even when two LFSR

30

s are used, the total size of the LFSR is the same as that of the existing LFSR. When a deterministic pattern is applied, it is determined by using the XOR gate 30 whether the two LFSR outputs are the same. When the two LFSR outputs are the same, the LFSR output is selected by using the MUX 40. When the two LFSR outputs are different from each other, a previous scan input value is selected by the MUX 40. When the previous scan input value is selected, since if a modified pattern value is 1, the previous scan input value has to be inverted, the XOR 30 operation is performed with respect to the previous scan input value and the modified pattern value. The output of the XOR operation is applied to a scan chain through MUX 40.

Mechanism of reducing the number of transitions of the pattern applied to a scan operation

In the existing LFSR reseeding method, a seed value is obtained by solving a linear equation obtained from a characteristic polynomial of the LFSR with respect to a given test cube. The LFSR generates all the specific bits except of X values of the test cube by using the seed value. The X values are filled with pseudo random patterns generated by the LFSR. The X values that are filled with pseudo random patterns generated by the LFSR cause unnecessary transitions in a scan chain. Accordingly, in order to minimize the number of transitions in a test pattern, X values have to be filled with suitable values.

Given a signal S, $P_1(S)$ represents a probability that the signal S is 1. $P_0(S)$ represents a probability that the signal S is 0. When it is assumed that the signal S is a random pattern generated by the LFSR, $P_0(S) + P_1(S) = 1$, and $P_0(S) = P_1(S) = 0.5$. In this case, a transition probability $P_{tr}(S)$ of the signal S represents a probability that a current value of the signal S is different from its previous value. The transition probability $P_{tr}(S)$ of the signal S can be computed as $P_{tr}(S) = P_0(S) \times P_1(S) + P_0(S) \times P_1(S) = 0.5 \times 0.5 + 0.5 \times 0.5 = 0.5$.

In order to reduce the number of transitions in the test pattern, the transition probability $P_{tr}(S)$ of the signal S has to be reduced. When the values that are previously input into the scan chain can replace all the X values of the test pattern, the transition probability $P_{tr}(S)$ of the test pattern can be reduced to a minimum. For example, in the test cube, when it is assumed that the probability that the values of the test pattern are not the X values is 5 %, the probability that the values of the test pattern are 0 is 50 %, and

the probability that the values of the test pattern are 1 is 50 %, the transition probability $P_{tr}(S)$ of the test pattern is 2.5 %. However, if the previous input values can replace the X values as much as possible, the transition probability $P_{tr}(S)$ of the test pattern can be considerably reduced, thereby reducing the number of switching operations.

When it is assumed that $C=(c_0, \dots, c_{m-1}) \in \{0, 1, X\}^m$ is a deterministic test cube C, $S(C)=\{i|c_i \neq X\}$ is a specific bit set of the deterministic test cube C, $S(C)$ can be divided into a zero-set cube and a one-set cube. In this case, when $S_0(C)=\{i|c_i=0\}$ is the zero-set cube, and $S_1(C)=\{i|c_i=1\}$ is the one-set cube, an initial seed for generating the deterministic test cube C can be obtained by solving a known linear equation. An initial seed for generating the zero-set cube and the one-set cube can also be obtained through the same procedures. All 1 bits in the pattern generated through the zero-set cube and all 0 bits in the pattern generated through the one-set cube are X values with respect to each cube.

Table 1 is a table for comparing patterns generated from the zero-set cube and the one-set cube. Table 1 represents the values generated through the LFSR for the zero-set cube and the one-set cube and values of an original test cube corresponding to the generated values. 0_x and 1_x at first and second columns represent a 0 or 1 bit in which X values of the zero-set and one-set cubes are filled with the values generated in each LFSR. Similarly, 0_s and 1_s represent a 0 or 1 bit in which specific bit values of the zero-set and one-set cubes are filled with the values generated in each LFSR. According to the definition of the zero-set and one-set cubes, two LFSRs cannot generate 0_s and 1_s at the same time.

【Table 1】

Zero-set cube pattern value	One-set cube pattern value	Original test cube value
0_x	0_x	X
0_s	0_x	0
0_x	1_s	1
0_x	1_x	X
0_s	1_x	0
1_x	0_x	X
1_x	1_x	X

1_x	1_s	1
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Referring to Table 1, when the values of the zero-set cube pattern and the one-set cube pattern are all 0, the value of the original test cube is 0 or X. Accordingly, in this case, when value of 0 is used as the scan input value, the original test cube value can be compatible with the original test cube. Similarly, when the values of the zero-set cube pattern and the one-set cube pattern are 1, the value of the original test cube is 1 or X. Accordingly, the value of 1 can be used as the scan input value. When the value of 1 is generated in the zero-set cube, the value of 0 is generated in the one-set cube and the value of the original test cube is X. Accordingly, in this case, when the previous input value is used as the scan input value, the transition does not occur in the scan chain. Finally, when the zero-set cube generates 0 and the one-set cube generates 1, the value of the original test cube may be 0, 1, or X. Accordingly, like the aforementioned case, when the previous scan input value is used, the previous scan input value may be incompatible with the value of the original test cube. In this case, additional information is necessary so that the previous scan input value may be compatible with the value of the original test cube. That is, when the previous scan input value is inverted and used at the incompatible location, the value of the original test cube can be accurately applied. In general, since the ratio of the X values in the test cube is very high, the frequency of the aforementioned modifications is not high. Practically, a ratio of large circuits among ISCAS circuits which need the aforementioned modification are equal to or less than 2 %. Accordingly, when the aforementioned cases are neglected, the transitions occur only when the values of the patterns generated in the two LFSRs are the same.

Even in this case, since the transitions occur only when the generated values are different from the previous scan input values, the transition probability is 25 %. As such, the transition probability is reduced by 50 % as compared with the case using one LFSR

Encoding algorithm

In the present embodiment, an encoding method suggested in the present invention in order to reduce the number of transitions in the test pattern will be described. An algorithm source, which generates low power patterns and modified patterns by using the structure of the BIST device of FIG. 1, is illustrated in FIG. 2. In FIG. 2, C is a test cube generated by automatic test pattern generation (ATPG). $C[i]$ represents the i-th

value of C . C is divided into a zero-set cube C_0 and a one-set cube C_1 . Patterns P_0 and P_1 are generated by the LFSR for generating a zero-set cube and a one-set cube. $P_0[i]$ and $P_1[i]$ represent i -th values of the patterns P_0 and P_1 .

FIG. 3 illustrates a flowchart of the encoding method of FIG. 2.

5 First, in order to easily remove detectable defects, pseudo-random patterns are applied (operation 102). Then, in order to detect the rest of the defects, which are not detected by the pseudo-random patterns, ATPG is performed to generate deterministic patterns in the form of test cubes (operation 104). Each test cube generated by the ATPG is divided into zero-set and one-set cubes C_0 and C_1 (operation 106). Initial seed
10 values with respect to the divided test cubes are calculated by the existing LFSR reseeding method (operations 108 and 110). The low power test pattern $P_L[i]$ generated by the split LFSR in the present invention is obtained by combining the test patterns generated by the two divided test cubes (operations 112 and 114).

Next, the values of the zero-set and one-set cubes generated in each LFSR are
15 compared with each other (operation 116). When the generated values are the same, a value is used as an input value of a scan chain (operation 120). When the generated values are different from each other, previous scan chain input values are used as the input value of the scan chain (operation 122). As described above, when the two LFSR outputs are different, the previous scan input value may be incompatible with a value
20 of an original test cube. Therefore, when the previous scan input value is incompatible with the value of the original test cube, the previous scan input value has to be inverted and used. Then, the value of the modified pattern $P_C[i]$ is 1. That is, when the value of the modified pattern $P_C[i]$ is 0, the previous scan input value is applied to the scan chain without change. When the value of the modified pattern $P_C[i]$ is 1, the previous
25 scan input value is inverted and applied to the scan chain.

A computer program can perform the aforementioned method. The invention can also be embodied as a computer program on a computer readable recording medium. The computer readable recording medium is any data storage device that can store data that can be thereafter read by a computer system. Examples of the computer readable recording medium include read-only memory (ROM), random-access memory (RAM), CD-ROMs, magnetic tapes, floppy disks, optical data storage devices, and carrier waves (such as data transmission through the Internet).
30

Performance of the BIST according to an embodiment of the present invention

An experiment for examining efficiency of the BIST method according to an embodiment of the present invention is performed with respect to the largest circuits from among ISCAS '89 benchmark circuits. First, 10,000 pseudo-random patterns are applied, and easily detectable defects are removed. Then, ATPG is performed on the rest of the defects to generate deterministic test patterns in order to achieve a 100 % defect detection rate.

Table 2 represents the number of transitions of the patterns generated by using the existing LFSR reseeding method and the number of transitions of the low power patterns generated by the method according to an embodiment of the present invention, as an experiment result of the split LFSR structure using ISCAS '89 benchmark circuits. As known from Table 2, the number of transitions is reduced by about 50 % with respect to all the circuits.

【Table 2】

Circuit	Existing pattern	Low power pattern	Transition reduction rate (%)
S5378	350541	196439	43.96
S9234	4116302	2080515	49.46
S13207	17120326	9020954	47.31
S15850	18858953	9286490	50.76
S38417	554011356	275796859	50.22
S38584	122781180	65773590	46.43
Average	119539776	60359141	48.02

CLAIMS

1.

5 A deterministic built-in self test (BIST) method of testing a semiconductor device by applying a test pattern in a scan chain of the semiconductor device, the method comprising:

dividing a test cube generated by automatic test pattern generation (ATPG) into a zero-set cube and a one-set cube;

10 generating test patterns by combining test patterns generated by the zero-set cube and the one-set cube; and

comparing two generated test pattern values, and if the two test pattern values are the same, providing the generated test pattern value to an input of the scan chain, and otherwise, i.e. if the two test pattern values are different, providing the previous scan chain input value to an input of the scan chain

2

The method of claim 1, further comprising initially removing defects by applying pseudo-random patterns to the scan chain before dividing the test cube.

3.

The method of claim 1, wherein when the generated test pattern values generated in the generating of the test patterns are different from each other, the previous scan input value is inverted and applied to the scan chain.

4.

A computer recording medium having embodied thereon a computer program for executing the method of any one of claims 1 to 3.

5.

30 A low power and deterministic built-in self test (BIST) device for testing a semiconductor device by applying a test pattern in a scan chain of the semiconductor device, the device comprising:

a first unit dividing a test cube generated by automatic test pattern generation (ATPG) into a zero-set cube and a one-set cube;

a second unit generating test patterns by combining test patterns generated by the zero-set cube and the one-set cube; and

5 a third unit comparing two generated test pattern values, and if the two test pattern values are the same, providing the generated test pattern value to an input of the scan chain, and otherwise, i.e. if the two test pattern values are different, providing the previous scan chain input value to an input of the scan chain.

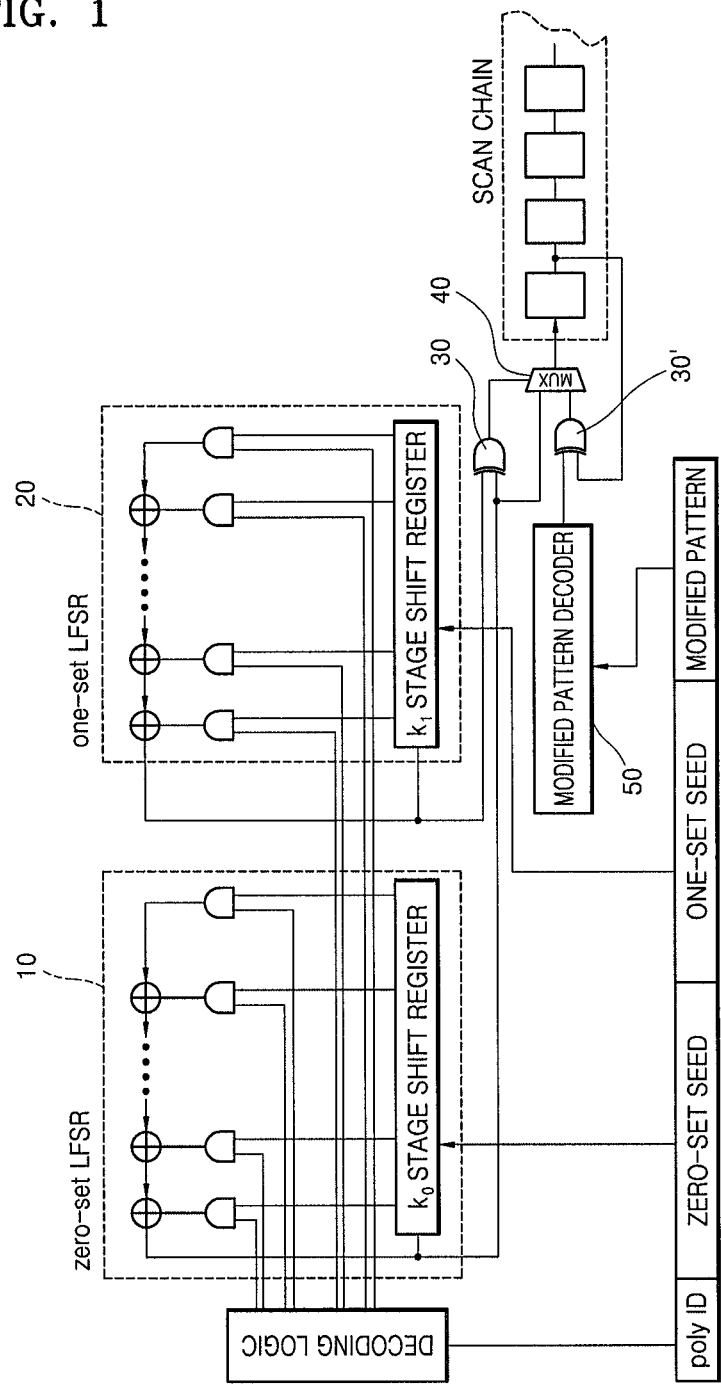
10 6.

The device of claim 5, wherein the first unit includes a linear feedback shift register (LFSR) for the zero-set cube and an LFSR for the one-set cube.

7.

15 The device of claim 5, wherein the third unit includes a selecting unit inputting the generated test pattern value as an input of the scan chain when the test pattern values are the same and inputting the previous scan chain input value as an input of the scan chain when the test pattern values are different from each other.

FIG. 1



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FIG. 2

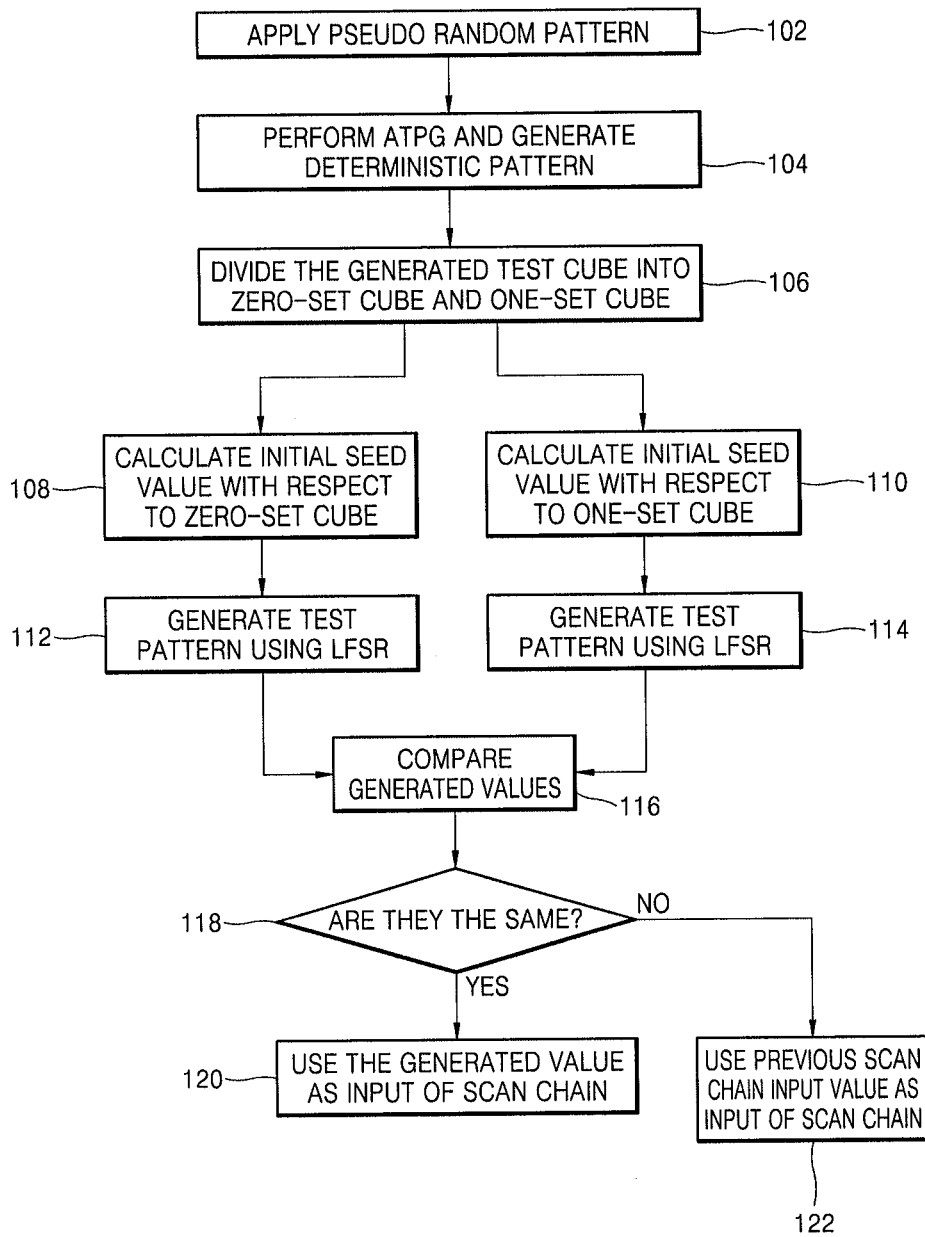
```

LP_PATTERN_GEN {
  do pseudo_random_fault_simulation ;
  do deterministic_ATPG ; /* generate the original test cube C */
  foreach ( C ) {
    do partition C into  $C_0$  and  $C_1$  ; /* test cube partitioning */
    do compute the initial seeds from  $C_0$  ; /* reseeding for the zero-set cube */
    do generate the zero-set cube pattern  $P_0$  ;
    do compute the initial seeds from  $C_1$  ; /* reseeding for the zero-set cube */
    do generate the one-set cube pattern  $P_1$  ;
     $P_L = 0$  ; /* initialize the low power pattern */
     $P_C = 0$  ; /* initialize the correction pattern */
    for (  $i = 1$  to pattern_size ) {
      if (  $P_0[i] = P_1[i]$  )
        then  $P_L[i] = P_0[i] = P_1[i]$  ;
      else
        then
          if (  $C[i] \neq 'X'$  and  $P_L[i-1] \neq C[i]$  ) /* a pattern to be corrected */
             $P_L[i] = \text{invert}(P_L[i-1])$  ; /* pattern correction */
             $P_C[i] = \text{bit } 1$  ; /* update the correction pattern */
          else
            then  $P_L[i] = P_L[i-1]$  ; /* the previous pattern value */
    }
  }
}

```

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FIG. 3



PCT

Paper Copy (NOT for submission)

VIII-5-1	Declaration: Non-prejudicial disclosure or exceptions to lack of novelty Declaration as to non-prejudicial disclosures or exceptions to lack of novelty (Rules 4.17(v) and 51bis.1(a)(v)): Name (LAST, First)	in relation to this international application INDUSTRY-ACADEMIC COOPERATION FOUNDATION, YONSEI UNIVERSITY declares that the subject matter claimed in this international application was disclosed as follows:
VIII-5-1(i)	Kind of disclosure:	publication
VIII-5-1(i)	Date of disclosure:	30 June 2006 (30.06.2006)
VIII-5-1(ii)	Title of disclosure:	A LOW POWER DETERMINISTIC BIST USING SPLIT LFSR
VIII-5-1(i)	Place of disclosure:	The 7th Korea Test Conference in Seoul, Rep. of Korea

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2006/004847**A. CLASSIFICATION OF SUBJECT MATTER***G11C 29/00(2006.01)i*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 :G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Utility models and applications for Utility Models since 1975

Japanese Utility Models and application for Utility Models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS (KIPO internal) "BIST, built in self test,built-in self test,LFSR,linear feedback shift register,semiconductor,test pattern,encod*"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/0073373 A1 (Michinobu Nakano, et al.) 13 JUNE 2002 See abstract, Fig 33~35, claim 1,claim 6, claim11	1-7
A	US 6816991 B2 (Amit Dinesh Sanghani) 9 NOVEMBER 2004 See abstract, Fig.2,Fig3,Fig4, claim 1, claim 9	5-7
A	US 5983009 (Yervant David Lepejian, et al.) 9 NOVEMBER 1999 See abstract, Fig1A, claim 1	1-4



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

18 APRIL 2007 (18.04.2007)

Date of mailing of the international search report

19 APRIL 2007 (19.04.2007)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

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