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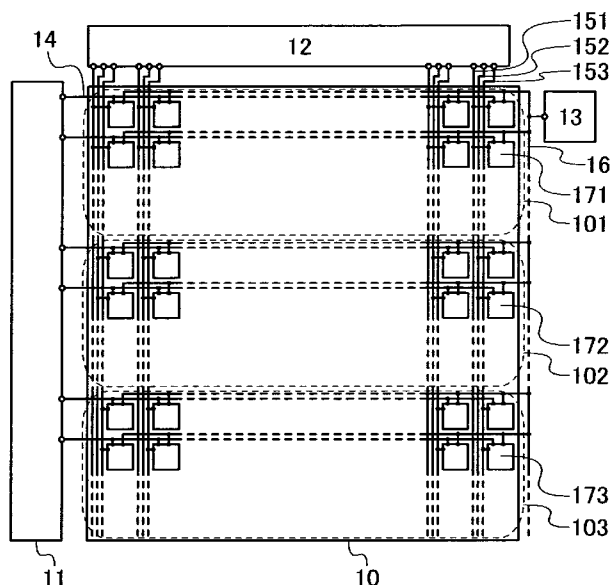
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(54) Title: LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR DRIVING THE SAME

FIG. 1A



(57) Abstract: To increase the frequency of input of image signals, a pixel portion of a liquid crystal display device is divided into a plurality of regions, and input of image signals is controlled in each of the plurality of regions. As a result, a plurality of scan lines can be selected at the same time in the liquid crystal display device. That is, in the liquid crystal display device, image signals can be simultaneously supplied to pixels placed in a plurality of rows, among pixels arranged in matrix. Thus, the frequency of input of an image signal to each pixel can be increased without change in response speed of a transistor or the like included in the liquid crystal display device.

DESCRIPTION

**LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR DRIVING THE
SAME**

5

TECHNICAL FIELD

[0001]

The present invention relates to a liquid crystal display device and a method for driving the liquid crystal display device. In particular, the present invention relates to a liquid crystal display device in which images are displayed by a field sequential method, and a method for driving the liquid crystal display device.

BACKGROUND ART

[0002]

A color filter method and a field sequential method are known as display methods for liquid crystal display devices. In a liquid crystal display device in which images are displayed by a color filter method, a plurality of subpixels each having a color filter that only transmits light with a wavelength of a given color (e.g., red (R), green (G), or blue (B)) are provided in each pixel. A desired color is produced in such a manner that transmission of white light is controlled in each subpixel and a plurality of colors are mixed in each pixel. On the other hand, in a liquid crystal display device in which images are displayed by a field sequential method, a plurality of light sources that emit lights of different colors (e.g., red (R), green (G), and blue (B)) are provided. A desired color is produced in such a manner that the plurality of light sources sequentially emit light and transmission of light of each color is controlled in each pixel. In other words, a desired color is produced by dividing the area of one pixel by lights of given colors in a color filter method, whereas a desired color is produced by dividing a display period by lights of given colors in a field sequential method.

[0003]

The liquid crystal display device in which images are displayed by a field sequential method has the following advantages over the liquid crystal display device in which images are displayed by a color filter method. First, in the liquid crystal display

device employing a field sequential method, it is not necessary to provide subpixels in a pixel. Thus, the aperture ratio or the number of pixels can be increased. In addition, in the liquid crystal display device employing a field sequential method, it is not necessary to provide a color filter. That is, loss of light due to light absorption in the color filter does not occur. For that reason, the transmittance can be increased and power consumption can be reduced.

[0004]

Patent Document 1 discloses a liquid crystal display device in which images are displayed by a field sequential method. Specifically, Patent Document 1 discloses a liquid crystal display device in which pixels each include a transistor for controlling input of an image signal, a signal storage capacitor for holding the image signal, and a transistor for controlling transfer of electric charge from the signal storage capacitor to a display pixel capacitor. In the liquid crystal display device having this structure, writing of an image signal to the signal storage capacitor and display corresponding to electric charge held at the display pixel capacitor can be performed at the same time.

[Reference]

[0005]

Patent Document 1: Japanese Published Patent Application No. 2009-042405

DISCLOSURE OF INVENTION

[0006]

In a liquid crystal display device in which images are displayed by a field sequential method, the frequency of input of an image signal to each pixel needs to be increased. For example, in the case where images are displayed by a field sequential method in a liquid crystal display device including three kinds of light sources, each of which emits one of red (R) light, green (G) light, and blue (B) light, the frequency of input of an image signal to each pixel needs to be at least three times as high as that of a liquid crystal display device in which images are displayed by a color filter method. Specifically, in the case where the frame frequency is 60 Hz, an image signal needs to be input to each pixel 60 times per second in the liquid crystal display device in which images are displayed by a color filter method; whereas an image signal needs to be input to each pixel 180 times per second in the case where images are displayed by a

field sequential method in the liquid crystal display device including three kinds of light sources.

[0007]

Note that high-speed response of an element included in each pixel is required, accompanied by the increase in the input frequency of image signals. Specifically, the increase in mobility of a transistor provided in each pixel is required, for example. However, it is not easy to improve characteristics of the transistor or the like.

[0008]

In view of the above, an object of one embodiment of the present invention is to increase the frequency of input of image signals in terms of design.

[0009]

The above-described object can be achieved in the following manner: a pixel portion of a liquid crystal display device is divided into a plurality of regions, and input of an image signal is controlled in each of the plurality of regions.

[0010]

According to one embodiment of the present invention, a liquid crystal display device includes a first signal line supplied with a first image signal in a horizontal scan period, a second signal line supplied with a second image signal in the horizontal scan period, a first scan line and a second scan line supplied with a selection signal in the horizontal scan period, a first pixel electrically connected to the first signal line and the first scan line, and a second pixel electrically connected to the second signal line and the second scan line.

[0011]

In the liquid crystal display device according to one embodiment of the present invention, a plurality of scan lines can be selected at the same time. That is, in the liquid crystal display device according to one embodiment of the present invention, image signals can be simultaneously supplied to pixels placed in a plurality of rows, among pixels arranged in matrix. Thus, the frequency of input of an image signal to each pixel can be increased without change in response speed of a transistor or the like included in the liquid crystal display device.

BRIEF DESCRIPTION OF DRAWINGS

[0012]

In the accompanying drawings:

FIG. 1A illustrates a structural example of a liquid crystal display device, and FIGS. 1B to 1D each illustrate a configuration example of a pixel;

5 FIG. 2A illustrates a structural example of a scan line driver circuit, FIG. 2B illustrates a configuration example of a selector circuit, and FIG. 2C illustrates a configuration example of a buffer;

FIG. 3 illustrates operation of a scan line driver circuit;

10 FIG. 4A illustrates a structural example of a signal line driver circuit, and FIG. 4B illustrates an operation example of a liquid crystal display device;

FIG. 5A illustrates a variation of a buffer, and FIG. 5B illustrates change in potential of signals;

FIG. 6 illustrates a structural example of a transistor;

FIGS. 7A to 7C each illustrate a structural example of a transistor; and

15 FIGS. 8A to 8F each illustrate an example of an electronic device.

BEST MODE FOR CARRYING OUT THE INVENTION

[0013]

20 Embodiments of the present invention will be described below in detail with reference to the accompanying drawings. Note that the present invention is not limited to the description below, and it is easily understood by those skilled in the art that a variety of changes and modifications can be made without departing from the spirit and scope of the present invention. Therefore, the present invention should not be construed as being limited to the description of the embodiments.

25 [0014]

First, an example of a liquid crystal display device in which images are displayed by a field sequential method will be described with reference to FIGS. 1A to 1D, FIGS. 2A to 2C, FIG. 3, and FIGS. 4A and 4B.

[0015]

30 (Structural Example of Liquid Crystal Display Device)

FIG. 1A illustrates a structural example of a liquid crystal display device. The liquid crystal display device in FIG. 1A includes a pixel portion 10; a scan line driver

circuit 11; a signal line driver circuit 12; a transfer signal line driver circuit 13; $3n$ scan lines 14 (n is a natural number of 2 or more) arranged parallel or approximately parallel to each other; m signal lines 151, m signal lines 152, and m signal lines 153 (m is a natural number of 2 or more) arranged parallel or approximately parallel to each other; and a transfer signal line 16 having $3n$ branch lines arranged parallel or approximately parallel to the scan lines 14. The potentials of the scan lines 14 are controlled by the scan line driver circuit 11. The potentials of the signal lines 151, 152, and 153 are controlled by the signal line driver circuit 12.

[0016]

The pixel portion 10 is divided into three regions (regions 101 to 103), and each region includes a plurality of pixels arranged in matrix (of n rows and m columns). Each of the scan lines 14 is electrically connected to m pixels arranged in a given row, among the plurality of pixels arranged in matrix (of $3n$ rows and m columns) in the pixel portion 10. Each of the signal lines 151 is electrically connected to n pixels arranged in a given column, among the plurality of pixels arranged in matrix (of n rows and m columns) in the region 101. Each of the signal lines 152 is electrically connected to n pixels arranged in a given column, among the plurality of pixels arranged in matrix (of n rows and m columns) in the region 102. Each of the signal lines 153 is electrically connected to n pixels arranged in a given column, among the plurality of pixels arranged in matrix (of n rows and m columns) in the region 103. The transfer signal line 16 is electrically connected to all the plurality of pixels arranged in matrix (of $3n$ rows and m columns) in the pixel portion 10.

[0017]

To the scan line driver circuit 11, start signals (GSP1 to GSP3) for the scan line driver circuit, a clock signal (GCK) for the scan line driver circuit, and drive power supplies such as high power supply potentials (VDD1 and VDD2) and a low power supply potential (VSS) are input from the outside. To the signal line driver circuit 12, signals such as a start signal (SSP) for the signal line driver circuit, a clock signal (SCK) for the signal line driver circuit, and image signals (DATA1 to DATA3) and drive power supplies such as a high power supply potential and a low power supply potential are input from the outside.

[0018]

FIGS. 1B to 1D each illustrate an example of a circuit configuration of a pixel. Specifically, FIG. 1B illustrates an example of a circuit configuration of a pixel 171 placed in the region 101. FIG. 1C illustrates an example of a circuit configuration of a pixel 172 placed in the region 102. FIG. 1D illustrates an example of a circuit configuration of a pixel 173 placed in the region 103. The pixel 171 in FIG. 1B includes a transistor 1711, a capacitor 1712, a transistor 1713, and a liquid crystal element 1714. A gate of the transistor 1711 is electrically connected to the scan line 14. One of a source and a drain of the transistor 1711 is electrically connected to the signal line 151. One of electrodes of the capacitor 1712 is electrically connected to the other of the source and the drain of the transistor 1711. The other of the electrodes of the capacitor 1712 is electrically connected to a wiring that supplies a capacitor potential. A gate of the transistor 1713 is electrically connected to the transfer signal line 16. One of a source and a drain of the transistor 1713 is electrically connected to the other of the source and the drain of the transistor 1711 and one of the electrodes of the capacitor 1712. One of electrodes (a pixel electrode) of the liquid crystal element 1714 is electrically connected to the other of the source and the drain of the transistor 1713. The other of the electrodes (a counter electrode) of the liquid crystal element 1714 is electrically connected to a wiring that supplies a counter potential.

[0019]

The pixel 172 in FIG. 1C and the pixel 173 in FIG. 1D have the same circuit configuration as the pixel 171 in FIG. 1B. Note that the pixel 172 in FIG. 1C differs from the pixel 171 in FIG. 1B in that one of a source and a drain of a transistor 1721 is electrically connected to the signal line 152 instead of the signal line 151. The pixel 173 in FIG. 1D differs from the pixel 171 in FIG. 1B in that one of a source and a drain of a transistor 1731 is electrically connected to the signal line 153 instead of the signal line 151.

[0020]

Note that the liquid crystal element illustrated in FIGS. 1B to 1D is preferably formed using a liquid crystal material exhibiting a blue phase. Here, a liquid crystal material refers to a mixture that includes liquid crystals and is used for a liquid crystal layer. By using a liquid crystal material exhibiting a blue phase, the rise time and fall time of the liquid crystal element can be 200 microseconds or less.

[0021]

(Structural Example of Scan Line Driver Circuit 11)

FIG. 2A illustrates a structural example of the scan line driver circuit 11 included in the liquid crystal display device in FIG. 1A. The scan line driver circuit 11 illustrated in FIG. 2A includes shift registers 111 to 113 each having $3n$ output terminals, and $3n$ buffers 114 each having three input terminals and one output terminal. Three input terminals of the buffer 114 are electrically connected to different k -th output terminals (k is a natural number of 1 to $3n$) of the shift registers 111 to 113. The output terminal of the buffer 114 is electrically connected to the scan line 14 in the k -th row in the pixel portion 10.

[0022]

The shift register 111 includes pulse output circuits of $3n$ stages (pulse output circuits 111_1 to 111_3n) and selector circuits 1110_1 and 1110_2. The pulse output circuits 111_1 to 111_3n have a function of sequentially shifting a signal by using the start signal (GSP1) input to the first-stage pulse output circuit, as a trigger (i.e., a function of delaying the signal by a 1/2 cycle of the clock signal (GCK) and outputting the resulting signal). The selector circuits 1110_1 and 1110_2 each have a function of selecting an output signal of the shift register 111 from an output signal of the pulse output circuit and the low power supply potential (VSS). The selector circuit 1110_1 is provided between the $(n+1)$ th-stage pulse output circuit 111_3n+1, the $(n+2)$ th-stage pulse output circuit 111_3n+2, and the $(n+1)$ th output terminal of the shift register 111 (the $(n+1)$ th buffer 114). The selector circuit 1110_2 is provided between the $(2n+1)$ th-stage pulse output circuit 111_2n+1, the $(2n+2)$ th-stage pulse output circuit 111_2n+2, and the $(2n+1)$ th output terminal of the shift register 111 (the $(2n+1)$ th buffer 114). Output terminals of the pulse output circuits 111_1 to 111_n, 111_n+2 to 111_2n, and 111_2n+2 to 111_3n are provided to be directly connected to the corresponding output terminals of the shift register 111 (the corresponding buffers 114). Note that the shift registers 112 and 113 can have a structure similar to that of the shift register 111; therefore, the detailed structures of the shift registers 112 and 113 are not shown in FIG. 2A.

[0023]

FIG. 2B illustrates a configuration example of the selector circuit 1110_1 illustrated in FIG. 2A. The selector circuit 1110_1 in FIG. 2B includes a transistor 1111, an inverter 1112, and a transistor 1113. A gate of the transistor 1111 is electrically connected to a wiring that supplies a transfer signal (T). One of a source and a drain of the transistor 1111 is electrically connected to a wiring that supplies the low power supply potential (VSS). The other of the source and the drain of the transistor 1111 is electrically connected to the (n+1)th buffer 114. An input terminal of the inverter 1112 is electrically connected to the wiring that supplies the transfer signal (T). A gate of the transistor 1113 is electrically connected to an output terminal of the inverter 1112. One of a source and a drain of the transistor 1113 is electrically connected to the pulse output circuit 111_n+1. The other of the source and the drain of the transistor 1113 is electrically connected to the other of the source and the drain of the transistor 1111 and the (n+1)th buffer 114. Note that the transfer signal (T) is a signal supplied to the transfer signal line 16 illustrated in FIG. 1A. The selector circuit 1110_2 can have a structure similar to that of the selector circuit 1110_1.

[0024]

FIG. 2C illustrates a configuration example of the buffer 114 illustrated in FIG. 2A. Simply put, the buffer 114 in FIG. 2C is a three-input OR gate. Note that as for the two high power supply potentials (VDD1 and VDD2) used in the buffer 114 in FIG. 2C, the high power supply potential (VDD2) is higher than the high power supply potential (VDD1).

[0025]

The buffer 114 in FIG. 2C includes a transistor 1141, a transistor 1142, a transistor 1143, a transistor 1144, a transistor 1145, and a transistor 1146. A gate and one of a source and a drain of the transistor 1141 are electrically connected to a wiring that supplies the high power supply potential (VDD1). A gate of the transistor 1142 is electrically connected to a first input terminal of the buffer 114. One of a source and a drain of the transistor 1142 is electrically connected to the other of the source and the drain of the transistor 1141. The other of the source and the drain of the transistor 1142 is electrically connected to a wiring that supplies the low power supply potential (VSS). A gate of the transistor 1143 is electrically connected to a second input

terminal of the buffer 114. One of a source and a drain of the transistor 1143 is electrically connected to the other of the source and the drain of the transistor 1141 and one of the source and the drain of the transistor 1142. The other of the source and the drain of the transistor 1143 is electrically connected to the wiring that supplies the low power supply potential (VSS). A gate of the transistor 1144 is electrically connected to a third input terminal of the buffer 114. One of a source and a drain of the transistor 1144 is electrically connected to the other of the source and the drain of the transistor 1141, one of the source and the drain of the transistor 1142, and one of the source and the drain of the transistor 1143. The other of the source and the drain of the transistor 1144 is electrically connected to the wiring that supplies the low power supply potential (VSS). A gate and one of a source and a drain of the transistor 1145 are electrically connected to a wiring that supplies the high power supply potential (VDD2). The other of the source and the drain of the transistor 1145 is electrically connected to the scan line 14. A gate of the transistor 1146 is electrically connected to the other of the source and the drain of the transistor 1141, one of the source and the drain of the transistor 1142, one of the source and the drain of the transistor 1143, and one of the source and the drain of the transistor 1144. One of a source and a drain of the transistor 1146 is electrically connected to the other of the source and the drain of the transistor 1145 and the scan line 14. The other of the source and the drain of the transistor 1146 is electrically connected to the wiring that supplies the low power supply potential (VSS).

[0026]

(Operation Example of Scan Line Driver Circuit 11)

An operation example of the scan line driver circuit 11 will be described with reference to FIG. 3. FIG. 3 shows the clock signal (GCK) for the scan line driver circuit, the transfer signal (T), signals (SR111out) output from the $3n$ output terminals of the shift register 111, signals (SR112out) output from the $3n$ output terminals of the shift register 112, signals (SR113out) output from the $3n$ output terminals of the shift register 113, and signals (GD11out) output from $3n$ output terminals of the scan line driver circuit.

[0027]

In a sampling period (T1), the transfer signal (T) has a low-level potential, so

that the potential of GD11out is set at high level when any of SR111out, SR112out, and SR113out has a high-level potential. Here, in the shift register 111, a high-level potential is sequentially shifted every 1/2 clock cycle (horizontal scan period) from the first-stage pulse output circuit 111_1 to the n -th-stage pulse output circuit 111_ n . In the shift register 112, a high-level potential is sequentially shifted every 1/2 clock cycle (horizontal scan period) from the $(n+1)$ th-stage pulse output circuit to the $2n$ -th-stage pulse output circuit. In the shift register 113, a high-level potential is sequentially shifted every 1/2 clock cycle (horizontal scan period) from the $(2n+1)$ th-stage pulse output circuit to the $3n$ -th-stage pulse output circuit. Thus, the scan line driver circuit 11 supplies selection signals to three different scan lines 14 depending on horizontal scan periods.

[0028]

In a transfer period (T2), the transfer signal (T) has a high-level potential (is a selection signal), so that all the potentials of GD11out are set at low level. Note that in the shift registers 111 to 113, the following operation needs to be performed: the shift of a selection signal is temporarily stopped in the transfer period (T2) and restarted in a sampling period (T3) subsequent to the transfer period (T2). In order to realize such operation in the shift registers 111 to 113, the shift registers are designed, for example, so that a pulse output circuit starts an output operation of a high-level potential in accordance with input of a high-level potential output from the previous-stage pulse output circuit, and stops in accordance with input of a high-level potential output from the subsequent-stage pulse output circuit.

[0029]

In the sampling period (T3), the transfer signal (T) has a low-level potential as in the sampling period (T1), so that the potential of GD11out is set at high level when any of SR111out, SR112out, and SR113out has a high-level potential. Here, although output signals of the shift registers 111 to 113 are different from those in the sampling period (T1), a combination of the output signals is the same as in the sampling period (T1). That is, in one of the shift registers 111 to 113 (the shift register 113 in the sampling period (T3)), a high-level potential is sequentially shifted every 1/2 clock cycle (horizontal scan period) from the first-stage pulse output circuit 111_1 to the

n -th-stage pulse output circuit 111 _{n} . In another one of the shift registers 111 to 113 (the shift register 111 in the sampling period (T3)), a high-level potential is sequentially shifted every 1/2 clock cycle (horizontal scan period) from the $(n+1)$ -th-stage pulse output circuit to the $2n$ -th-stage pulse output circuit. In the other of the shift registers 111 to 113 (the shift register 112 in the sampling period (T3)), a high-level potential is sequentially shifted every 1/2 clock cycle (horizontal scan period) from the $(2n+1)$ -th-stage pulse output circuit to the $3n$ -th-stage pulse output circuit. Thus, as in the sampling period (T1), the scan line driver circuit 11 supplies selection signals to three different scan lines 14 depending on horizontal scan periods.

[0030]

(Structural Example of Signal Line Driver Circuit 12)

FIG. 4A illustrates a structural example of the signal line driver circuit 12 included in the liquid crystal display device in FIG. 1A. The signal line driver circuit 12 in FIG. 4A includes a shift register 120 having m output terminals, m transistors 121, m transistors 122, and m transistors 123. A gate of the transistor 121 is electrically connected to the j -th output terminal (j is a natural number of 1 to m) of the shift register 120. One of a source and a drain of the transistor 121 is electrically connected to a wiring that supplies the first image signal (DATA1). The other of the source and the drain of the transistor 121 is electrically connected to the signal line 151 in the j -th column in the pixel portion 10. A gate of the transistor 122 is electrically connected to the j -th output terminal of the shift register 120. One of a source and a drain of the transistor 122 is electrically connected to a wiring that supplies the second image signal (DATA2). The other of the source and the drain of the transistor 122 is electrically connected to the signal line 152 in the j -th column in the pixel portion 10. A gate of the transistor 123 is electrically connected to the j -th output terminal of the shift register 120. One of a source and a drain of the transistor 123 is electrically connected to a wiring that supplies the third image signal (DATA3). The other of the source and the drain of the transistor 123 is electrically connected to the signal line 153 in the j -th column in the pixel portion 10.

[0031]

The first image signal (DATA1) is supplied to the signal line 151 through the

transistor 121. That is, the first image signal (DATA1) is an image signal for the region 101 in the pixel portion 10. Similarly, the second image signal (DATA2) is an image signal for the region 102 in the pixel portion 10, and the third image signal (DATA3) is an image signal for the region 103 in the pixel portion 10. Here, as the first image signal (DATA1), a red (R) image signal, a green (G) image signal, and a blue (B) image signal are supplied to the signal line 151 in the sampling period (T1), the sampling period (T3), and a sampling period (T5), respectively. As the second image signal (DATA2), a green (G) image signal, a blue (B) image signal, and a red (R) image signal are supplied to the signal line 152 in the sampling period (T1), the sampling period (T3), and the sampling period (T5), respectively. As the third image signal (DATA3), a blue (B) image signal, a red (R) image signal, and a green (G) image signal are supplied to the signal line 153 in the sampling period (T1), the sampling period (T3), and the sampling period (T5), respectively.

[0032]

FIG. 4B illustrates an operation example of the liquid crystal display device. FIG. 4B shows change over time in image signals written into the regions 101, 102, and 103 and lights supplied to the regions 101, 102, and 103. As illustrated in FIG. 4B, in the liquid crystal display device, writing of image signals and supply of light of a given color can be simultaneously performed in each region (each of the regions 101, 102, and 103). In the liquid crystal display device, one image is produced in the pixel portion 10 by the operations in the transfer period (T2) to a sampling period (T7). That is, in the liquid crystal display device, the period from the transfer period (T2) to the sampling period (T7) corresponds to one frame period.

[0033]

(Liquid Crystal Display Device disclosed in this Specification)

In the liquid crystal display device disclosed in this specification, a plurality of scan lines can be selected at the same time. That is, in the liquid crystal display device, image signals can be simultaneously supplied to pixels placed in a plurality of rows, among the pixels arranged in matrix. Thus, the frequency of input of an image signal to each pixel can be increased without change in response speed of a transistor or the like included in the liquid crystal display device. Specifically, in the liquid crystal display device, the frequency of input of an image signal to each pixel can be tripled

without change in clock frequency or the like of the scan line driver circuit. In other words, the liquid crystal display device is preferably applied to a liquid crystal display device in which images are displayed by a field sequential method or a liquid crystal display device driven by high frame rate driving.

5 [0034]

The liquid crystal display device disclosed in this specification is preferably applied to a liquid crystal display device in which images are displayed by a field sequential method because of the following reasons. As described above, in a liquid crystal display device in which images are displayed by a field sequential method, a display period is divided by lights of given colors. For that reason, display perceived by a user is sometimes changed (degraded) from display based on original display information (such a phenomenon is also referred to as color breaks) because of a lack of a given piece of display information due to temporary interruption of display, such as a blink of the user. An increase in frame frequency is effective in reducing color breaks. Further, in order to perform display by a field sequential method, the frequency of input of an image signal to each pixel needs to be higher than the frame frequency. For that reason, in the case where images are displayed with a field sequential method and high frame frequency driving in a conventional liquid crystal display device, requirements for performance (high-speed response) of elements in the liquid crystal display device are extremely strict. In contrast, in the liquid crystal display device disclosed in this specification, the frequency of input of an image signal to each pixel can be increased regardless of characteristics of elements. Therefore, color breaks in the liquid crystal display device in which images are displayed by a field sequential method can be easily reduced.

25 [0035]

In addition, in the case where display is performed by a field sequential method, it is preferable to supply lights of different colors depending on regions as illustrated in FIG. 4B because of the following reasons. In the case where light of one color is supplied for the entire screen, the pixel portion only has information on a specific color at a given moment. Therefore, a lack of display information in a given period due to a blink of the user or the like corresponds to a lack of information on a specific color. In contrast, in the case where lights of different colors are supplied depending on regions,

the pixel portion has information on the colors at a given moment. Therefore, a lack of display information in a given period due to a blink of the user or the like does not correspond to a lack of information on a specific color. In other words, color breaks can be reduced by supplying lights of different colors depending on regions.

5 [0036]

(Variations)

The liquid crystal display device having the above-described structure is one embodiment of the present invention; the present invention also includes a liquid crystal display device that is different from the liquid crystal display device.

10 [0037]

For example, the above-described liquid crystal display device has the structure in which the pixel portion 10 is divided into three regions (the regions 101, 102, and 103) (see FIG. 1A); however, the liquid crystal display device of the present invention is not limited to having this structure. That is, in the liquid crystal display device of the present invention, the pixel portion 10 can be divided into a given number of regions. Although obvious, it is to be noted that in the case where the number of regions is changed, it is necessary to provide signal lines, shift registers, and the like as many as the regions.

[0038]

20

In the liquid crystal display device, three kinds of light sources, each of which emits one of red (R) light, green (G) light, and blue (B) light, are used as a plurality of light sources; however, the liquid crystal display device of the present invention is not limited to having this structure. That is, in the liquid crystal display device of the present invention, light sources that emit lights of given colors can be used in combination. For example, it is possible to use a combination of four kinds of light sources that emit lights of red (R), green (G), blue (B), and white (W); or a combination of three kinds of light sources that emit lights of cyan, magenta, and yellow. Moreover, it is possible to use a combination of six kinds of light sources that emit lights of light red (R), light green (G), light blue (B), dark red (R), dark green (G), and dark blue (B); or a combination of six kinds of light sources that emit lights of red (R), green (G), blue (B), cyan, magenta, and yellow.

25
30

[0039]

The liquid crystal display device has the structure in which a capacitor for holding a voltage applied to the liquid crystal element is not provided (see FIGS. 1B to 1D); alternatively, the capacitor can be provided in the liquid crystal display device.

[0040]

5 Furthermore, the liquid crystal display device has the structure in which the transfer signal (T) is input to the selector circuit (see FIGS. 2A and 2B); alternatively, a signal input to the selector circuit may be a signal different from the transfer signal (T). Specifically, a signal input to the selector circuit can be any signal that has a high-level potential in a period including a period during which the potential of the transfer signal
10 (T) is set at high level.

[0041]

In addition, in the liquid crystal display device, a three-input OR gate is used as the buffer (see FIG. 2C); however, the buffer is not limited to having this structure. As the buffer 114 electrically connected to the scan line 14 placed in the region 101, a
15 circuit illustrated in FIG. 5A can be used, for example. The buffer 114 illustrated in FIG. 5A includes a transistor 1147, a transistor 1148, a transistor 1149, and a transistor 1150. A gate of the transistor 1147 is electrically connected to a wiring that supplies a signal (A). One of a source and a drain of the transistor 1147 is electrically connected to the shift register 111. The other of the source and the drain of the transistor 1147 is
20 electrically connected to the scan line 14. A gate of the transistor 1148 is electrically connected to a wiring that supplies a signal (B). One of a source and a drain of the transistor 1148 is electrically connected to the shift register 112. The other of the source and the drain of the transistor 1148 is electrically connected to the scan line 14. A gate of the transistor 1149 is electrically connected to a wiring that supplies a signal
25 (C). One of a source and a drain of the transistor 1149 is electrically connected to the shift register 113. The other of the source and the drain of the transistor 1149 is electrically connected to the scan line 14. A gate of the transistor 1150 is electrically connected to a wiring that supplies the transfer signal (T). One of a source and a drain of the transistor 1150 is electrically connected to a wiring that supplies the low power supply potential (VSS). The other of the source and the drain of the transistor 1150 is
30 electrically connected to the scan line 14. Note that the signal (A), the signal (B), and the signal (C) are signals whose potentials are changed as illustrated in FIG. 5B. A

combination of electrical connections between the gates of the transistors and the wirings that supply the signal (A), the signal (B), and the signal (C) is changed as appropriate in the circuit in FIG. 5A, whereby the circuit in FIG. 5A can be used as the buffer 114 that is electrically connected to the scan line 14 placed in the region 102, or the buffer 114 that is electrically connected to the scan line 14 placed in the region 103.

[0042]

(Example of Transistor)

A structural example of a transistor included in the liquid crystal display device will be described below with reference to FIG. 6. Note that in the liquid crystal display device, a transistor provided in the pixel portion 10 and a transistor provided in the scan line driver circuit 11 may have the same structure or different structures.

[0043]

A transistor 211 illustrated in FIG. 6 includes a gate layer 221 provided over a substrate 220 having an insulating surface, a gate insulating layer 222 provided over the gate layer 221, a semiconductor layer 223 provided over the gate insulating layer 222, and a source layer 224a and a drain layer 224b provided over the semiconductor layer 223. Moreover, FIG. 6 illustrates an insulating layer 225 that covers the transistor 211 and is in contact with the semiconductor layer 223, and a protective insulating layer 226 provided over the insulating layer 225.

[0044]

Examples of the substrate 220 are a semiconductor substrate (e.g., a single crystal substrate and a silicon substrate), an SOI substrate, a glass substrate, a quartz substrate, a conductive substrate having a surface on which an insulating layer is formed, and a flexible substrate such as a plastic substrate, a bonding film, paper containing a fibrous material, and a base film. Examples of a glass substrate are a barium borosilicate glass substrate, an aluminoborosilicate glass substrate, and a soda lime glass substrate. For a flexible substrate, a flexible synthetic resin such as plastics typified by polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polyether sulfone (PES), or acrylic can be used, for example.

[0045]

For the gate layer 221, an element selected from aluminum (Al), copper (Cu), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr),

neodymium (Nd), and scandium (Sc); an alloy containing any of these elements; or a nitride containing any of these elements can be used. Alternatively, the gate layer 221 can have a stacked structure of any of these materials.

[0046]

5 For the gate insulating layer 222, an insulator such as silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, or tantalum oxide can be used. A stacked structure of any of these materials can also be used. Note that silicon oxynitride refers to a material that contains more oxygen than nitrogen and contains oxygen, nitrogen, silicon, and hydrogen at given concentrations ranging from
10 55 to 65 atomic%, 1 to 20 atomic%, 25 to 35 atomic%, and 0.1 to 10 atomic%, respectively, where the total percentage of atoms is 100 atomic%. Further, silicon nitride oxide refers to a material that contains more nitrogen than oxygen and contains oxygen, nitrogen, silicon, and hydrogen at given concentrations ranging from 15 to 30 atomic%, 20 to 35 atomic%, 25 to 35 atomic%, and 15 to 25 atomic%, respectively,
15 where the total percentage of atoms is 100 atomic%.

[0047]

The semiconductor layer 223 can be formed using any of the following semiconductor materials, for example: a material containing an element belonging to Group 14 of the periodic table, such as silicon (Si) or germanium (Ge), as its main
20 component; a compound such as silicon germanium (SiGe) or gallium arsenide (GaAs); an oxide such as zinc oxide (ZnO) or zinc oxide containing indium (In) and gallium (Ga); or an organic compound exhibiting semiconductor characteristics. Alternatively, the semiconductor layer 223 can have a stacked structure of layers formed using any of these semiconductor materials.

25 [0048]

Moreover, in the case where an oxide (an oxide semiconductor) is used for the semiconductor layer 223, any of the following oxide semiconductors can be used: an In-Sn-Ga-Zn-O-based oxide semiconductor which is an oxide of four metal elements; an In-Ga-Zn-O-based oxide semiconductor, an In-Sn-Zn-O-based oxide semiconductor,
30 an In-Al-Zn-O-based oxide semiconductor, a Sn-Ga-Zn-O-based oxide semiconductor, an Al-Ga-Zn-O-based oxide semiconductor, and a Sn-Al-Zn-O-based oxide

semiconductor which are oxides of three metal elements; an In-Ga-O-based oxide, an In-Zn-O-based oxide semiconductor, a Sn-Zn-O-based oxide semiconductor, an Al-Zn-O-based oxide semiconductor, a Zn-Mg-O-based oxide semiconductor, a Sn-Mg-O-based oxide semiconductor, and an In-Mg-O-based oxide semiconductor which are oxides of two metal elements; and an In-O-based oxide semiconductor, a Sn-O-based oxide semiconductor, and a Zn-O-based oxide semiconductor which are oxides of one metal element. Further, SiO_2 may be contained in the above oxide semiconductor. Here, for example, an In-Ga-Zn-O-based oxide semiconductor is an oxide containing at least In, Ga, and Zn, and there is no particular limitation on the composition ratio of the elements. An In-Ga-Zn-O-based oxide semiconductor may contain an element other than In, Ga, and Zn.

[0049]

As the semiconductor layer 223, a thin film expressed by a chemical formula of $\text{InMO}_3(\text{ZnO})_m$ ($m > 0$) can be used. Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, M can be Ga, Ga and Al, Ga and Mn, or Ga and Co.

[0050]

In the case where an In-Zn-O-based material is used as an oxide semiconductor, a target to be used has a composition ratio of In:Zn = 50:1 to 1:2 in an atomic ratio (In_2O_3 : ZnO = 25:1 to 1:4 in a molar ratio), preferably In:Zn = 20:1 to 1:1 in an atomic ratio (In_2O_3 : ZnO = 10:1 to 1:2 in a molar ratio), further preferably In:Zn = 15:1 to 1.5:1 in an atomic ratio (In_2O_3 : ZnO = 15:2 to 3:4 in a molar ratio). For example, when a target used for forming an In-Zn-O-based oxide semiconductor has an atomic ratio of In:Zn:O = X : Y : Z , the relation of $Z > (1.5X+Y)$ is satisfied.

[0051]

For the source layer 224a and the drain layer 224b, an element selected from aluminum (Al), copper (Cu), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc); an alloy containing any of these elements; or a nitride containing any of these elements can be used. Alternatively, the source layer 224a and the drain layer 224b can have a stacked structure of any of these materials.

[0052]

A conductive film to be the source layer 224a and the drain layer 224b (including a wiring layer formed using the same layer as the source and drain layers) may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an alloy of indium oxide and tin oxide ($\text{In}_2\text{O}_3\text{-SnO}_2$, referred to as ITO), an alloy of indium oxide and zinc oxide ($\text{In}_2\text{O}_3\text{-ZnO}$), or any of these metal oxide materials containing silicon or silicon oxide can be used.

[0053]

For the insulating layer 225, an insulator such as silicon oxide, silicon oxynitride, aluminum oxide, or aluminum oxynitride can be used. A stacked structure of any of these materials can also be used.

[0054]

For the protective insulating layer 226, an insulator such as silicon nitride, aluminum nitride, silicon nitride oxide, or aluminum nitride oxide can be used. A stacked structure of any of these materials can also be used.

[0055]

A planarization insulating film may be formed over the protective insulating layer 226 in order to reduce surface roughness due to the transistor. The planarization insulating film can be formed using an organic material such as polyimide, acrylic, or benzocyclobutene. Other than such organic materials, it is possible to use a low-dielectric constant material (low-k material) or the like. Note that the planarization insulating film may be formed by stacking a plurality of insulating films formed from these materials.

[0056]

The liquid crystal display device disclosed in this specification can be formed using a transistor having the above-described structure. For example, a transistor including a semiconductor layer formed of amorphous silicon can be used in the pixel portion 10, and a transistor including a semiconductor layer formed of polycrystalline silicon or single crystal silicon can be used in the scan line driver circuit 11. Alternatively, a transistor including a semiconductor layer formed of an oxide semiconductor can be used in the pixel portion 10 and the scan line driver circuit 11.

In the case where transistors having the same structure are used in the pixel portion 10 and the scan line driver circuit 11, reduction in cost and increase in yield due to reduction in the number of manufacturing steps can be achieved.

[0057]

5 (Variations of Transistor)

FIG. 6 illustrates the transistor 211 with a bottom-gate structure called a channel-etch structure; however, the transistor provided in the liquid crystal display device is not limited to having this structure. Transistors illustrated in FIGS. 7A to 7C can be used, for example.

10 [0058]

A transistor 510 illustrated in FIG. 7A has a kind of bottom-gate structure called a channel-protective type (channel-stop type).

[0059]

15 The transistor 510 includes, over a substrate 220 having an insulating surface, a gate layer 221, a gate insulating layer 222, a semiconductor layer 223, an insulating layer 511 functioning as a channel protective layer that covers a channel formation region of the semiconductor layer 223, a source layer 224a, and a drain layer 224b. Moreover, a protective insulating layer 226 is formed to cover the source layer 224a, the drain layer 224b, and the insulating layer 511.

20 [0060]

As the insulating layer 511, an insulator such as silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, or tantalum oxide can be used. Alternatively, the insulating layer 511 can have a stacked structure of any of these materials.

25 [0061]

A transistor 520 illustrated in FIG. 7B is a bottom-gate transistor. The transistor 520 includes, over a substrate 220 having an insulating surface, a gate layer 221, a gate insulating layer 222, a source layer 224a, a drain layer 224b, and a semiconductor layer 223. Furthermore, an insulating layer 225 that covers the source layer 224a and the drain layer 224b and is in contact with the semiconductor layer 223 is provided. A protective insulating layer 226 is provided over the insulating layer 225.

30

[0062]

In the transistor 520, the gate insulating layer 222 is provided on and in contact with the substrate 220 and the gate layer 221, and the source layer 224a and the drain layer 224b are provided on and in contact with the gate insulating layer 222. Further, the semiconductor layer 223 is provided over the gate insulating layer 222, the source layer 224a, and the drain layer 224b.

[0063]

A transistor 530 illustrated in FIG. 7C is a kind of top-gate transistor. The transistor 530 includes, over a substrate 220 having an insulating surface, an insulating layer 531, a semiconductor layer 223, a source layer 224a and a drain layer 224b, a gate insulating layer 222, and a gate layer 221. A wiring layer 532a and a wiring layer 532b are provided in contact with the source layer 224a and the drain layer 224b, to be electrically connected to the source layer 224a and the drain layer 224b, respectively.

[0064]

As the insulating layer 531, an insulator such as silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, or tantalum oxide can be used. Alternatively, the insulating layer 531 can have a stacked structure of any of these materials.

[0065]

The wiring layers 532a and 532b can be formed using an element selected from aluminum (Al), copper (Cu), titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc); an alloy containing any of these elements; or a nitride containing any of these elements. Alternatively, the wiring layers 532a and 532b can have a stacked structure of any of these materials.

[0066]

(Various Electronic Devices including Display Device)

Examples of electronic devices including any of the display devices disclosed in this specification will be described below with reference to FIGS. 8A to 8F.

[0067]

FIG. 8A illustrates a notebook personal computer including a main body 2201, a housing 2202, a display portion 2203, a keyboard 2204, and the like.

[0068]

FIG. 8B illustrates a personal digital assistant (PDA). A main body 2211 is provided with a display portion 2213, an external interface 2215, operation buttons 2214, and the like. A stylus 2212 is provided as an accessory for operating the PDA.

[0069]

5 FIG. 8C illustrates an e-book reader 2220 as an example of electronic paper. The e-book reader 2220 includes two housings of a housing 2221 and a housing 2223. The housings 2221 and 2223 are united with an axis portion 2237, along which the e-book reader 2220 can be opened and closed. With such a structure, the e-book reader 2220 can be used like a paper book.

10 [0070]

A display portion 2225 is incorporated in the housing 2221, and a display portion 2227 is incorporated in the housing 2223. The display portion 2225 and the display portion 2227 may display one image or different images. In the case where the display portions 2225 and 2227 display different images, for example, the right display portion (the display portion 2225 in FIG. 8C) can display text and the left display portion (the display portion 2227 in FIG. 8C) can display pictures.

15 [0071]

Further, in FIG. 8C, the housing 2221 is provided with an operation portion and the like. For example, the housing 2221 is provided with a power switch 2231, an operation key 2233, and a speaker 2235. Pages can be turned with the operation key 2233. Note that a keyboard, a pointing device, or the like may also be provided on the surface of the housing, on which the display portion is provided. An external connection terminal (e.g., an earphone terminal, a USB terminal, or a terminal that can be connected to an AC adapter or various cables such as a USB cable), a recording medium insertion portion, and the like may be provided on the back surface or the side surface of the housing. Further, the e-book reader 2220 may have a function of an electronic dictionary.

20 [0072]

The e-book reader 2220 may be configured to transmit and receive data wirelessly. Through wireless communication, desired book data or the like can be purchased and downloaded from an e-book server.

25 [0073]

Note that electronic paper can be applied to devices in a variety of fields as long as they display data. For example, electronic paper can be used for posters, advertisement in vehicles such as trains, and display in a variety of cards such as credit cards in addition to e-book readers.

5 [0074]

FIG. 8D illustrates a mobile phone. The mobile phone includes two housings of a housing 2240 and a housing 2241. The housing 2241 is provided with a display panel 2242, a speaker 2243, a microphone 2244, a pointing device 2246, a camera lens 2247, an external connection terminal 2248, and the like. The housing 2240 is provided with a solar cell 2249 for charging the mobile phone, an external memory slot 2250, and the like. An antenna is incorporated in the housing 2241.

[0075]

The display panel 2242 has a touch panel function. In FIG. 8D, a plurality of operation keys 2245 displayed as images are shown by dashed lines. Note that the mobile phone includes a booster circuit for increasing a voltage output from the solar cell 2249 to a voltage needed for each circuit. Moreover, the mobile phone can include a contactless IC chip, a small recording device, or the like in addition to the above components.

[0076]

20 The display orientation of the display panel 2242 changes as appropriate in accordance with the application mode. Further, the camera lens 2247 is provided on the same surface as the display panel 2242, so that the mobile phone can be used as a video phone. The speaker 2243 and the microphone 2244 can be used for videophone calls, recording, playing sound, and the like as well as voice calls. The housings 2240 and 2241 which are unfolded as illustrated in FIG. 8D can slide so that one overlaps the other. Thus, the size of the mobile phone can be reduced, which makes the mobile phone suitable for being carried.

[0077]

30 The external connection terminal 2248 can be connected to an AC adapter or a variety of cables such as a USB cable, which enables charging of the mobile phone and data communication. Moreover, a larger amount of data can be saved and moved by inserting a recording medium to the external memory slot 2250. Further, the mobile

phone may have an infrared communication function, a television reception function, or the like in addition to the above functions.

[0078]

FIG. 8E illustrates a digital camera. The digital camera includes a main body
5 2261, a display portion (A) 2267, an eyepiece 2263, an operation switch 2264, a display
portion (B) 2265, a battery 2266, and the like.

[0079]

FIG. 8F illustrates a television set. In a television set 2270, a display portion
2273 is incorporated in a housing 2271. The display portion 2273 can display images.
10 Here, the housing 2271 is supported by a stand 2275.

[0080]

The television set 2270 can be operated by an operation switch of the housing
2271 or a separate remote controller 2280. With operation keys 2279 of the remote
controller 2280, channels and volume can be controlled and an image displayed on the
15 display portion 2273 can be controlled. Moreover, the remote controller 2280 may
have a display portion 2277 that displays data output from the remote controller 2280.

[0081]

Note that the television set 2270 is preferably provided with a receiver, a
modem, and the like. A general television broadcast can be received with the receiver.
20 Moreover, when the television set is connected to a communication network with or
without wires via the modem, one-way (from a sender to a receiver) or two-way
(between a sender and a receiver or between receivers) data communication can be
performed.

25 This application is based on Japanese Patent Application serial no.
2010-083480 filed with Japan Patent Office on March 31, 2010, the entire contents of
which are hereby incorporated by reference.

CLAIMS

1. A liquid crystal display device comprising:

a first signal line supplied with a first image signal in a horizontal scan period;

5 a second signal line supplied with a second image signal in the horizontal scan period;

a first scan line and a second scan line supplied with a selection signal in the horizontal scan period;

a first pixel electrically connected to the first signal line and the first scan line;

10 and

a second pixel electrically connected to the second signal line and the second scan line.

2. The liquid crystal display device according to claim 1, further comprising a

15 scan line driver circuit configured to control potentials of the first scan line and the second scan line,

wherein the scan line driver circuit includes:

a first shift register and a second shift register each having a first output terminal and a second output terminal;

20 a first OR gate having a first input terminal electrically connected to the first output terminal of the first shift register, a second input terminal electrically connected to the first output terminal of the second shift register, and an output terminal electrically connected to the first scan line; and

25 a second OR gate having a first input terminal electrically connected to the second output terminal of the first shift register, a second input terminal electrically connected to the second output terminal of the second shift register, and an output terminal electrically connected to the second scan line.

3. A liquid crystal display device comprising:

30 a first signal line supplied with a first image signal in a horizontal scan period;

a second signal line supplied with a second image signal in the horizontal scan period;

a first scan line and a second scan line supplied with a selection signal in the horizontal scan period;

a first pixel electrically connected to the first signal line and the first scan line;

5 a second pixel electrically connected to the second signal line and the second scan line; and

a transfer signal line supplied with a selection signal in a transfer period subsequent to the horizontal scan period, the transfer signal line being electrically connected to the first pixel and the second pixel.

10 4. The liquid crystal display device according to claim 3,
wherein the first pixel includes:

a first transistor having one of a source and a drain electrically connected to the first signal line, and a gate electrically connected to the first scan line;

15 a first capacitor having one of electrodes electrically connected to the other of the source and the drain of the first transistor, and the other of the electrodes electrically connected to a wiring supplying a capacitor potential;

a second transistor having one of a source and a drain electrically connected to the other of the source and the drain of the first transistor and one of the electrodes of the first capacitor, and a gate electrically connected to the transfer signal line; and

20 a first liquid crystal element having one of electrodes electrically connected to the other of the source and the drain of the second transistor, and the other of the electrodes electrically connected to a wiring supplying a counter potential, and

wherein the second pixel includes:

25 a third transistor having one of a source and a drain electrically connected to the second signal line, and a gate electrically connected to the second scan line;

a second capacitor having one of electrodes electrically connected to the other of the source and the drain of the third transistor, and the other of the electrodes electrically connected to the wiring supplying the capacitor potential;

30 a fourth transistor having one of a source and a drain electrically connected to the other of the source and the drain of the third transistor and one of the electrodes of the second capacitor, and a gate electrically connected to the transfer signal line; and

a second liquid crystal element having one of electrodes electrically connected

to the other of the source and the drain of the fourth transistor, and the other of the electrodes electrically connected to the wiring supplying the counter potential.

5 5. The liquid crystal display device according to claim 3, further comprising a scan line driver circuit configured to control potentials of the first scan line and the second scan line,

wherein the scan line driver circuit includes:

a first shift register and a second shift register each having a first output terminal and a second output terminal;

10 a first OR gate having a first input terminal electrically connected to the first output terminal of the first shift register, a second input terminal electrically connected to the first output terminal of the second shift register, and an output terminal electrically connected to the first scan line; and

15 a second OR gate having a first input terminal electrically connected to the second output terminal of the first shift register, a second input terminal electrically connected to the second output terminal of the second shift register, and an output terminal electrically connected to the second scan line.

6. A liquid crystal display device comprising:

20 a plurality of pixels arranged in kn rows and m columns (k , n , and m are each a natural number);

m number of first signal lines supplied with a first image signal in a horizontal scan period to m number of k -th signal lines supplied with a k -th image signal in the horizontal scan period; and

25 first to k -th scan lines supplied with a selection signal in the horizontal scan period,

wherein a plurality of pixels arranged in the $(jn+1)$ th to $(j+1)n$ -th rows (j is an integer of 0 or more and less than k) among the plurality of pixels are electrically connected to the $(j+1)$ th scan line and any one of the m number of $(j+1)$ th signal lines.

30 7. The liquid crystal display device according to claim 6, further comprising a

scan line driver circuit configured to control potentials of the first to k -th scan lines,

wherein the scan line driver circuit includes first to k -th shift registers each having first to k -th output terminals, and first to k -th OR gates, and

5 wherein the $(j+1)$ th OR gate has first to k -th input terminals electrically connected to the $(j+1)$ th output terminals of the first to k -th shift registers, respectively, and an output terminal electrically connected to the $(j+1)$ th scan line.

8. A liquid crystal display device comprising:

10 a plurality of pixels arranged in kn rows and m columns (k , n , and m are each a natural number);

m number of first signal lines supplied with a first image signal in a horizontal scan period to m number of k -th signal lines supplied with a k -th image signal in the horizontal scan period;

15 first to k -th scan lines supplied with a selection signal in the horizontal scan period; and

a transfer signal line supplied with a selection signal in a transfer period subsequent to the horizontal scan period, the transfer signal line being electrically connected to all the plurality of pixels arranged in the kn rows and the m columns,

20 wherein a plurality of pixels arranged in the $(jn+1)$ th to $(j+1)n$ -th rows (j is an integer of 0 or more and less than k) among the plurality of pixels are electrically connected to the $(j+1)$ th scan line and any one of the m number of $(j+1)$ th signal lines.

9. The liquid crystal display device according to claim 8,

25 wherein each of the plurality of pixels arranged in the $(jn+1)$ th to $(j+1)n$ -th rows includes:

a first transistor having one of a source and a drain electrically connected to the m number of $(j+1)$ th signal lines, and a gate electrically connected to the $(j+1)$ th scan line;

30 a first capacitor having one of electrodes electrically connected to the other of the source and the drain of the first transistor, and the other of the electrodes electrically connected to a wiring supplying a capacitor potential;

a second transistor having one of a source and a drain electrically connected to the other of the source and the drain of the first transistor and one of the electrodes of the first capacitor, and a gate electrically connected to the transfer signal line; and

5 a first liquid crystal element having one of electrodes electrically connected to the other of the source and the drain of the second transistor, and the other of the electrodes electrically connected to a wiring supplying a counter potential.

10. The liquid crystal display device according to claim 8, further comprising a scan line driver circuit configured to control potentials of the first to k -th scan lines,

10 wherein the scan line driver circuit includes first to k -th shift registers each having first to k -th output terminals, and first to k -th OR gates, and

wherein the $(j+1)$ th OR gate has first to k -th input terminals electrically connected to the $(j+1)$ th output terminals of the first to k -th shift registers, respectively, and an output terminal electrically connected to the $(j+1)$ th scan line.

15

11. A method for driving a liquid crystal display device including a matrix of pixels each including a first transistor controlling input of an image signal, a capacitor holding the image signal, and a second transistor transferring the image signal held at the capacitor to a liquid crystal element, the method comprising the steps of:

20 in a first sampling period, shifting a selection signal sequentially from first to n -th scan lines (n is a natural number of 2 or more) so that a first image signal is input to a first pixel, and shifting a selection signal sequentially from $(n+1)$ th to $2n$ -th scan lines so that a second image signal is input to a second pixel;

25 in a transfer period subsequent to the first sampling period, by inputting a transfer signal to the first pixel and the second pixel, applying a voltage based on the first image signal to a first liquid crystal element included in the first pixel and applying a voltage based on the second image signal to a second liquid crystal element included in the second pixel; and

30 in a second sampling period subsequent to the transfer period, shifting a selection signal sequentially from the first to n -th scan lines so that a third image signal is input to the first pixel, and shifting a selection signal sequentially from the $(n+1)$ th to

2*n*-th scan lines so that a fourth image signal is input to the second pixel; and controlling transmission of light emitted from a light source for the first image signal in the first pixel, and controlling transmission of light emitted from a light source for the second image signal in the second pixel.

5

12. The method for driving a liquid crystal display device, according to claim 11, wherein a color of the light emitted from the light source for the first image signal and a color of the light emitted from the light source for the second image signal are different from each other.

10

1/10

FIG. 1A

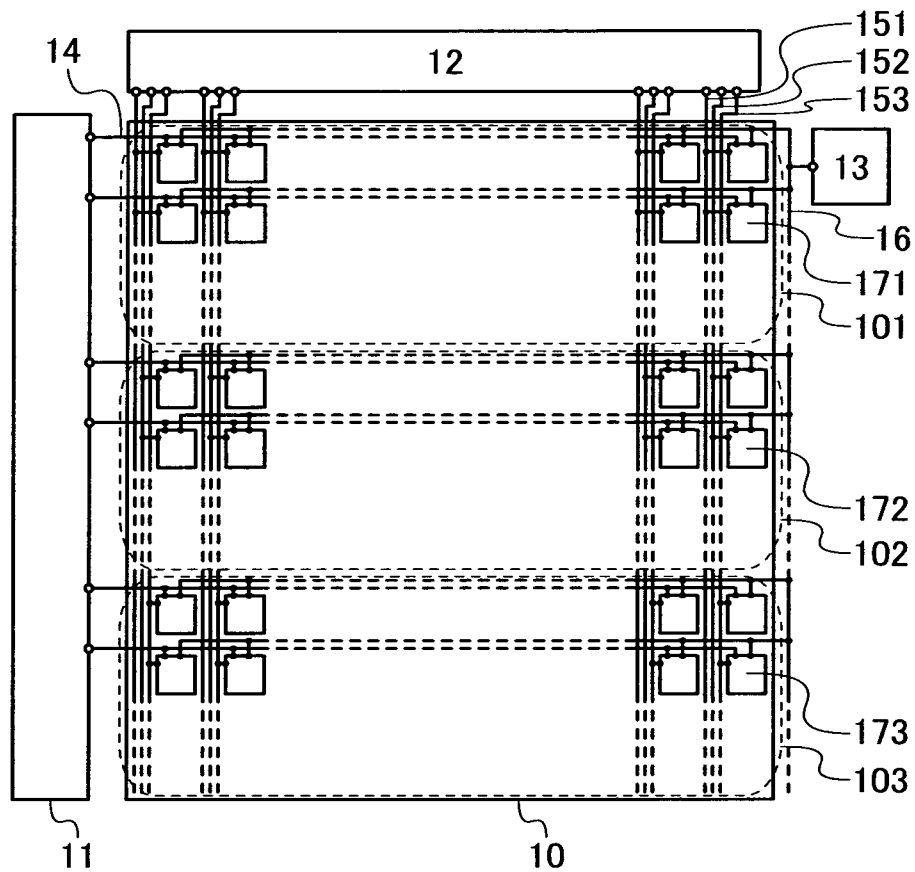


FIG. 1B

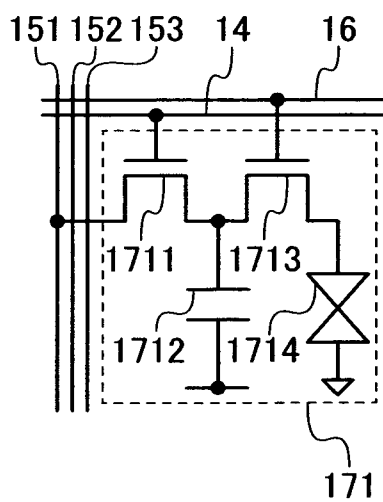


FIG. 1C

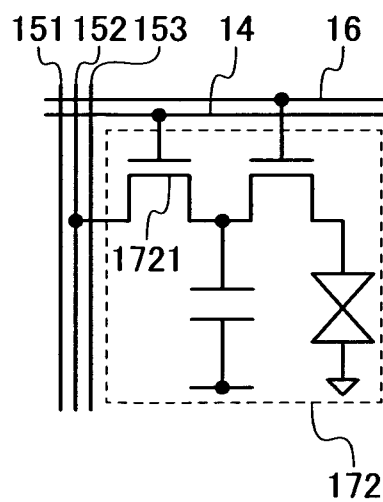


FIG. 1D

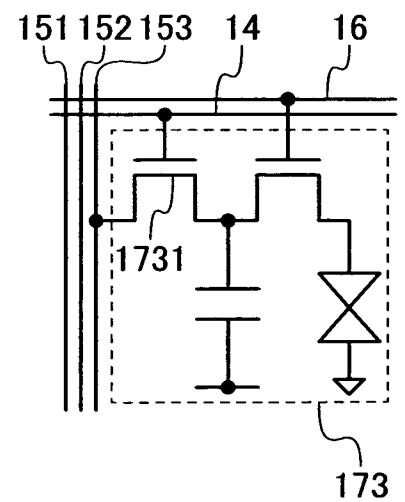


FIG. 2A

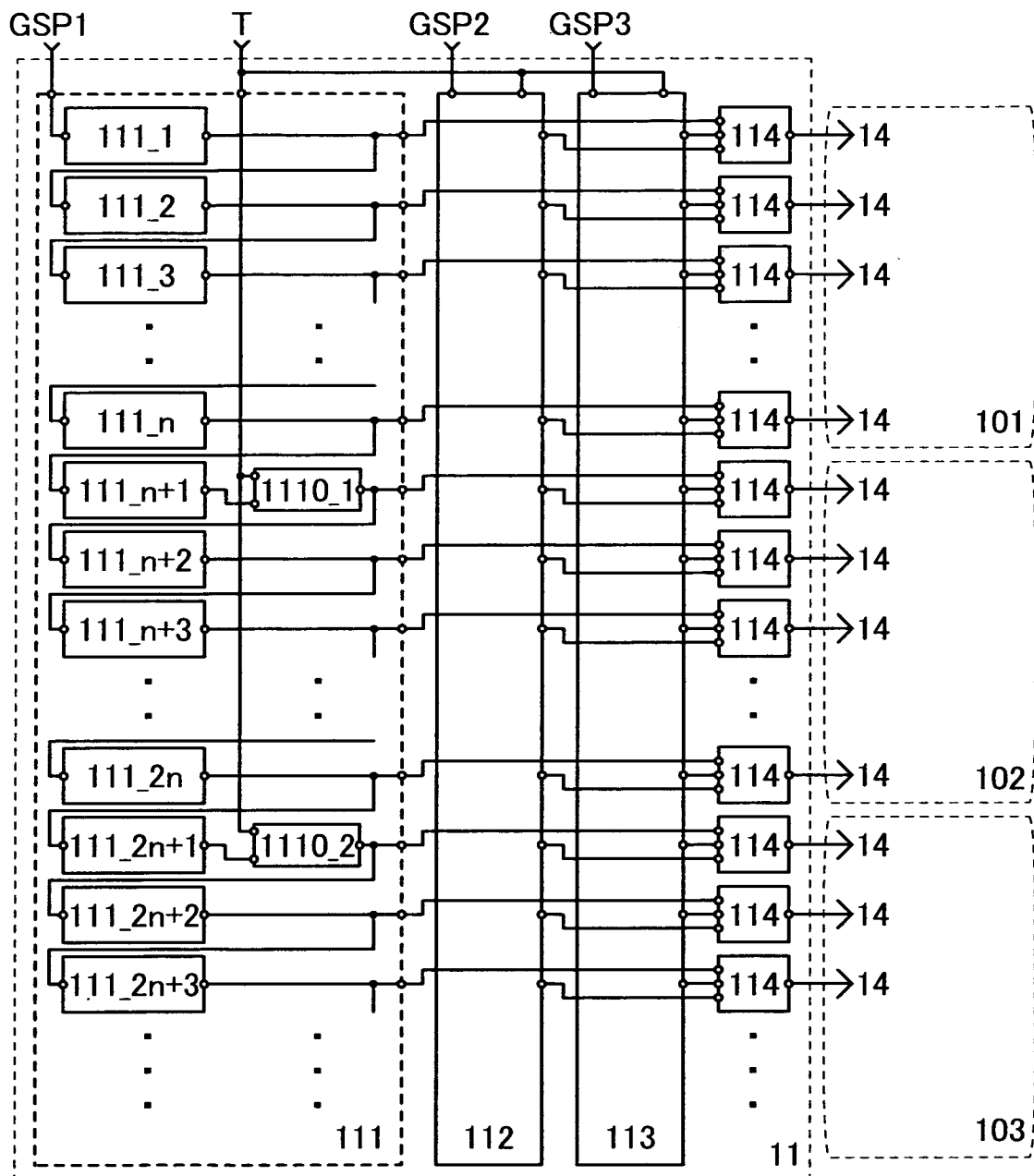


FIG. 2B

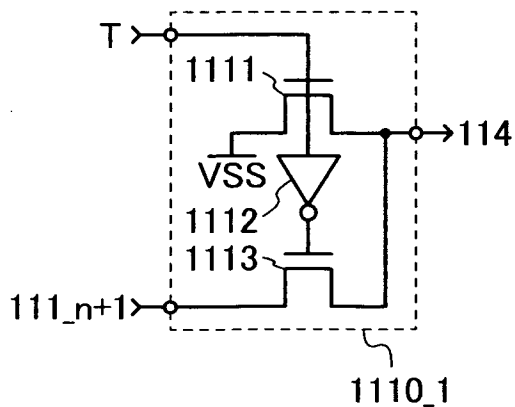


FIG. 2C

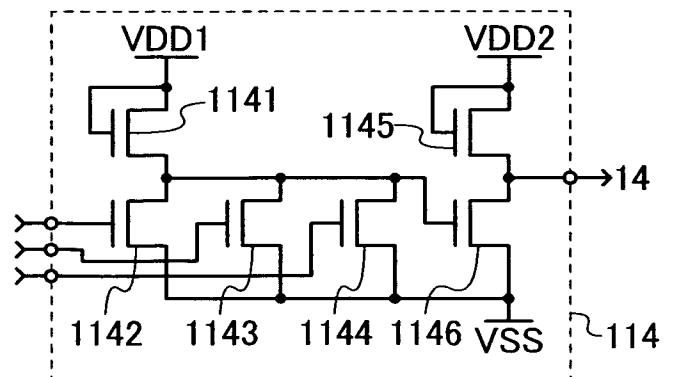
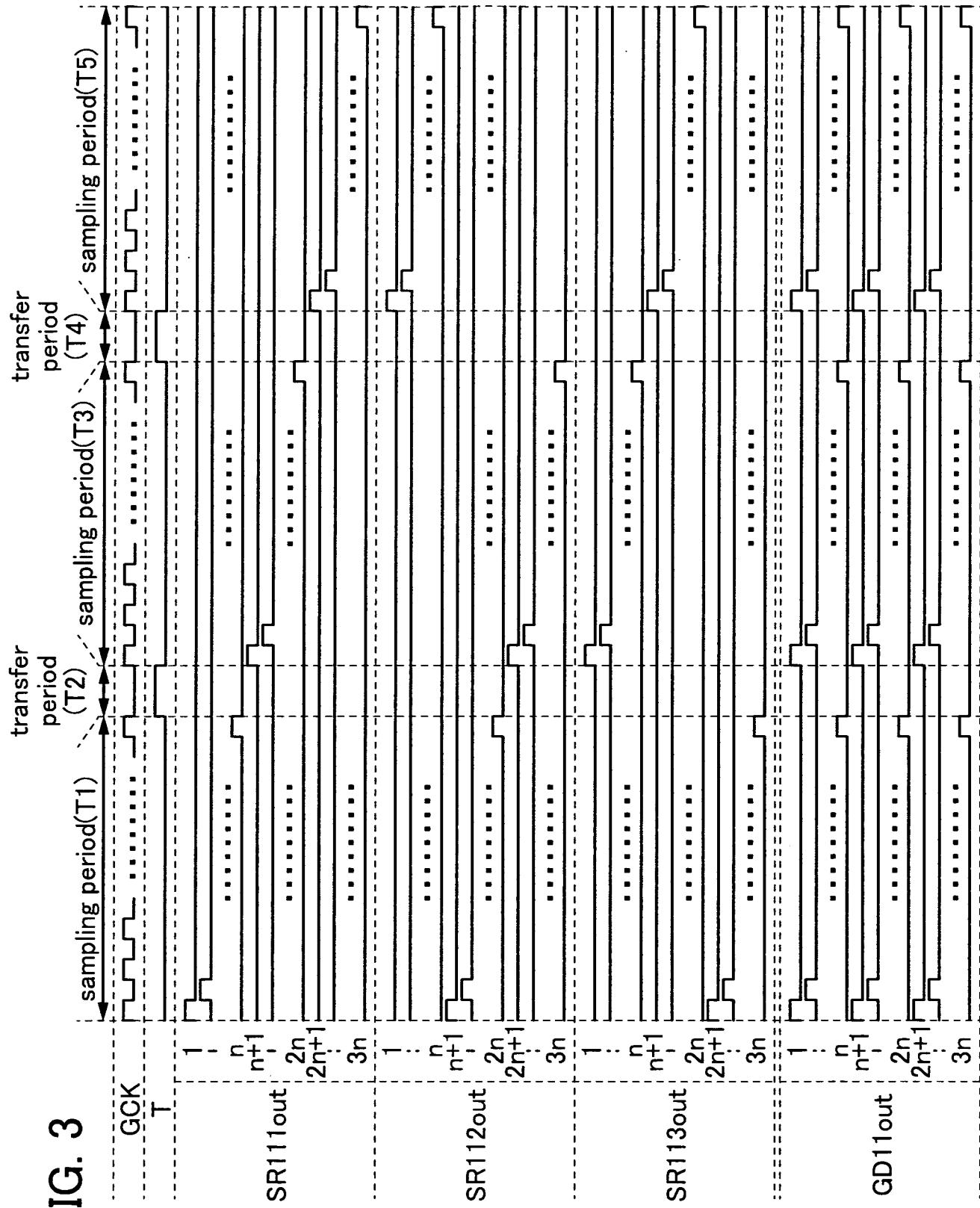


FIG. 3



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FIG. 4A

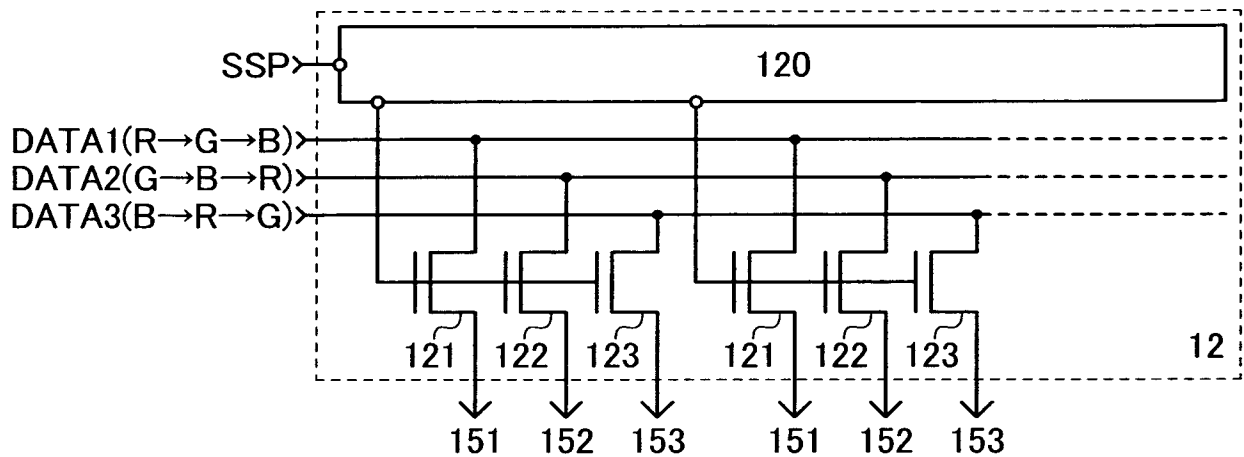


FIG. 4B

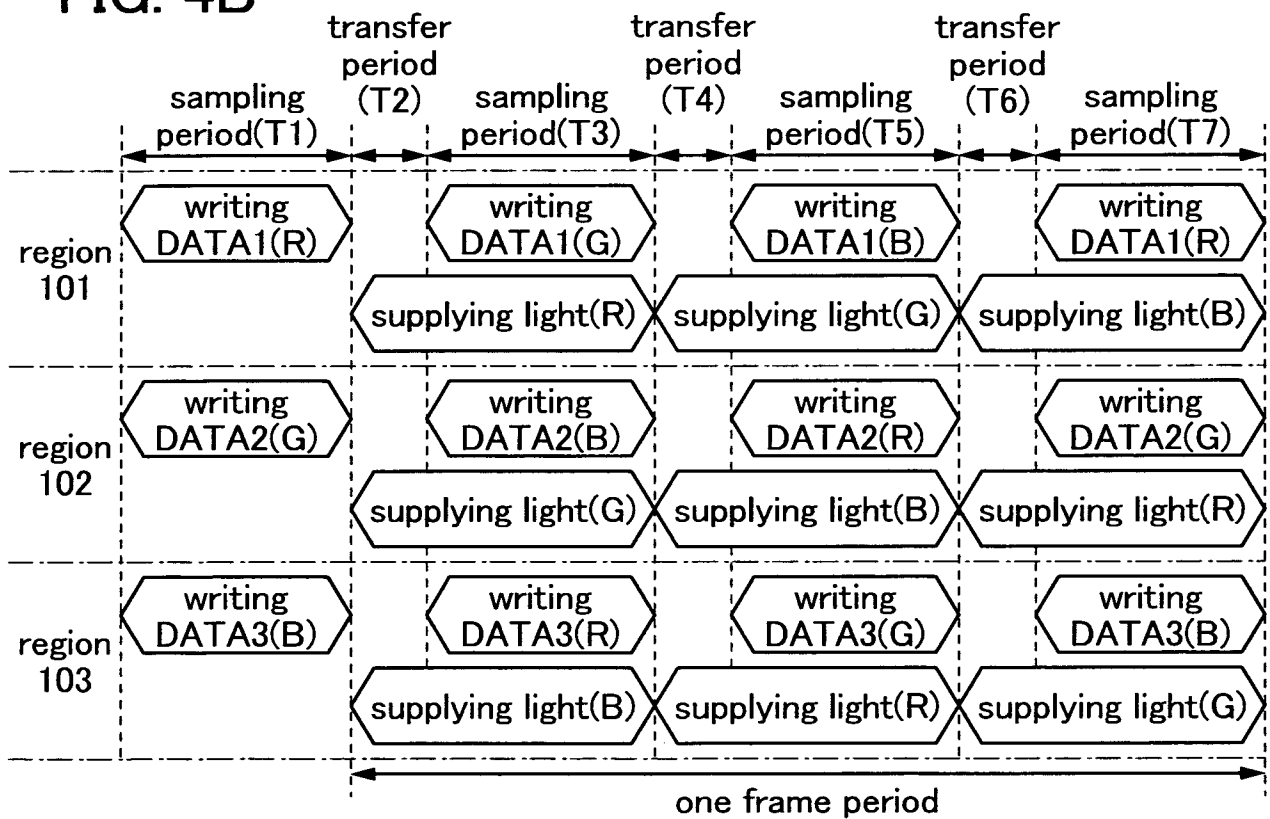


FIG. 5A

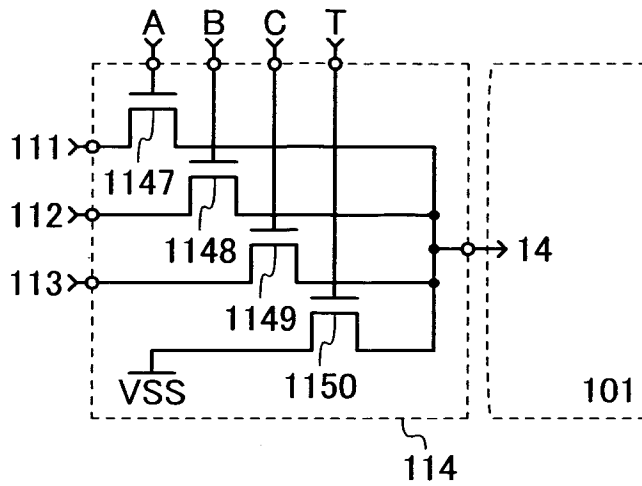
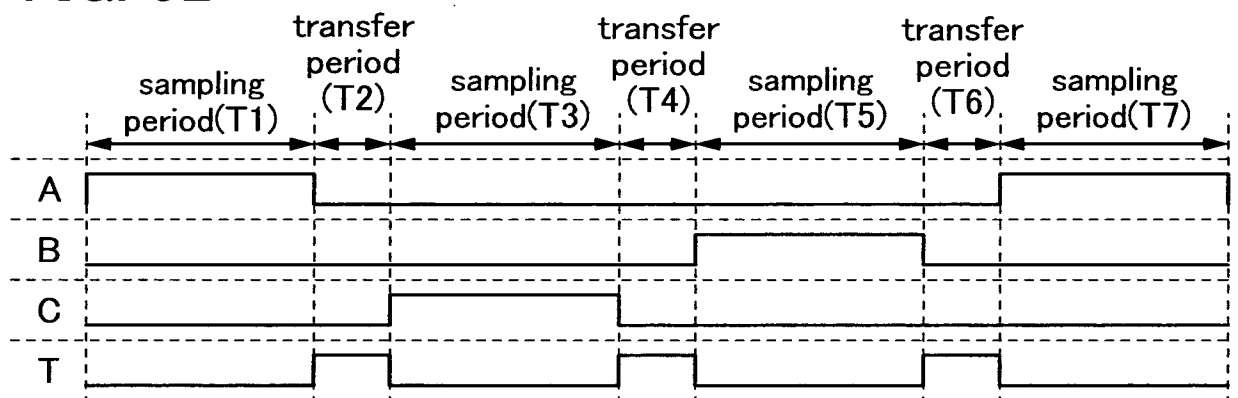
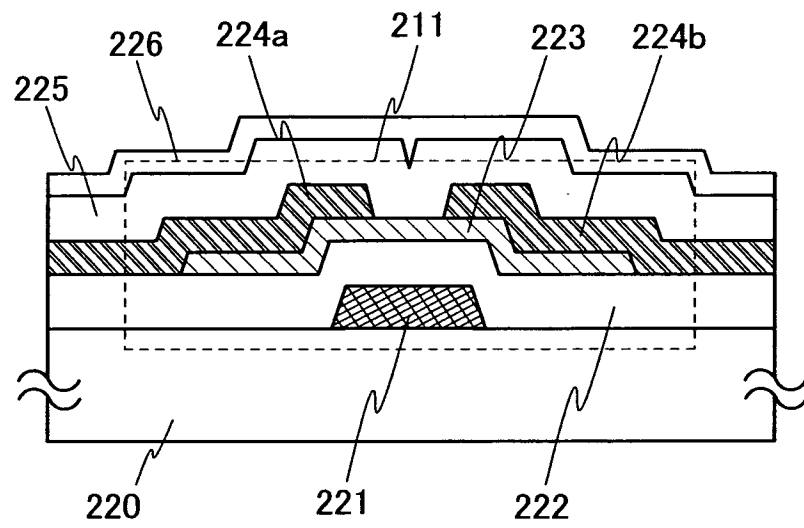


FIG. 5B



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FIG. 6



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FIG. 7A

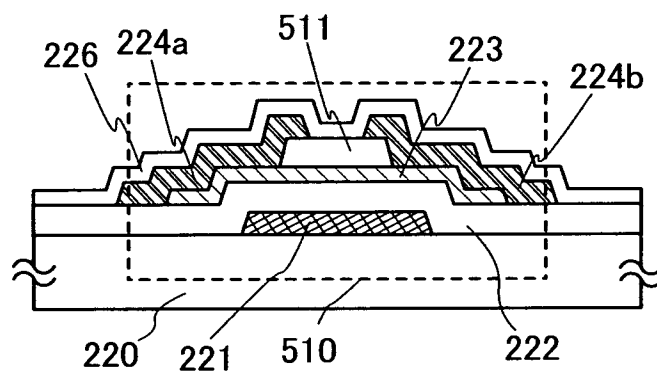


FIG. 7B

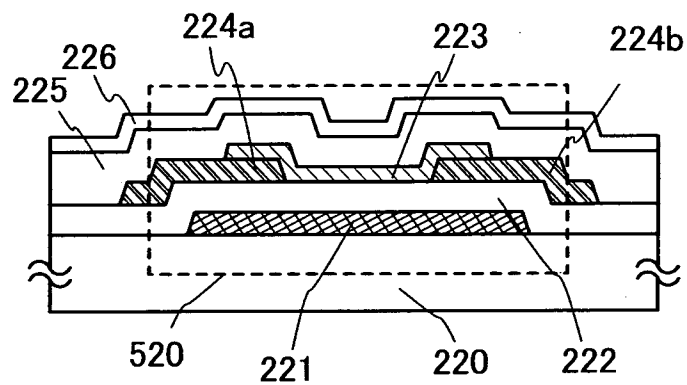


FIG. 7C

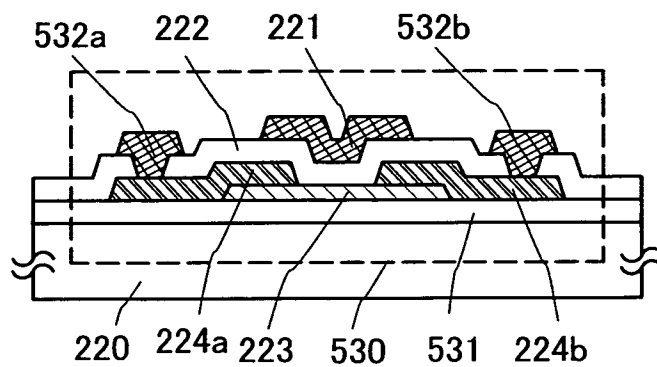


FIG. 8A

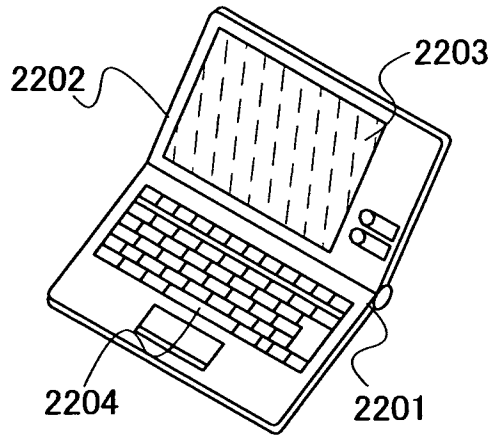


FIG. 8B

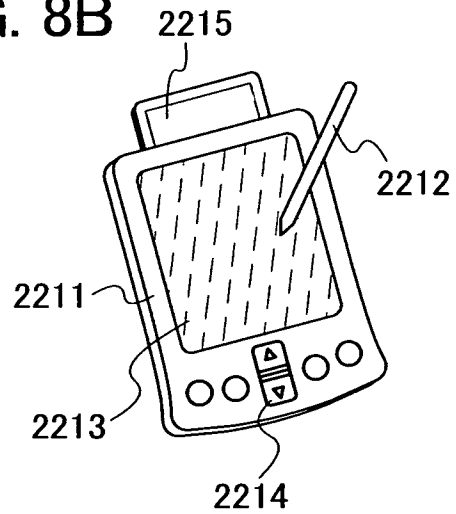


FIG. 8C

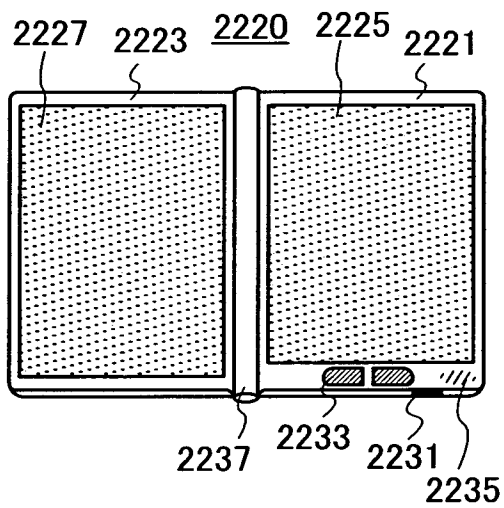


FIG. 8D

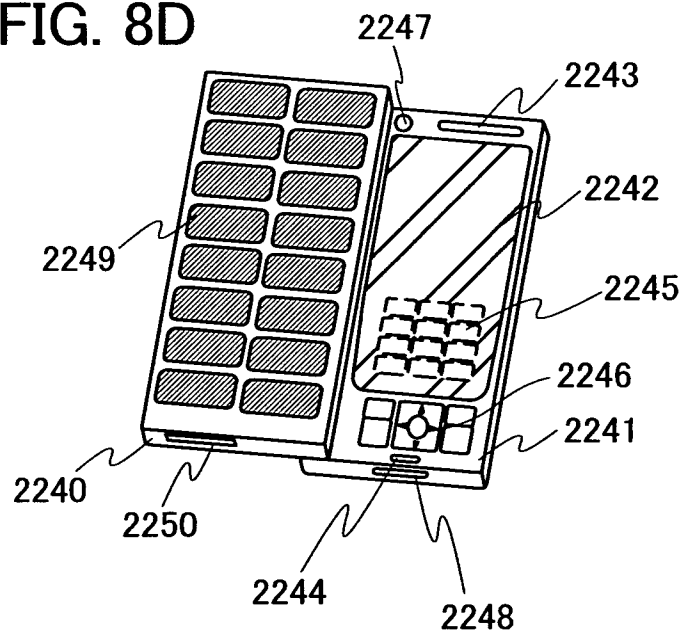


FIG. 8E

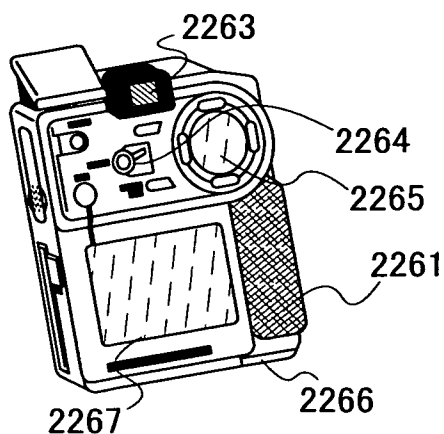
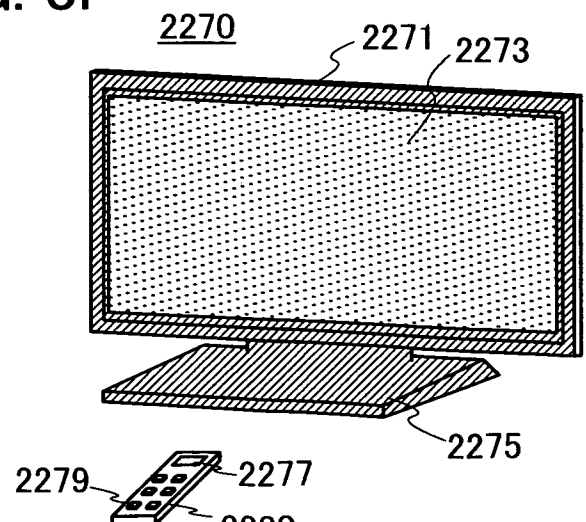


FIG. 8F



EXPLANATION OF REFERENCE

10: pixel portion, 11: scan line driver circuit, 12: signal line driver circuit, 13: transfer signal line driver circuit, 14: scan line, 16: transfer signal line, 101: region, 102: region, 103: region, 111: shift register, 111_1 to 111_3n: pulse output circuit, 112: shift register, 113: shift register, 114: buffer, 120: shift register, 121: transistor, 122: transistor, 123: transistor, 151: signal line, 152: signal line, 153: signal line, 171: pixel, 172: pixel, 173: pixel, 211: transistor, 220: substrate, 221: gate layer, 222: gate insulating layer, 223: semiconductor layer, 224a: source layer, 224b: drain layer, 225: insulating layer, 226: protective insulating layer, 510: transistor, 511: insulating layer, 520: transistor, 530: transistor, 531: insulating layer, 532a: wiring layer, 532b: wiring layer, 1110_1: selector circuit, 1110_2: selector circuit, 1111: transistor, 1112: inverter, 1113: transistor, 1141: transistor, 1142: transistor, 1143: transistor, 1144: transistor, 1145: transistor, 1146: transistor, 1147: transistor, 1148: transistor, 1149: transistor, 1150: transistor, 1711: transistor, 1712: capacitor, 1713: transistor, 1714: liquid crystal element, 1721: transistor, 1731: transistor, 2201: main body, 2202: housing, 2203: display portion, 2204: keyboard, 2211: main body, 2212: stylus, 2213: display portion, 2214: operation button, 2215: external interface, 2220: e-book reader 2221: housing, 2223: housing, 2225: display portion, 2227: display portion, 2231: power switch, 2233: operation key, 2235: speaker, 2237: axis portion, 2240: housing, 2241: housing, 2242: display panel, 2243: speaker, 2244: microphone, 2245: operation key, 2246: pointing device,

2247: camera lens, 2248: external connection terminal, 2249: solar cell, 2250: external memory slot, 2261: main body, 2263: eyepiece, 2264: operation switch, 2265: display portion (B), 2266: battery, 2267: display portion (A), 2270: television set, 2271: housing, 2273: display portion, 2275: stand, 2277: display portion, 2279: operation key, 2280: remote controller

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/055859

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. G02F1/1368 (2006.01) i, G02F1/133 (2006.01) i, G09G3/20 (2006.01) i,
G09G3/36 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. G02F1/1368, G02F1/133, G09G3/20, G09G3/36

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	JP 7-333574 A (Kashio Keisanki Co., Ltd.) 1995.12.22 Full text; all drawings (Family:none)	1, 6 3-4, 8-9, 11-12 2, 5, 7, 10
X Y A	JP 11-258573 A (NEC Corporation) 1999.09.24 Full text; all drawings & US 2005-225545 A1	1, 6 3-4, 8-9, 11 2, 5, 7, 10
Y	JP 61-281692 A (Oy Lohja Ab) 1986.12.12 Full text; all drawings & US 4907862 A & GB 2172733 A & DE 3606404 A1 & FR 2578705 A1	3-4, 8-9, 11-12



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

24.03.2011

Date of mailing of the international search report

14.06.2011

Name and mailing address of the ISA/JP

Japan Patent Office

3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/055859

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 8-95526 A (Kashio Keisanki Co., Ltd.) 1996.04.12 Full text; all drawings (Family:none)	3-4, 8-9, 11-12
Y	JP 11-295694 A (Hoshiden Philips Display Co., Ltd.) 1999.10.29 Full text; all drawings (Family:none)	3-4, 8-9, 11-12

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/055859

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

The subject matter of claim 1 does not meet the requirement of novelty for JP 7-333574 A(Kashio Keisanki Co., Ltd.) 1995.12.22 ([0028], Fig. 3, 8) and JP 11-258573 A(NEC Corporation) 1999.09.24 ([0025]-[0027], Fig. 7-8).

Claim 1 does not the "special technical features".

There are two inventions.

(Invention 1) Claim 1-2, 6-7

(Invention 2) Claim 3-5, 8-12

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.