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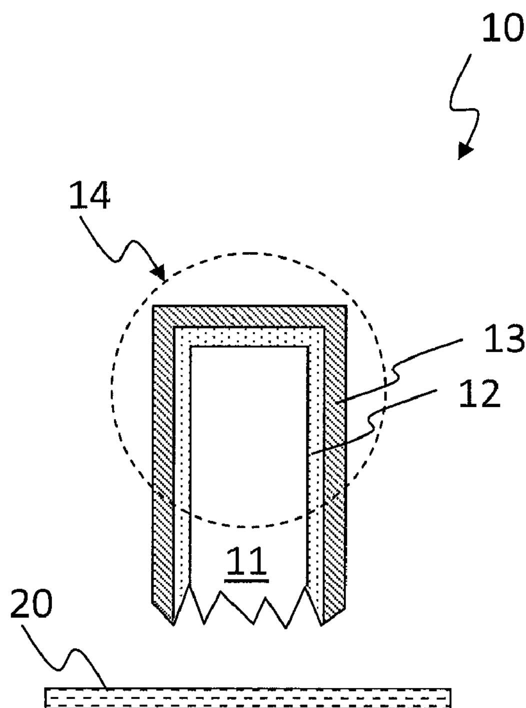

Fig. 1A

(57) **Abstract**: Described herein is a device comprising: a substrate; one or more of a nanostructure extending essentially perpendicularly from the substrate; wherein the nanostructure comprises a core of a doped semiconductor, an first layer disposed on the core, and a second layer of an opposite type from the core and disposed on the first layer.

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PASSIVATED UPSTANDING NANOSTRUCTURES AND METHODS OF MAKING THE SAME

Cross-reference to related applications

[0001] This application is related to U.S. Patent Application Serial Nos. 61/266,064, 61/357,429, 61/360,421, 12/204,686 (granted as U.S. Pat. No. 7,646,943), 12/270,233, 12/472,264, 12/472,271, 12/478,598, 12/633,297, 12/621,497, 12/648,942, 12/910,664, 12/966,514, 12/573,582, 12/575,221, 12/633,323, 12/633,318, 12/633,313, 12/633,305, 12/982,269, 12/966,573, 12/967,880, 12/974,499, 12/945,492, 13/047,392, 13/048,635 and 12/966,535, and the disclosures each of which are hereby incorporated by reference in their entirety.

Background

[0002] Semiconductor surface is often a source of defects that adversely affect the electric, optical and chemical properties of the semiconductor. A suitable passivation technique eliminates the defects or prevent the adverse effects of the defects.

Summary

[0003] Described herein is a device comprising: a substrate; one or more of a nanostructure extending essentially perpendicularly from the substrate; wherein the nanostructure comprises a core of a doped semiconductor, an intrinsic amorphous semiconductor layer disposed on the core, and a heavily doped amorphous semiconductor layer of an opposite type from the core and disposed on the intrinsic amorphous semiconductor layer.

[0004] Also described herein is a device comprising: a substrate; one or more of a nanostructure extending essentially perpendicularly from the substrate; wherein the nanostructure comprises a core and a passivation layer, the passivation layer comprising an amorphous material, configured to passivate at least a surface of the core and configured to form a p-i-n junction with the core.

Brief Description Of the Figures

[0005] Figs. 1A-1C each show a partial cross-sectional view of a nanostructure.

[0006] Fig. S1A shows a nanostructure on a substrate.

[0007] Fig. S1B shows simulated absorptance of the nanostructure of Fig. S1A.

[0008] Fig. S1C shows optional couplers on the nanostructure.

[0009] Fig. S2A and S2B show a perspective view and a top view of an image sensor according an embodiment.

[0010] Fig. S9 shows a block diagram of a solar-blind image sensor.

[0011] Fig. S10 shows a schematic of the SBUV detector being used as fore optics.

[0012] Fig. P1 is a perspective view of the device according one embodiment.

[0013] Fig. P2 shows a schematic of nanostructures in one subpixel when light with different polarization impinges thereon.

[0014] Fig. P10 shows a polarization detector array.

[0015] Fig. P12 shows a top view and a perspective view of a nanostructure in the device of Fig. P1, wherein the feature has metal layers on its sidewalls.

[0016] Fig. V2A is a schematic cross sectional view of a photovoltaic device according to an embodiment.

[0017] Fig. V5 shows a schematic of light concentration in the structures of the photovoltaic device.

[0018] Fig. V6 shows an exemplary top cross sectional view of the photovoltaic device.

[0019] Fig. V7 shows an exemplary perspective view of the photovoltaic device.

[0020] Fig. V8B shows schematics of drawing electrical current from the photovoltaic device of Fig. V2A.

[0021] Fig. V9 shows an alternative stripe-shaped structures of the photovoltaic device.

[0022] Fig. V10 shows an alternative mesh-shaped structures of the photovoltaic device.

[0023] Fig. W2A is a schematic cross sectional view of a photovoltaic device according to an embodiment.

[0024] Fig. W5 shows a schematic of light concentration in the structures of the photovoltaic device.

[0025] Fig. W11A and Fig. W11B show a process of making vias.

[0026] Fig. W12A and Fig. W12B show top views of exemplary vias.

[0027] Fig. W8B shows schematics of drawing electrical current from the photovoltaic device of Fig. W2A.

[0028] Figs. S4 and S5 show an apparatus comprising the image sensor, according to an embodiment.

[0029] Fig. S6 shows another apparatus comprising the image sensor, according to an embodiment.

[0030] Figs. S7A and S7B show schematics of a pixel of the image sensor, the pixel having more than one nanopillar sized to absorb and/or detect light of different wavelength or color, according to embodiments.

[0031] Fig. F1A shows a schematic cross-sectional view of an image sensor according to an embodiment.

[0032] Fig. F1B shows a schematic top view of the image sensor of Fig. F1A.

[0033] Fig. F1C shows exemplary absorption spectra of two nanowires in two subpixels in a pixel of the image sensor of Fig. F1A and a photodiode on the substrate of the image sensor of Fig. F1A.

[0034] Fig. F2A shows a schematic cross-sectional view of an image sensor according to an embodiment.

[0035] Fig. F2B shows a schematic top view of the image sensor of Fig. F2A.

[0036] Fig. F2C shows exemplary absorption spectra of three nanowires in three subpixels in a pixel of the image sensor of Fig. F2A and the substrate of the image sensor of Fig. F2A.

[0037] Fig. F2D shows exemplary absorption spectra of four nanowires in four subpixels in a pixel of the image sensor of Fig. F2A and the substrate of the image sensor of Fig. F2A.

[0038] Fig. F3 shows a schematic of couplers and an infrared filter.

[0039] Fig. F4 shows exemplary color-matching functions of three subpixels in the image sensor, and color-matching functions the CIE standard observer.

[0040] Fig. D2 illustrates a simplified cross sectional view of an embodiment of a pixel with a nanowire structured photodetector with front side illumination.

[0041] FIG. D2b illustrates an aspect of the embodiment illustrated in Fig. D2 with a binary microlens on the NW structured photodetector.

[0042] Fig. D3 illustrates simplified cross section view of an embodiment of a pixel with a nanowire structured photodetector with backside illumination.

[0043] Fig. D4 illustrates an embodiment having a CMOS pixel with a nanowire and a vertical photogate (VPG).

[0044] Fig. D5b, illustrates a potential profile of an embodiment.

[0045] Fig. D8 illustrates a cross section view of an embodiment with a dual photodiode structure in which the p doped NW is coated with an n+ epitaxial layer to form a p-n junction.

[0046] Fig. D9 illustrates an embodiment of a CMOS pixel with a nanowire structured photogate detector.

[0047] Fig. D10 illustrates an embodiment of a CMOS active pixel with nanowire structured p-i-n photodiodes and vertical photogates around the NW.

[0048] Fig. D11 illustrates another embodiment of a CMOS active pixel with nanowire structured p-i-n photodiodes and vertical photogates around the NW.

[0049] Fig. D12 illustrates an embodiments of a back-side illuminated image sensor.

[0050] Fig. D13 illustrates an embodiments of another back-side illuminated image sensor.

[0051] Figs. D23C and D23D show illustrative embodiments of a cross-sectional view of a waveguide structure, such as a nanowire, containing backside-illuminated image sensor with nanowires located on the backside of the image sensor.

Detailed Description

[0052] The terms “passivation” and “passivate” as used herein means a process of eliminating dangling bonds (i.e., unsatisfied valence on immobilized atoms). The term “image sensor” as used herein means a device that converts an optical image to an electric signal. The term “color image sensor” as used herein means an image sensor capable of converting an optical image in the visible spectrum (i.e. a color image) to an electric signal. The term “transparent” as used herein means a transmittance of at least 70%. The term “polarized light” as used herein means light with polarization. “Linear polarization” as used herein means the electric field of light is confined to a given plane along the direction of propagation of the light. “Circular polarization” as used herein means the electric field of light does not change strength but only changes direction in a rotary type manner. “Elliptical polarization” as used herein means electric field of light describes an ellipse in any fixed plane intersecting, and normal to, the direction of propagation of the light. The term “photovoltaic device” as used herein means a device that can generate electrical power by converting light such as solar radiation into electricity. That the structures are single crystalline as used herein means that the crystal lattice of the entire structures is continuous and unbroken throughout the entire structures, with no grain boundaries therein. An electrically conductive material can be a material with essentially zero band gap. The electrical conductivity of an electrically conductive material is generally above 103 S/cm. A semiconductor can be a material with a finite band gap upto about 3 eV and general has an electrical conductivity in the range of 103 to 10−8 S/cm. An electrically insulating material can be a material with a band gap greater than about 3 eV and generally has an electrical conductivity below 10−8 S/cm. The term “structures essentially perpendicular to the substrate” as used herein means that angles between the structures and the substrate is greater than zero, preferably greater than 5°, more preferably are from 85° to 90°. The term “recess” as used herein means a hollow space in the substrate and is open to a space outside the substrate. A group III-V compound material as used herein means a compound consisting of a group III element and a group V element. A group III element can be B, Al, Ga, In, Tl, Sc,

Y, the lanthanide series of elements and the actinide series of elements. A group V element can be V, Nb, Ta, Db, N, P, As, Sb and Bi. A group II-VI compound material as used herein means a compound consisting of a group II element and a group VI element. A group II element can be Be, Mg, Ca, Sr, Ba and Ra. A group VI element can be Cr, Mo, W, Sg, O, S, Se, Te, and Po. A quaternary material is a compound consisting of four elements. The term "mesh" as used herein means a web-like pattern or construction. The term "overhanging portion" as used herein means a portion of the structures that project over the sidewall of the recesses. The term "contour of a top surface of the structures" as used herein means the edge of the top surface of the structures. The term "electrode" as used herein means a conductor used to establish electrical contact with the photovoltaic device. The term "continuous" as used herein means having no gaps, holes, or breaks. The term "p-i-n junction" as used herein means a structure of a lightly doped or intrinsic semiconductor region sandwiched between a p-type semiconductor region and an n-type semiconductor region. The p-type and n-type regions can be heavily doped for Ohmic contacts. The term "p-n junction" as used herein means a structure with a p-type semiconductor region and an n-type semiconductor region in contact with each other. The term "gate electrode" as used herein means an electrode operable to control electrical current flow by a voltage applied on the gate electrode. The term "nanopillar" as used herein means a structure that has a size constrained to at most 1000 nm in two dimensions and unconstrained in the other dimension. The term "nanopillar" can also mean a structure that has a size constrained to at most 10 microns in two dimensions and unconstrained in the other dimension. The term "gate line" as used herein means an electrode or a conductor line operable to transmit an electrical signal to the gate electrodes. The term "multiplexer" as used herein means a device that performs multiplexing; it selects one of many analog or digital input signals and forwards the selected input into a single line. An analog-to-digital converter (abbreviated ADC, A/D or A to D) is a device that converts a continuous quantity to a discrete digital number. A digital-to-analog converter (DAC or D-to-A) is a device that converts a digital (usually binary) code to an analog signal (current, voltage, or electric charge). The term "foreoptics" as used herein means optical components (e.g., lenses, mirrors) placed in an optical path before the image sensor..

[0053] An intrinsic semiconductor, also called an undoped semiconductor or i-type semiconductor, is a substantially pure semiconductor without any significant dopant species present. A heavily doped semiconductor is a semiconductor with such a high doping level that the semiconductor starts to behave electrically more like a metal than as a

semiconductor. A lightly doped semiconductor is a doped semiconductor but not have a doping level as high as a heavily doped semiconductor. In a lightly doped semiconductor, dopant atoms create individual doping levels that can often be considered as localized states that can donate electrons or holes by thermal promotion (or an optical transition) to the conduction or valence bands respectively. At high enough impurity concentrations (i.e. heavily doped) the individual impurity atoms may become close enough neighbors that their doping levels merge into an impurity band and the behavior of such a system ceases to show the typical traits of a semiconductor, e.g. its increase in conductivity with temperature. A "single crystalline" semiconductor as used herein means that the crystal lattice of the semiconductor is continuous and unbroken, with no grain boundaries therein. A semiconductor being "multi-crystalline" as used herein means that the semiconductor comprises grains of crystals separated by grain boundaries. A semiconductor being "amorphous" as used herein means that the semiconductor has a disordered atomic structure.

[0054] Figs. 1A-1C each show a partial cross-sectional view of a nanostructure 1 extending essentially perpendicularly from a substrate 20.

[0055] As shown in a partial cross-sectional view of Fig. 1A, a nanostructure 1, according to an embodiment, extends essentially perpendicularly from a substrate 20 and comprises a core 11 of a doped semiconductor material, an intrinsic amorphous semiconductor layer 12 disposed isotropically over at least an end portion 14 away from the substrate 20, and a heavily doped amorphous semiconductor layer 13 of an opposite type from the core 11 and disposed isotropically over at least a portion of the intrinsic amorphous semiconductor layer 12.

[0056] As shown in a partial cross-sectional view of Fig. 1B, a nanostructure 1, according to an embodiment, extends essentially perpendicularly from a substrate 20 and comprises a core 11 of a doped semiconductor material, an intrinsic amorphous semiconductor layer 12 disposed on an end surface 16 away from the substrate 20, and a heavily doped amorphous semiconductor layer 13 of an opposite type from the core 11 and disposed on the intrinsic amorphous semiconductor layer 12. Preferably, the intrinsic amorphous semiconductor layer 12 and the heavily doped amorphous semiconductor layer 13 are coextensive with the core 11 in at least a direction parallel to the substrate 20. Preferably, sidewalls of the core 11 are at least partially covered by an electrically insulating layer 15.

[0057] As shown in a partial cross-sectional view of Fig. 1C, a nanostructure 1, according to an embodiment, extends essentially perpendicularly from a substrate 20 and comprises a core

11 of a doped semiconductor material, an intrinsic amorphous semiconductor layer 12 disposed on an end surface 16 away from the substrate 20, and a heavily doped amorphous semiconductor layer 13 of an opposite type from the core 11 and disposed on the intrinsic amorphous semiconductor layer 12. Preferably, sidewalls of the core 11 are at least partially covered by an electrically insulating layer 15. Preferably, the intrinsic amorphous semiconductor layer 12 and the heavily doped amorphous semiconductor layer 13 are coextensive with the electrically insulating layer 15 in at least a direction parallel to the substrate 20.

[0058] The substrate 20 can comprise any suitable material: semiconductor (e.g., silicon), insulator (e.g., glass), metal (e.g., gold). The substrate 20 can comprise any suitable electronic components such as transistors, interconnects, vias, diodes, amplifiers, etc.

[0059] The core 11 can comprise any suitable doped semiconductor material, such as doped silicon, doped germanium, doped III-V group compound semiconductor (e.g., gallium arsenide, gallium nitride, etc.), doped II-VI group compound semiconductor (e.g., cadmium selenide, cadmium sulfide, cadmium telluride, zinc oxide, zinc selenide, etc.), or doped quaternary semiconductor (e.g., copper indium gallium selenide). The core 11 is preferably substantially crystalline semiconductor material. The core 11 is preferably lightly doped. The core 11 can comprise a p-n junction or a p-i-n junction therein.

[0060] The intrinsic amorphous semiconductor layer 12 can comprise any suitable intrinsic amorphous semiconductor material, such as intrinsic amorphous silicon, intrinsic amorphous germanium, intrinsic amorphous III-V or II-VI group compound semiconductor. The intrinsic amorphous semiconductor layer 12 preferably has a thickness of about 2 nm to about 100 nm, more preferably about 2 nm to about 30 nm. The intrinsic amorphous semiconductor layer 12 is configured to passivate at least a surface of the core 11. The intrinsic amorphous semiconductor layer 12 can be deposited by any suitable method such as atomic layer deposition (ALD) or chemical vapor deposition (CVD).

[0061] The heavily doped amorphous semiconductor layer 13 can comprise any suitable heavily doped amorphous semiconductor material, such as heavily doped amorphous silicon, heavily doped amorphous germanium, heavily doped amorphous III-V or II-VI group compound semiconductor. The heavily doped amorphous semiconductor layer 13 being an opposite type from the core 11 means that if the core is p-type, the heavily doped amorphous semiconductor layer 13 is n-type and that if the core is n-type, the heavily doped amorphous semiconductor layer 13 is p-type. The heavily doped amorphous semiconductor layer 13

preferably has a thickness of at least about 10 nm, for example, from about 10 nm to about 200 nm. The heavily doped amorphous semiconductor layer 13 can be deposited by any suitable method such as atomic layer deposition (ALD) or chemical vapor deposition (CVD).

[0062] The heavily doped amorphous semiconductor layer 13, the intrinsic amorphous semiconductor layer 12 and the core 11 form a p-i-n junction.

[0063] The electrically insulating layer 15 can comprise any suitable material, such as HfO_2, SiO_2, Al_2O_3, Si_3N_4, etc.

[0064] The nanostructure 1 can be a nanowire or a nanoslab. The term "nanowire" used herein means a structure whose dimension in a direction perpendicular to the substrate (hereafter referred to as the "normal direction") is substantially greater than dimensions of the structure in any direction perpendicular to the normal direction (hereafter referred to as a "transverse direction") and the dimensions in the transverse directions are less than 1000 nm. The term "nanoslab" used herein means a structure whose dimensions in the normal direction and in the transverse direction are substantially greater than a dimension of the structure in a direction perpendicular to both the normal direction and the transverse direction (hereafter referred to as the "thickness direction") and the dimension in the thickness direction is less than 1000 nm. A nanoslab can have any suitable shape in a cross-section parallel to the substrate, such as a rectangle, an ellipse, convex-convex (i.e. like a double-convex lens), concave-concave (i.e. like a double-concave lens), plano-convex (i.e. like a plano-convex lens), plano-concave (i.e. like a plano- concave lens).

[0065] According to an embodiment, the nanostructure 1 is configured as a solar blind ultra violet (SBUV) detector. The SBUV region is the range of wavelengths in which the earth atmosphere absorbs essentially all UV radiation from the sun to the earth. For example, the wavelength region of 300 nm to 200 nm is within the SBUV region. A device that detects radiation only in the SBUV region and rejects visible and infrared radiation is called an SBUV detector or an SBUV sensor.

[0066] Sunlight does not interfere or blind a SBUV detector of the embodiments herein. Therefore, the SBUV detector of the embodiments herein is particularly useful for detecting manmade radiation sources that emit in the SBUV region and enjoys a very low false alarm rate. Such manmade radiation sources can include exhaust plumes of shoulder launched surface to air missiles (SLSAM), fire and flame, or any other UV emitting source including hydrogen flames. An SBUV detector of the embodiments herein can function at all lightning

conditions including full daylight, without interference from the solar radiation and with very high signal to background ratio.

[0067] According to an embodiment, the SBUV detector comprises a substrate having a plurality of regions defined thereon (hereafter referred to as "pixels"). In each pixel, the SBUV detector comprises a plurality of nanostructures 1 extending essentially perpendicularly from the substrate. The nanostructures 1 in the SBUV detector are nanowires. The plurality of nanostructures 1 can be equally or unequally spaced from each other, arranged in a regular array or in random. The plurality of nanostructures 1 are configured to react only to radiations in the SBUV region and not to react to radiations outside the SBUV region. Here, the term "react" is meant to broadly encompass absorbing, reflecting, coupling to, detecting, interacting with, converting to electrical signals, etc.

[0068] Fig. S1A shows one of the plurality of nanostructures 1 (a nanowire in the SBUV) on an SBUV S10. For brevity, only one nanostructure 1 is shown but the SBUV S10 can comprise a plurality of nanostructures 1, such as more than 1000, or more than 1000000. The nanostructures 1 extend essentially perpendicularly from a substrate S130. Each of the nanostructures 1 preferably comprises a cladding S120 surrounding the nanostructures 1. The substrate S130 is preferably a metal. The nanostructures 1 preferably have higher refractive index than the cladding S120. The term "cladding" or "clad" as used herein means a layer of substance surrounding the nanostructures 1.

[0069] Fig. S1B shows simulated absorptance of the SBUV detector S10 of UV light with wavelengths between 100 and 400 nm, incident in the normal direction. Fig. S1B clearly shows that absorptance of the SBUV detector S10 of UV light with wavelengths between 140 and 290 nm is greater than 50% and absorptance of UV light drops quickly to almost zero outside wavelength region of 140-290 nm. Fig. S1B indicate that the SBUV detector S10 indeed only reacts to radiations in the SBUV region. As shown in Fig. S1C, each of the nanostructures 1 can further comprise a coupler S140 disposed on an end of the nanostructures 1 away from the substrate S130 (hereafter referred to as the "receiving end"). The term "coupler" as used herein means a layer effective to guide light into the nanostructures 1.

[0070] According to an embodiment, the nanostructures 1 are nanowires and have a diameter of from about 5 nm to about 30 nm, preferably about 20 nm. According to an embodiment, the nanostructures 1 have a diameter of from about 5 nm to about 150 nm. The cladding S130 has a thickness of about 10 nm to about 200 nm, preferably about 30 nm. Pitch of the

nanostructures 1 (i.e. center-to-center distance of one of the plurality of nanowires to a nearest neighbor thereof) is from about 0.2 µm to about 2 µm. Height (i.e. dimension in the normal direction) of the nanostructures 1 is from about 0.1 µm to about 5 µm. Each pixel can have one or more nanostructures 1.

[0071] Fig. S2A and Fig. S2B shows a perspective view and a top view, respectively, of the SBUV detector S10. For brevity, only four pixels (regions enclosed by dotted rectangles) are shown. The nanostructures 1 preferably detect UV radiation in the SBUV region by converting it to an electrical signal. For example, each nanostructure 1 can comprise a photodiode (such as an avalanche photodiode) or form a photodiode (such as an avalanche photodiode) with the substrate S130. The SBUV detector S10 can further comprise electrical components configured to detect the electrical signal from the nanostructures 1, for example, Readout Integrated Circuits (ROIC) in the substrate S130, an electrode S150 disposed between and electrically connected to all the nanostructures 1 on each pixel, a common electrode S160 disposed on and electrically connected to the receiving ends of all the nanostructures 110 in the entire SBUV detector S10. Preferably, the SBUV detector S10 can detect electrical signals from the nanostructures 1 in different pixels separately.

[0072] According to one embodiment as shown in Fig. S9, the SBUV detector S10 can be integrated with electronic circuitry into a solar-blind image sensor. The electronic circuitry can include address decoders, a correlated double sampling circuit (CDS), a signal processor, a multiplexor and a high voltage supply (e.g. a DC high voltage supply capable of supplying at least 50 V, 100 V, 200 V or higher) for driving the nanostructures 1. The electronic circuitry is functional to detect the electrical signal generated by the nanostructures 1.

[0073] The SBUV detector S10 can also be used as fore optics in a light detector apparatus as shown in the schematic in Fig. S10.

[0074] Polarization is a property of certain types of waves that describes the orientation of their oscillations. Electromagnetic waves including visible light can exhibit polarization. By convention, the polarization of light is described by specifying the orientation of the light's electric field at a point in space over one period of the oscillation. When light travels in free space, in most cases it propagates as a transverse wave, i.e. the polarization is perpendicular to the light's direction of travel. In this case, the electric field may be oriented in a single direction (linear polarization), or it may rotate as the wave travels (circular or elliptical polarization). In the latter cases, the oscillations can rotate either towards the right or towards the left in the direction of travel. Depending on which rotation is present in a given wave it is

called the wave's chirality or handedness. Polarization of fully polarized light can be represented by a Jones vector. The x and y components of the complex amplitude of the electric field of light travel along z-direction, $E_x(t)$ and $E_y(t)$, are represented as $\begin{pmatrix} E_x(t) \\ E_y(t) \end{pmatrix} = E_0 \begin{pmatrix} E_{0x} e^{i(kz-\omega t+\phi_x)} \\ E_{0y} e^{i(kz-\omega t+\phi_x)} \end{pmatrix} = E_0 e^{i(kz-\omega t)} \begin{pmatrix} E_{0x} e^{i\phi_x} \\ E_{0y} e^{i\phi_y} \end{pmatrix}$. $\begin{pmatrix} E_{0x} e^{i\phi_x} \\ E_{0y} e^{i\phi_y} \end{pmatrix}$ is the Jones vector. Polarization of light with any polarization, including unpolarized, partially polarized, and fully polarized light, can be described by the Stokes parameters, which are four mutually independent parameters.

[0075] A device that can detect polarization of light, or even measure the light's Jones vector or Stokes parameters can be useful in many application.

[0076] According to an embodiment, the device comprises a substrate having a plurality of regions defined thereon (hereafter referred to as "subpixels"; a group of related "subpixels" may be referred to as a "pixel"). In each subpixel, the device comprises a plurality of nanostructures 1 being nanoslabs. The plurality of nanostructures 1 can be equally or unequally spaced from each other. The plurality of nanostructures 1 in different subpixels are functional to react differently to light with a same polarization. Here, the term "react" is meant to broadly encompass absorbing, reflecting, coupling to, detecting, interacting with, converting to electrical signals, etc. The plurality of nanostructures 1 in a first subpixel extends in a first transverse direction; the plurality of nanostructures 1 in a second subpixel extends in a second transverse direction, wherein the first and second pixels are adjacent and the first transverse direction is different from the second transverse direction.

[0077] Fig. P1 shows a device P10 according to one embodiment. For brevity, two subpixels P10a and P10b of a substrate P110 are illustrated. The device P10, however, can comprise a plurality of pixels such as more than 100, more than 1000, more than 1000000. The subpixels preferably have a pitch of about 1 micron to 100 microns (more preferably 5 microns). In each of the subpixels P10a and P10b, the device P10 comprises a plurality of nanostructures 1 (e.g. at least 2 features), respectively. The nanostructures 1 in the subpixel P10a and the nanostructures 1 in the subpixel P10b extend in different transverse directions. The nanostructures 1 preferably have a pitch (i.e. spacing between adjacent features 100 in the thickness direction thereof) of about 0.5 to 5 microns (further preferably about 1 micron), a height (i.e. dimension in the normal direction) of about 0.3 to 10 microns (further preferably about 5 micron) and an aspect ratio (i.e. ratio of a dimension in the transverse direction to a

dimension in the thickness direction) of at least 4:1, preferably at least 10:1. Each of the nanostructures 1 forms a p-i-n diode with the substrate P110, the p-i-n diode being functional to convert at least a portion of light impinged thereon to an electrical signal. The device P10 preferably further comprises electrical components configured to detect the electrical signal from the nanostructures 1, for example, a transparent electrode disposed on each subpixel and electrically connected to all nanostructures 1 therein. The transparent electrode on each subpixel preferably is separate from the transparent electrode on adjacent subpixels. A reflective material can be deposited on areas of the substrate P110 between the nanostructures 1. The substrate P110 can have a thickness in the normal direction of about 5 to 700 microns (preferably 120 microns).

[0078] Fig. P2 shows a schematic of the nanostructures 1 in one subpixel when light with different polarization impinges thereon. For light P15a with a wavelength of about 400 nm and a linear polarization essentially in the thickness direction of the nanostructures 1, the absorptance of the nanostructures 1 is about 35%. In contrast, for light P15b with the same wavelength as light P15a and a linear polarization essentially in the transverse direction of the nanostructures 1, the absorptance of the nanostructures 1 is about 95%.

[0079] According to one embodiment as shown in Fig. P10, the device P10 can be integrated with electronic circuitry into a polarization detector array. The electronic circuitry can include address decoders in both directions of the detector array, a correlated double sampling circuit (CDS), a signal processor, a multiplexor. The electronic circuitry is functional to detect the electrical signal converted by the nanostructures 100 from at least a portion of light impinged thereon. The electric circuitry can be further functional to calculate an interpolation of electrical signals from several subpixels, the features on which extend in the same transverse direction. Other function of the electronic circuitry can include a gain adjustment, a calculation of Stoke's parameters. In particular, the subpixels can be arranged into a group (i.e. pixel). For example, in Fig. P10, a subpixel A and subpixels B, C and D can be arranged adjacent to each other and referred to as a pixel, wherein features on the subpixels B, C and D extend in transverse directions at 45°, 90° and -45° relative to a transverse direction in which features on the subpixel A extend.

[0080] According to an embodiment as shown in Fig. P12, the nanostructures 100 can each comprise a metal layer on each sidewall (i.e. surface extending in the transverse direction and the normal direction). The metal layer preferably has a thickness of about 5 nm to about 100 nm, more preferably about 50 nm. The metal layer substantially covers the entire sidewall

and the metal layer does not extend to either end of the nanostructures in the normal direction.

[0081] A photovoltaic device, also called a solar cell is a solid state device that converts the energy of sunlight directly into electricity by the photovoltaic effect. Assemblies of cells are used to make solar modules, also known as solar panels. The energy generated from these solar modules, referred to as solar power, is an example of solar energy.

[0082] The photovoltaic effect is the creation of a voltage (or a corresponding electric current) in a material upon exposure to light. Though the photovoltaic effect is directly related to the photoelectric effect, the two processes are different and should be distinguished. In the photoelectric effect, electrons are ejected from a material's surface upon exposure to radiation of sufficient energy. The photovoltaic effect is different in that the generated electrons are transferred between different bands (i.e. from the valence to conduction bands) within the material, resulting in the buildup of a voltage between two electrodes.

[0083] Photovoltaics is a method for generating electric power by using solar cells to convert energy from the sun into electricity. The photovoltaic effect refers to photons of light–packets of solar energy–knocking electrons into a higher state of energy to create electricity. At higher state of energy, the electron is able to escape from its normal position associated with a single atom in the semiconductor to become part of the current in an electrical circuit. These photons contain different amounts of energy that correspond to the different wavelengths of the solar spectrum. When photons strike a PV cell, they may be reflected or absorbed, or they may pass right through. The absorbed photons can generate electricity. The term photovoltaic denotes the unbiased operating mode of a photodiode in which current through the device is entirely due to the light energy. Virtually all photovoltaic devices are some type of photodiode.

[0084] A conventional solar cell often has opaque electrodes on a surface that receives light. Any light incident on such opaque electrodes is either reflected away from the solar cell or absorbed by the opaque electrodes, and thus does not contribute to generation of electricity. Therefore, a photovoltaic device that does not have this drawback is desired.

[0085] Fig. V2A shows a schematic cross-section of a photovoltaic device V200, according to another embodiment. The photovoltaic device V200 comprises a substrate V205, a plurality of nanostructures 1 essentially perpendicular to the substrate V205 and one or more recesses V230 between the nanostructures 1. Each recess V230 has a sidewall V230a and a bottom wall V230b. The bottom wall V230b has a planar reflective layer V232. The

sidewall V230a does not have any planar reflective layer V232. A continuous cladding layer 240 is disposed over an entire the nanostructures 1. The photovoltaic device V200 can further comprise a coupling layer V260 disposed on the cladding layer V240 and only directly above the top surface V220a.

[0086] The nanostructures 1 can have any cross-sectional shape. For example, the nanostructures 1 can be cylinders or prisms with elliptical, circular, rectangular, polygonal cross-sections. The nanostructures 1 can also be strips as shown in Fig. V9, or a mesh as shown in Fig. V10. According to one embodiment, the nanostructures 1 are pillars with diameters from 50 nm to 5000 nm, heights from 1000 nm to 20000 nm, a center-to-center distance between two closest pillars of 300 nm to 15000 nm. Preferably, the nanostructures 1 have an overhanging portion V224 along an entire contour of the top surface V220a of the nanostructures 1.

[0087] Each recess V230 preferably has a rounded or beveled inner edge between the sidewall V230a and the bottom wall V230b.

[0088] The planar reflective layer V232 can be any suitable material, such as ZnO, Al, Au, Ag, Pd, Cr, Cu, Ti, a combination thereof, etc. The planar reflective layer V232 preferably is an electrically conductive material, more preferably a metal. The planar reflective layer V232 preferably has a reflectance of at least 50%, more preferably has a reflectance of at least 70%, most preferably has a reflectance of at least 90%, for visible light of any wavelength. The planar reflective layer V232 has a thickness of preferably at least 5 nm, more preferably at least 20 nm. The planar reflective layer V232 in all the recesses V230 is preferably connected. The planar reflective layer V232 is functional to reflect light incident thereon to the nanostructures 1 so the light is absorbed by the nanostructures 1. The planar reflective layer V232 preferably is functional as an electrode of the photovoltaic device V200.

[0089] The cladding layer V240 is substantially transparent to visible light, preferably with a transmittance of at least 50%, more preferably at least 70%, most preferably at least 90%. The cladding layer V240 can be made of an electrically conductive material. The cladding layer V240 preferably is made of a transparent conductive oxide, such as ITO (indium tin oxide), AZO (aluminum doped zinc oxide), ZIO (zinc indium oxide), ZTO (zinc tin oxide), etc. The cladding layer V240 can have a thickness of 50 nm to 5000 nm. The cladding layer V240 preferably forms an Ohmic contact with the nanostructures 1. The cladding layer V240

preferably forms an Ohmic contact with the planar reflective layer V232. The cladding layer V240 preferably is functional as an electrode of the photovoltaic device V200.

[0090] The substrate V205 preferably has a flat surface V250 opposite the nanostructures 1. The flat surface V250 can have a doped layer V251 of the opposite conduction type from the core 11 of the nanostructures 1, i.e. if the core 11 is n type, the doped layer V251 is p type; if the core 11 is p type, the doped layer V251 is n type. The doped layer V251 is electrically connected to each of the nanostructures 1. The flat surface V250 can also have a metal layer V252 disposed on the doped layer V251. The metal layer V252 forms an Ohmic contact with the doped layer V251. The substrate V205 preferably has a thickness of at least 50 microns. Total area of the planar reflective layer V232 is preferable at least 40% of a surface area of the flat surface 250.

[0091] The coupling layer V260 can be of the same material as the cladding layer V240 or different material from the cladding layer V240. As shown in Fig. V5, refractive index of the core 11 of the nanostructure 1 n_1, refractive index of the cladding layer V240 n_2, refractive index of the coupling layer V260 n_3, refractive index of the space between the nanostructures 1 n_4, preferably satisfy relations of $n_1>n_2>n_4$ and $n_1>n_3>n_4$, which lead to enhanced light concentration in the nanostructures 1.

[0092] In one embodiment, the nanostructures 1 are pillars arranged in an array, such as a rectangular array, a hexagonal array, a square array, concentric ring. Each pillar is about 5 microns in height. A pitch of the nanostructures 1 is from 300 nm to 15 microns. The cladding layer V240 is about 175 nm thick.

[0093] Fig. V6 shows an exemplary top cross sectional view of the photovoltaic device V200. Fig. V7 shows an exemplary perspective view of the photovoltaic device V200.

[0094] A method of converting light to electricity comprises: exposing the photovoltaic device V200 to light; reflecting light to the nanostructures 1 using the planar reflective layer V232; absorbing the light and converting the light to electricity using the nanostructures 1; drawing an electrical current from the photovoltaic device V200. As shown in Fig. V8B, the electrical current can be drawn from the metal layer V252 and/or the planar reflective layer V232 in the photovoltaic device V200.

[0095] Fig. W2A shows a schematic cross-section of a photovoltaic device W200, according to another embodiment. The photovoltaic device W200 comprises a substrate W205, a plurality of nanostructures 1 essentially perpendicular to the substrate W205, one or more recesses W230 between the nanostructures 1 and an electrode layer W280. Each recess

W230 is filled with a transparent material W240. Each recess W230 has a sidewall W230a and a bottom wall W230b. The bottom wall W230b has a planar reflective layer W232. The sidewall W230a does not have any planar reflective layer. The transparent material W240 preferably has a surface coextensive with the top surface W220a of the nanostructures 1. The photovoltaic device W200 further comprises an electrode layer W280 disposed on the transparent material W240 and the nanostructures 1. The photovoltaic device W200 can further comprise a coupling layer W260 disposed on the electrode layer W280 and only directly above the top surface W220a.

[0096] The nanostructures 1 can have any cross-sectional shape. For example, the nanostructures 1 can be cylinders or prisms with elliptical, circular, rectangular, polygonal cross-sections. The nanostructures 1 can also be strips as shown in Fig. V9, or a mesh as shown in Fig. V10. According to one embodiment, the nanostructures 1 are pillars with diameters from 50 nm to 5000 nm, heights from 1000 nm to 20000 nm, a center-to-center distance between two closest pillars of 300 nm to 15000 nm. Preferably, the nanostructures 1 have an overhanging portion W224 along an entire contour of the top surface W220a of the nanostructures 1.

[0097] Each recess W230 preferably has a rounded or beveled inner edge between the sidewall W230a and the bottom wall W230b.

[0098] The planar reflective layer W232 can be any suitable material, such as ZnO, Al, Au, Ag, Pd, Cr, Cu, Ti, Ni, a combination thereof, etc. The planar reflective layer W232 preferably is an electrically conductive material, more preferably a metal. The planar reflective layer W232 preferably has a reflectance of at least 50%, more preferably has a reflectance of at least 70%, most preferably has a reflectance of at least 90%, for visible light of any wavelength. The planar reflective layer W232 has a thickness of preferably at least 5 nm, more preferably at least 20 nm. The planar reflective layer W232 in all the recesses W230 is preferably connected. The planar reflective layer W232 is functional to reflect light incident thereon to the nanostructures 1 so the light is absorbed by the nanostructures 1. The planar reflective layer W232 preferably is functional as an electrode of the photovoltaic device W200.

[0099] The transparent material W240 is substantially transparent to visible light, preferably with a transmittance of at least 50%, more preferably at least 70%, most preferably at least 90%. The transparent material W240 can be an electrically conductive material. The transparent material W240 preferably is made of a transparent conductive oxide, such as ITO

(indium tin oxide), AZO (aluminum doped zinc oxide), ZIO (zinc indium oxide), ZTO (zinc tin oxide), etc. The transparent material W240 preferably forms an Ohmic contact with the heavily doped amorphous semiconductor layer 13 of the nanostructures 1. The transparent material W240 preferably forms an Ohmic contact with the planar reflective layer W232. The transparent material W240 preferably is functional as an electrode of the photovoltaic device W200. The transparent material W240 can also be a suitable electrically insulating material such as SiO_2 or a polymer.

[00100] The substrate W205 preferably has a flat surface W250 opposite the nanostructures 1. The flat surface W250 can have a doped layer W251 of the opposite conduction type from the core 11 of the nanostructures 1, i.e. if the core 11 is n type, the doped layer W251 is p type; if the core 11 is p type, the doped layer W251 is n type. The doped layer W251 is electrically connected to each of the nanostructures 1. The flat surface W250 can also have a metal layer W252 disposed on the doped layer W251. The metal layer W252 forms an Ohmic contact with the doped layer W251. The substrate W205 preferably has a thickness of at least 50 microns. Total area of the planar reflective layer W232 is preferable at least 40% of a surface area of the flat surface W250.

[00101] The electrode layer W280 can be the same material as the transparent material W240 or different material from the transparent material W240. The electrode layer W280 is substantially transparent to visible light, preferably with a transmittance of at least 50%, more preferably at least 70%, most preferably at least 90%. The electrode layer W280 is an electrically conductive material. The electrode layer W280 preferably is a transparent conductive oxide, such as ITO (indium tin oxide), AZO (aluminum doped zinc oxide), ZIO (zinc indium oxide), ZTO (zinc tin oxide), etc. The electrode layer W280 preferably forms an Ohmic contact with the heavily doped amorphous semiconductor layer 13. The electrode layer W280 preferably is functional as an electrode of the photovoltaic device W200.

[00102] The coupling layer W260 can be the same material as the transparent material W240 or different material from the transparent material W240. As shown in Fig. W5, refractive index of the core 11 of the nanostructure 1 n_1, refractive index of the transparent material W240 n_2, refractive index of the coupling layer W260 n_3, preferably satisfy relations of $n_1>n_2$ and $n_1>n_3$, which lead to enhanced light concentration in the nanostructures 1.

[00103] In one embodiment, the nanostructures 1 are pillars arranged in an array, such as a rectangular array, a hexagonal array, a square array, concentric ring. Each pillar is about 5 microns in height. A pitch of the nanostructures 1 is from 300 nm to 15 microns.

[00104] As shown in Fig. W11B, the photovoltaic device W200 can further comprise at least one via W599 in the transparent material W240 and between the electrode layer W280 and the planar reflective layer W232, wherein the at least one via W599 is an electrically conductive material, preferably an electrically conductive transparent material (e.g. ITO, AZO, etc.) and the at least one via electrically connects the electrode layer W280 and the planar reflective layer W232. As shown in Fig. W11A, the via W599 can be made by etching a recess W598 through the electrode layer W280 and the transparent material W240 until the planar reflective layer W232 is exposed and then filling the recess W598 to form the via W599. As shown in Figs. W12A and W12B, the vias W599 can be any suitable shape such as rod-shaped or bar-shaped.

[00105] A method of converting light to electricity comprises: exposing the photovoltaic device W200 to light; reflecting light to the structures W220 using the planar reflective layer W232; absorbing the light and converting the light to electricity using the structures W220; drawing an electrical current from the photovoltaic device W200. As shown in Fig. W8B, the electrical current can be drawn from the metal layer W252 and the planar reflective layer W232, in the photovoltaic device W200.

[00106] According to an embodiment, an image sensor comprises a plurality of pixels, each pixel of which has at least a nanostructure 1 in a form of a nanowire that can convert light impinging thereon to electrical signals and a gate electrode surrounding the nanostructure 1 preferably near its lower end (i.e. the end connected to a substrate). The gate electrode may be located at another location of the nanostructure 1. The gate electrodes are functional to individually electrically connect the nanostructures 1 to or disconnect the nanostructures 1 from external readout circuitry. The pixels can be arranged in any suitable pattern such as a square grid, a hexagonal grid, and concentric rings. The pixels can be fabricated to absorb light in the ultraviolet (UV), visible (VIS) or infrared (IR) regions and to generate a detectable electrical signal in response thereto.

[00107] The nanostructures 1 essentially extend perpendicularly from the substrate, which can also be referred to as “standing-up”.

[00108] The image sensor can be configured for various types of uses such as compact image sensors and spectrophotometers.

[00109] In one embodiment, the pixels are organized into a plurality of “rows”. The pixels in each row are electrically connected in parallel to a readout line. Pixels in different rows are electrically connected to different readout lines. The pixels can be organized into a

plurality of "columns" such that the gate electrodes of the pixels in each column are electrically connected in parallel to a gate line, the gate electrodes of the pixels in different columns are electrically connected to different gate lines, and no two different pixels are connected to a same readout line and their gate electrodes are connected to a same gate line. The terms "row" and "column" do not require that pixels are physically aligned or arranged in any particular way, but rather are used to describe topological relationship between the pixels, readout lines and gate lines. An exemplary image sensor according to this embodiment comprises first, second, third, fourth pixels, each of which has a gate electrode, a first readout line electrically connected to the first and second pixels, a second readout line electrically connected to the third and fourth pixels, a first gate line electrically connected to the gate electrodes of the first and third pixels and a second gate line electrically connected to the gate electrodes of the second and fourth pixels.

[00110] In one embodiment, each pixel has at least one nanostructure 1. The nanostructures 1 in the pixels can be configured to absorb, confine and transmit light impinging thereon. For example, the nanostructures 1 can function as waveguides to confine and direct light in a direction determined by its physical boundaries.

[00111] In one embodiment, more than one pixels can have a common electrode electrically connected thereto, for example, for providing a bias voltage. The common electrode can be a top layer made of a transparent conductive material, such as ITO (indium tin oxide) or aluminum doped ZnO (AZO).

[00112] In one embodiment, the readout lines and the gate lines can have suitable electronic devices connected thereto, such as, amplifiers, multiplexers, D/A or A/D converters, computers, microprocessing units, digital signal processors, etc.

[00113] In one embodiment, the nanostructures 1 and the substrate can comprise suitable semiconductor materials and/or metals such as Si, GaAs, InAs, Ge, ZnO, InN, GaInN, GaN, AlGaInN, BN, InP, InAsP, GaInP, InGaP:Si, InGaP:Zn, GaInAs, AlInP, GaAlInP, GaAlInAsP, GaInSb, InSb, Al, Al-Si, $TiSi_2$, TiN, W, $MoSi_2$, PtSi, $CoSi_2$, WSi_2, In, AuGa, AuSb, AuGe, PdGe, Ti/Pt/Au, Ti/Al/Ti/Au, Pd/Au, ITO (InSnO). The nanostructures 1 and the substrate can be doped by suitable dopants such as GaP, Te, Se, S, Zn, Fe, Mg, Be, Cd, etc. It should be noted that the use nitrides such as Si_3N_4, GaN, InN and AlN can facilitate fabrication of image sensors that can detect light in wavelength regions not easily accessible by conventional techniques. Doping levels of the nanostructures 1 and the substrate can be up to 10^{20} atoms/cm^3. Other suitable materials are possible.

[00114] Methods of fabrication of the image sensor can include shallow trench isolation (STI), also known as "Box Isolation Technique." STI is generally used on CMOS process technology nodes of 250 nanometers and smaller. Older CMOS technologies and non-MOS technologies commonly use isolation based on Local Oxidation of Silicon (LOCOS). STI is typically created early during the semiconductor device fabrication process, before transistors are formed. Steps of the STI process include, for instance, etching a pattern of trenches in the substrate, depositing one or more dielectric materials (such as silicon dioxide) to fill the trenches, and removing the excess dielectric using a technique such as chemical-mechanical planarization.

[00115] The nanostructures 1 can be formed by a dry etching process, such as a deep etching process, or a Bosch process, in combination with a suitable lithography technique (e.g. photolithography, e-beam lithography, holographic lithography). The nanostructures 1 can also be formed by a Vapor Liquid Solid (VLS) method. Diameters of the nanostructures 1 can be from 10 to 2000 nm, preferably 50 to 150 nm, more preferably 90 to 150 nm. Lengths of the nanpillars can be from 10 nm to 10000 nm, preferably 1000 nm to 8000 nm, more preferably 4000 nm to 6000 nm. The nanostructures 1 can have any suitable cross-sectional shape such as a circle, a square, a hexagon.

[00116] The nanostructures 1 can be sized to selectively absorb a wavelength region of interest, for instance, as described in co-pending U.S. Patent Application Serial No. 61/357,429 filed June 22, 2010, herein incorporation by reference in its entirety. Absorptance can be adjusted by varying the nanostructure 1 spacing (pitch), particularly to near unity.

[00117] The nanostructures 1 can have a cladding material. The nanostructures 1 can selectively absorb UV light, red light, green light, blue light, or IR light.

[00118] The image sensor can have large number of nanostructures 1, for instance, a million or more.

[00119] A method of using the image sensor comprises: (a) exposing the pixels to light; (b) reading electrical signals from a pixel by connecting at least one nanopillar in the pixel to external readout circuitry using the gate electrode surrounding the at least one nanopillar of the pixel. The electrical signals can be electric charge accumulated on the nanopillar, a change of electrical current through the nanopillar, or a change of electrical impedance of the nanopillar.

[00120] Figs. S4 and S5 show an apparatus comprising the image sensor and a control circuit. The control circuit comprises a decoder S410 and a trans-impedance amplifier (TIA) and multiplexer circuit S420. The image sensor and the control circuit can be formed as an integrated circuit or chip. To control or address the nanopillars, a gate voltage can be selectively applied to one of the gate lines S1570 at a time to allow electrical current through those nanopillars connected to that particular gate line S1570 and the readout lines S1021 can be used to read electrical current from each of those nanopillars. In this way, a row-by-row (i.e. gate line by gate line) addressing scheme may be executed. The TIA and multiplexer circuit S420 is connected to each readout line S1021 and can include a multiplexer to sequentially output electrical current one each readout line S1021 to a single terminal. The TIA and multiplexer circuit S420 can amplify the electrical current from each readout line S1021 and convert it into a voltage signal. The decoder array S410 is connected to each gate line S1570 and can include a multiplexer to sequentially apply gate voltages to each gate line S1570. The TIA and multiplexer circuit S420 and the decoder array S410 can be synchronized by a common timing signal from a timing pulse input. A controller can be used to generate the timing signal. The control circuit can further comprise other functional components, such as, for example, an analog-to-digital converter, an exposure controller, and a bias voltage circuit, etc. An exemplary TIA can be OPA381; an exemplary multiplexer can be ADG732, and an exemplary decoder can be SN74154 (all from Texas Instruments Inc). It will be appreciated, of course, that other readout circuitry components may also be used.

[00121] The control circuit can be connected to the image sensor by any suitable interconnect techniques, such as wire-bonding, flip-chip bonding or bump bonding.

[00122] The readout lines S1021 and the gate lines S1570 can be parallel as shown in Fig. S4 or can have a "fan-out" shape as shown in Fig. S5. As will be appreciated the fan out shaped electrodes provide greater room for connections to external circuitry.

[00123] The image sensor described herein can be used as various image sensors, including contact image sensors (CIS). Contact image sensors are capable of resolving features of a size approximately equal to the size of the pixel. The size of the pixel may be determined by the size of the nanopillar and the surrounding region in which the evanescent field propagates. CISs are a relatively recent technological innovation in the field of optical flatbed scanners that are rapidly replacing charge-coupled devices (CCDs) in low power and portable applications. As the name implies, CISs place the image sensor in near direct contact with an object to be scanned in contrast to using mirrors to bounce light to a stationary

sensor, as is the case in conventional CCD scanners. A CIS typically consists of a linear array of detectors, covered by a focusing lens and flanked by red, green, and blue LEDs for illumination. Usage of LEDs allows the CIS to be relatively power efficient, with many scanners being powered through the minimal line voltage supplied, for instance, via a universal serial bus (USB) connection. CIS devices typically produce lower image quality compared to CCD devices; in particular, the depth of field is limited, which poses a problem for material that is not perfectly flat. However, a CIS contact sensor is typically modularized. All the necessary optical elements may be included in a compact module. Thus, a CIS module can help to simplify the inner structure of a scanner. Further, a CIS contact sensor is typically smaller and lighter than a CCD line sensor. With a CIS, the scanner can be portable with a height around 30 mm.

[00124] A CIS can include an elongate optical assembly comprising illumination, optical imaging, and detection systems. The illumination source illuminates a portion of the object (commonly referred to as a "scan region"), whereas the optical imaging system collects light reflected by the illuminated scan region and focuses a small area of the illuminated scan region (commonly referred to as a "scan line") onto the pixels of the CIS. The pixels convert light incident thereon into electrical signals. Image data representative of the entire object then may be obtained by sweeping the CIS across the entire object.

[00125] A method of scanning an object using a CIS essentially comprises three steps: first, the pixels of the CIS convert reflected light they receive from the object into analog electrical signals; second, the analog electrical signals are amplified; third, the amplified analog electrical signals are converted to digital electrical signals by an analog-to-digital (A/D) converter. The digital signals may then be further processed and/or stored as desired.

[00126] Fig. S6 shows a schematic of an apparatus S600 in accordance with an embodiment. The apparatus S600 comprises foreoptics S610, the image sensor S620, a readout circuit (ROC) S630, and a processor S640. A housing may enclose and protect one of more the foregoing components of the apparatus S600 from excessive or ambient light, the environment (e.g., moisture, dust, etc.), mechanical damage (e.g., vibration, shock), etc.

[00127] Light (L) from a scene (S) emanates toward the apparatus S600. For clarity, only L from S impinging upon the apparatus S600 is depicted (although it will be appreciated that L from S propagates in all directions).

[00128] The foreoptics S610 may be configured to receive L from S and focus or collimate the received L onto the image sensor S620. For instance, foreoptics S610 may include one or more of: a lens, an optical filter, a polarizer, a diffuser, a collimator, etc.

[00129] The pixels in the image sensor S620 may include nanopillars of different sizes (e.g. from about 50 to 200 nm) for selective detection of light across a wavelength regions of interest.

[00130] The ROC S630 may be connected to the image sensor S620 and is configured to receive output therefrom.

[00131] The processor S640 is configured to receive output from the ROC S630. The processor S640 may, in some instances, be configured to provide defect correction, linearity correction, data scaling, zooming/magnification, data compression, color discrimination, filtering, and/or other imaging processing, as desired.

[00132] In one embodiment, the processor S640 may include hardware, such as Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), digital signal processors (DSPs), or other integrated formats. However, those skilled in the art will recognize that the processor S640 may, in whole or in part, can be equivalently implemented in integrated circuits, as one or more computer programs having computer-executable instructions or code running on one or more computers (e.g., as one or more programs running on one or more computer systems), as one or more programs running on one or more processors (e.g., as one or more programs running on one or more microprocessors), as firmware, or as virtually any combination thereof, and that designing the circuitry and/or writing the code for the software and/or firmware would be well within the skill of one skilled in the art in light of this disclosure. In addition, those skilled in the art will appreciate that the mechanisms of the subject matter described herein are capable of being distributed as a program product in a variety of forms, and that an illustrative embodiment of the subject matter described herein applies regardless of the particular type of computer-readable medium used to actually carry out the distribution.

[00133] In some implementations, the apparatus S600 may also be configured as a spectrophotometer to measure intensity of reflection or absorption at one more wavelengths.

[00134] Depending on the construction of the image sensor S620, light at different wavelengths may be detected nanopillars at different locations and with different sizes. A three- or four-nanopillar pixel may be fabricated. Of course, pixels having additional pillars are also possible.

[00135] Figs. S7A and S7B show an exemplary three-nanopillar pixel and an exemplary four-nanopillar pixel according to embodiments. These pixels may be incorporated into the image sensor.

[00136] Fig. S7A shows a pixel S710 including three nanopillars R, G, B, having different sizes configured to absorb and/or detect red, green, and blue light, respectively, according to an embodiment. For instance, the R, G, B nanopillars can have sizes effective to absorb and/or detect light of about 650 nm, 510 nm, and 475 nm in wavelength, respectively. The diameter of the pixel S710 may be 10 μm or less. The pixel S710 may be used in traditional shadow masked based display device.

[00137] Fig. S7B shows a pixel S720 including four nanopillars R, G, B, G, having different sizes configured to absorb and/or detect red, green, and blue light, respectively, according to an embodiment. Two of the nanopillars, G, absorb and/or detect green light. The diameter of the pixel S720 may be 10 μm or less.

[00138] A cladding may, in some instance, surround at least one pixel of the image sensor to increase light absorption. The cladding of pixel S710 and S720 may be formed, for instance, from hafnium oxide or silicon nitride.

[00139] The human eye has photoreceptors (called cone cells) for medium- and high-brightness color vision, with sensitivity peaks in short (S, 420–440 nm), middle (M, 530–540 nm), and long (L, 560–580 nm) wavelengths (there is also the low-brightness monochromatic "night-vision" receptor, called rod cell, with peak sensitivity at 490-495 nm). Thus, in principle, three parameters describe a color sensation. The tristimulus values of a color are the amounts of three primary colors in a three-component additive color model needed to match that test color. The tristimulus values are most often given in the CIE 1931 color space, in which they are denoted X, Y, and Z.

[00140] In the CIE XYZ color space, the tristimulus values are not the S, M, and L responses of the human eye, but rather a set of tristimulus values called X, Y, and Z, which are roughly red, green and blue, respectively (note that the X, Y, Z values are not physically observed red, green, blue colors. Rather, they may be thought of as 'derived' parameters from the red, green, blue colors). Two light sources, made up of different mixtures of various wavelengths, may appear to be the same color; this effect is called metamerism. Two light sources have the same apparent color to an observer when they have the same tristimulus values, no matter what spectral distributions of light were used to produce them.

[00141] Due to the nature of the distribution of cones in the eye, the tristimulus values depend on the observer's field of view. To eliminate this variable, the CIE defined the standard (colorimetric) observer. Originally this was taken to be the chromatic response of the average human viewing through a 2° angle, due to the belief that the color-sensitive cones resided within a 2° arc of the fovea. Thus the CIE 1931 Standard Observer is also known as the CIE 1931 2° Standard Observer. A more modern but less-used alternative is the CIE 1964 10° Standard Observer, which is derived from the work of Stiles and Burch, and Speranskaya.

[00142] The color matching functions are the numerical description of the chromatic response of the observer as described above.

[00143] The CIE has defined a set of three color-matching functions, called, $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$, which can be thought of as the spectral sensitivity curves of three linear light detectors that yield the CIE XYZ tristimulus values X, Y, and Z. These functions are known collectively as the CIE standard observer.

[00144] The tristimulus values for a color with a spectral power distribution $I(\lambda)$ are given in terms of the standard observer by: $X = \int_0^\infty I(\lambda)\bar{x}(\lambda)d\lambda$, $Y = \int_0^\infty I(\lambda)\bar{y}(\lambda)d\lambda$, $Z = \int_0^\infty I(\lambda)\bar{z}(\lambda)d\lambda$, wherein λ is the wavelength of the equivalent monochromatic light (measured in nanometers).

Examples

[00145] Fig. F1A shows a schematic partial cross-sectional view of an image sensor F100, according to an embodiment. The image sensor F100 comprises a substrate F110, one or more pixels F150. At least one pixel F150 comprises a clad F140 and a plurality of subpixels embedded in the clad F140. Two subpixels F151 and F152 are shown in Fig. F1A as an example. Each of the subpixels comprises a nanostructure 1 (e.g. a nanowire F151a in the subpixel F151 and a nanowire F152a in the subpixel F152) extending essentially perpendicularly from the substrate F110. Space between the pixels F150 is preferably filled with a material F160. Each pixel F150 can further comprise one or more photodiodes F120 located between the substrate F110 and the nanowires F151a and F152a.

[00146] The substrate F110 can comprise any suitable material such as silicon, silicon oxide, silicon nitride, sapphire, diamond, silicon carbide, gallium nitride, germanium, indium gallium arsenide, lead sulfide, and/or a combination thereof.

[00147] The photodiode F120 can be any suitable photodiode. The photodiode F120 can have a p-n junction of a p-i-n junction and any suitable circuitry. The photodiode F120 preferably has a footprint that completely encloses a footprint of the clad F140.

[00148] The clad F140 can comprise any suitable material, such as silicon nitride, silicon oxide, and/or a combination thereof. The clad 140 is preferably substantially transparent to visible light, preferably with a transmittance of at least 50%, more preferably at least 70%, most preferably at least 90%. In one example, the clad F140 is silicon nitride and has a cylindrical shape with a diameter of about 300 nm.

[00149] The material F160 can comprise any suitable material such as silicon dioxide. A refractive index of the material F160 is preferably smaller than a refractive index of the clad F140.

[00150] The nanostructures 1 (e.g. nanowires F151a and F152a) in the subpixels (e.g. F151 and F152) have refractive indexes equal to or greater than the refractive index of the clad F140. The nanostructures 1 (e.g. nanowires F151a and F152a) and the photodiode F120 have different absorption spectra. For example, the nanowire F151a has strong absorptance in blue wavelengths, as shown by an exemplary absorption spectrum F181 in Fig. F1C; the nanowire F152a has a strong absorptance in green wavelengths, as shown by an exemplary absorption spectrum F182 in Fig. F1C; the photodiode F120 has strong absorptance in red wavelengths, as shown by an exemplary absorption spectrum F180 in Fig. F1C. The nanowires can have different diameters and/or different materials. Each nanowire in one pixel F150 preferably has a distance of at least 100 nm, preferable at least 200nm, to a nearest neighboring nanowire in the same pixel. The nanowires can be positioned at any suitable positions in the clad F140.

[00151] The nanostructures 1 (e.g. nanowires F151a and F152a) in the subpixels (e.g. 151 and 152) are operable to generate electrical signals upon receiving light. One exemplary nanowire is a photodiode with a p-n or p-i-n junction therein, details of which can be found in U.S. Patent Application Publication Nos. 12/575,221 and 12/633,305, each of which is hereby incorporated by reference in its entirety. The electrical signals can comprise an electrical voltage, an electrical current, an electrical conductance or resistance, and/or a change thereof. The nanowires can have a surface passivation layer.

[00152] Substantially all visible light (e.g. >50%, >70%, or >90%) impinged on the image sensor F100 is absorbed by the subpixels (e.g. 151 and 152) and the photodiode F120. The subpixels and the photodiode absorb light with different wavelengths.

[00153] The image sensor F100 can further comprise electronic circuitry F190 operable to detect electrical signals from the subpixels and the photodiode F120.

[00154] In one specific example, each pixel F150 has two subpixels F151 and F152. Each subpixel F151 and F152 has only one nanostructure 1 (e.g. nanowires F151a and F152a), respectively. The nanowire F151a comprises silicon, has a radius of about 25 nm, and has a strong absorptance in blue wavelengths. The nanowire F152a comprises silicon, has a radius of about 40 nm and has a strong absorptance in cyan wavelengths. The nanowires F151a and F152a are about 200 nm apart but embedded in the same clad F140. Each of the pixels F150 can have more than two subpixels according to an embodiment. The nanowires can comprise other suitable materials such as mercury cadmium telluride. The nanowires can have other suitable radii from 10 nm to 250 nm.

[00155] Fig. F1B shows a schematic partial top view of the image sensor F100. As shown in exemplary Fig. F1B, the pixels F150 can have different orientations, which reduces or eliminates effects of directions of incident light.

[00156] In one embodiment, the subpixels F151 and F152 and the photodiode F120 in each pixel F150 of the image sensor F100 has color matching functions substantially the same as the color matching functions of the CIE 1931 2° Standard Observer or the CIE 1964 10° Standard Observer.

[00157] Fig. F2A shows a schematic partial cross-sectional view of an image sensor F200, according to an embodiment. The image sensor F200 comprises a substrate F210, one or more pixels F250. The substrate F210 preferably does not comprise any photodiode therein. At least one pixel F250 comprises a clad F240 and a plurality of subpixels embedded in the clad F240. Three subpixels F251, F252 and F253 are shown in Fig. F2A as an example. Each of the subpixels comprises a nanostructure 1 (e.g. a nanowire F251a in the subpixel F251, a nanowire F252a in the subpixel F252 and a nanowire F253a in the subpixel F253) extending essentially perpendicularly from the substrate F210. Space between the pixels F250 is preferably filled with a material F260.

[00158] The substrate F210 can comprise any suitable material such as silicon, silicon oxide, silicon nitride, sapphire, diamond, silicon carbide, gallium nitride, germanium, indium gallium arsenide, lead sulfide and/or a combination thereof.

[00159] The clad F240 can comprise any suitable material, such as silicon nitride, silicon oxide, etc. The clad F240 is preferably substantially transparent to visible light, preferably with a transmittance of at least 50%, more preferably at least 70%, most preferably at least 90%. In one example, the clad F240 is silicon nitride and has a cylindrical shape with a diameter of about 300 nm.

[00160] The material F260 can comprise any suitable material such as silicon dioxide. A refractive index of the material F260 is preferably smaller than a refractive index of the clad F240.

[00161] The nanostructures 1 (e.g. nanowires 251a, 252a and 253a) in the subpixels (e.g. F251, F252 and F253) have refractive indexes equal to or greater than the refractive index of the clad F240. The nanowires and the substrate F210 have different absorption spectra. For example, the nanowire F251a has strong absorptance in blue wavelengths, as shown by an exemplary absorption spectrum F281 in Fig. F2C; the nanowire F252a has a strong absorptance in green wavelengths, as shown by an exemplary absorption spectrum F282 in Fig. F2C; the nanowire F253a has a strong absorptance across the entire visible spectrum, as shown by an exemplary absorption spectrum F283 in Fig. F2C; the substrate F210 has a strong absorptance in red wavelengths, as shown by an exemplary absorption spectrum F280 in Fig. F2C. The nanowires can have different diameters and/or different materials. Each nanowire in one pixel F250 preferably has a distance of at least 100 nm, preferable at least 200nm, to a nearest neighboring nanowire in the same pixel. The nanowires in the clad F240 can be positioned at any suitable positions in the clad F240. The nanowires can have a surface passivation layer. The nanowires can comprise other suitable materials such as mercury cadmium telluride. The nanowires can have other suitable radii from 10 nm to 250 nm.

[00162] The nanostructures 1 (e.g. nanowires F251a, F252a and F253a) in the subpixels (e.g. F251, F252 and F253) are operable to generate electrical signals upon receiving light. One exemplary nanowire is a photodiode with a p-n or p-i-n junction therein, details of which can be found in U.S. Patent Application Publication Nos. 12/575,221 and 12/633,305, each of which is hereby incorporated by reference in its entirety. The electrical signals can comprise an electrical voltage, an electrical current, an electrical conductance or resistance, and/or a change thereof.

[00163] Substantially all visible light impinged on the image sensor F200 is absorbed by the subpixels (e.g. F251, F252 and F253). The subpixels absorb light with different wavelengths.

[00164] The image sensor F200 can further comprise electronic circuitry F290 operable to detect electrical signals from the subpixels.

[00165] In one specific example, each pixel F250 has three subpixelsF 251, F252 and F253. Each subpixel F251, F252 and F253 has only one nanowire F251a, F252a and F253a, respectively. The nanowire F251a comprises silicon, has a radius of about 25 nm, and has a strong absorptance in blue wavelengths. The nanowire F252a comprises silicon, has a radius of about 40 nm and has a strong absorptance in green wavelengths. The nanowire F253a comprises silicon, has a radius of about 45 nm and has a strong absorptance across the entire visible spectrum. The nanowires F251a, F252a and F253a are about 200 nm apart but embedded in the same clad F240. The clad F240 is cylindrical in shape with a diameter of about 400 nm. Each of the pixels F250 can have more than three subpixels according to an embodiment.

[00166] In another specific example, each pixel F250 has four subpixels F251, F252, F253 and F254. Each subpixel F251, F252, F253 and F254 has only one nanostructure 1 (e.g., nanowire F251a, F252a, F253a and F254a respectively). The nanowire F251a comprises silicon, has a radius of about 25 nm, and has a strong absorptance in blue wavelengths. The nanowire F252a comprises silicon, has a radius of about 40 nm and has a strong absorptance in green wavelengths. The nanowire F253a comprises silicon, has a radius of about 45 nm and has a strong absorptance across the entire visible spectrum. The nanowire F254a comprises silicon, has a radius of about 35 nm and has a strong absorptance in blue green wavelength (e.g. 400 to 550 nm). The nanowires F251a, F252a, F253a and F254a are about 200 nm apart but embedded in the same clad F240. The clad F240 is cylindrical in shape with a diameter of about 400 nm. Fig. F2D shows exemplary absorption spectra F291, F292, F293 and F294 of the nanowires F251a, F252a, F253a and F254a, respectively.

[00167] Fig. F2B shows a schematic partial top view of the image sensor F200. As shown in exemplary Fig. F2B, the pixels F250 can have different orientations, which reduces or eliminates effects of directions of incident light.

[00168] According to an embodiment, the image sensor F100 or F200 can further comprise couplers F350 above each pixel F150 or F250, as shown in Fig. F3. Each of the

couplers F350 preferably has substantially the same footprint as the pixel underneath and has a convex surface. The coupler F350 is effective to focus substantially all visible light impinged thereon into the clad F140 or F240.

[00169] According to an embodiment, as shown in Fig. F3, the image sensor F100 or F200 can further comprise an infrared filter F360, which is operable to prevent infrared light, such as light with wavelengths above 650 nm, from reaching the pixels. According to an embodiment, the image sensor F100 or F200 does not comprise an infrared filter.

[00170] According an embodiment, the nanowires can be made by a dry etching process or a Vapor Liquid Solid (VLS) growth method. Of course, it will be appreciated that other materials and/or fabrication techniques may also be used for fabricating the nanowires in keeping with the scope of the invention. For instance, nanowires fabricated from an indium arsenide (InAs) wafer or related materials could be used for IR applications.

[00171] The nanowires can also be made to have a strong absorption in wavelengths not in the visible spectrum, such as in the ultraviolet (UV) or infrared (IR) spectra. In an embodiment, each nanowire can have transistor therein or thereon.

[00172] In one embodiment, the subpixels F251, F252 and F253 in each pixel F250 of the image sensor F200 has color matching functions substantially the same as the color matching functions of the CIE 1931 2° Standard Observer or the CIE 1964 10° Standard Observer.

[00173] Fig. F4 shows exemplary color-matching functions F451, F452 and F453 of the subpixels F251, F252 and F253, respectively. The color-matching functions F461, F462 and F463 are the $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$ of the CIE standard observer.

[00174] The image sensor F100 or F200 can be used to sense and capture images. A method of sensing an image comprises projecting the image onto the image sensor FS100 or F200 using any suitable optics such as lenses and/or mirrors; detecting an electrical signal from the nanowire in each subpixel in each pixel using suitable circuitry; calculating a color of each pixel from the electrical signals of the subpixels therein.

[00175] Fig. D2 shows a simplified cross section view of a pixel in an imaging device. Each pixel includes a readout circuit D100 formed on a semiconductor substrate D101 with metal lines D103 above the substrate. As a photosensitive element, a nanostructure 1 is formed standing up from the substrate. Photo absorption takes place along the length of the nanostructure 1. The output of the nanostructure 1 can be connected to the readout circuit

D100 located in the substrate. Since the footprint of the nanostructure 1 is small, more than one nanostructure 1 can be formed in a pixel. The role of the long vertical structure of the nanostructure 1 is to absorb a certain bandwidth of light energy and generate a corresponding electrical signal and/or to guide the unabsorbed light energy to the substrate diode with minimum loss, thus performing as a waveguide. At the top end of the nanostructure 1, an optical coupler (e.g., a lens) D105 could be formed to couple the incident light into the nanostructure 1 with minimum energy loss or reflections. In this embodiment, a micro lens may be used as a coupler. The microlens may be, but not limited to, a spherical ball lens. The coupling efficiency of a spherical ball lens is typically higher than 90%. In another aspect, a binary microlens may be used as shown in Fig. D2b.

[00176] Fig. D3 shows a simplified cross section view of a pixel which has a nanostructure 1 at the back side of a thinned semiconductor substrate. The nanostructure 1 generates photo charges by absorbing light energy in a certain bandwidth and dumping the charges into the thinned substrate. The charges are then collected by readout circuits D100 in the thinned substrate using an electrical field. Also, the nanowire guides and couples unabsorbed light into the substrate D108. An advantage of employing a nanostructure 1 at the back side of the substrate D108 is the ease of fabricating the nanowires. When forming nanowires at the front side, it is necessary to remove the thick dielectric layers D104 illustrated in Fig. D2 in a region where the nanostructure 1 is supposed to be constructed. In contrast, the embodiment disclosed in Fig. D3 could be made without this removal step. Further, the nanostructure 1 may fabricated without modifying front side structure of the CMOS devices. This embodiment includes both front side metal and insulating layers D106 and backside metal and insulating layers D107. Further, as in the front side embodiment, a micro lens of an optical coupler D105 may be coupled to the nanostructure 1.

[00177] A nanostructure 1 could be configured in a variety of photodetector configurations. These configurations include: a photo conductor, a photodiode, or a photogate device. A photo conductor is a photo sensitive device whose resistivity varies as a function of incident light. A photodiode is a p-n diode or a p-i-n diode which generates electron-hole pairs as a photo charge. A photogate device is a MOS (metal-oxide-semiconductor) device with a biased gate that creates a potential well in the semiconductor and accumulates photo charge in the potential well. In the following embodiments, various configurations of photodiodes, photogate devices, or combinations of a photodiode and a photogate detector are implemented as photo detecting elements.

[00178] Fig. D4 shows a cross sectional view of a CMOS pixel with a nanostructure 1 configured as photogate device. In this embodiment, there are two photodetectors per pixel, the nanostructure 1 and a substrate diode. The nanostructure 1 with a dielectric cladding layer and a vertical gate. The role of the vertical gate surrounding the nanostructure 1 is to deplete the nanostructure 1 and create a potential well at the nanostructure 1 as shown in Fig. D5b by applying a slight bias voltage to the vertical gate. Further increase of the bias voltage would invert the surface region of the nanostructure 1. As a result, the nanostructure 1 acts similarly to a pinned photodiode, however, without impurity doping.

[00179] The electrical potential of the nanostructure 1 is not constant along the axial direction C1-C2 of the nanostructure 1. This is because the top end of the nanostructure 1 is open and influenced most by the gate bias while the bottom end of the nanostructure 1 is connected to the N-well that has positive bias voltage during reset and holds the bias after reset.

[00180] In the substrate, a p-n junction diode may be formed between the p-type substrate and n-well region. A p+ layer covers the n-well surface except the nanostructure 1 junction. This p+ shape allows receiving the photo charges coming from the nanostructure 1 and suppress the dark current due to the surface states of the substrate. Since light passing through the nanostructure 1 can illuminate the substrate diode, photo charges are generated in the substrate diode and collected in the potential well. Consequently, the potential well collects the charges both from the NW and the substrate diode. Compared to conventional CMOS pixels which utilize only a fraction of incident photons, this embodiment can enhance the quantum efficiency by utilizing most of the incident photons.

[00181] The n-well of the substrate photo diode is lightly doped so that the n-region can be easily depleted with a low bias voltage. The depleted n-well is preferred for a complete charge transfer from the substrate diode to the sense node when the transfer gate is turned on. Complete charge transfer allows for a low noise readout of the photo charges similar to CCD devices.

[00182] The sense node is formed with n+ diffusion in the substrate. The sense node is connected to an amplifying transistor, e.g., a transistor configured as a source follower transistor. A select switch transistor may be used to control the connection of the amplifier output to an output node. A reset transistor may also be connected to the sense node so that sense node is biased to VDD when the reset gate is activated. When the transfer gate is activated, the n-well is electrically connected to the sense node. Then, the n-well becomes

positively biased and a potential gradient in the nanostructure 1 is established between the n-well potential and the vertical photogate bias voltage. Fig. D8 shows a cross section view of a dual photodiode structure.

[00183] Fig. D9 shows an embodiment of a CMOS pixel with a nanostructure 1. This embodiment includes two vertical photogates (VP Gate1, VP Gate 2) around the NW, a substrate photodiode, and a readout circuit. The readout circuit includes a transfer gate (TX), a reset gate (RG), a source follower transistor, and a pixel select switch. The buffer amplifier in Fig. D9 represents the source follower transistor and the pixel select switch for simplification. In this embodiment, an upstanding nanowire is formed with an n-, i.e. lightly doped n-type or an intrinsic semiconductor so that the nanostructure 1 can be easily depleted with a low negative bias voltage from VP Gate 1. Preferably, a negative bias voltage from the vertical photogate VP Gate 1 could cause accumulation of holes at the surface of the nanostructure 1to suppress dark current due to the surface states of the nanostructure 1 as illustrated in the Fig. D5b.

[00184] The second vertical photogate VP Gate 2 could be an on/off switch. This switch could be configured to separate the photo charges generated in the nanostructure 1 from the photo charges integrated in the substrate photodiode. Photo charges are integrated in both the nanostructure 1 and substrate photodiode at the same time. The photo charges, however, are integrated in separate potential wells because the off-state of the second photogate VP Gate 2 forms a potential barrier between the NW and substrate photodiode. In this manner, signal from the nanostructure 1 and the substrate photodiodes do not mix together. These two photodiodes can be used to collect charges created by radiations of different wavelengths.

[00185] The vertical photogates implemented in this embodiment allow the ability to easily modify the potential profile in the nanostructure 1 without using a complicated ion implantation process. The conventional photogate pixel suffers from very poor quantum efficiency and poor blue response. The conventional photogate is normally made of polysilicon which covers the top surface of the substrate photodiode and absorbs short wavelengths near the blue light, thereby reducing the blue light reaching the photodiode. The vertical photogate, in contrast, does not block the light path. This is because the vertical photogate (VPG) does not lie laterally across the photodiode to control the potential profile in the semiconductor.

[00186] Additionally, as the pixel size of the image sensors scales down, the aperture size of the image sensor becomes comparable to the wavelength of light propagated. For a conventional planar type photodiode, this results in poor quantum efficiency (QE). The combination of a VPG structure with nanostructure 1, however, allows for an ultra small pixel with good QE.

[00187] The pixel of the present embodiment uses a two step process to read out the signals separately between the nanostructure 1 and substrate photodiodes. In the first step, the signal charges in the substrate photodiodes are read out. Then, the n- region in the substrate is depleted. In the second step, the second photogate VP Gate 2 may be first turned on. Next, the signal charges in the nanostructure 1 are read out.

[00188] A device of this embodiment may be operated in a "snapshot" operation. In a "snapshot" operation, preferably all of the photogates VP gate 2 in the pixel array are turned on or off at the same time. The same could be true for the transfer gate TX. To accomplish this, the second photogate VP Gates 2 are all connected with a global connection. Further, all the transfer gates TX are connected with a second global connection.

[00189] Generally, global operation of the reset gate RG should be avoided for practical reasons. In a pixel array, it is a common practice to globally reset the array row by row. If the snapshot operation is not used, individual pixel operation is possible. In this case, it is not necessary to have global connections.

[00190] Fig. D10 and Fig. D11 show embodiments of CMOS active pixels with nanowire structured p-i-n photodiodes and vertical photogates around the nanostructure 1. The nanostructure 1 can have one or more vertical photogates comprising epitaxially grown layers such as conductive layers and metal layers.

[00191] In one embodiment such as that shown in Fig. D10, the picxel could include two photodiodes, a nanostructure 1 photodiode and a substrate photodiode. This embodiment also includes two vertical photogates (VP Gate1, VP Gate 2), a transfer gate (TX) and a reset gate (RG). Preferably, both of the photodiodes are lightly doped. This is because a lightly doped region can be easily depleted with a low bias voltage.

[00192] The surface region of the substrate photodiode could be prone to defects due to process induced damage caused during fabrication and to lattice stress associated with the nanostructure 1. These defects may serve as a source for dark current.

[00193] Preferably, the substrate is connected to ground, that is, zero voltage. In this embodiment, the reset drain is preferably doped n+ and is positively biased. When the

transfer gate TX and reset gate are on, the n- region in the substrate becomes positively biased. This reset operation results in the n- region being depleted due to a reverse bias condition between the p substrate and n- region. When the transfer gate TX and reset gate RG are off, the n- region retains its positive bias, forming a floating capacitor with respect to the p-sub region.

[00194] The first vertical photogate VP Gate 1 could be configured to control the potential in the nanostructure 1 so that a potential gradient can be formed between the NW photodiode and the substrate photodiode. In this way, photo charges in the nanostructure 1 can drift quickly to the n- region of the substrate during readout. The second vertical photogate VP Gate 2 could be an on/off switch.

[00195] Fig. D12 and Fig. D13 show embodiments of back-side illuminated image sensors. The nanostructure 1 could be formed at the back side of a p-substrate. The substrate may be thinned by removing semiconductor substrate material over the area containing the pixel array. For example, a p-substrate can be thinned to a thickness between 3 and 50 microns, more preferably, between 6 and 20 microns. The substrate photodiode could now get all of its light from the back-side and not from the side containing all the metal lines as in conventional image sensors.

[00196] The front side could include a 4-T readout circuit including a transfer gate TX, a reset switch with a reset gate RG, a source follower amplifier, and a select switch. The readout circuits also could be configured as a 3-T pixel circuit including, a reset switch with a reset gate RG, a source follower amplifier, and a select switch. In the front side, a substrate photodiode may be formed with a shallow p+ layer as shown in Fig. D12 and Fig. D13. The purpose of having p+ at both sides of the substrate is to suppress dark current. A buried p layer could be placed underneath the n+ diffusion layer to block incoming charge flow from the backside and deflect the charges toward the n- region. Preferably, doping of the buried p layer is higher than that of the p- substrate, but not as high as that of the p+ layer. The front side photodiode is not for photo absorption, but rather for collecting the charges coming from the nanostructure 1 and from the backside p- substrate where photon absorption takes place. The nanostructure 1 could have a dielectric layer (cladding layer) surrounding the NW and two vertical photogates, one for the switch and the other for controlling the potential in the NW.

[00197] Typically, in the embodiments of Fig. D12 and Fig. D13, a two step process is used to read out the signal charges separately from each of the photodiodes. The first step

would be to read out the charges from the substrate diode at the front side. Immediately after this, by turning on the VP Gate 1, the charges from the nanostructure 1 would be read out.

[00198] Preferably, the embodiments of Fig. D12 and Fig. D13 should have a shallow p+ layer at the backside substrate with a hole in the center so that the p+ layer does not block the charges coming from the backside nanostructure 1. Also, preferably, at the front side there should be a lightly doped n-well or n- layer underneath the shallow p+ layer so that n-well could be easily depleted.

[00199] Fig. D13 shows an alternative embodiment of a backside illuminated CMOS pixel. In this embodiment, instead of having vertical photogate for the nanostructure 1, the p+ layer could be coated at the outer shell of the NW to help create a built-in electric field in the nanostructure 1. With this configuration, photo charges can easily drift in the upward direction. The features of the back-side illumination CMOS pixel are similar to those of the pixel of Fig. D12.

[00200] Fig. D23C is an embodiment showing nanostructures 1 on the back-side of a fully processed wafer containing substrate photodiodes. Fig. D23D is an embodiment showing nanostructures 1 on the back-side of a fully processed wafer containing substrate photodiodes. The substrate photodiodes absorb the radiation that was not allowed to propagate in the nanowires. Examples of the structures of the backside thinned image sensor having photodiodes therein are shown in Fig. D24A and Fig. D24B.

[00201] The foregoing detailed description has set forth various embodiments of the devices and/or processes by the use of diagrams, flowcharts, and/or examples. Insofar as such diagrams, flowcharts, and/or examples contain one or more functions and/or operations, it will be understood by those within the art that each function and/or operation within such diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof.

[00202] Those skilled in the art will recognize that it is common within the art to describe devices and/or processes in the fashion set forth herein, and thereafter use engineering practices to integrate such described devices and/or processes into data processing systems. That is, at least a portion of the devices and/or processes described herein can be integrated into a data processing system via a reasonable amount of experimentation.

[00203] The subject matter described herein sometimes illustrates different components contained within, or connected with, other components. It is to be understood that such depicted architectures are merely exemplary, and that in fact many other

architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermediate components.

[00204] With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various singular/plural permutations may be expressly set forth herein for sake of clarity.

[00205] All references, including but not limited to patents, patent applications, and non-patent literature are hereby incorporated by reference herein in their entirety.

[00206] While various aspects and embodiments have been disclosed herein, other aspects and embodiments will be apparent to those skilled in the art. The various aspects and embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

We Claim:

1. A device comprising:

a substrate;

one or more of a nanostructure extending essentially perpendicularly from the substrate;

wherein the nanostructure comprises a core of a doped semiconductor of a first type, a first layer comprising a lightly doped amorphous semiconductor or an intrinsic amorphous semiconductor, and a second layer comprising a heavily doped amorphous semiconductor layer of a second type opposite from the first type, wherein the first layer is disposed on the core and the second layer is disposed on the first layer.

2. The device of Claim 1, wherein the first layer is configured to passivate at least a surface of the core.

3. The device of Claim 1, wherein the first layer is disposed isotropically over at least an end portion of the core away from the substrate.

4. The device of Claim 3, wherein the second layer is disposed isotropically over at least a portion of the first layer.

5. The device of Claim 1, wherein the first layer is disposed on an end surface of the core away from the substrate.

6. The device of Claim 5, wherein the second layer is disposed on the first layer.

7. The device of Claim 6, wherein the first layer and the second layer are coextensive with the core in at least a direction parallel to the substrate.

8. The device of Claim 5, wherein sidewalls of the core are at least partially covered by an electrically insulating layer.

9. The device of Claim 8, wherein the first layer and the second layer are coextensive with the electrically insulating layer in at least a direction parallel to the substrate.

10. The device of Claim 1, wherein the core comprises one or more doped semiconductor material selected from the group consisting of doped silicon, doped germanium, doped III-V group compound semiconductor, doped II-VI group compound semiconductor, and doped quaternary semiconductor; wherein the first layer comprises one or more intrinsic amorphous semiconductor material selected from the group consisting intrinsic amorphous silicon, intrinsic amorphous germanium, intrinsic amorphous III-V group compound semiconductor and intrinsic amorphous II-VI group compound semiconductor; and wherein the second layer comprises one or more heavily doped amorphous semiconductor material selected from the group consisting heavily doped amorphous silicon, heavily doped amorphous germanium, heavily doped amorphous III-V group compound semiconductor and heavily doped amorphous II-VI group compound semiconductor.

11. The device of Claim 1, wherein the core is lightly doped.

12. The device of Claim 1, wherein the first layer has a thickness of about 2 nm to about 100 nm.

13. The device of Claim 1, wherein the second layer has a thickness of at least about 10 nm.

14. The device of Claim 1, wherein the second layer, the first layer and the core form a p-i-n junction.

15. The device of Claim 1, wherein the nanostructure is a nanowire or a nanoslab.

16. A method of manufacturing the device of Claim 1, comprising depositing the first layer on the core by atomic layer deposition (ALD) or chemical vapor deposition (CVD); and depositing the second layer on the first layer by ALD or CVD.

17. A device comprising:

a substrate;

one or more of a nanostructure extending essentially perpendicularly from the substrate;

wherein the nanostructure comprises a core and a passivation layer, the passivation layer configured to passivate at least a surface of the core and configured to form a p-i-n junction with the core.

18. The device of Claim 17, wherein the passivation layer comprises an amorphous material.

19. A device comprising:

a substrate;

one or more of a nanostructure extending essentially perpendicularly from the substrate;

wherein the nanostructure comprises a core and a passivation layer, the passivation layer configured to passivate at least a surface of the core;

wherein the device is configured to convert light to electricity.

20. The device of Claim 19, wherein the passivation layer is configured to form a p-i-n junction with the core and the p-i-n junction is functional to convert light to electricity.

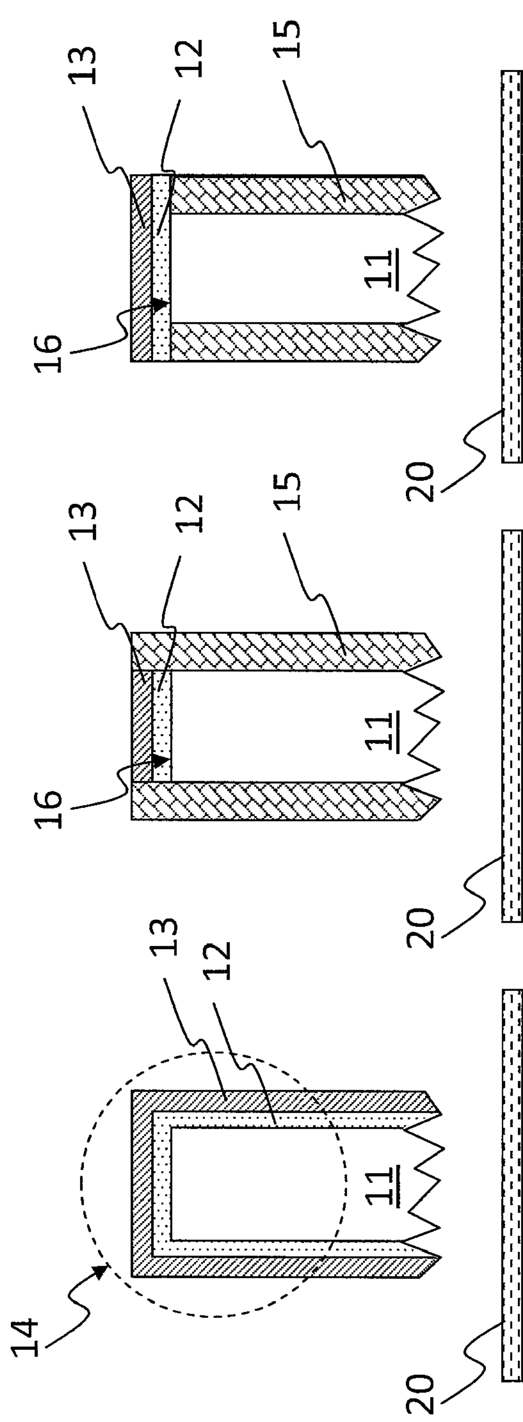


Fig. 1A

Fig. 1B

Fig. 1C

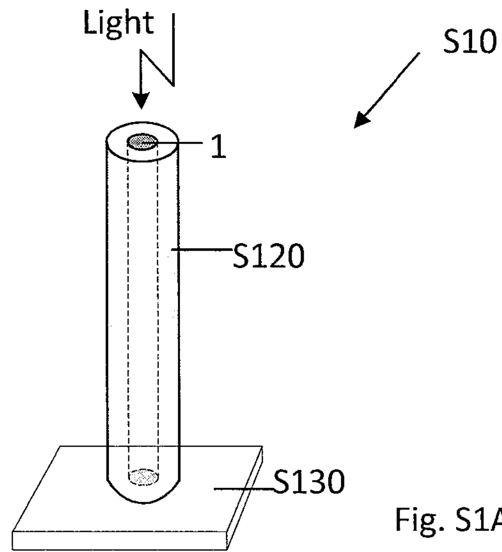


Fig. S1A

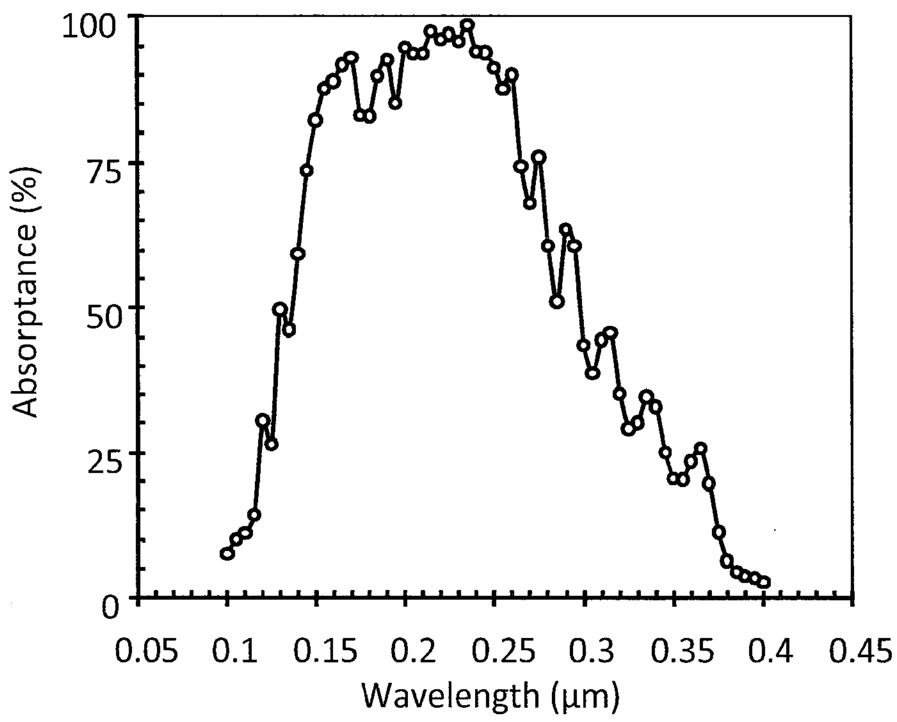


Fig. S1B

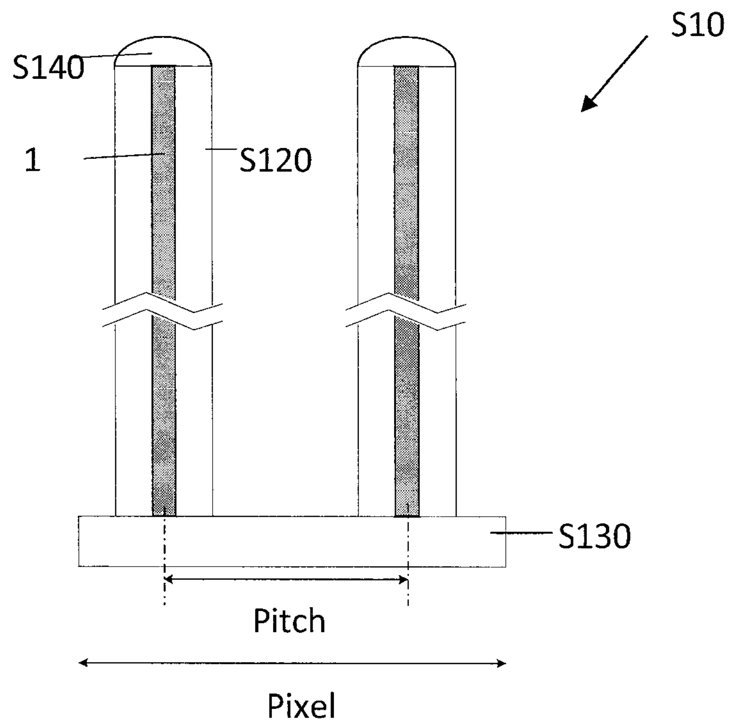


Fig. S1C

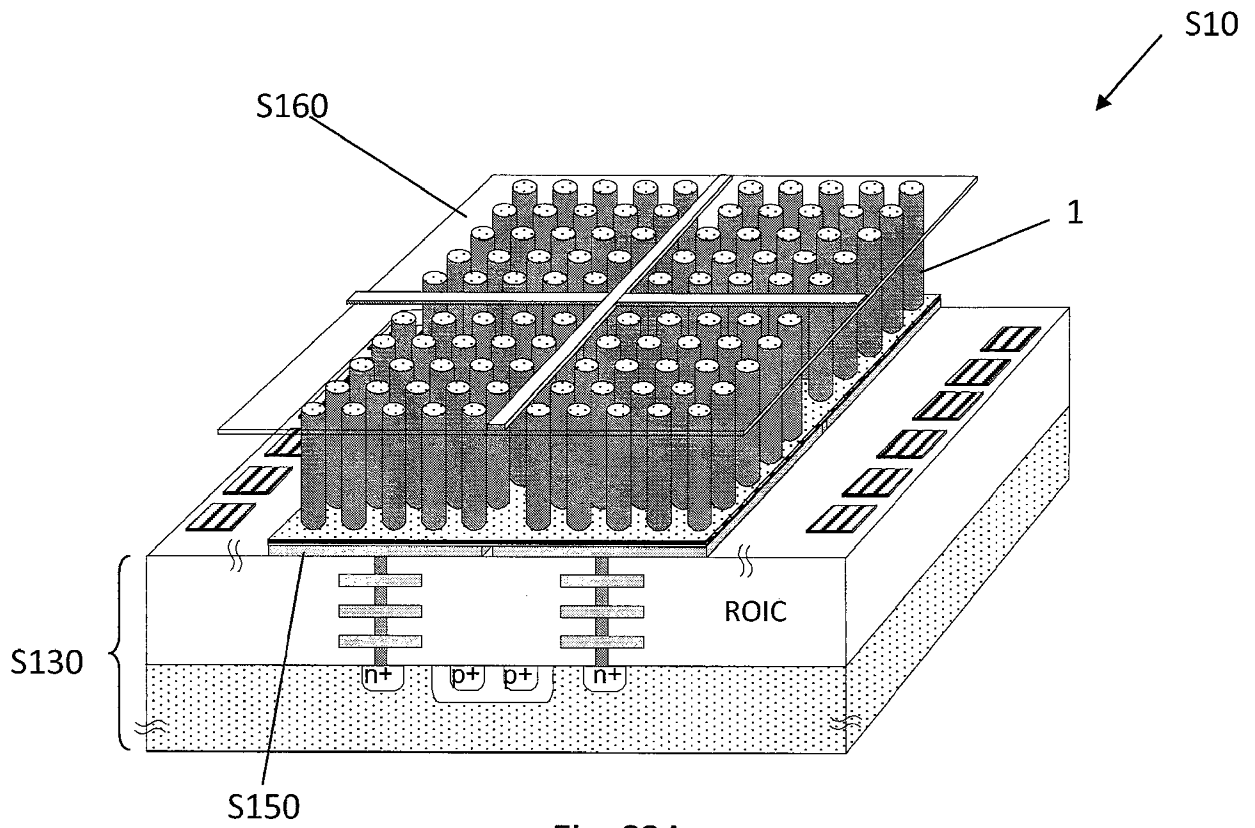


Fig. S2A

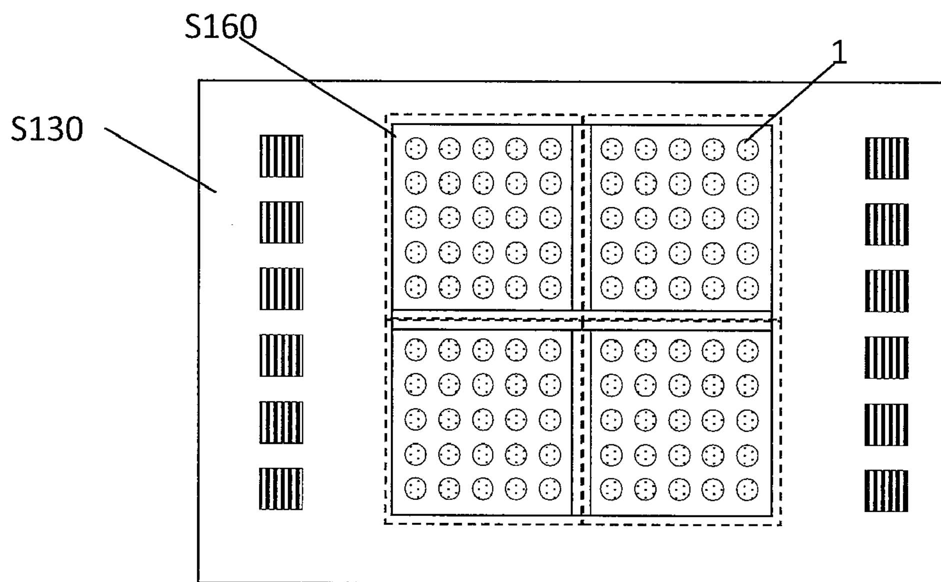


Fig. S2B

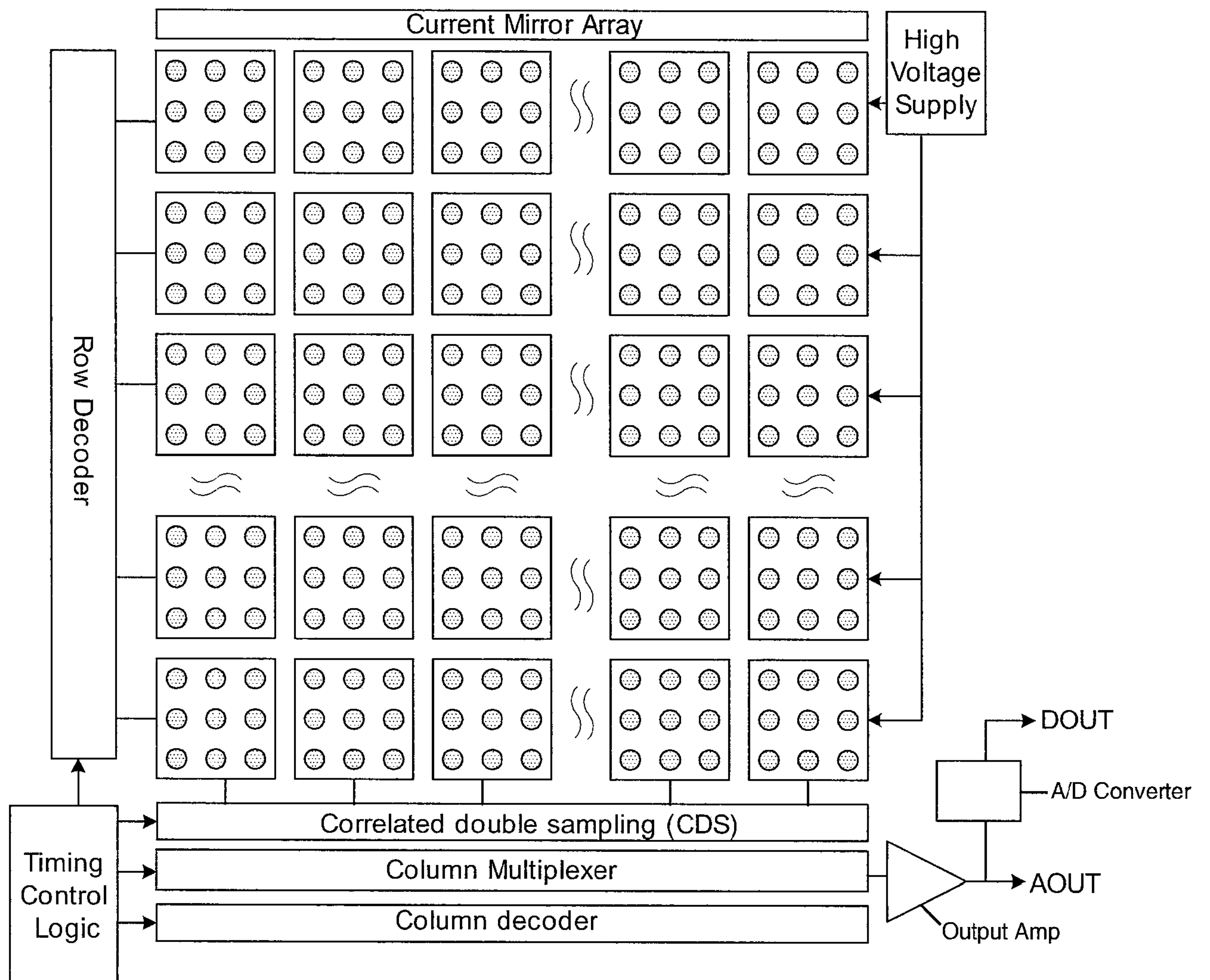


Fig. S9

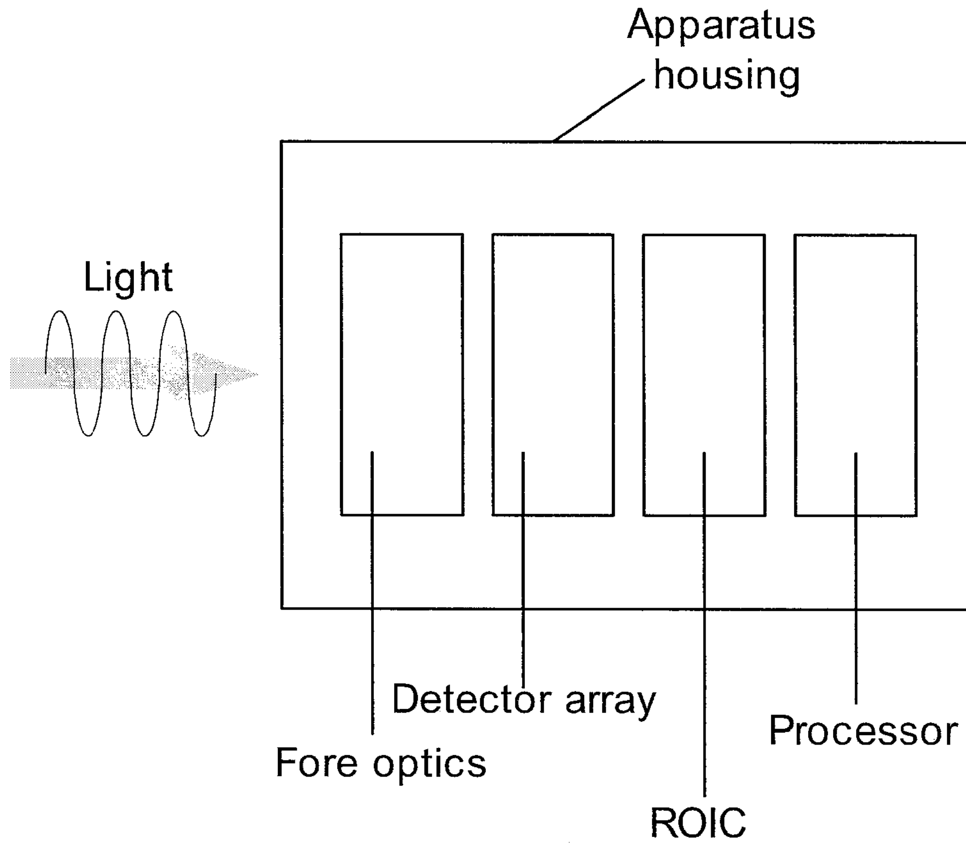


Fig. S10

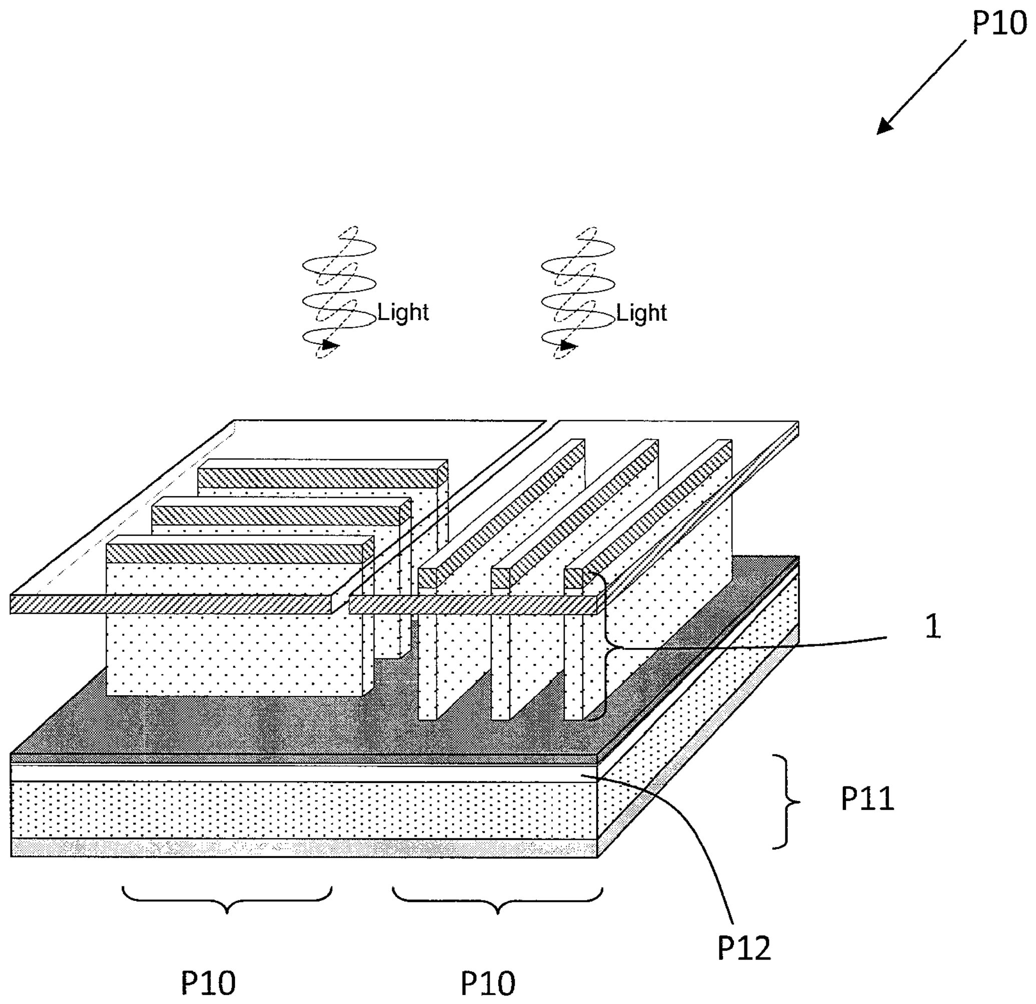


Fig. P1

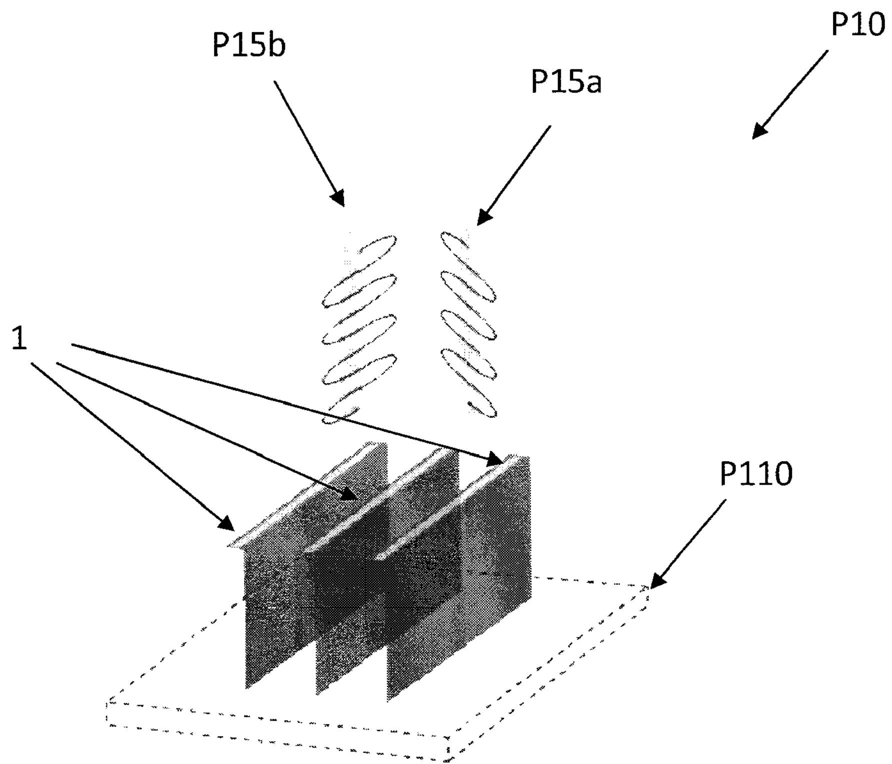


Fig. P2

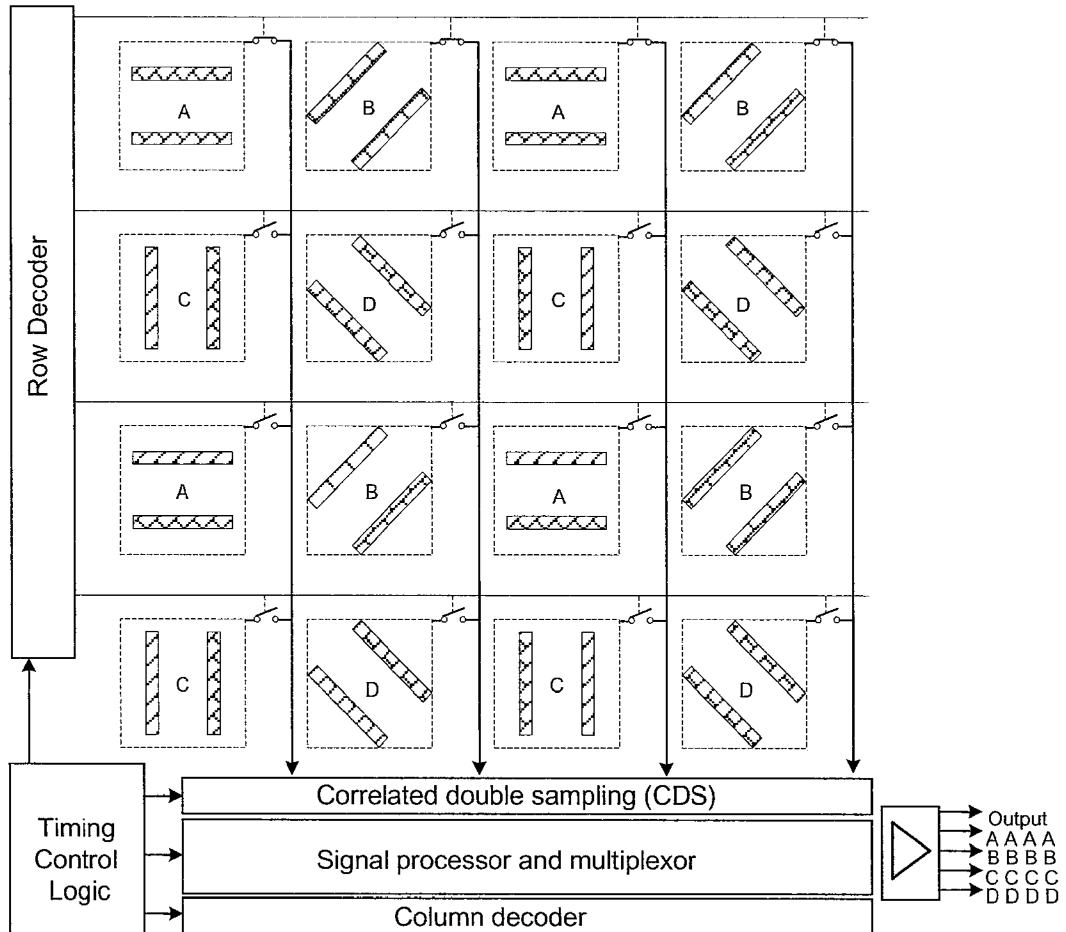


Fig. P10

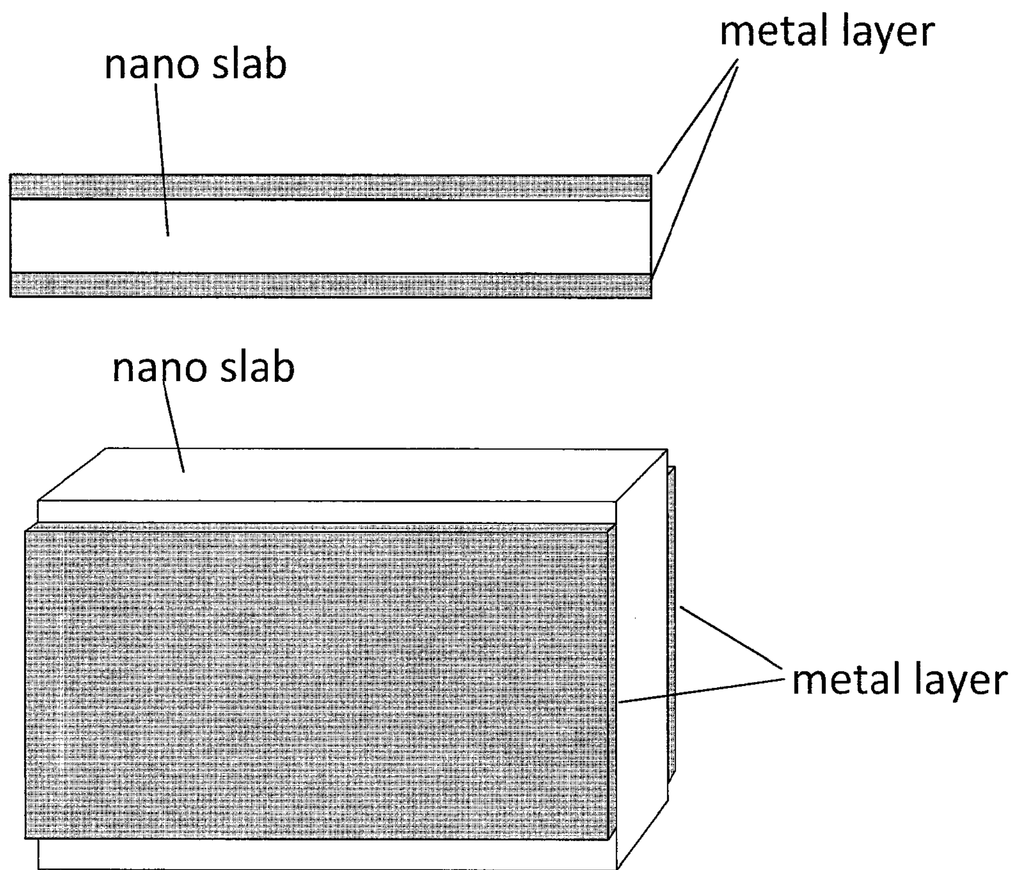


Fig. P12

V224
V260
V231
V240
V232
V230
V230
V250
V251
V252
V232
V220
V230
V230
V205

Fig. V2A

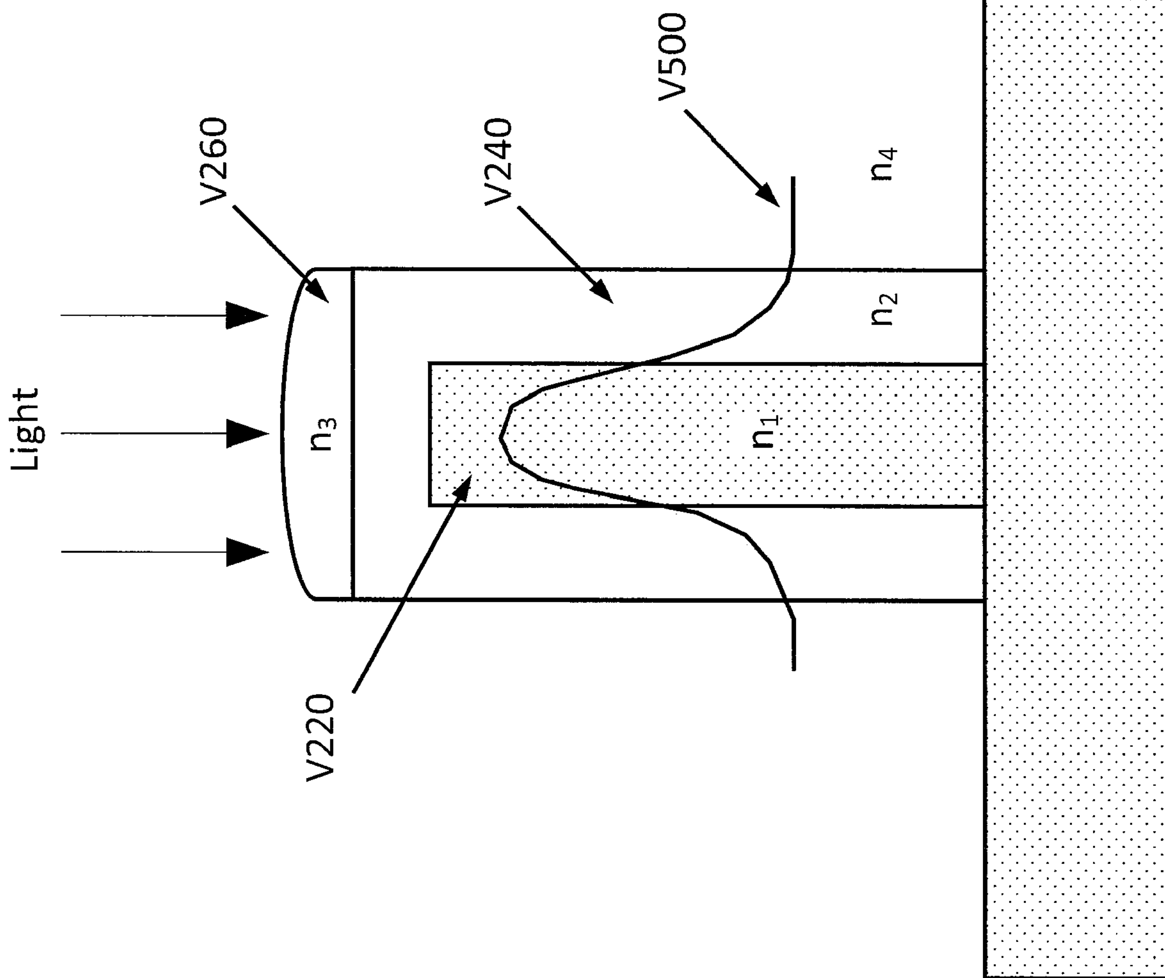


Fig. V5

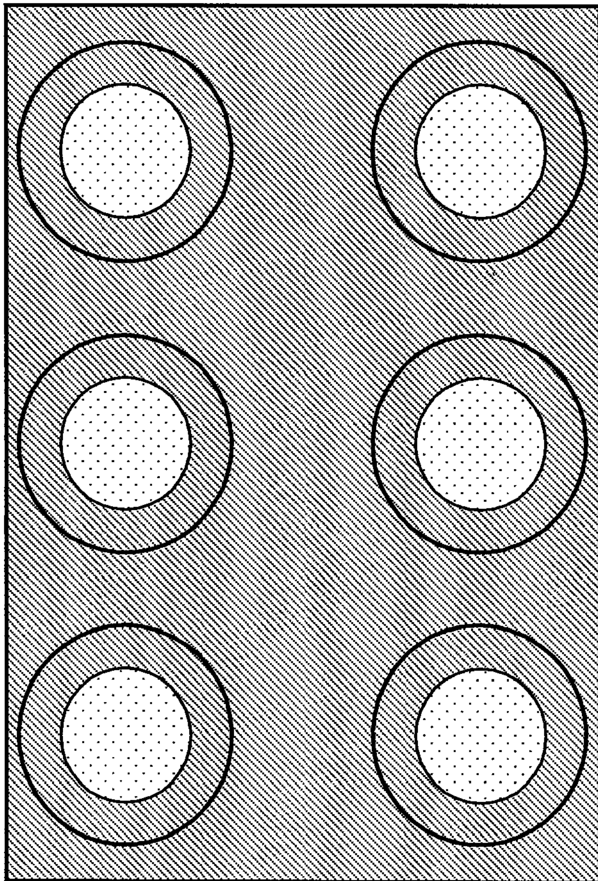


Fig. V6

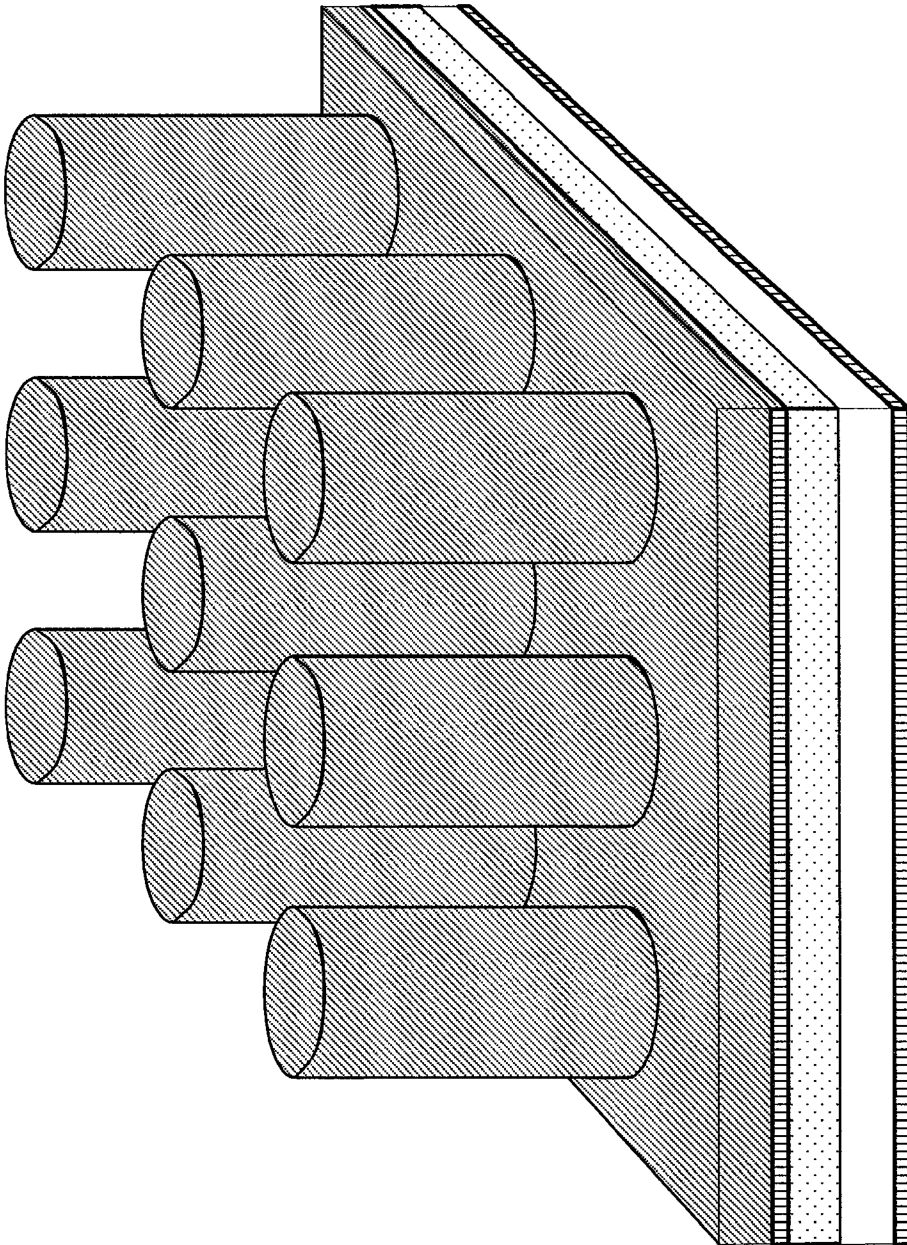


Fig. V7

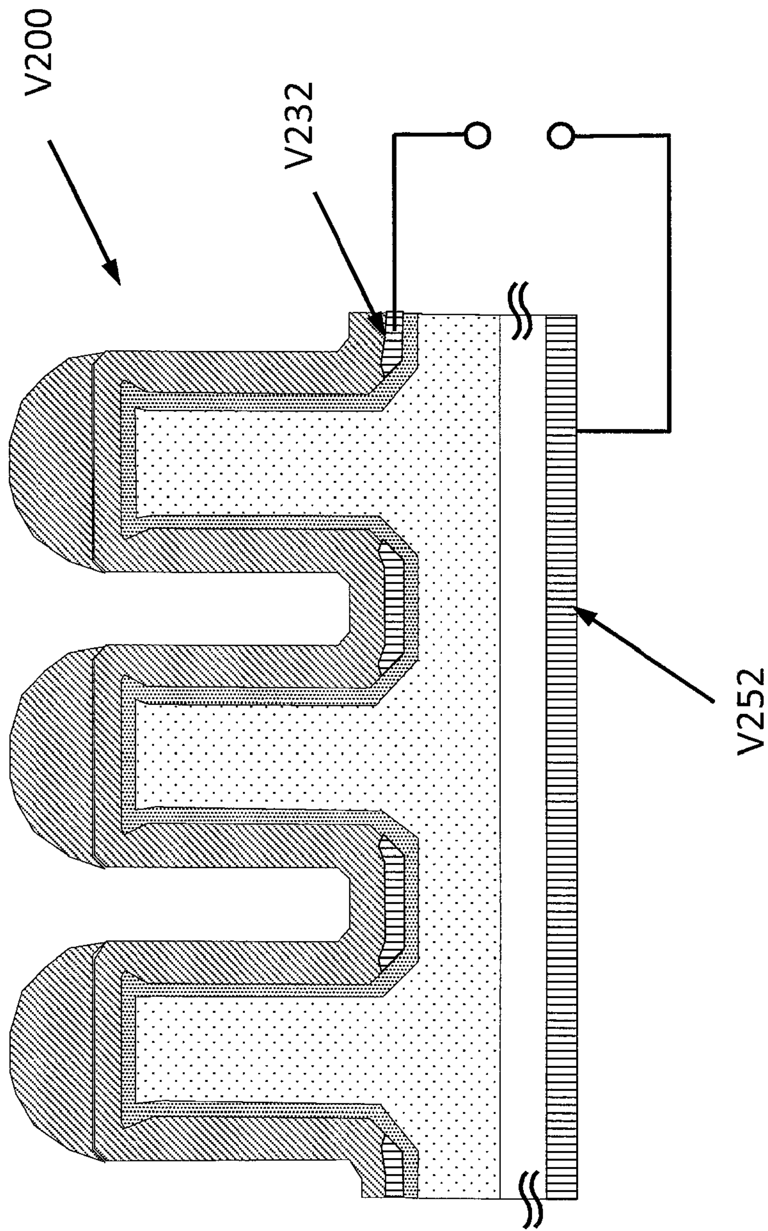


Fig. V8B

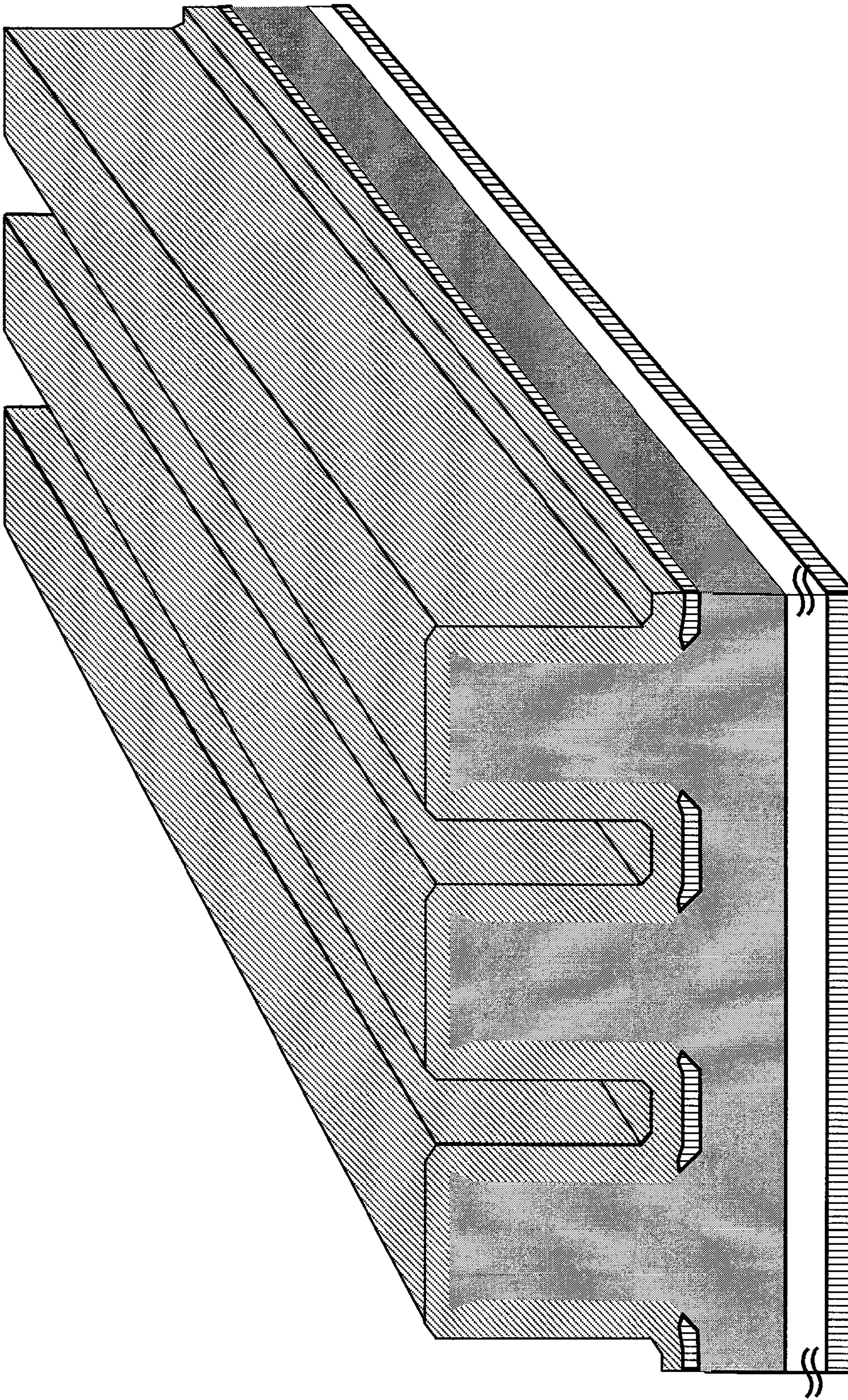


Fig. V9

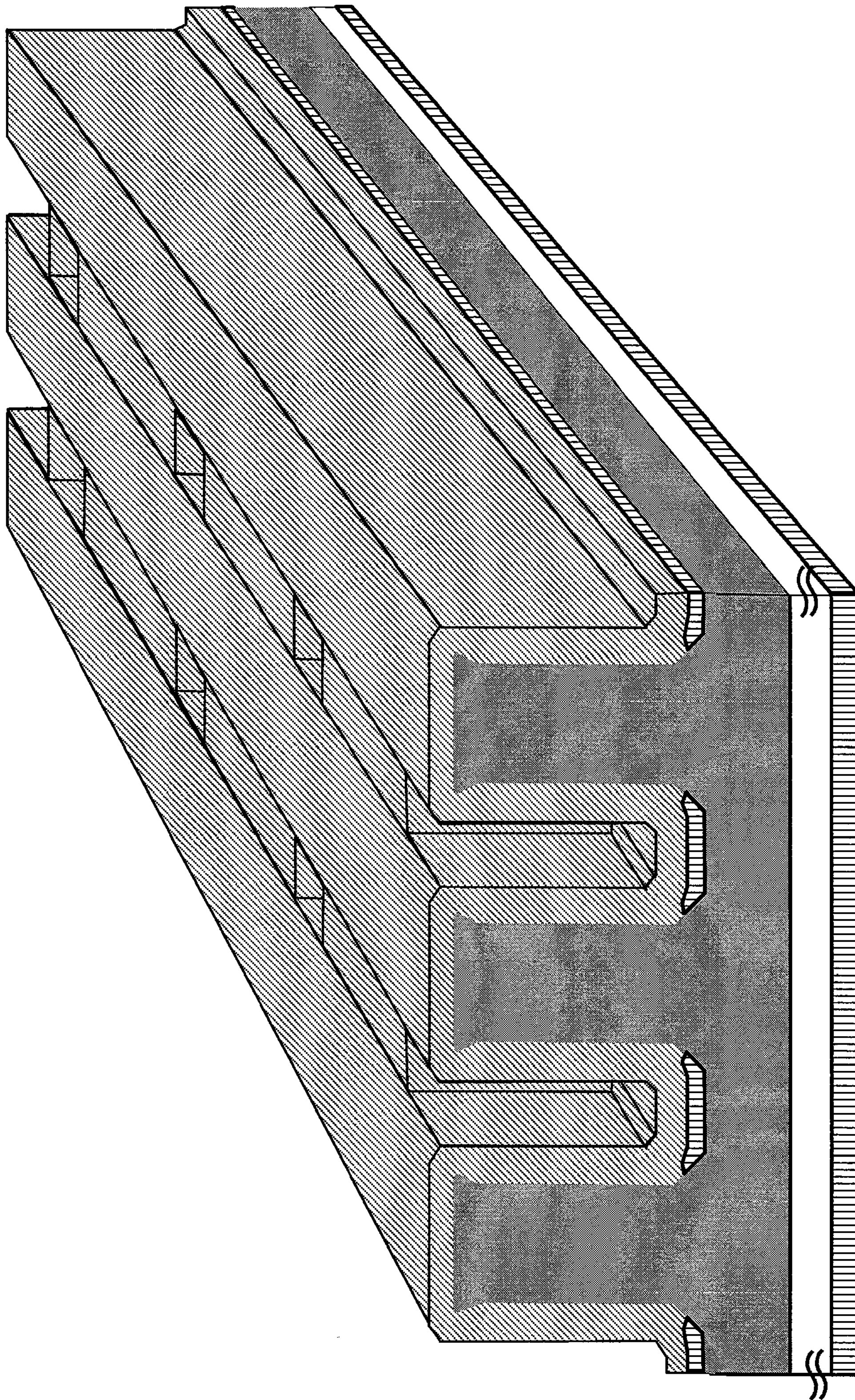


Fig. V10

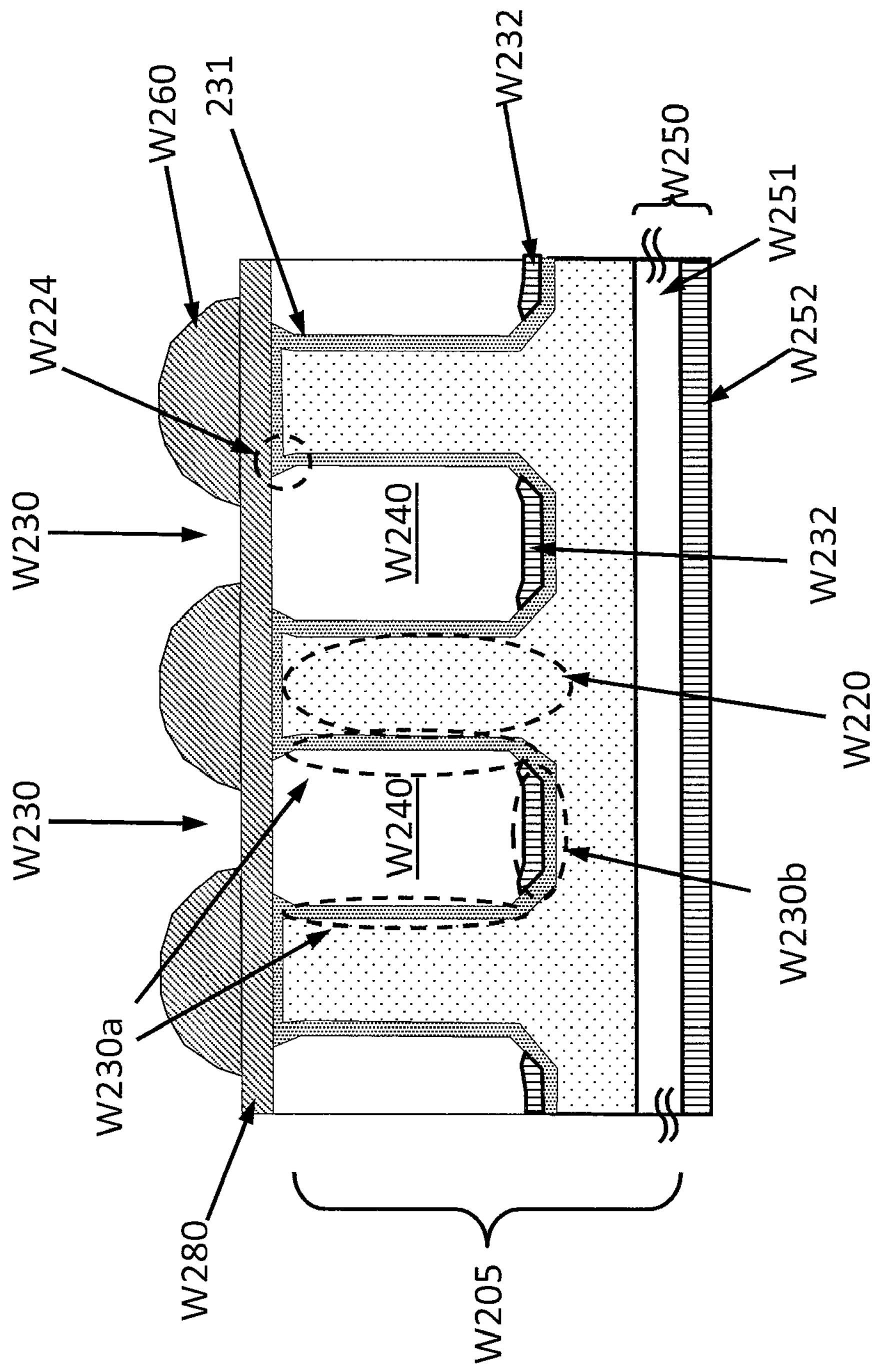
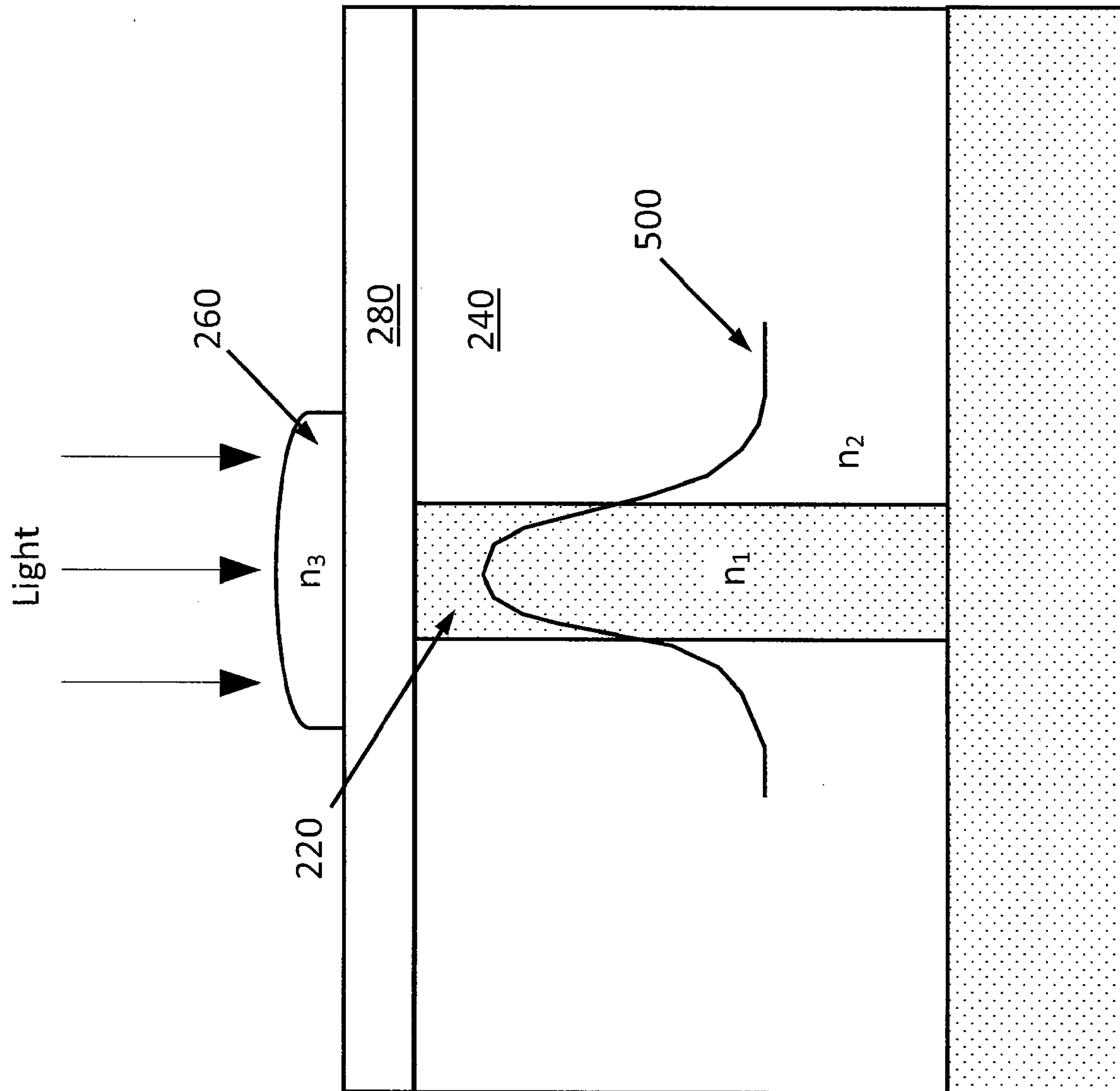


Fig. W2A

Fig. W5



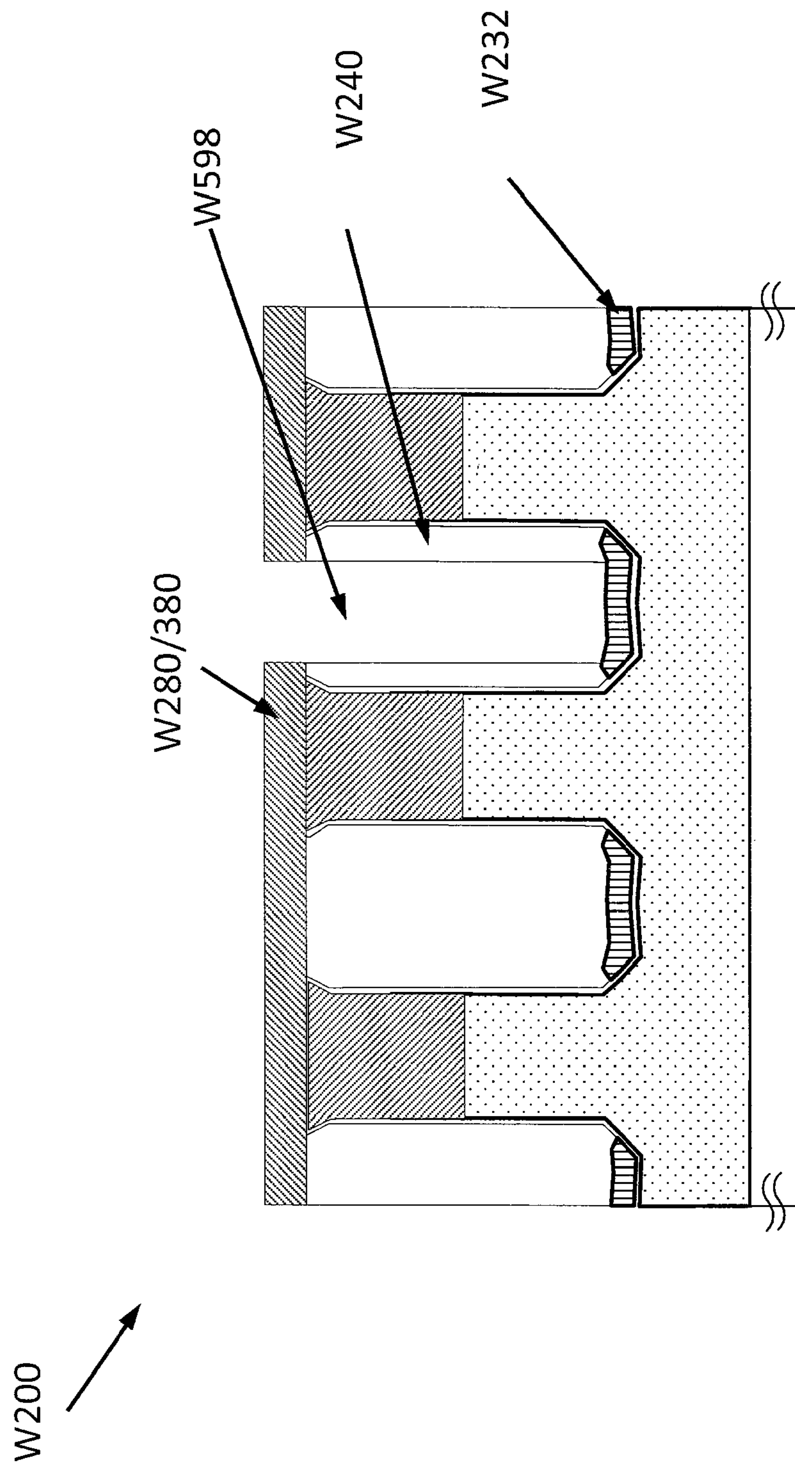


Fig. W11A

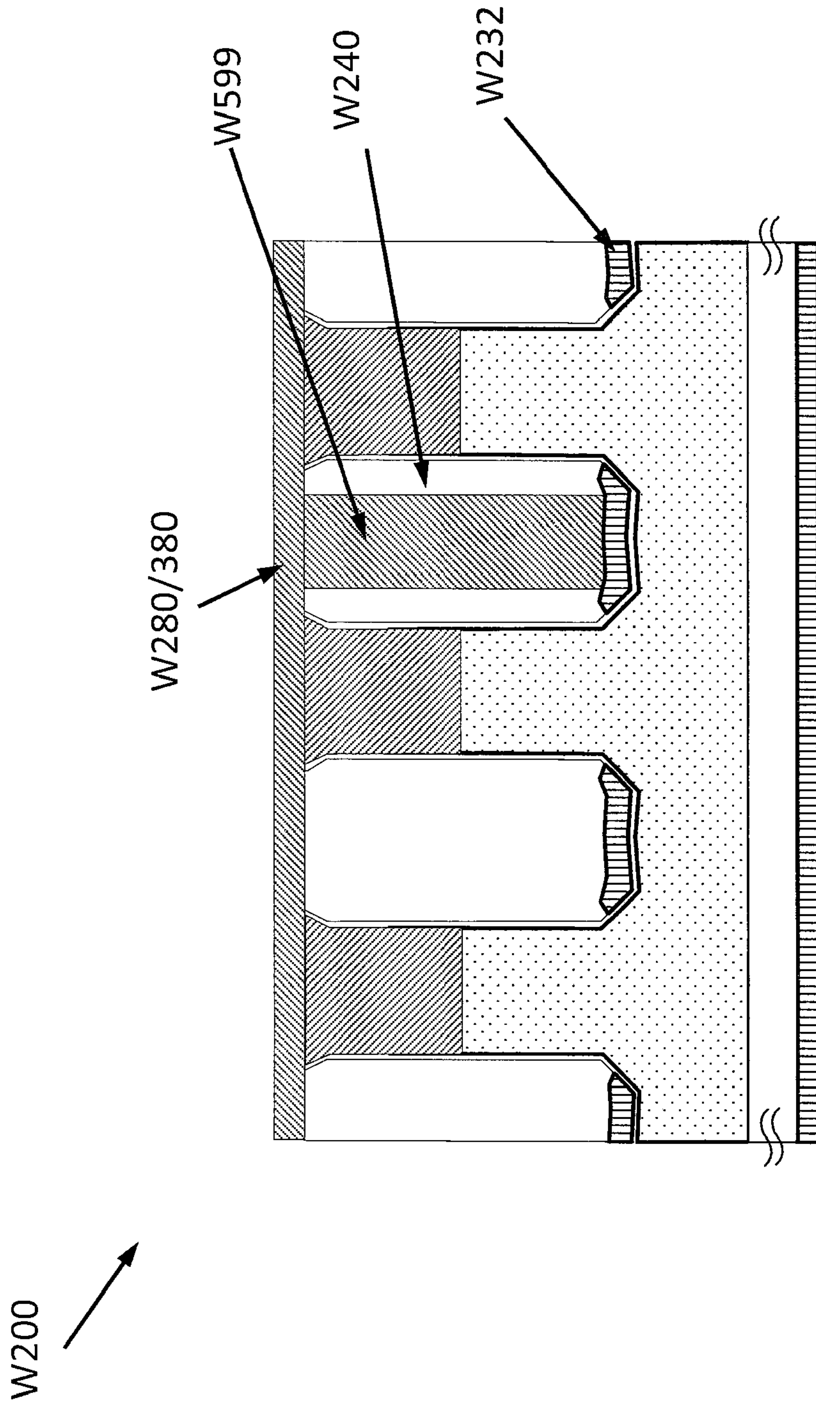


Fig. W11B

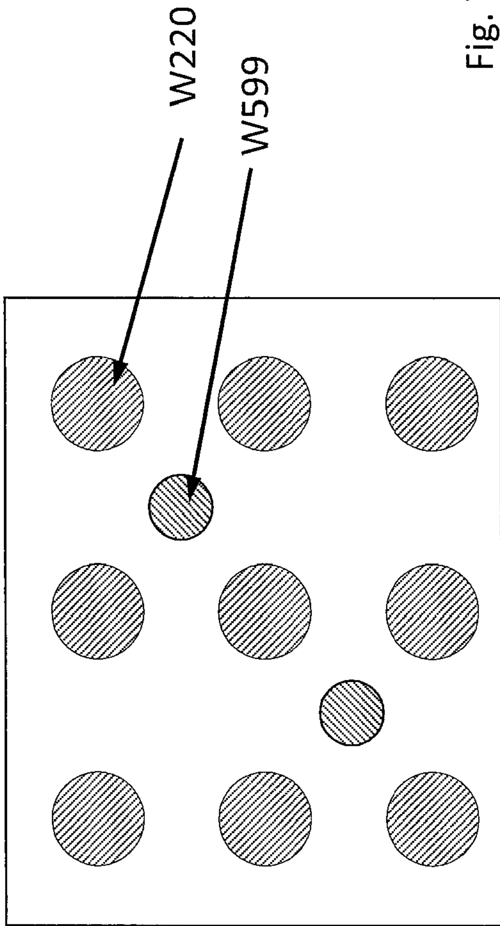


Fig. W12A

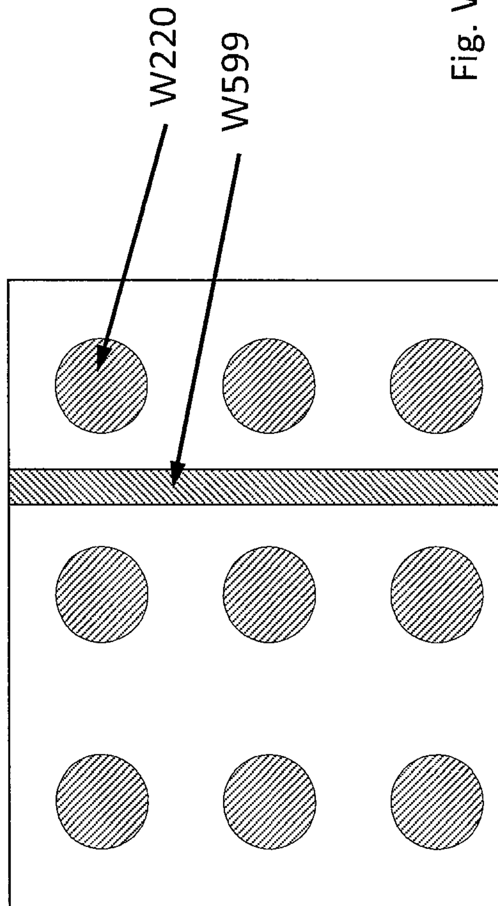


Fig. W12B

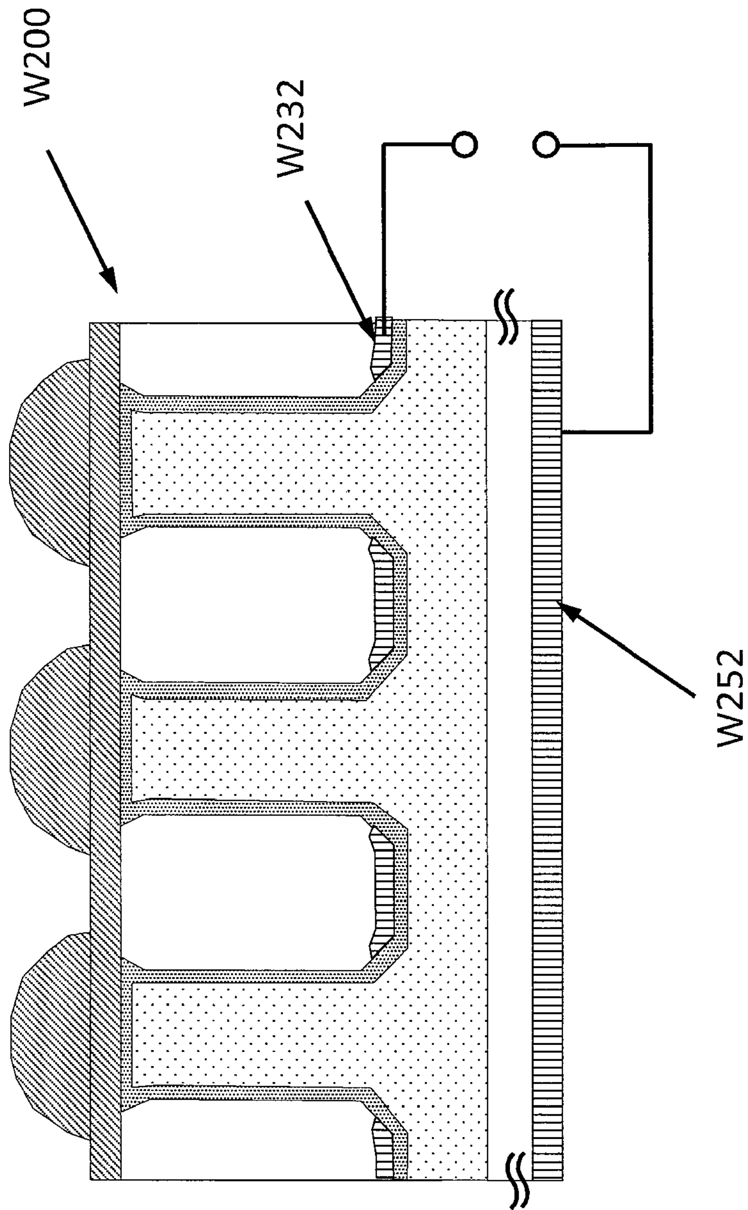


Fig. W8B

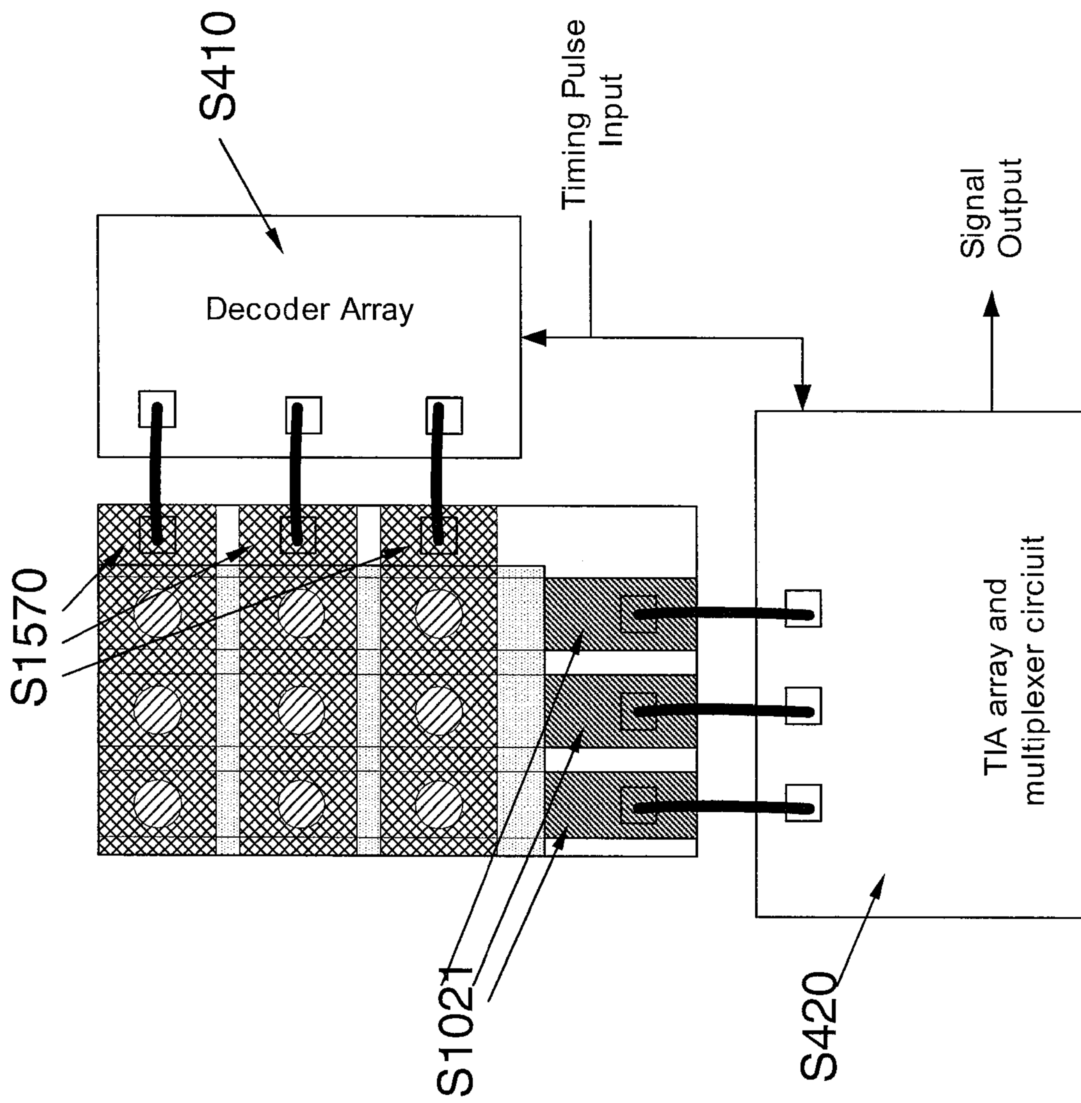


FIG. S4

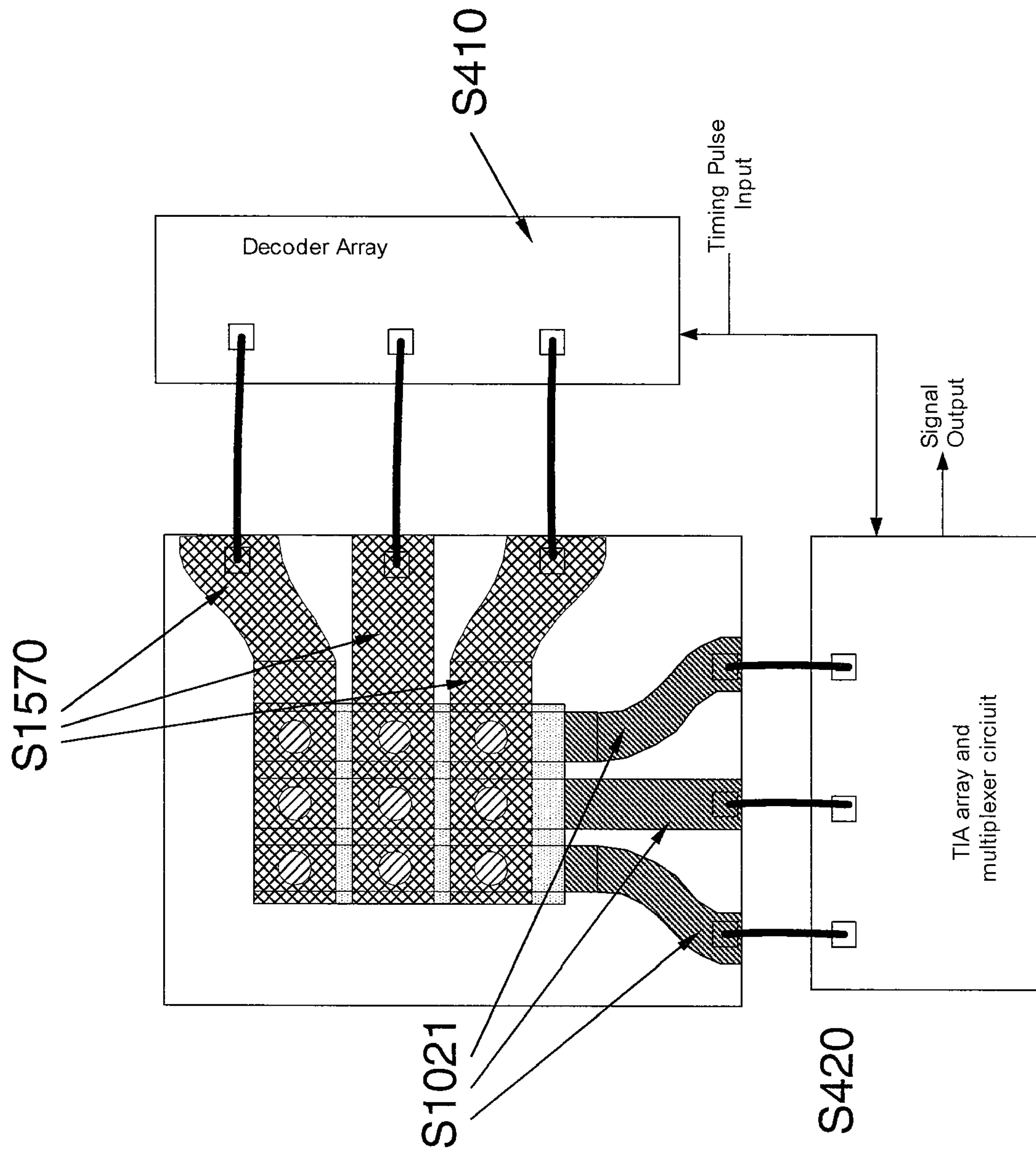


FIG. S5

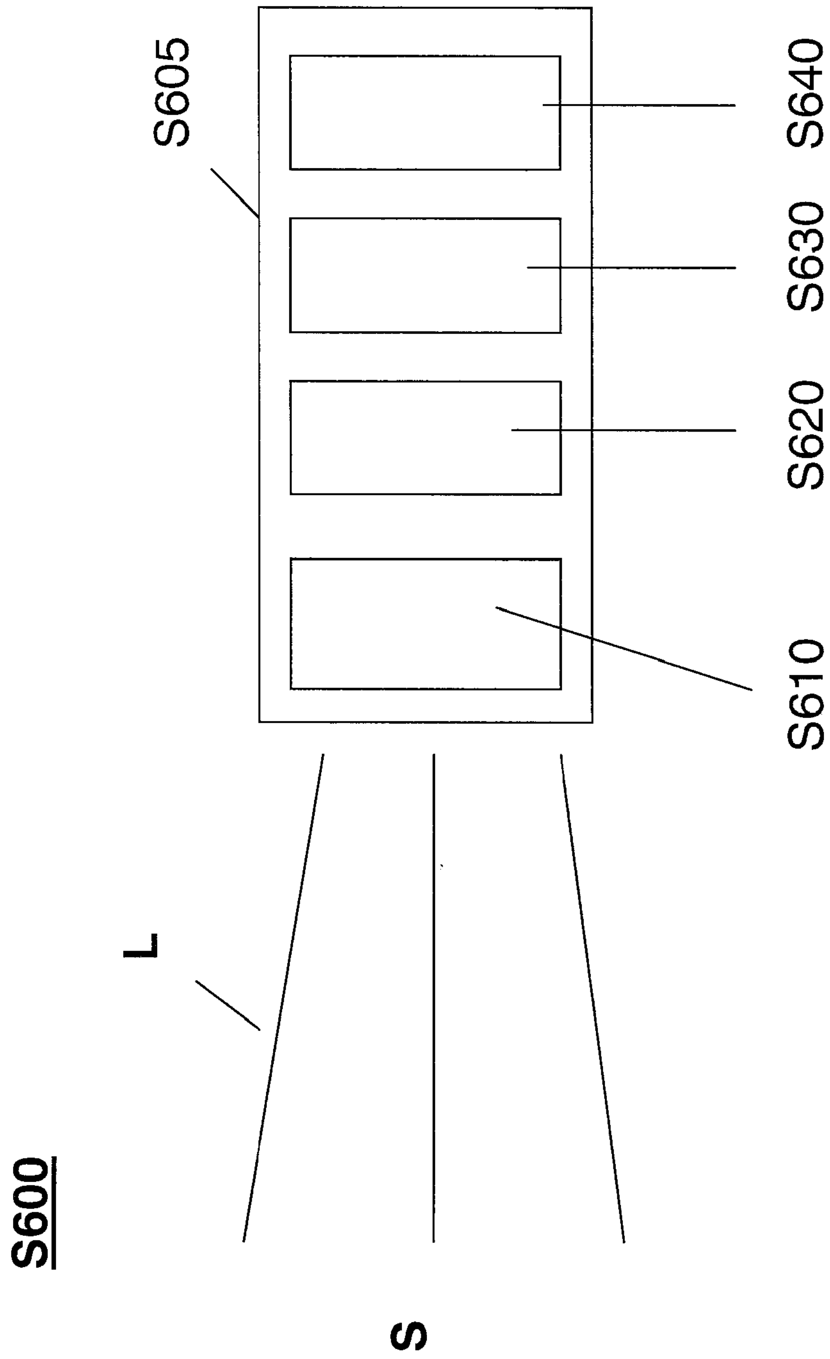


FIG. S6

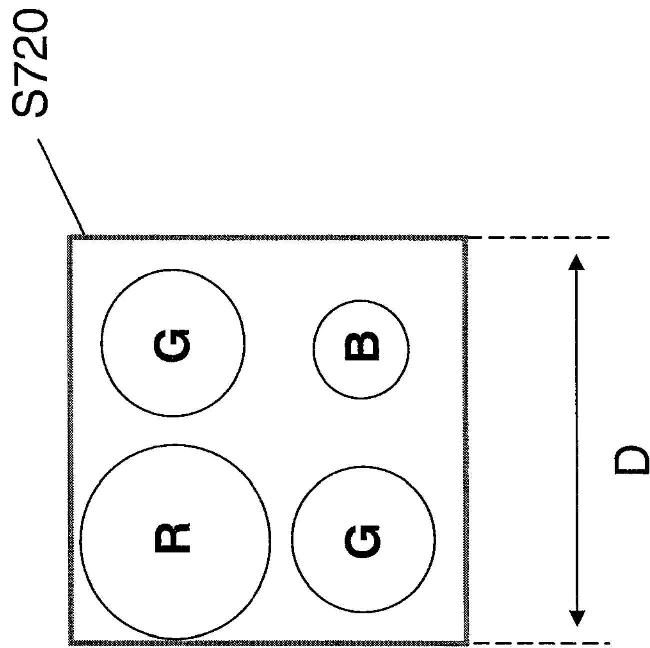


FIG. S7B

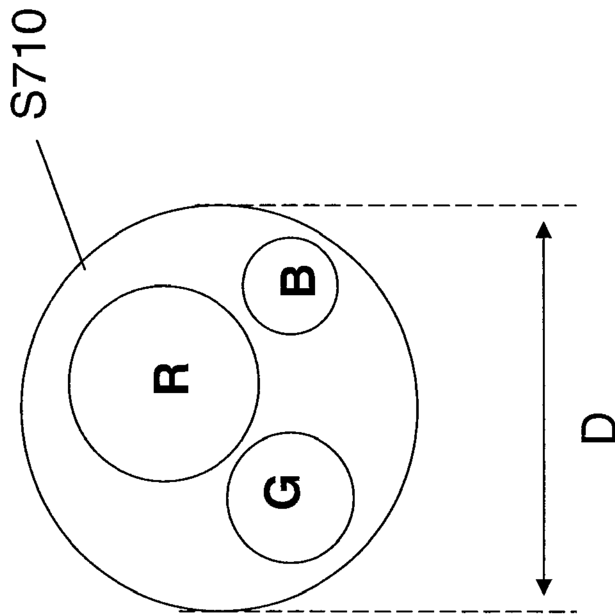


FIG. S7A

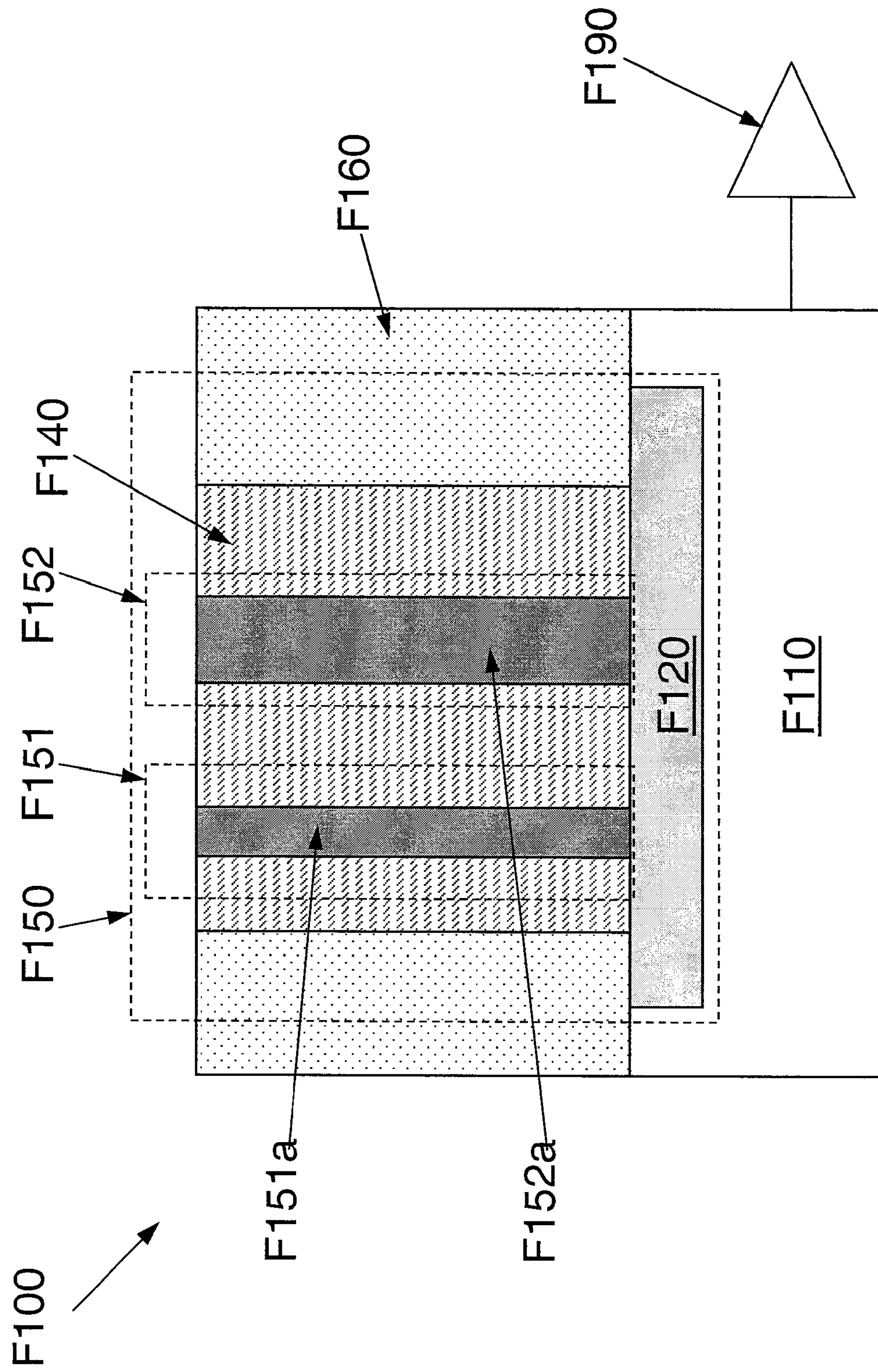


Fig. F1A

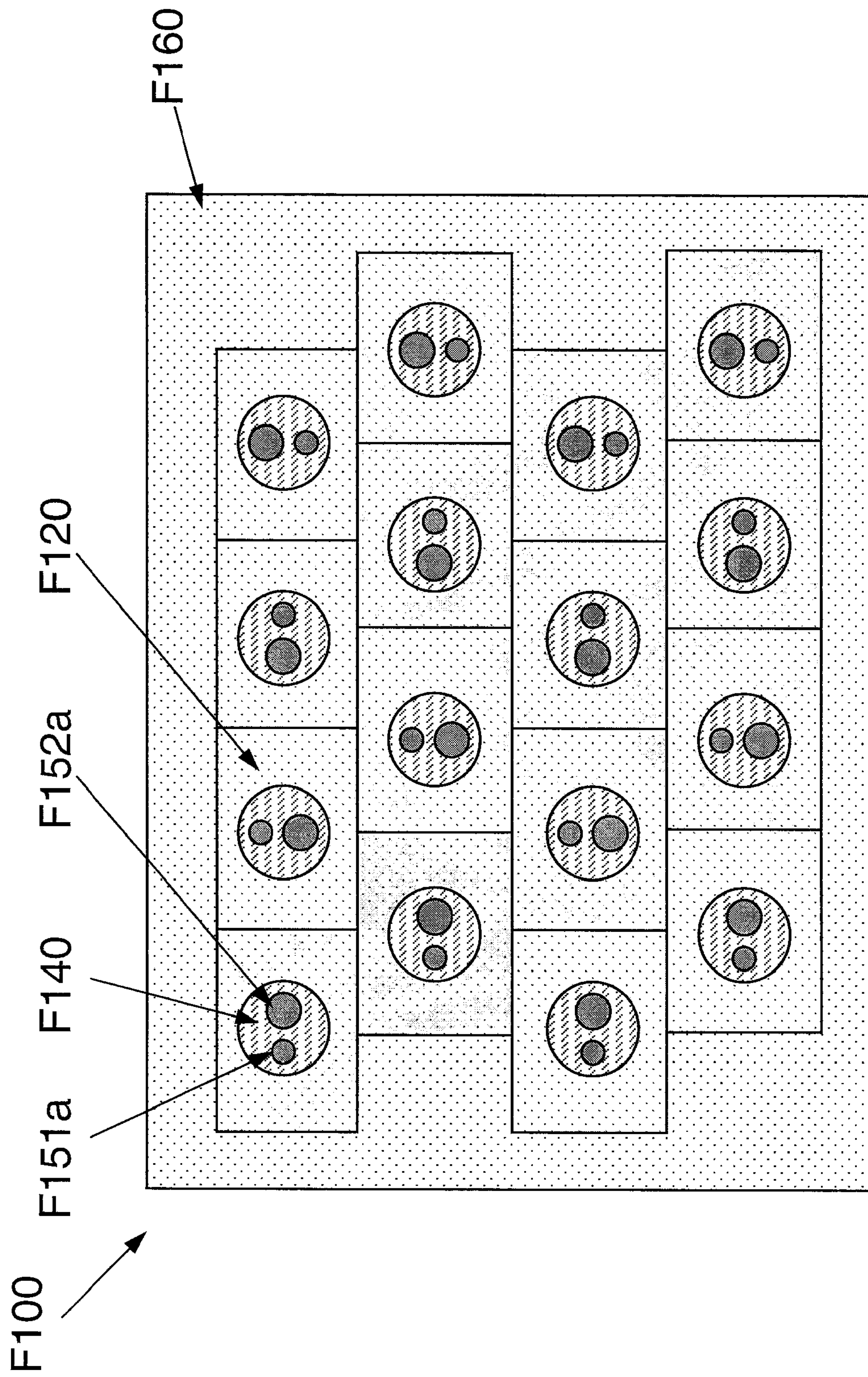


Fig. F1B

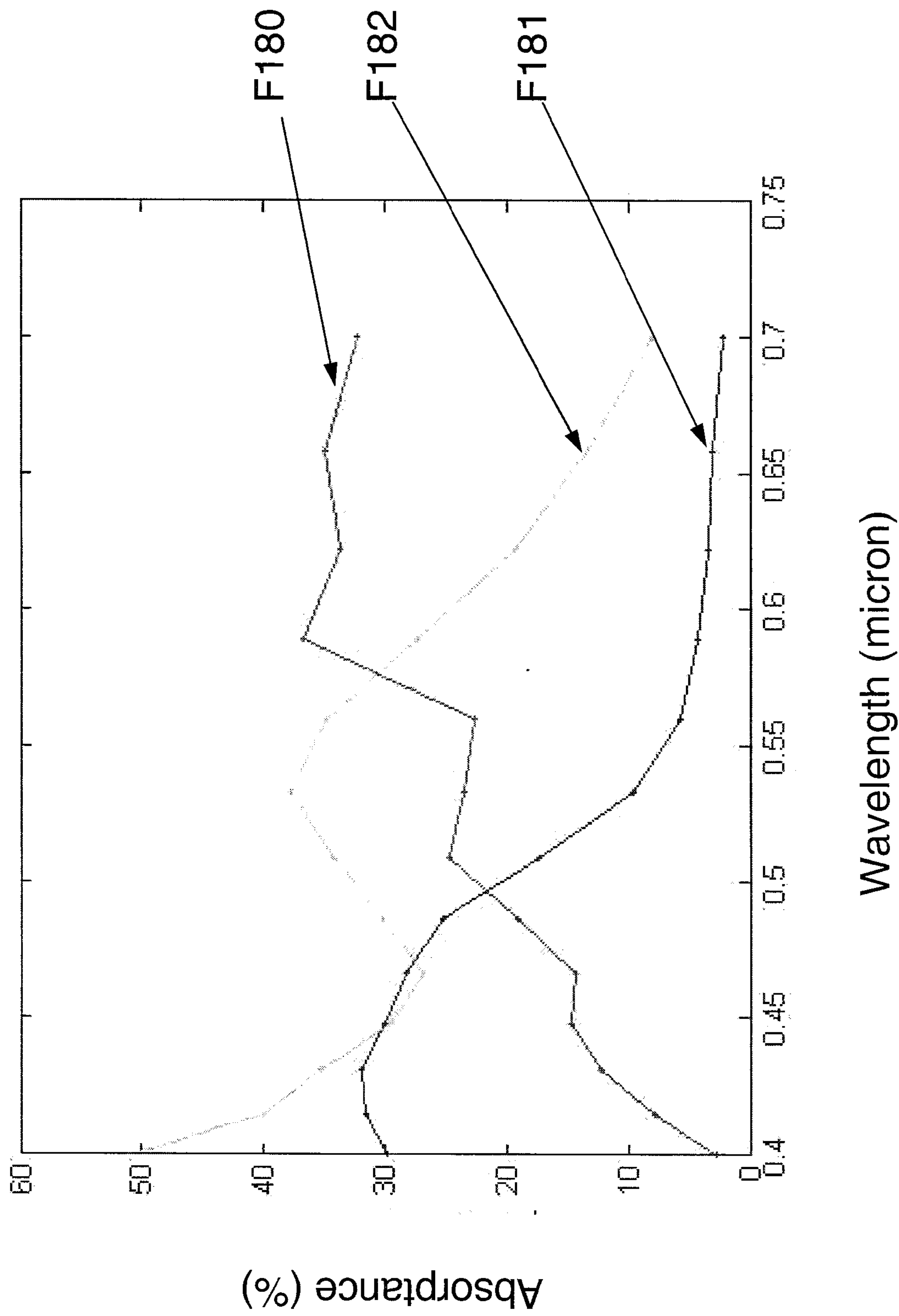


Fig. F1C

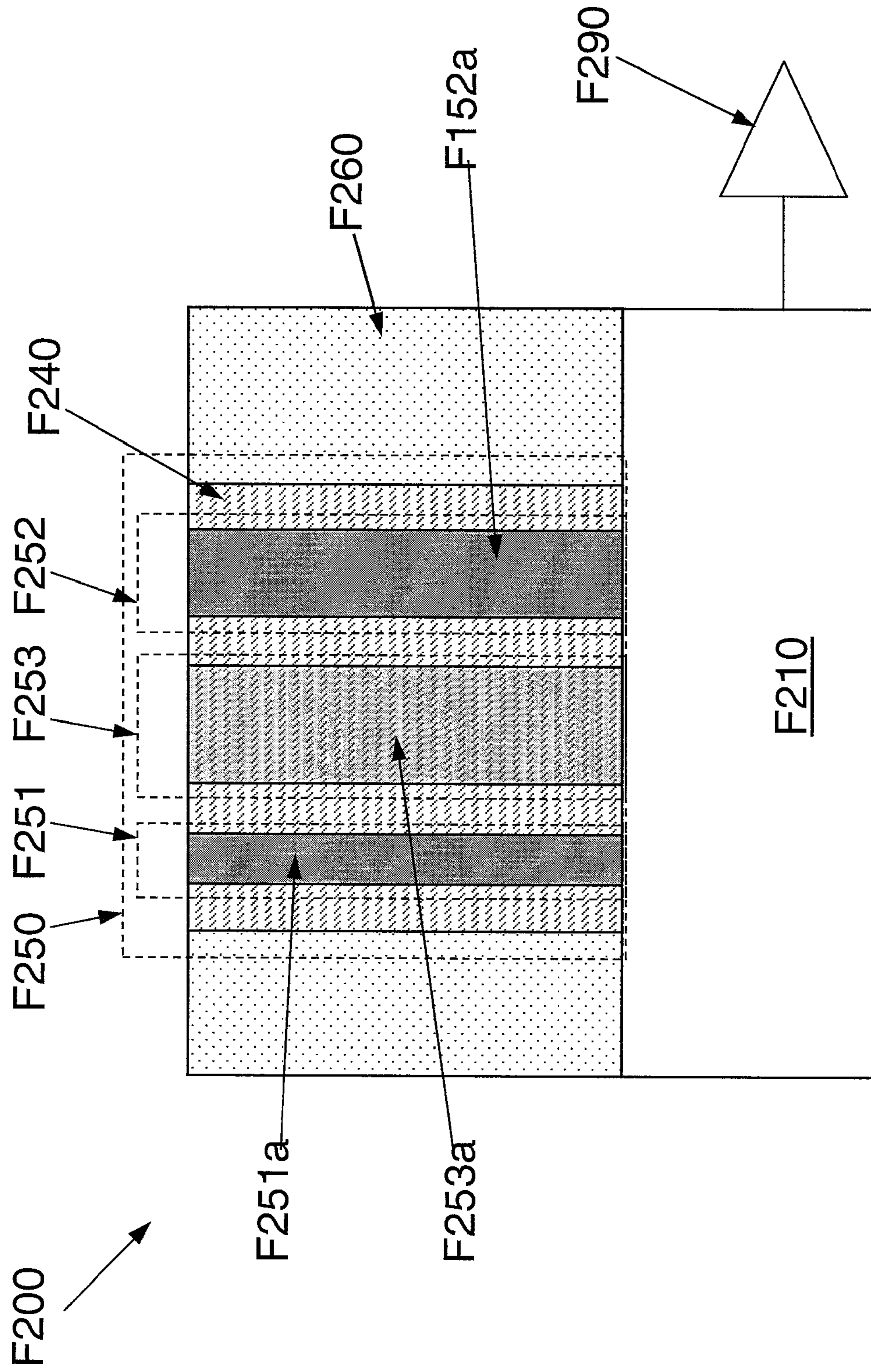


Fig. F2A

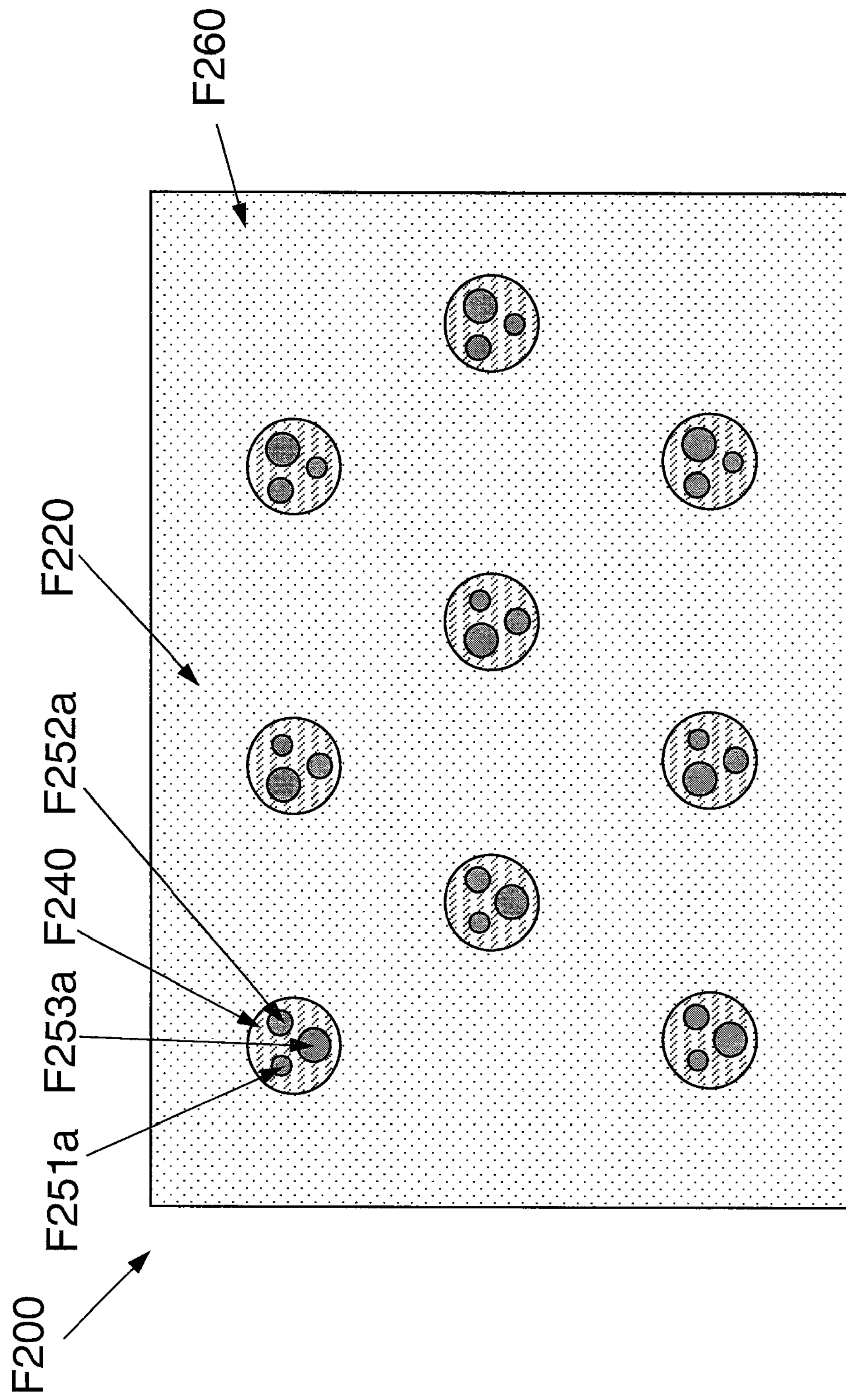


Fig. F2B

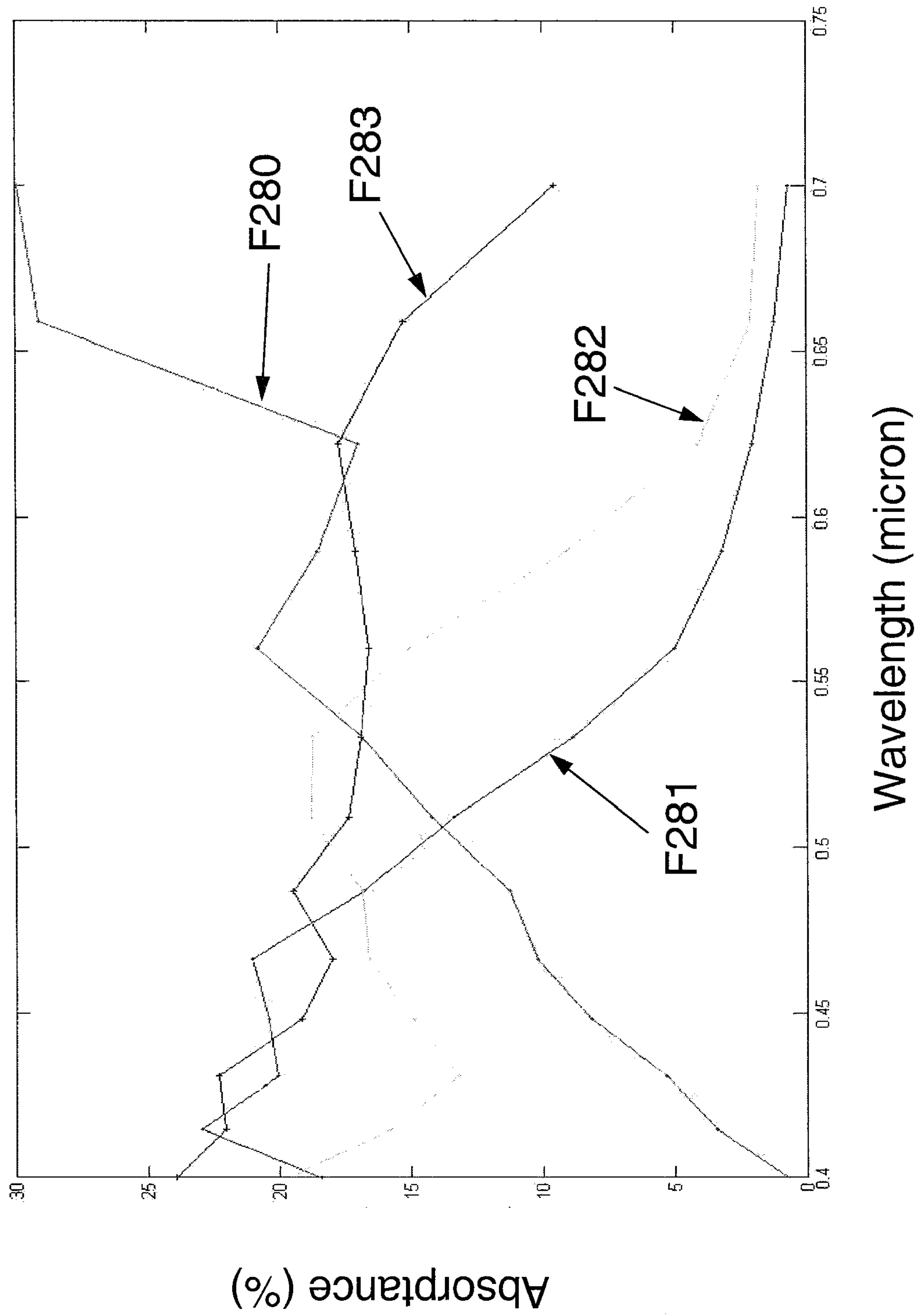


Fig. F2C

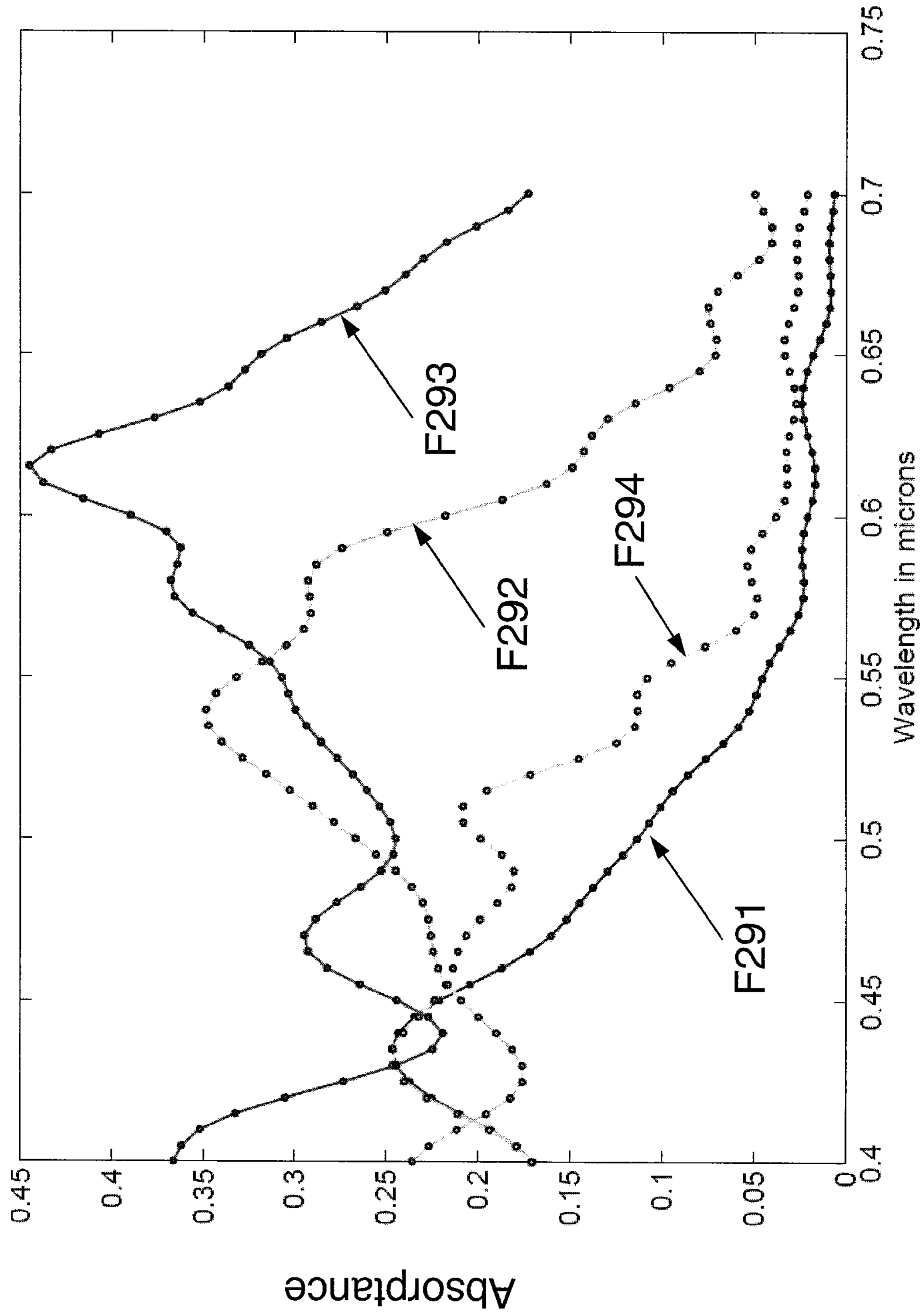


Fig. F2D

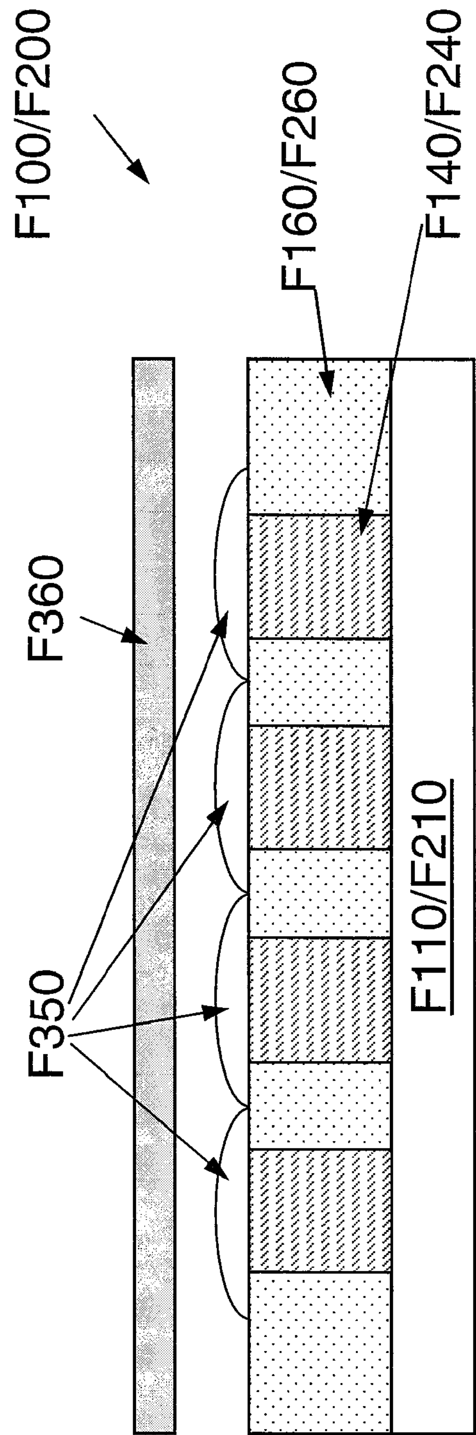


Fig. F3

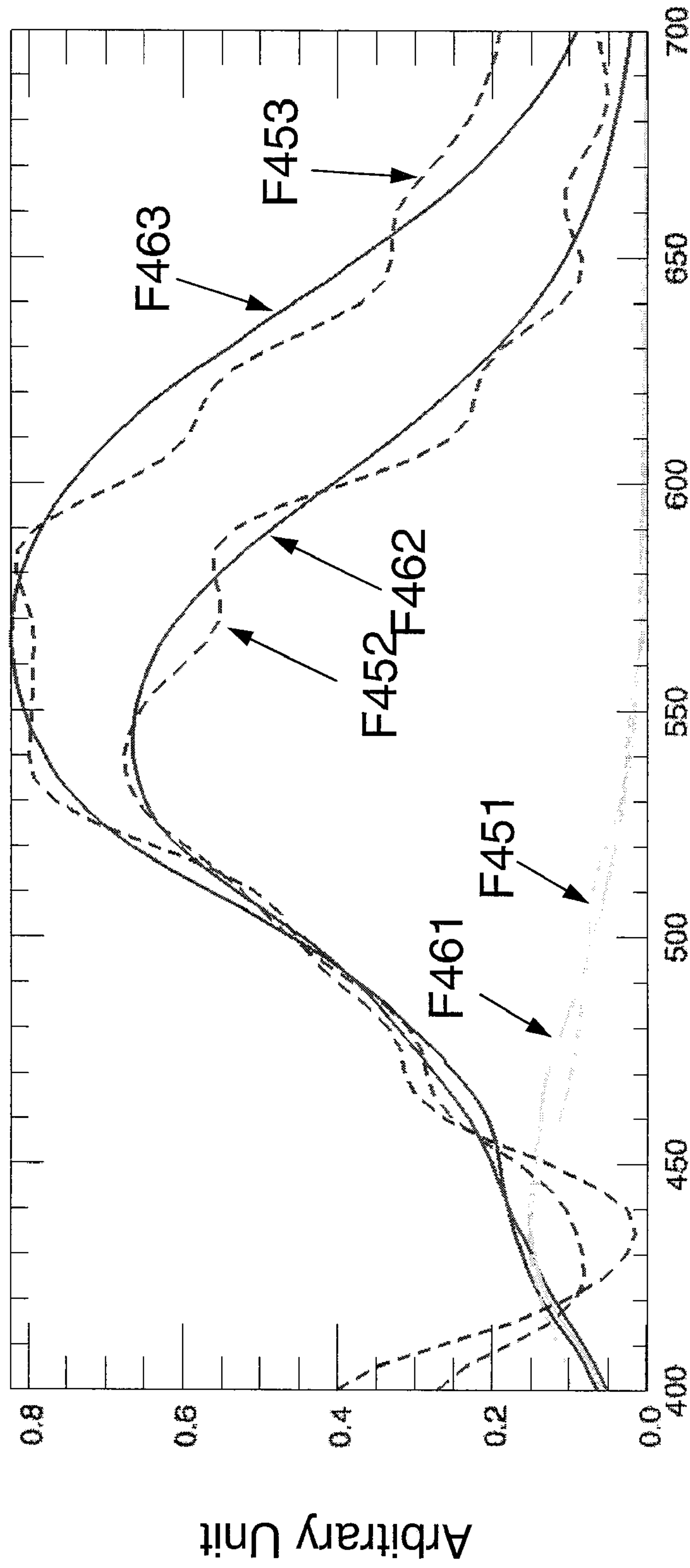


Fig. F4

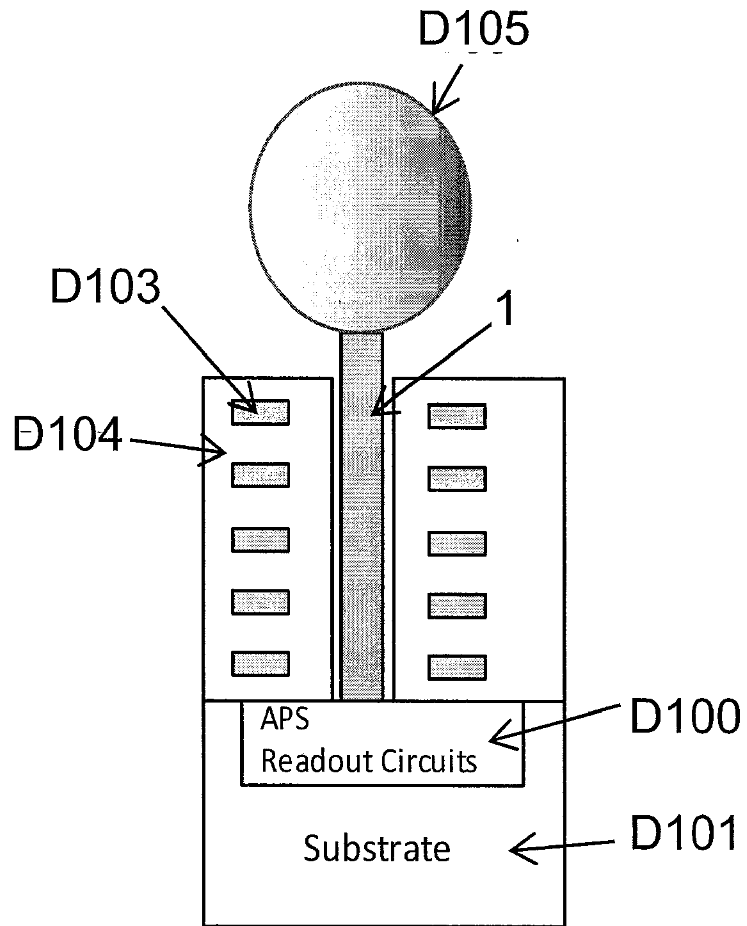


Fig. D2

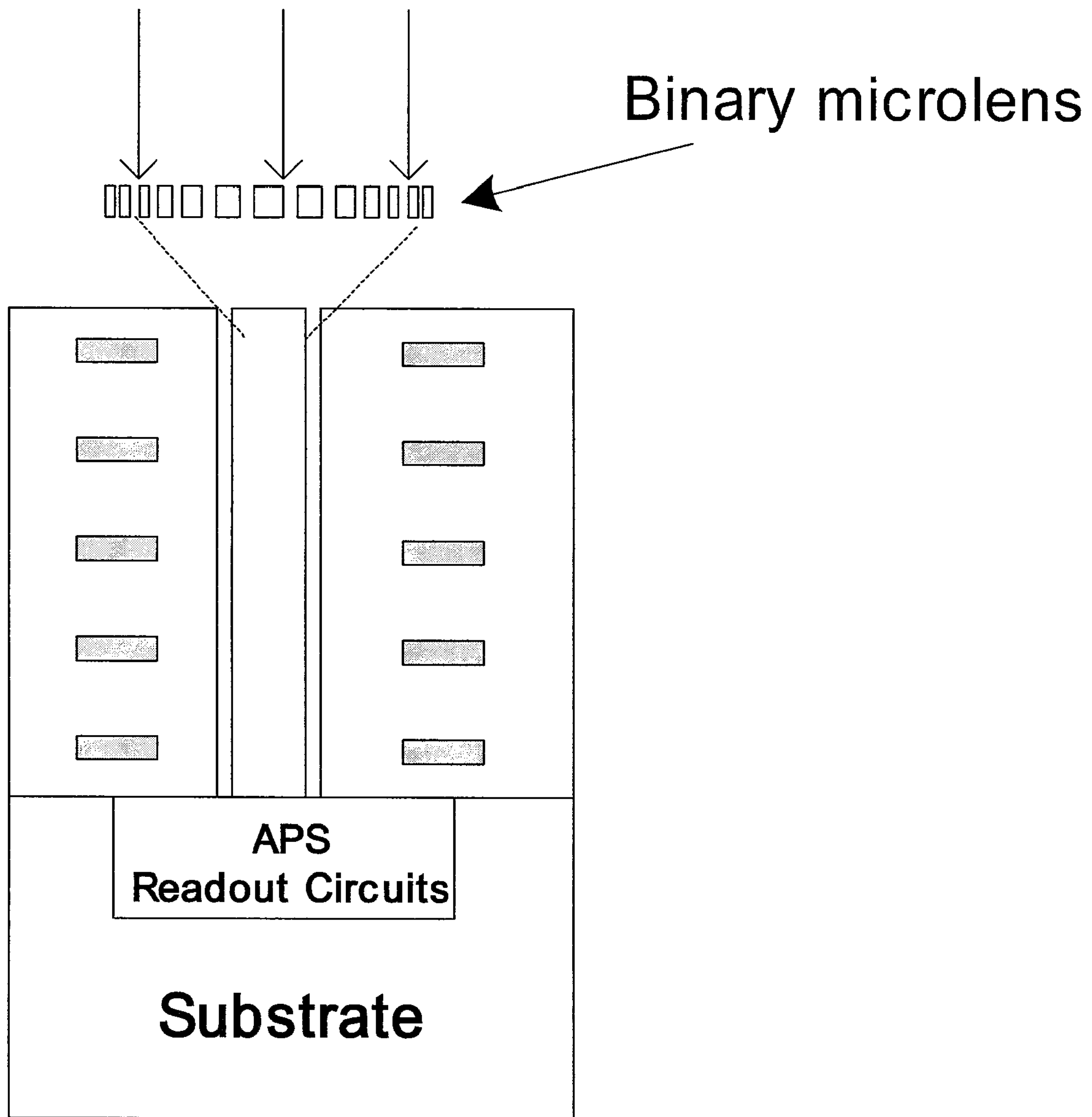


Fig. D2B

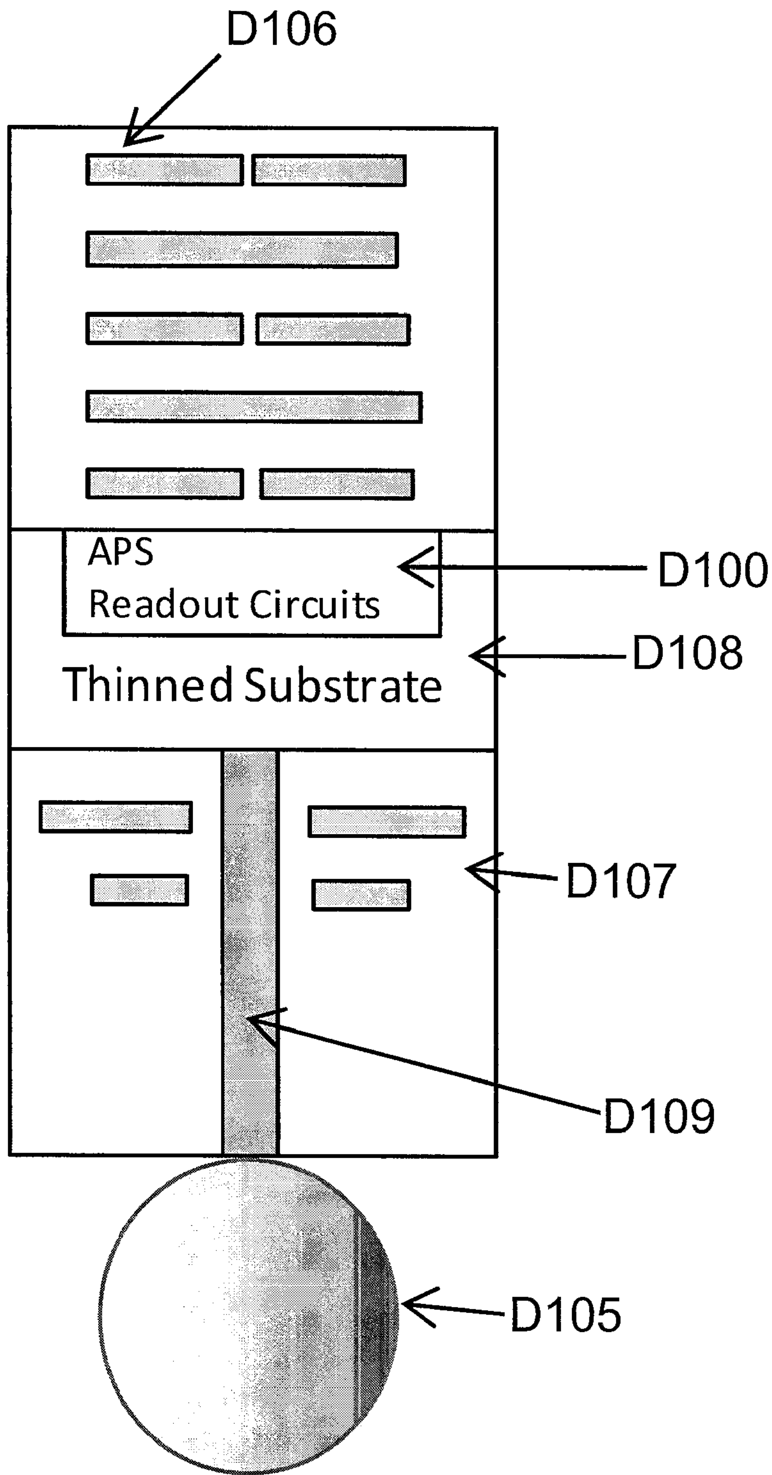


Fig. D3

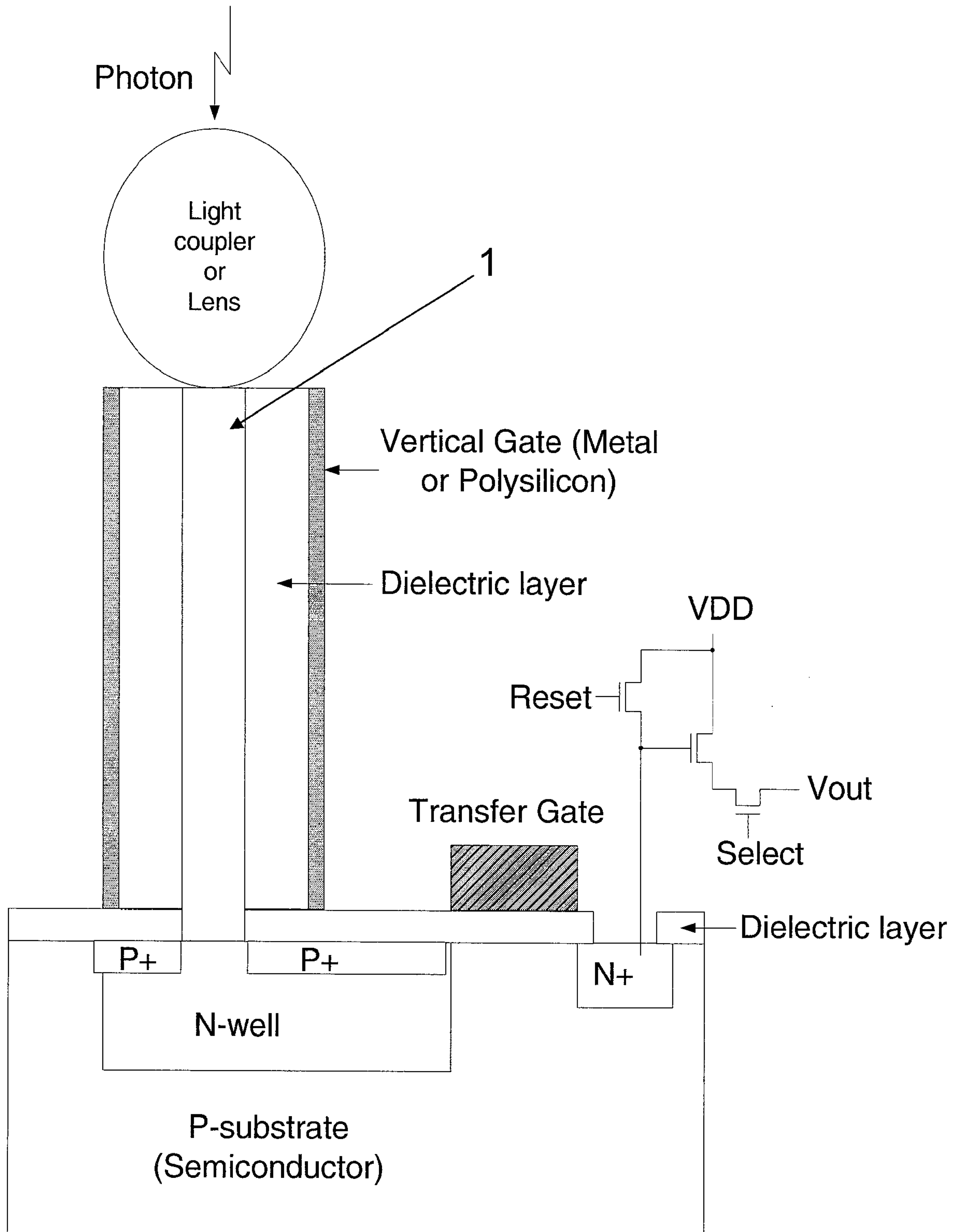


Fig. D4

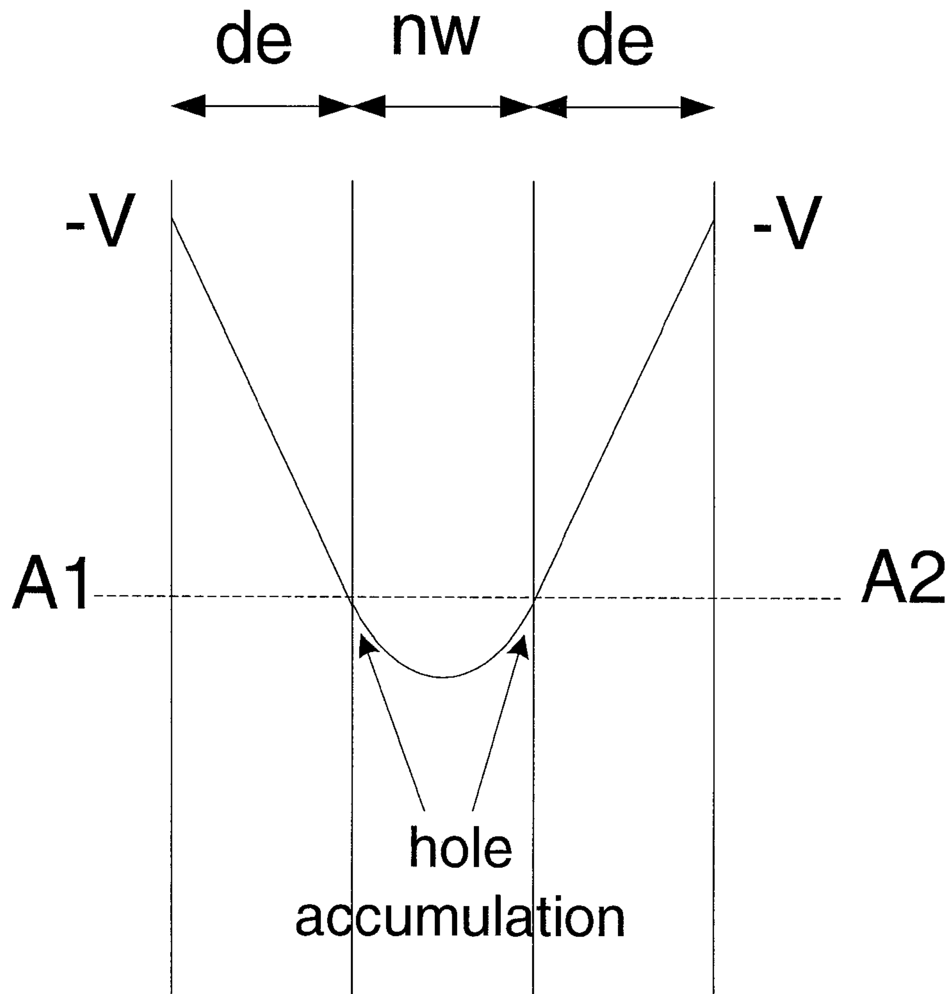


Fig. D5B

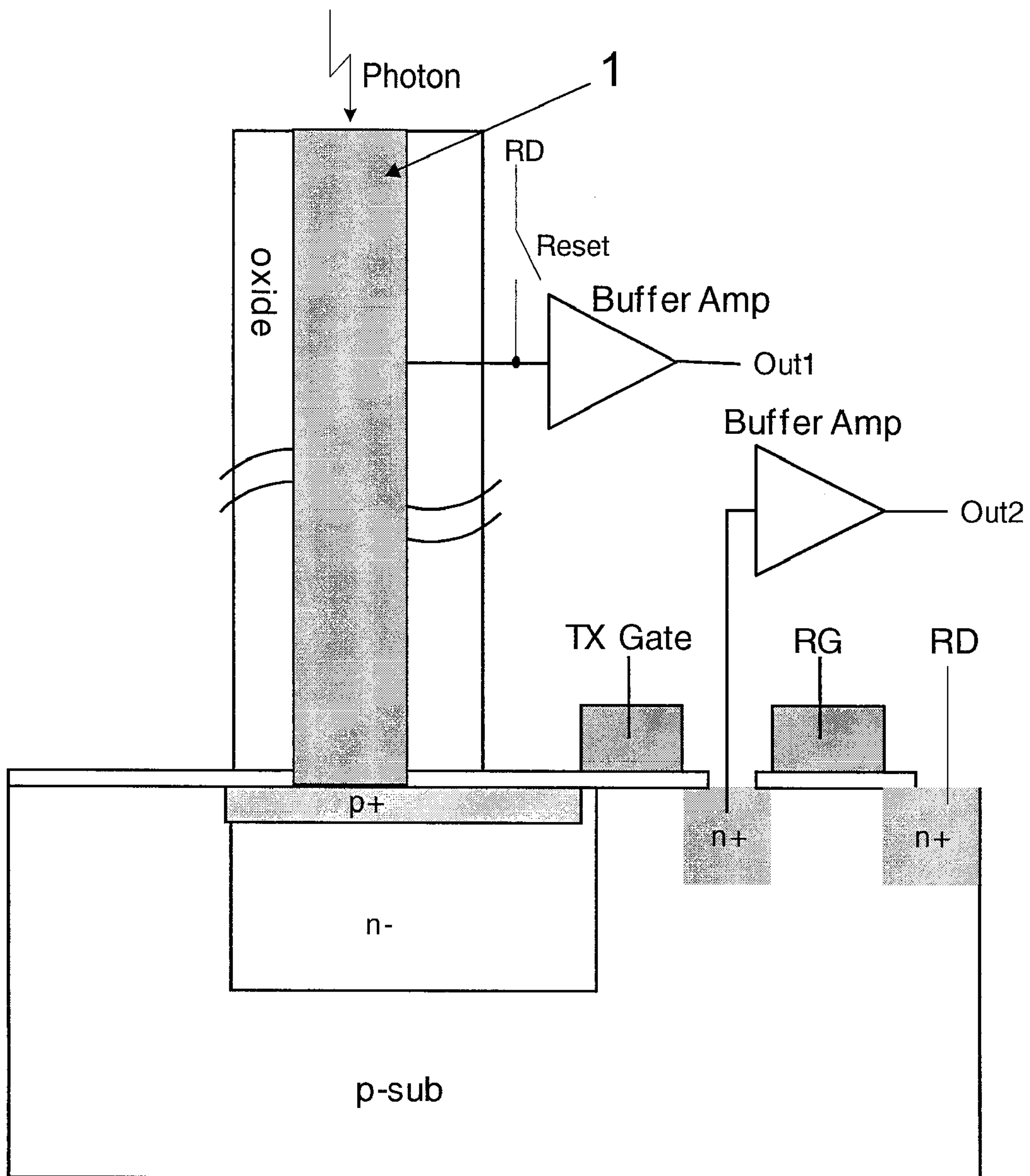


Fig. D8

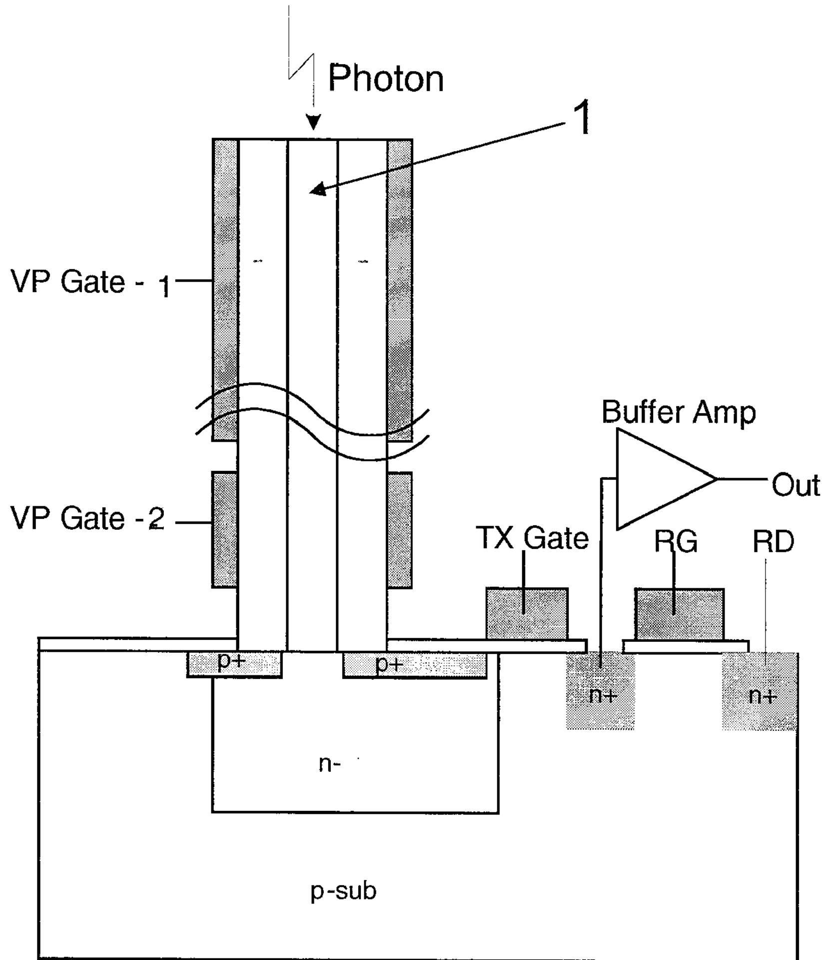


Fig. D9

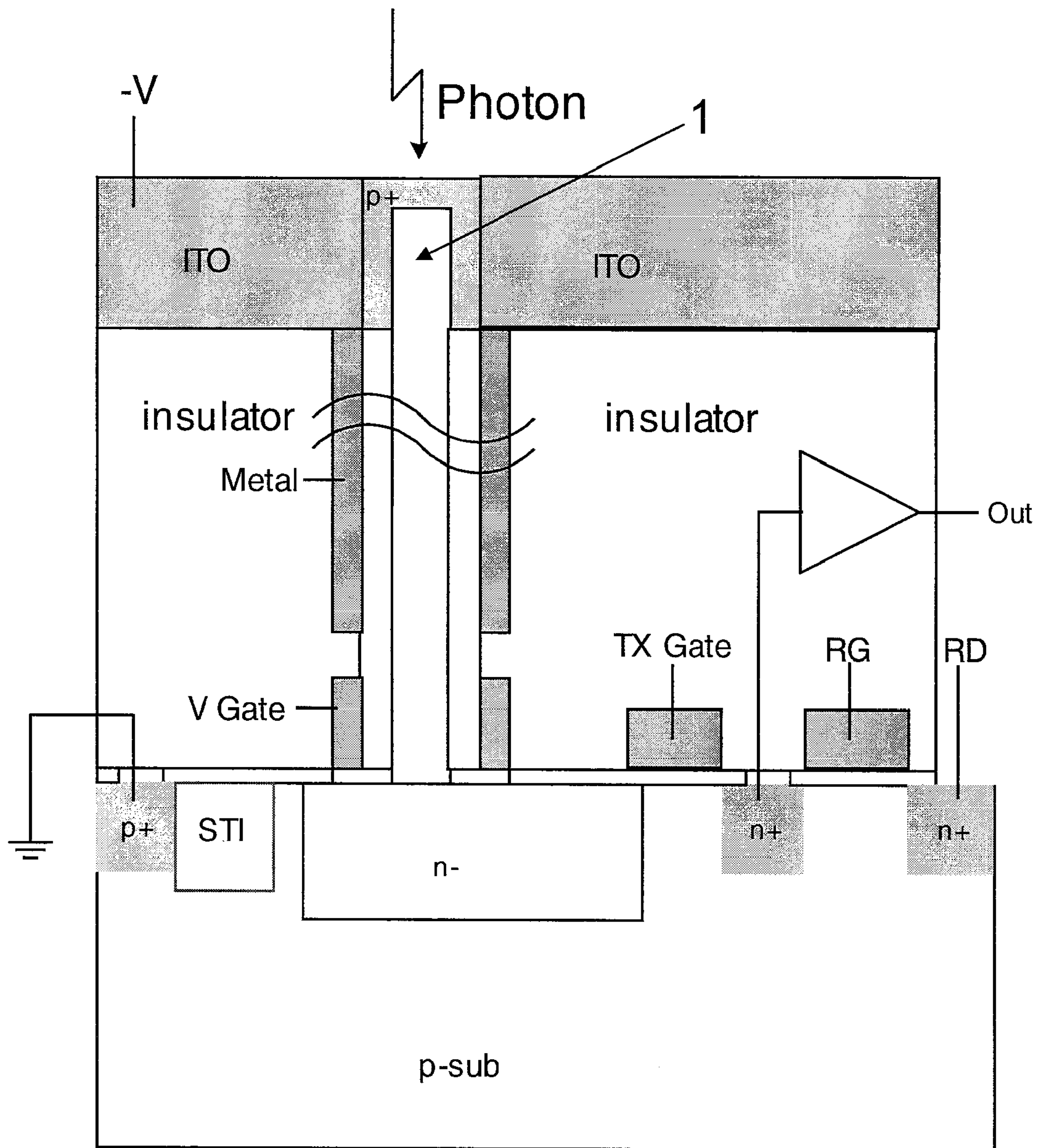


Fig. D10

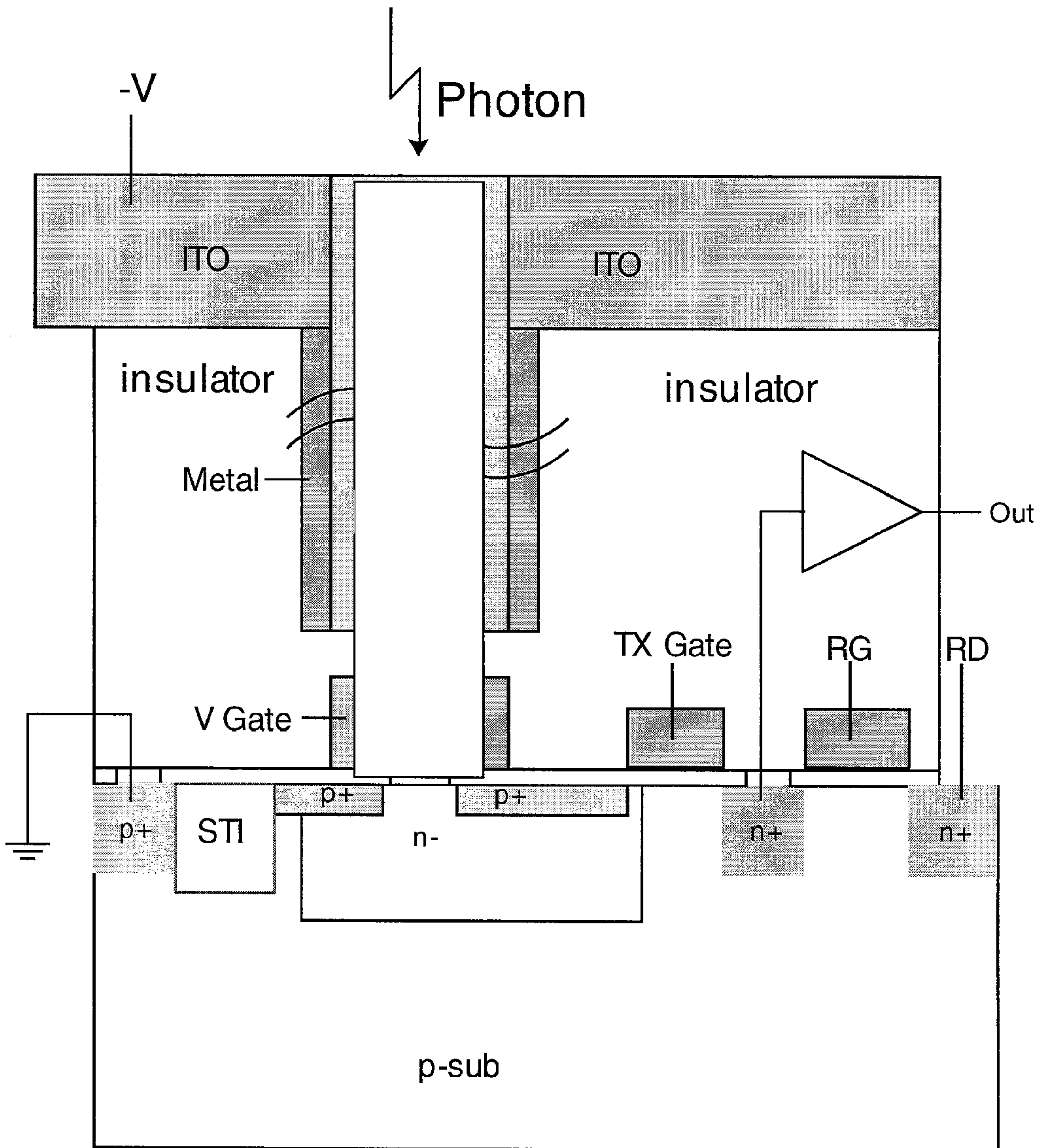


Fig. D11

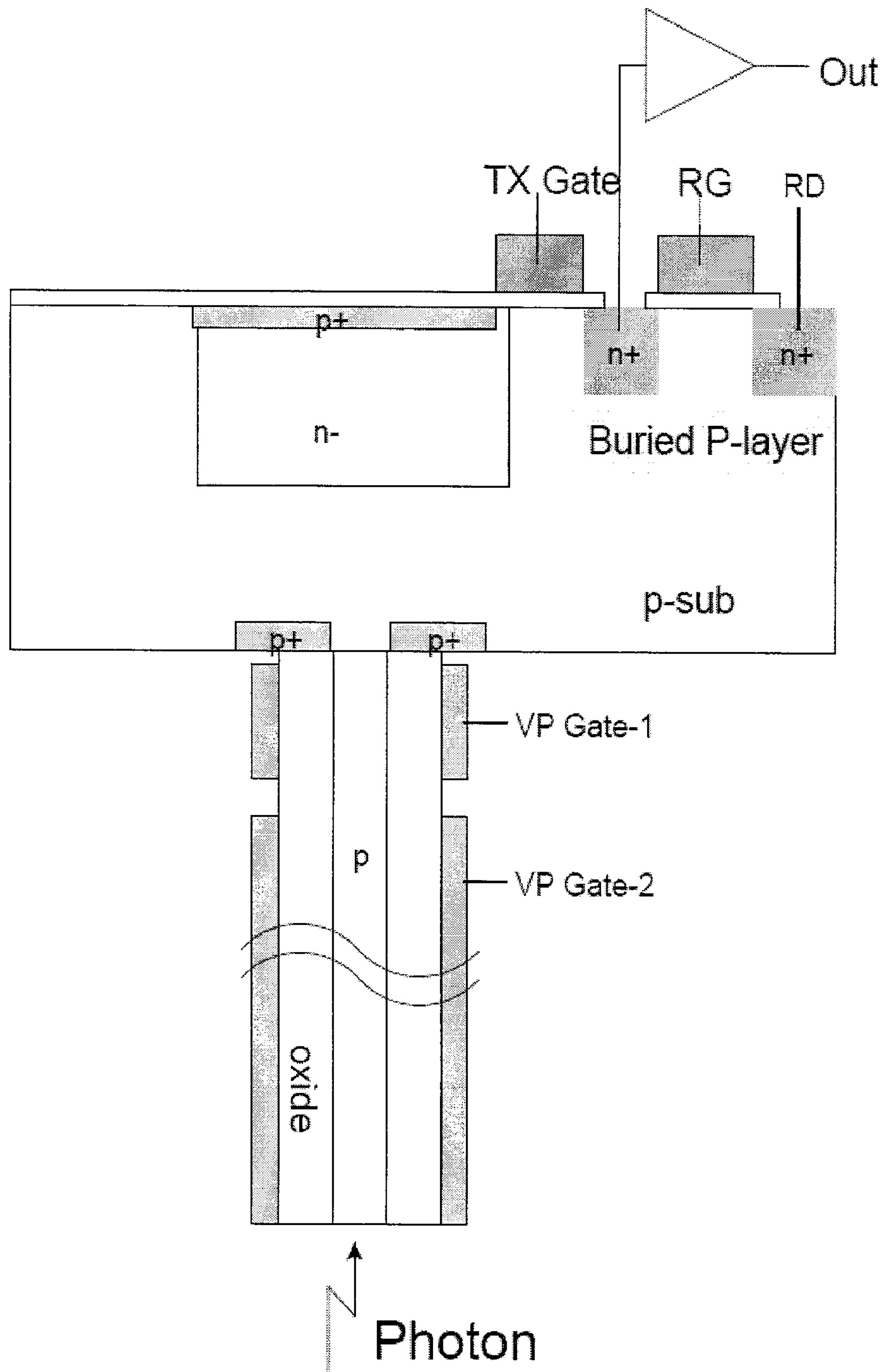


FIG. D12

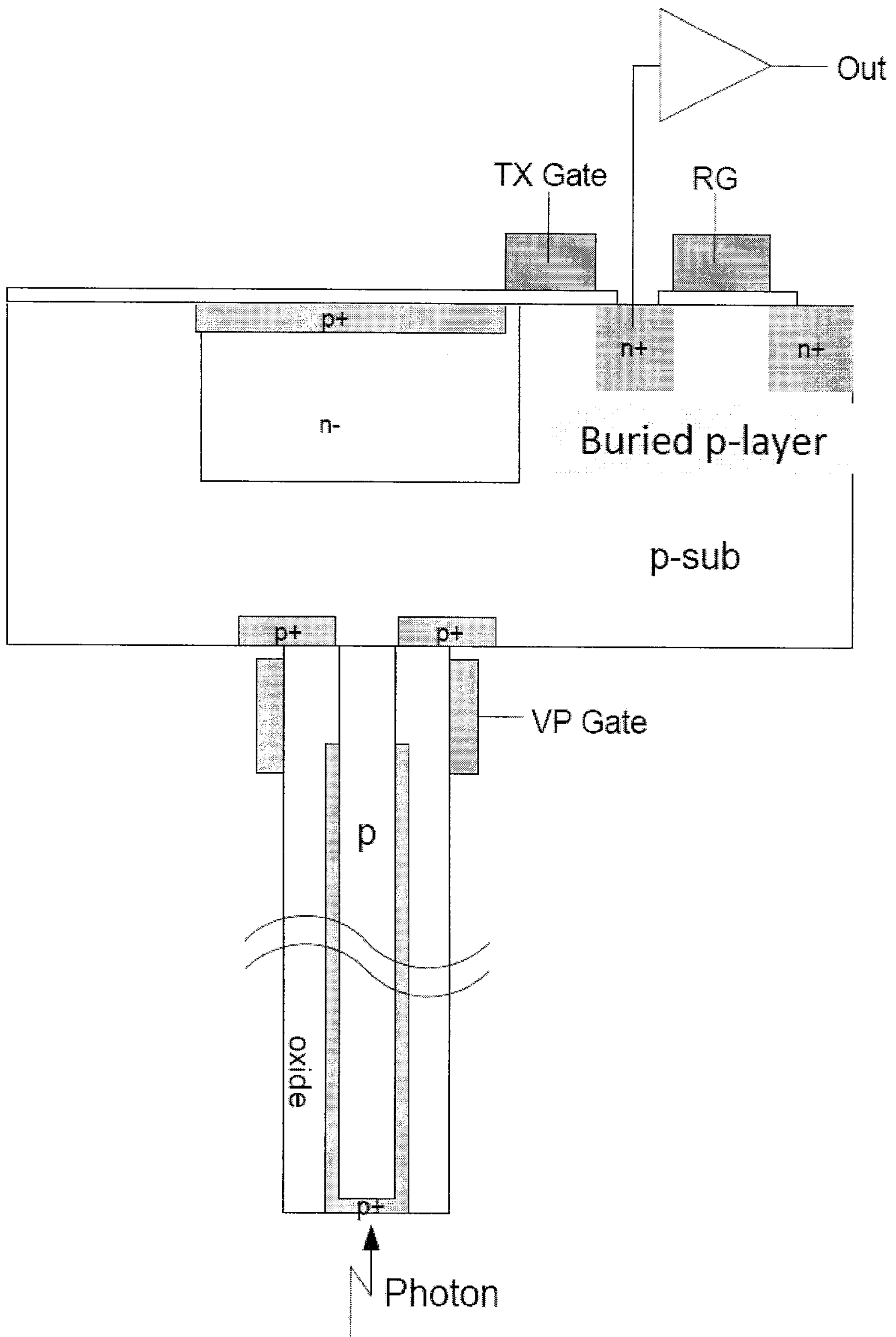


FIG. D13

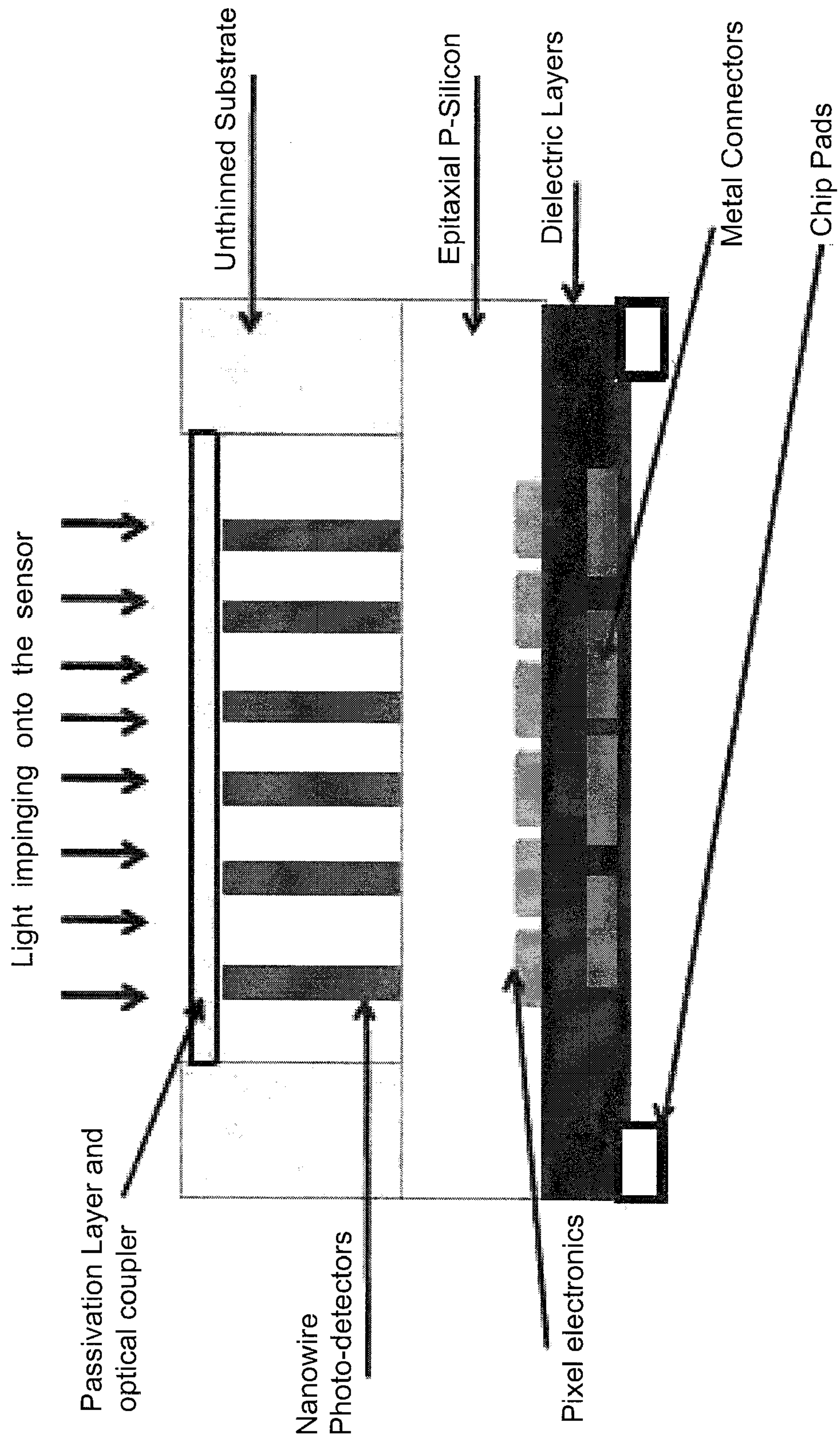


FIG. D23C

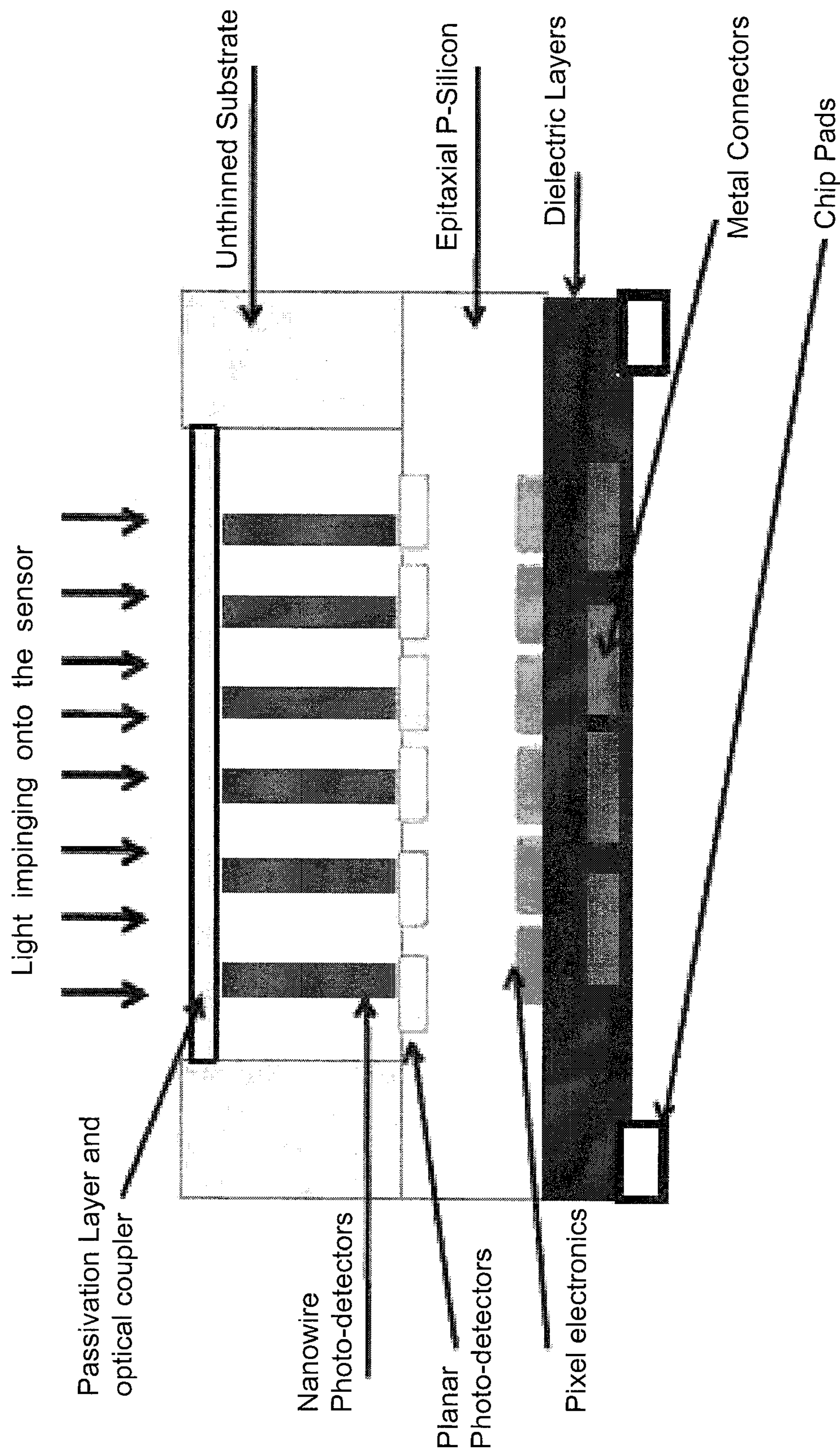


FIG. D23D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 12/20608

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 27/15 (2012.01)
USPC - 257/79
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 257/79

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IPC (8): H01L 27/15 (2012.01); (keyword limited; terms below)
USPC: 257/79, 98 (keyword limited; terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DialogWeb (123; 144; 340; 345; 347; 348; 349; 371; 447; 652; 654; Google Scholar, Google Patents;
Search terms used: semiconductor; core; p-i-n junction; amorphous; passivate; light; electricity

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2008/0169019 A1 (KOREVAAR et al.) 17 July 2008 (17.07.2008), entire document, especially; para [0003], [0006], [0009], [0032]-[0034], [0038], [0039], [0041], [0051], [0056], [0057], [0060]-[0066], [0077], [0079]	1 - 20
A	US 5,247,349 A (OLEGO et al.) 21 September 1993 (21.09.1993), entire document	1 - 20
X, P	US 2011/0127490 A1 (MI) 02 June 2011 (02.06.2011), entire document	1 - 20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 March 2012 (13.03.2012)	19 MAR 2012

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774