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(56) Documents Cited
GB 2130009 A EP 0521644 A1
JAPIO Abstract No:03921051 & JP4286151A (NEC) 12/10/92 see abstract JAPIO Abstract NO:03921052 & JP4286152A (SONY) 12/10/92 see abstract

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(54) A method of making a capacitor in a semiconductor device

(57) A method of making a charge storage element includes the steps of exposing an active region of a substrate through a contact hole, introducing an amorphous silicon layer (8, Figure 1) which includes oxygen into the contact hole, thermally treating the amorphous silicon layer such that the amorphous silicon layer is crystallized into porous polysilicon regions 9, whereby oxygenous by-products 10 are formed, and applying a wet-etching process to the oxygenous by-products to enable the porous polysilicon layers to be used as a charge storage element.

FIG. 1B

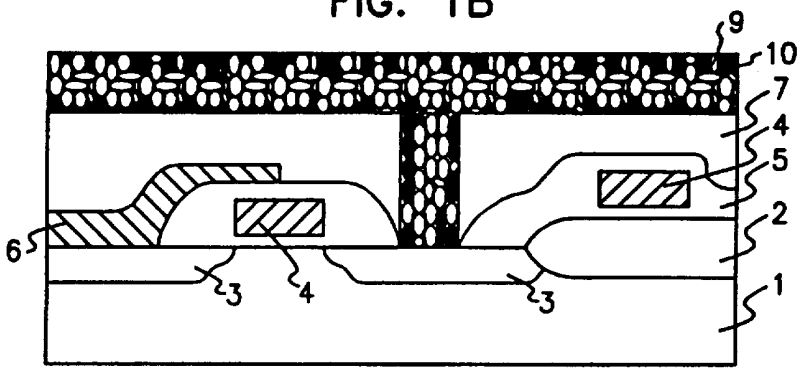

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FIG. 1A

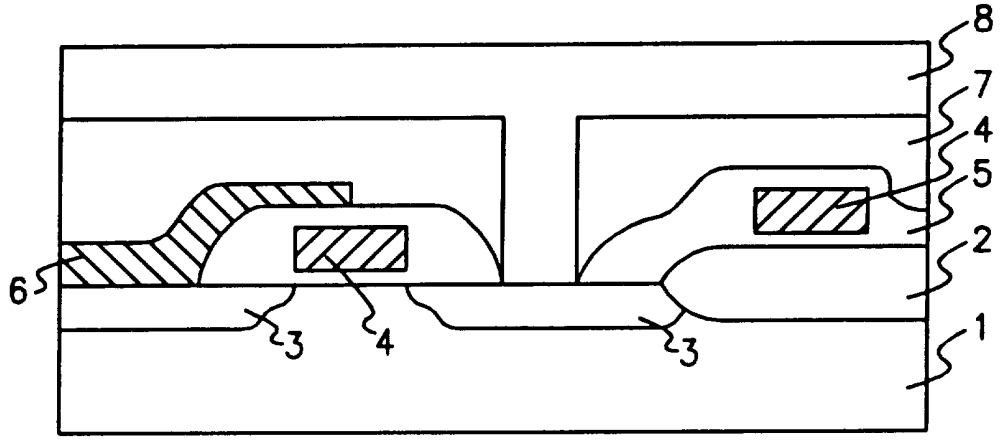


FIG. 1B

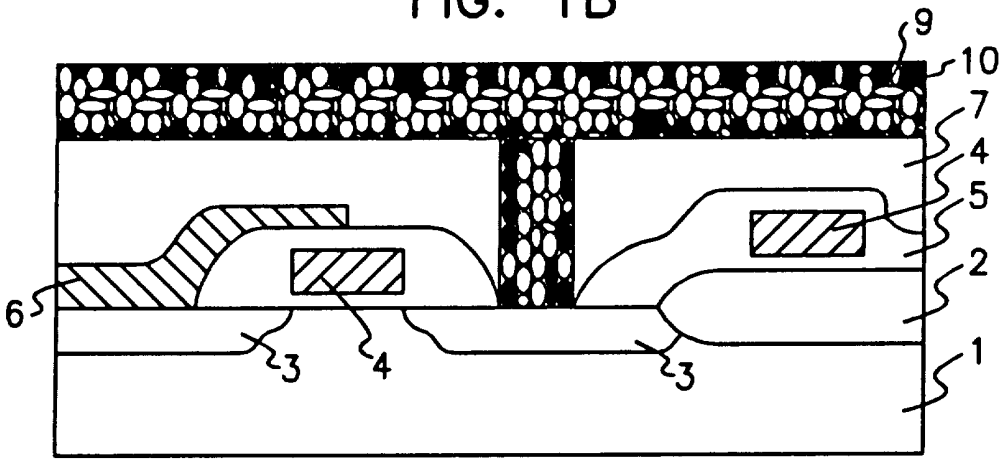
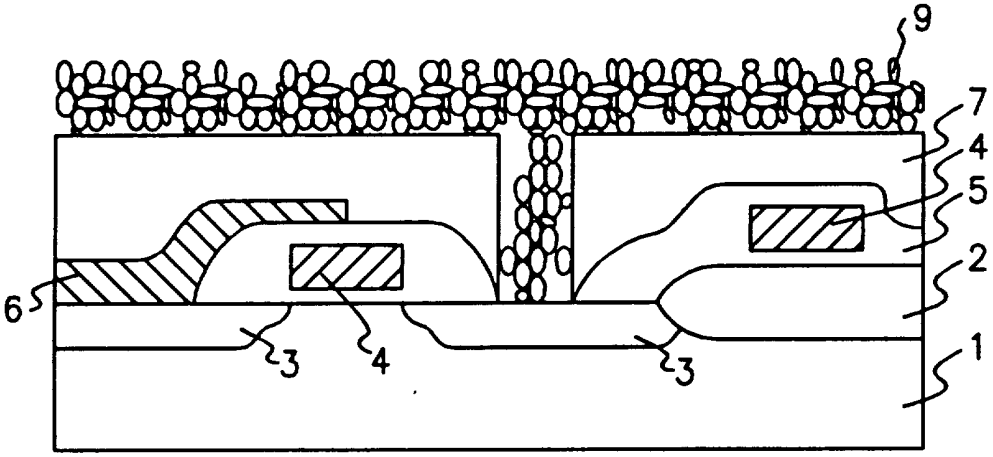


FIG. 1C



A METHOD OF MAKING A CAPACITOR IN A SEMICONDUCTOR DEVICE AND A SEMICONDUCTOR DEVICE CONTAINING A CAPACITOR

The present invention relates to a method of making a capacitor in a semiconductor device, and to a semiconductor device having a memory, and in particular, although not exclusively, to a way of increasing the capacitance of a charge storage element in a Dynamic Random Access Memory (DRAM).

In order to increase the effective area of a charge storage electrode element in a semiconductor device, it has previously been proposed to form a Dynamic Random Access Memory (DRAM) using stacked capacitors, by forming a capacitor over the bit line.

However, in spite of a variety of developments in DRAMs, it is difficult to achieve a sufficiently effective area of a capacitor because the devices are highly integrated.

A feature of a method for making a capacitor having high capacitance to be described below, by way of example, is that the effective area of a charge storage element is increased.

A particular method to be described below, by way of example, for making a charge storage element, includes the steps of providing a substrate having an active region, exposing the active region through a contact hole, introducing an amorphous silicon layer, which includes oxygen, into the contact hole, thermally treating the amorphous silicon layer such that the

amorphous silicon layer is crystallized into porous polysilicon layers, whereby oxygenous by-products are formed between the porous polysilicon layers, and treating the oxygenous by-products by a wet-etching process to enable the porous polysilicon layers to be used as a charge storage element.

An arrangement illustrative of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figs. 1A to 1C are cross-sectional views illustrating steps in a method for making a capacitor in a semiconductor device.

Referring first to Figs. 1A, the numeral 1 denotes a silicon substrate, 2 a filled oxide layer, 3 an active region, 4 a gate electrode, 5 an insulation layer, 6 a bit line, 7 an insulation layer, and 8 an amorphous silicon layer which contacts the active region 3.

A method of forming the structure shown in Fig. 1A is well-known to those having ordinary skill in the art concerned with making charge storage elements.

In the arrangement being described as an example, a charge storage element employs an amorphous silicon layer 8. This amorphous silicon layer 8 incorporates oxygen. The amorphous silicon layer 8 is formed using the gases SiH_4(silane) and N_2O at a comparatively low temperature between 550°C and 700°C.

The ratio of oxygen to the silicon atoms must be

between 10% and 30%. The amorphous silicon layer is thermally treated for between 4 and 6 hours at a temperature of between 850°C and 1150°C in a N_2 atmosphere. The amorphous silicon layer is then crystallized into polysilicon layers 9, and oxygenous by-products 10, such as SiO_2 or SiO_x, are formed in the polysilicon layers 9, as shown in Fig. 1B.

Finally, as shown in Figs. 1C, a wet etching process is applied to the oxygen by-product using an HF etchant, and porous polysilicon layers are formed and provide a charge storage element in a DRAM.

As mentioned above, the arrangement described has the effect of increasing the effective area of a charge storage electrode in a highly integrated semiconductor device by forming a porous polysilicon layer.

Although a preferred embodiment of the invention has been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope of the invention as defined in the accompanying claims.

CLAIMS

1. A method of making a charge storage element, including the steps of providing a substrate having an active region, exposing the active region through a contact hole, introducing an amorphous silicon layer, which includes oxygen, into the contact hole, thermally treating the amorphous silicon layer such that the amorphous silicon layer is crystallized into porous polysilicon layers, whereby oxygenous by-products are formed between the porous polysilicon layers, and treating the oxygenous by-products by a wet-etching process to enable the porous polysilicon layers to be used as a charge storage element.

2. A method as claimed in claim 1, wherein the amorphous silicon layer is made from SiH_4 and N_2O gases.

3. A method as claimed in either claim 1 or claim 2, wherein the amorphous silicon layer is introduced by deposition at a temperature of between 550°C and 700°C.

4. A method as claimed in any one of the preceding claims wherein the amorphous silicon layers is thermally treated for 4 to 6 hours.

5. A method according to any one of the preceding claims, wherein the thermal treatment step is carried out at a temperature of between 850°C and 1150°C.

6. A method as claimed in any one of the preceding claims wherein the amorphous silicon layer includes between 10% and 30% of oxygen.

7. A method as claimed in any one of the preceding claims including the step of treating the oxygenous by-products by a wet-etching process which employs an HF etchant.

8. A method as claimed in claim 1 substantially as described herein with reference to the accompanying drawings.

9. A semiconductor device including a charge storage element made by a method as claimed in any one of the preceding claims.

Patents Act 1977 6 **Examiner's report to the Comptroller under Section 17 (The Search report)**	Application number GB 9525651.7
Relevant Technical Fields (i) UK Cl (Ed.O) H1K (KFLS, KFLT, KFLX, KHABP, KHAC, KLHA) (ii) Int Cl (Ed.6) H01L	Search Examiner S J MORGAN Date of completion of Search 9 FEBRUARY 1996
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE: WPI, JAPIO, INSPEC	Documents considered relevant following a search in respect of Claims :- 1-7

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages	Relevant to claim(s)
Y	GB 2130009 A (RCA) see line 120, page 1 - line 70, page 2	
Y	EP 0521644 A1 (NEC) see line 40, column 5 - line 36, column 6	
Y	Japio Abstract No. 03921051 & JP 4286151 A (NEC) 12 October 1992. See Abstract	
Y	Japio Abstract No. 03921052 & JP 4286152 A (SONY) 12 October 1992. See Abstract	1 at least

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