



(51) International Patent Classification:

H01L 29/47 (2006.01) *H01L 29/778* (2006.01)
H01L 29/66 (2006.01) *H01L 29/49* (2006.01)
H01L 29/872 (2006.01)

(21) International Application Number:

PCT/US2017/032927

(22) International Filing Date:

16 May 2017 (16.05.2017)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/337,015	16 May 2016 (16.05.2016)	US
62/337,028	16 May 2016 (16.05.2016)	US

(71) Applicant: **THE GOVERNMENT OF THE UNITED STATES OF AMERICA, AS REPRESENTED BY THE SECRETARY OF THE NAVY** [US/US]; Naval Research Laboratory, 4555 Overlook Ave., SW, Code 1008.2, Washington, DC 20375 (US).

(72) Inventors: **WHEELER, Virginia D.**; 6559 Parish Glebe Lane, Alexandria, VI 22315 (US). **KOEHLER, Andrew D.**; 3004 Mark Pat Dr., Alexandria, VA 22310 (US). **HO-BART, Karl D.**; 1006 Ramsey St., Alexandria, VI 22301 (US). **KUB, Francis, J.**; 1103 Spy Glass Dr, Arnold, MD 21012 (US). **TADJER, Marko J.**; 7219 Calamo St., Springfield, VA 22150 (US). **SHAHIN, David**; 6611 Comet Cr., Apt 403, Springfield, VA 22150 (US).

(74) Agent: **BROOME, Kerry L.**; US Naval Research Laboratory, 4555 Overlook Ave, SW, Code 1008.2, Washington, DC 20375 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,

(54) Title: METAL NITRIDE ALLOY CONTACT FOR SEMICONDUCTOR

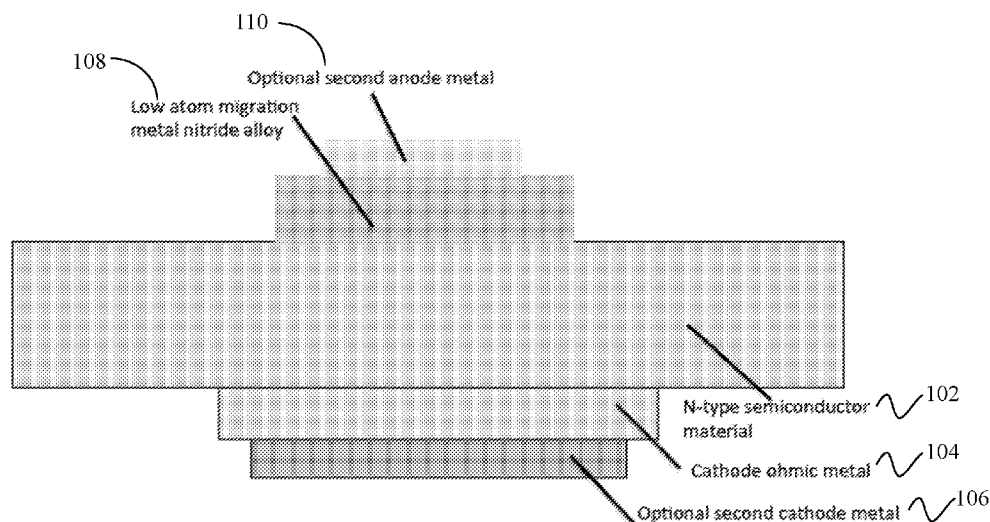


FIG. 1A

(57) Abstract: Systems and methods are provided that enable the production of semiconductor devices having a metal nitride layer in direct contact with a semiconductor layer to form a Schottky diode, such as a TiN gate on an AlGaIn/GaN high electron mobility transistor (HEMT). Metal nitrides offer exceptional thermal stability and a lower diffusion coefficient. Technology enabled by embodiments of the present disclosure improves the reliability of GaN-based microwave power transistors



SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

METAL NITRIDE ALLOY CONTACT FOR SEMICONDUCTOR

This application claims the benefit of U.S. Provisional Patent Application Number 62/337,015, filed on May 16, 2016, and U.S. Provisional Patent Application Number 62/337,028, filed on May 16, 2016, both of which are incorporated by reference herein in their entireties.

TECHNICAL FIELD

This disclosure relates to semiconductors, including Group III-nitride based high electron mobility transistors (HEMTs).

DESCRIPTION OF RELATED ART

Group III-nitride based high electron mobility transistors (HEMTs) are attracting significant interest (e.g., for microwave and power switching applications). Electrically and thermally stable device schemes are essential for reaching the maximum potential of GaN devices. The reliability of Ni/Au-based Schottky gate metallizations has been limited by gate degradation from Ni migration into nearby metal and semiconductor layers when subjected to electrical and thermal stress. As such, development of alternative gate schemes resistant to these degradation mechanisms is highly desirable for fabrication of reliable HEMTs.

In conventional devices, nickel metal is in direct contact with III-nitride alloy material, such as gallium nitride. The nickel metal layer typically has a gold metal top layer. The nickel atoms are known to diffuse into the gallium nitride III-Nitride material with thermal stress, causing degraded Schottky to III-Nitride junction reliability, which is undesirable.

BRIEF SUMMARY

In a first embodiment, this disclosure describes a low atom migration (diffusion) metal nitride alloy (e.g., titanium nitride) material layer to a III-Nitride device that comprises a metal nitride alloy material layer having a first surface and a second surface, with the second surface in direct atomic contact with the III-Nitride surface, wherein the atoms comprising the metal nitride alloy material layer have low migration (low diffusion) into the III-Nitride material, and the atoms comprising the III-Nitride have low migration into the metal nitride alloy material layer (during storage or under stress).

In a second embodiment, this disclosure describes a low atom migration (diffusion) composite metal nitride alloy material layer to semiconductor device that comprises a high work function metal nitride alloy material layer having a first surface and a second surface with the second surface in direct atomic contact with the semiconductor surface and a second metal nitride

alloy material layer with a first and second surface with the second surface in direct contact with the first surface of the high work function metal nitride alloy material layer, wherein the atoms comprising the metal nitride alloy material layer have low migration (low diffusion) into the semiconductor material, and the atoms comprising the semiconductor have low migration into the metal nitride alloy material layer (during storage or under stress).

In a third embodiment, this disclosure describes a low atom migration (diffusion) metal nitride alloy material layer to semiconductor device that comprises one or more than one tunneling material layer(s) at the interface between the metal nitride alloy material layer and the semiconductor, wherein the atoms comprising the metal nitride alloy material layer have low migration (low diffusion) into the semiconductor material, and the atoms comprising the semiconductor have low migration into the metal nitride alloy material layer (during storage or under stress).

In a first exemplary method, the low atom migration metal nitride alloy material layer may be deposited by atomic layer deposition. In a second exemplary method, the low atom migration metal nitride alloy material layer may be deposited by a non-plasma process metal which may include atomic layer deposition, metal organic chemical vapor deposition, chemical vapor deposition, or molecular beam deposition.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute part of the specification, illustrate embodiments of the disclosure and, together with the general description given above and the detailed descriptions of embodiments given below, serve to explain the principles of the present disclosure. In the drawings:

FIG. 1A is a cross-section of a low atom migration metal nitride alloy material layer diode on III-Nitride material in accordance with an embodiment of the present disclosure;

FIG. 1B is a cross-section of a low atom migration metal nitride alloy material layer diode on III-Nitride material including a high work function metal nitride alloy in accordance with an embodiment of the present disclosure;

FIG. 1C is a cross-section of a low atom migration metal nitride alloy material layer diode including a dielectric and field plate in accordance with an embodiment of the present disclosure;

FIG. 1D is a cross-section of a low atom migration metal nitride alloy material layer diode including a vertically graded low atom migration metal nitride alloy material layer in accordance with an embodiment of the present disclosure;

FIG. 2 is a schematic of a three-terminal HEMT device in accordance with an embodiment of the present disclosure;

FIG. 3 is a table (Table I) showing parameters devices listed in Table I in accordance with an embodiment of the present disclosure;

5 FIG. 4 is a diagram showing gate leakage during gate voltage sweeping from 0V to reverse breakdown for Ni/Au-, TiN-, and NCD-gated HEMTs in accordance with an embodiment of the present disclosure;

FIG. 5 is a table (Table II) showing breakdown voltages for Ni/Au- and Ti/N-gated HEMTs in accordance with an embodiment of the present disclosure;

10 FIG. 6 is a diagram showing turn-on (I_{ds} - V_{gs}) characteristics at $V_{ds} = 10V$ for HEMT devices with Ni/Au, TiN, and NCD gates in accordance with an embodiment of the present disclosure;

FIG. 7 is a diagram showing static drain current-drain voltage (I_{ds} - V_{ds}) behavior for Ni/Au, TiN, and NCD-gated HEMTs in accordance with an embodiment of the present disclosure;

FIG. 8 is a diagram showing Ni/Au, TiN, and NCD gate during stressing at $V_{gs} = -140$ V for 1 hour in accordance with an embodiment of the present disclosure;

FIG. 9 is a diagram showing Ni/Au and TiN gate leakage currents before and after stressing at $V_{gs} = -140$ V for 1 hour in accordance with an embodiment of the present disclosure;

20 and
FIG. 10 is a flowchart of a method for creating a semiconductor device in accordance with an embodiment of the present disclosure.

Features and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.

30 DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

In the following description, numerous specific details are set forth to provide a thorough understanding of the disclosure. However, it will be apparent to those skilled in the art that the disclosure, including structures, systems, and methods, may be practiced without these specific

details. The description and representation herein are the common means used by those experienced or skilled in the art to most effectively convey the substance of their work to others skilled in the art. In other instances, well-known methods, procedures, components, and circuitry have not been described in detail to avoid unnecessarily obscuring aspects of the disclosure.

References in the specification to “one embodiment,” “an embodiment,” “an exemplary embodiment,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

1. Exemplary Devices

AlGaIn/GaN high electron mobility transistors (HEMTs) commonly rely on Ni/Au-based Schottky gate metallizations that have been shown to degrade when subjected to electrical stress, thermal stress, and radiation due to Ni migration into adjacent metal or semiconductor layers. The instability of these Ni-based gates limits device reliability, rendering the search for alternative gate materials that are electrically and thermally stable a topic of tremendous importance.

Materials such as the transition metal nitrides (TiN, etc.) and boron-doped nanocrystalline diamond represent candidate materials for replacement of the Ni-based gates. Of the transition metal nitrides, TiN is a particularly promising material, due to its near-metallic conductivity, suitable Schottky barrier heights and ideality factors on GaN and AlGaIn, and high temperature stability. These nitrides can be easily deposited by atomic layer deposition (ALD), sputtering, or molecular beam epitaxy (MBE), which is particularly attractive due to the ability to deposit in-situ immediately after the AlGaIn/GaN growth without exposing the material to atmosphere, thereby further improving device quality and reliability. Boron-doped p⁺ diamond gates have also been shown to be candidates for HEMT gates and are attractive due to the high thermal conductivity and low leakage in the heterojunction gate. Though these materials show promise for HEMT gates, little work has been done to assess their contributions to device reliability under extended electrical or thermal stress.

Conventional Ni/Au metallization fails in GaN devices due to diffusion. Metal Schottky gate contacts often fail due to metal diffusion into the semiconductor. Transition metal nitrides

offer low sheet resistance and suitable work function to behave as Schottky gate electrodes in GaN transistor structures. The use of metal nitride electrodes mitigates the diffusion failure mechanism for improved reliability, resulting in significantly higher breakdown voltage and thermal stability.

Embodiments of the present disclosure provide semiconductor devices having a metal nitride layer in direct contact with a semiconductor layer to form a Schottky diode, such as a TiN gate on an AlGaIn/GaN HEMT. Embodiments of the present disclosure provide transistors (i.e., AlGaIn/GaN HEMT) with a metal nitride gate (i.e. TiN) and semiconductor Schottky diodes with a metal nitride electrode.

Embodiments of the present disclosure provide systems and methods including TiN-based Schottky contacts to GaN devices, as opposed to a use as ohmic contacts or diffusion barriers. In accordance with embodiments of the present disclosure, the films can be deposited using conventional thin film growth techniques such as ALD, which are compatible with semiconductor fabrication processes. Metal nitrides offer exceptional thermal stability and lower diffusion coefficient. Technology enabled by embodiments of the present disclosure will improve the reliability of the GaN-based microwave power transistor.

1.1. Two Terminal Device with Electrical Stability for Metal Nitride Alloy Electrode

FIG. 1A is a cross-section of a low atom migration metal nitride alloy material layer diode on III-Nitride material in accordance with an embodiment of the present disclosure. In an embodiment, the low atom migration metal nitride alloy material layer diode of FIG. 1A is a Schottky diode. FIGS. 1B-1D are additional embodiments of cross-sections of a low atom migration metal nitride alloy material layer diode on III-Nitride material in accordance with embodiments of the present disclosure. Specifically, FIG. 1B is a cross-section of a low atom migration metal nitride alloy material layer diode on III-Nitride material including a high work function metal nitride alloy in accordance with an embodiment of the present disclosure. FIG. 1C is a cross-section of a low atom migration metal nitride alloy material layer diode including a dielectric 116 and field plate 118 in accordance with an embodiment of the present disclosure. FIG. 1D is a cross-section of a low atom migration metal nitride alloy material layer diode including a vertically graded low atom migration metal nitride alloy material layer 120 in accordance with an embodiment of the present disclosure.

FIG. 1A includes N-type semiconductor material 102 and cathode ohmic metal 104. FIG. 1A also includes optional second cathode metal 106 and optional second anode metal 110. As

shown in FIG. 1A, low atom migration metal nitride alloy material layer 108 is deposited on N-type semiconductor material 102. In an embodiment, low atom migration metal nitride alloy material layer 108 has a layer that is in direct atomic contact with the III-Nitride surface of N-type semiconductor material 102. In an embodiment, the atoms comprising low atom migration metal nitride alloy material layer 108 have low migration (low diffusion) into the III-Nitride material of N-type semiconductor material 102, and the atoms comprising the III-Nitride material of N-type semiconductor material 102 have low migration into low atom migration metal nitride alloy material layer 108 (during storage or under stress).

As discussed above, in an embodiment, low atom migration (diffusion) metal nitride alloy material layer 108 to a III-Nitride device may be a two terminal device which may include, but not be limited, to a Schottky diode, a junction barrier Schottky (JBS) diode, or a merged PIN Schottky diode. Low atom migration metal nitride alloy material layer 108 may have a reverse voltage in the range of 0.2V to 50kV. In some embodiments, low atom migration metal nitride alloy material layer 108 has low atom diffusion in III-nitride alloy material for reverse voltages in the range of about 0.1V to about 5 volts. In some embodiments, low atom migration metal nitride alloy material layer 108 may have low atom diffusion in III-nitride alloy material for two terminal devices for reverse voltages to about 30 volts. In some embodiments, low atom migration metal nitride alloy material layer 108 has low atom diffusion in III-nitride alloy material for two terminal devices for reverse voltages to about 100 volts. In some embodiments, low atom migration metal nitride alloy material layer 108 has low atom diffusion in III-nitride alloy material for two terminal devices for reverse voltages to about 200 volts.

In some embodiments, low atom migration metal nitride alloy material layer 108 has low atom diffusion in III-nitride alloy material for two terminal devices for reverse voltages to about 600 volts. In some embodiments, low atom migration metal nitride alloy material layer 108 has low atom diffusion in III-nitride alloy material for two terminal devices for reverse voltages to about 1200 volts. In some embodiments, low atom migration metal nitride alloy material layer 108 has low atom diffusion in III-nitride alloy material for two terminal devices for reverse voltages to about 3300 volts. In some embodiments, low atom migration metal nitride alloy material layer 108 has low atom diffusion in III-nitride alloy material for two terminal devices to about 6500 volts. In some embodiments, low atom migration metal nitride alloy material layer 108 has low atom diffusion in III-nitride alloy material for two terminal devices for reverse voltages to about 10000 volts. In some embodiments, low atom migration metal nitride alloy material layer 108 has low atom diffusion in III-nitride alloy material for two terminal devices for reverse voltages 15000 volts.

1.2. Three Terminal Devices

In an embodiment, low atom migration metal nitride alloy material layer 108 may comprise the gate current control device structure of a three terminal field effect transistor (FET) device having terminals that comprise source, gate, and drain. In an embodiment, low atom migration metal nitride alloy material layer 108 to III-Nitride material structures or devices may be a current control device structure within a three terminal device field effect transistor device.

FIG. 2 is a schematic of a three-terminal HEMT device in accordance with an embodiment of the present disclosure. FIG. 2 includes substrate 202, GaN layer 204, AlGaIn layer 206, source 208, drain 210, overlays 212, SiN_x layers 214, and a gate/metal stack formed by gate 216 and metal 218. In an embodiment, gate 216 comprises a metal nitride electrode (e.g., TiN). In an embodiment, gate/metal stack 216 and 218 consists of Ni/Au or TiN/Ti/Au or an NCD gate.

In an embodiment, Ni/Au- and TiN-gated HEMTs were fabricated from AlGaIn/GaN HEMT structures grown by metal organic chemical vapor deposition (MOCVD) on a SiC substrate, as shown in FIG. 2. In an embodiment, devices had a gate-source spacing of 2 μm, gate length of 3 μm, gate-drain spacing of 10 μm, and gate width of 75 μm. The HEMT structure consisted of an AlN nucleation layer, Fe-doped GaN buffer layer, AlN interlayer, and an undoped Al_{0.22}Ga_{0.78}N barrier layer, with two-dimensional electron gas (2DEG) carrier density and mobility of $9.4 \times 10^{12} \text{ cm}^{-2}$ and $2070 \text{ cm}^2/(\text{V}\cdot\text{s})$ respectively, as indicated by Hall effect measurements.

In an embodiment, mesa isolation was performed using Cl₂/Ar-based inductively coupled plasma (ICP) etching. Ohmic metallization was performed by lift-off of electron-beam (e-beam) evaporated Ti/Al/Ni/Au metal, followed by rapid thermal annealing at 850 °C for 30s in flowing N₂. Overlay metallization was deposited by lift-off of e-beam evaporated Ti/Au. The devices were subsequently passivated with plasma-enhanced chemical vapor deposition (PECVD) SiN_x, and contact windows were etched using SF₆-based reactive ion etching (RIE) conducted with calibration witness SiN_x films to minimize plasma damage to the underlying AlGaIn. Ni/Au gates were fabricated on the reference sample by e-beam evaporation and lift-off. TiN gates were fabricated by blanket ALD using tetrakis (dimethylamido) titanium (IV) and N₂/H₂ plasma at 350 °C for 1000 cycles (approximately 5.5 hour growth time). TiN films produced through this process exhibited decreasing sheet resistivity with increased TiN thickness; as such, 75 nm TiN was deposited to obtain a sheet resistivity, as determined by contactless resistivity measurements. Ti/Au top gate contacts were then fabricated by e-beam deposition and liftoff, and were used as an etch mask for self-aligned SF₆-RIE etching to remove the TiN outside the gate regions. Calibration

witness samples were again utilized to minimize over-etching the TiN into the underlying SiN_x layer.

As-fabricated HEMTs and corresponding van der Pauw structures were initially tested using standard static I-V measurements to assess device performance and process effects on the HEMT structure itself. Pulsed I-V measurements were also performed to compare dynamic on-resistance ($R_{on,dyn}$) for devices with each gate material; testing was conducted from quiescent drain voltages (V_{dsq}) between 0-50 V, with a quiescent gate voltage $V_{gsq} = -6$ V, pulse width 500 ns and 1ms pulse spacing for a duty cycle of 0.05%. Electrical stress stability was conducted through reverse bias sweep, step-stress, and constant bias timed stressing in a normal air atmosphere. Thermal stability was evaluated through sequential device annealing in flowing N₂ at temperatures between 400-1000 °C in 100 °C increments for 10 minutes at a time, with device characteristics compared after each anneal.

1.3. Metal Nitride Alloy Composition

In an embodiment, low atom migration metal nitride alloy material layer 108 may be selected from a group comprising titanium nitride, titanium carbon nitride, titanium niobium nitride, titanium aluminum nitride, tantalum nitride, tungsten nitride, niobium nitride, niobium titanium nitride, molybdenum nitride, tantalum nitride (Ta_3N_5), zirconium nitride (Zr_3N_4), zirconium titanium nitride, hafnium nitride (Hf_3N_4), and copper nitride (Cu_3N). The low atom migration metal nitride may be a binary metal nitride or a ternary metal nitride alloy material. In some embodiments, the low atom migration metal nitride may be nitrogen rich TiN_x with ratio of nitrogen to titanium atoms greater than 1.0.

1.4. Semiconductor Material

The semiconductor may include, but not be limited to, elemental semiconductors, semiconductor alloy material layers, or compound semiconductors. The semiconductor may include, but not be limited to, III-V compound semiconductors or III-Nitride semiconductors. The compound semiconductor may include, but not be limited to, gallium nitride, gallium aluminum nitride, aluminum nitride, gallium aluminum indium nitride, silicon carbide, gallium oxide, or zinc oxide. The elemental semiconductors may include, but not be limited to, silicon or germanium. The semiconductor alloy material layer may include, but not be limited to, silicon germanium.

1.5. High Work Function Metal Nitride Alloy Material Layer

In an embodiment, the composite metal nitride alloy material layer may have a first metal nitride alloy material layer (e.g., a high work function metal nitride alloy material layer) having a first surface and a second surface, with the second surface in direct atomic contact with the semiconductor surface, and a second metal nitride alloy material layer with a first and second surface, with the second surface in direct contact with the first surface of the first metal nitride alloy material layer (e.g., a high work function metal nitride alloy material layer). The second metal nitride alloy material layer may have properties that include, but are not limited to, being a low resistivity metal nitride alloy material layer or being a barrier metal nitride alloy material layer. The barrier metal layer function to reduce the diffusions of atoms from the thick overlay metal through the barrier layer metal into and through the first metal nitride alloy material layer.

In an embodiment, low atom migration metal nitride alloy material layer 108 may have a selected work function within the range of about 3.2 eV to about 5.4 eV. A metal nitride alloy material layer material with high work function is desirable to reduce the reverse bias leakage current of a metal nitride Schottky diode.

Approaches to increase the work function metal nitride alloy material layer material may include, but not be limited to, increasing the nitrogen content in the metal nitride alloy material layer, increasing the carbon content in the metal nitride alloy material layer, increasing the oxygen content in the metal nitride alloy material layer, or combinations therein. For example, increasing both the nitrogen and the carbon content in the metal nitride alloy material or increasing the nitrogen and oxygen in the metal nitride alloy material will increase the work function of the metal nitride alloy material layer.

FIG. 1B is a cross-section of a low atom migration metal nitride alloy material layer diode on III-Nitride material including a high work function metal nitride alloy in accordance with an embodiment of the present disclosure. In FIG. 1B, low atom migration metal nitride alloy material layer 108 includes two layers: high work function metal nitride alloy layer 112 and low migration metal nitride alloy material layer 114.

High work function metal nitride alloy material layer 112 will typically have a work function value in the range of about 4.5 eV to about 5.4eV. High work function metal nitride alloy material layer 112 may be a binary metal nitride alloy material layer having a nitrogen rich material with a ratio of nitrogen to metal atoms greater than 1.0. In some embodiments, the nitrogen to metal atom ratio is greater than 1.1. In some embodiments, the nitrogen to metal atom ratio is

greater than 1.2. High work function metal nitride alloy material layer 202 may also have carbon dopants or oxygen dopants.

High work function metal nitride alloy material layer 112 may also be a ternary metal nitride alloy material layer, such as titanium carbon nitride alloy material layer, tantalum carbon nitride, or titanium oxide nitride. The carbon or oxygen dopants or sufficient high concentration to form a ternary alloy material layer can be incorporated during metal nitride alloy material layer material deposition or can be incorporated by annealing in a carbon based molecule ambient such as methane or an oxygen containing ambient. The oxygen annealing can remove oxygen vacancies and thus increase the work function.

High work function metal nitride alloy material layer 112 may also be a laminated material structure, such a stacked material layer structure of titanium oxide and titanium nitride that can be formed by alternating deposition titanium oxide and titanium nitride in an atomic layer deposition system.

In an embodiment, the work function of high work function metal nitride alloy material layer 112 also varies as a function of thickness of the material layer. The work function of high work function metal nitride alloy material layer 112 increases with increasing thickness of the metal nitride alloy material layer.

High work function metal nitride alloy material layer 112 may be a low atom migration high work function metal nitride alloy material layer. High work function metal nitride alloy material layer 112 may be a low plasma damage or non-energetic high work function metal nitride alloy material layer. Titanium nitride typically has a work function in the range of about 4.2eV to about 5.2eV.

Low migration metal nitride alloy material layer 114 may comprise dopant atoms that may include but not be limited to nitrogen, carbon, tantalum, titanium, tungsten or combinations thereof. Low migration metal nitride alloy material layer 114 may also comprise dopant atoms that may include but not be limited to oxygen, platinum, silicon, aluminum, vanadium or combinations therein.

2. Stable Material Under Electric Field or Thermal Stress

In an embodiment, low atom migration metal nitride alloy material layer 108 may be an enhanced device that includes, but is not limited to, an enhanced high electric field reliable device, an enhanced high temperature reliable device, or combinations thereof. In an embodiment,

low atom migration metal nitride alloy material layer 108 is stable under stresses which may include, but not be limited to, electric field stress, thermal stress, radiation stress, or combination therein. In an embodiment, low atom migration metal nitride alloy material layer 108 may be an enhanced high electric field reliable device and/or an enhanced high temperature reliable device.

- 5 In an embodiment, low atom migration metal nitride alloy material layer 108 may be an enhanced high temperature reliable device or an enhanced high radiation reliable device.

3. Non-Plasma Damage or Non-Energetic Ion Damage

- 10 The semiconductor material can be damaged by energetic ions, energetic electrons, or ultraviolet light that can be present in the environment in the apparatus that is used to deposit the metal nitride alloy material layer. For example, a sputtering deposition approach has energetic ions in the deposition tool environment that impact into the semiconductor material and creates point defects within about 30nm of the semiconductor surface and surface state traps at the semiconductor surface. Plasma deposition approaches, such as Plasma Enhanced Chemical Vapor
15 deposition, also have energetic ions and ultraviolet wavelengths within the deposition tool environment that impact into the semiconductor material and create point defects within about 30nm of the semiconductor surface and surface state traps at the semiconductor surface. The additional plasma damage or energetic ion damage point defects within the semiconductor and additional
20 surface state traps can create enhanced leakage current and reduced carrier mobility in a device such as a two-terminal Schottky diode or a three-terminal field effect transistor that is formed in the region near of the semiconductor surface.

- Thus, a deposition metal may be selected to have low plasma damage or low energetic ion damage at the surface of the semiconductor. Low atom migration metal nitride alloy material
25 layer 108 may have a low density of displaced atoms (point defects) within the semiconductor within 100nm of the metal nitride alloy material layer to semiconductor interface (within 100nm of the semiconductor surface). Deposition methods for the metal nitride alloy material layer that have low plasma damage or low energetic ion damage in the semiconductor include, but may not be limited to, atomic layer deposition, chemical vapor deposition, or metal organic chemical va-
30 por deposition. In addition, additional deposition techniques that have low plasma damage or low energetic ion damage within the semiconductor include remote plasma assisted atomic layer deposition, ozone assisted atomic layer deposition, or plasma assisted atomic layer deposition. Low atom migration metal nitride alloy material layer 108 may be a non-plasma damaged device or a non-energetic ion damaged device or a non-ultraviolet light damage device.

4. Large Area Uniform Deposition

Low atom migration metal nitride alloy material layer 108 may have lateral material composition uniformity and material thickness uniformity over the lateral dimension of a substrate surface. For selected deposition methods, the lateral thickness uniformity may be less than 2% thickness non-uniformity over the substrate surface (excluding 2 millimeters from the edge of the substrate). Deposition methods for the metal nitride alloy material layer that have lateral uniform material composition and material thickness uniformity lateral material composition uniformity and material thickness uniformity over the lateral dimension of a substrate surface include, but are not limited to, atomic layer deposition, chemical vapor deposition, metal organic chemical vapor deposition, remote plasma assisted atomic layer deposition, ozone assisted atomic layer deposition, or plasma assisted atomic layer deposition.

5. Large Area Electrically Uniform Characteristics

Low atom migration metal nitride alloy material layer 108 may comprise an electrically uniform interface. Low atom migration metal nitride alloy material layer 108 may comprise an electrically uniform interface across the substrate surface. For selected deposition methods, the forward voltage of a Schottky Diode may have a value that is less than +/- 5% forward voltage non-uniformity over the substrate surface (excluding 2 millimeters from the edge of the substrate).

Deposition methods for low atom migration metal nitride alloy material layer 108 that have lateral uniform material composition and material thickness uniformity over the lateral dimension of a substrate surface include, but are not limited to, atomic layer deposition, chemical vapor deposition, metal organic chemical vapor deposition, remote plasma assisted atomic layer deposition, ozone assisted atomic layer deposition, or plasma assisted atomic layer deposition.

6. Non-alloy material layer III-Nitride material interface

In an embodiment, low atom migration metal nitride alloy material layer 108 may comprise a non-alloy material layer of the titanium nitride alloy material layer with the III-Nitride at the metal nitride/III-Nitride interface.

TiN and nanocrystalline diamond have been evaluated as potential replacements for conventional Ni-based gate schemes in AlGaIn/GaN HEMTs using reverse bias electrical stressing. TiN gates deposited by atomic layer deposition were found to be viable substitutes, as TiN-gated devices exhibited improved on-state characteristics in comparison to the Ni/Au-gated devices.

- 5 TiN was also determined to have a much higher critical reverse gate voltage ($V_{gs} = -210$ V for TiN vs. -120 V for Ni/Au) at which gate degradation occurs. The TiN gates also catastrophically failed at slightly higher and much less variable breakdown voltages than the Ni/Au gates. Stressing at reverse gate biases slightly above the Ni/Au critical voltage but well below the TiN critical voltage ($V_{gs} = -140$ V) led to nearly an order of magnitude increase in leakage current for the
- 10 Ni/Au, but decreased leakage in the TiN.

Nanocrystalline diamond gates exhibited critical voltages of $V_{gs} = -90$ V and broke down at much lower reverse bias, possibly due to testing in air without encapsulation to protect the gate material.

15 7. Conformal Material Deposition

- In an embodiment, low atom migration metal nitride alloy material layer 108 may have a conformal material layer thickness on a three-dimensional substrate surface. For example, FIG. 1C is a cross-section of a low atom migration metal nitride alloy material layer diode including a
- 20 dielectric 116 and field plate 118 in accordance with an embodiment of the present disclosure.

8. Vertical Graded Material Composition and Laminated Material Composition

- Low atom migration metal nitride alloy material layer 108 to semiconductor device may
- 25 have a vertically graded composition. FIG. 1D is a cross-section of a low atom migration metal nitride alloy material layer diode including a vertically graded low atom migration metal nitride alloy material layer 120 in accordance with an embodiment of the present disclosure.

- In an embodiment, vertically graded low atom migration metal nitride alloy material layer 120 may be formed by a laminate growth process in an atomic layer deposition tool. For exam-
- 30 ple, a metal nitride alloy material layer that would have higher work function is the sequential deposition of a titanium nitride atomic layer and a titanium carbide layer. The percentage of carbon in the film can be varied by selecting the ratio of the number of titanium carbide layers to the number of titanium nitride layers. The can be mixing of the atomic layers after an anneal process. Thus, an alloy such as titanium carbide nitride can be formed by a laminated growth structure.

Deposition methods for the metal nitride alloy material layer that may have a graded vertical material composition or laminated material composition include, but are not limited to, atomic layer deposition, remote plasma assisted atomic layer deposition, ozone assisted atomic layer deposition, or plasma assisted atomic layer deposition.

5

9. Experimental

TiN and nanocrystalline diamond have been evaluated as potential replacements for conventional Ni-based gate schemes in AlGaIn/GaN HEMTs using reverse bias electrical stressing.

10 TiN gates deposited by atomic layer deposition were found to be viable substitutes, as TiN-gated devices exhibited improved on-state characteristics in comparison to the Ni/Au-gated devices. TiN was also determined to have a much higher critical reverse gate voltage ($V_{gs} = -210$ V for TiN vs. -120 V for Ni/Au) at which gate degradation occurs. The TiN gates also catastrophically failed at slightly higher and much less variable breakdown voltages than the Ni/Au gates.

15 Stressing at reverse gate biases slightly above the Ni/Au critical voltage but well below the TiN critical voltage ($V_{gs} = -140$ V) led to nearly an order of magnitude increase in leakage current for the Ni/Au, but decreased leakage in the TiN. Nanocrystalline diamond gates exhibited critical voltages of $V_{gs} = -90$ V and broke down at much lower reverse bias, possibly due to testing in air without encapsulation to protect the gate material.

20 Devices with Ni/Au, TiN, and p⁺ diamond gates (e.g., as shown schematically in FIG. 1A) were fabricated from an AlGaIn/GaN HEMT structure grown by metal organic chemical vapor deposition (MOCVD) on a SiC substrate, consisting of an AlN nucleation layer, Fe-doped GaN buffer, AlN interlayer, and an undoped Al_{0.22}Ga_{0.78}N barrier layer. Hall effect measurements indicated that the two-dimensional electron gas (2DEG) carrier density and mobility were
25 9.4×10^{12} cm⁻² and 2070 cm²/(V·sec), respectively. The devices had a gate-source spacing of 2 μ m, a gate length of 3 μ m, gate-drain spacing of 10 μ m, and gate width of 75 μ m. Device mesas were fabricated using Cl₂-based inductively coupled plasma (ICP) etching. Ohmic contacts were formed by lift-off and rapid thermal annealing (RTA) of electron-beam (e-beam) evaporated Ti/Al/Ni/Au metal.

30 After Ohmic contact processing, all devices were passivated with 100 nm plasma-enhanced chemical vapor deposition (PECVD) SiN_x. SF₆-based reactive ion etching (RIE) was used to open gate and overlay windows in the SiN_x. On the reference sample, Ni/Au gates were fabricated by e-beam evaporation and lift-off. TiN-gated HEMTs were fabricated by atomic layer deposition (ALD) of 75 nm TiN, followed by e-beam deposition and lift-off of Ti/Au contacts.

The Ti/Au was then used as an etch mask for self-aligned SF₆-RIE etching to remove the TiN outside the device gate regions. NCD gates were fabricated by blanket growth of 500 nm boron-doped nanocrystalline diamond by microwave chemical vapor deposition (MW-CVD).

After NCD growth, Ti/Al/Ni/Au gate contacts were fabricated by e-beam deposition and lift-off; the contacts were then used as a self-aligned etch mask for removal of NCD outside the gate regions using an O₂-RIE etch. Overlay metal was deposited on all samples by lift-off of e-beam evaporate.

10. Results

10.1. Device Performance

As-fabricated device performance was evaluated via static I-V measurements using a Keithley 4200 III-Nitride Characterization System. FIG. 3 is a table (Table I) showing relevant parameters for each device listed in Table I. The TiN-gated HEMTs offered improved on-state characteristics in the form of higher maximum transconductance ($g_{m,max}$), higher maximum on-state drain current ($I_{ds,max}$), and lower on-resistance (R_{on}) than the Ni/Au-gated HEMTs, albeit at the expense of higher off-state gate and device leakage (I_{off}). Hall Effect measurements were also performed on gated van der Pauw patterns fabricated with the devices to characterize the effects of the recess etch and gate deposition processes on the 2DEG density (n_s) and carrier mobility (μ_{2DEG}). The decreased 2DEG density and mobility of the Ni/Au devices relative to the as-grown structure was attributed to fluorination of the AlGa_N barrier layer during the recess etch. The TiN-gated devices were less degraded, as the structure was effectively annealed during the TiN growth process (350 °C for multiple hours). The on-state performance and Hall characteristics of the NCD-gated HEMTs was worse than expected in comparison to previous results; this could be due to either nonuniform boron doping or damage to the AlGa_N barrier during diamond growth.

10.2. Electrical Stressing

All three device schemes were initially tested by reverse bias sweeping from $V_{gs} = 0$ to breakdown. FIG. 4 is a diagram showing gate leakage during gate voltage sweeping from 0V to reverse breakdown for Ni/Au-, TiN-, and NCD-gated HEMTs. In FIG. 4, critical voltage limits after which gate degradation occurs are marked for each gate scheme.

As shown in FIG. 4, the Ni/Au-gated HEMTs exhibited a critical voltage of $V_{gs} = -120$ V, as evidenced by the sudden increase and subsequent instability in gate leakage for higher reverse voltage; this is consistent with previous reports of Ni/Au gate instability under reverse bias stressing. TiN gates were found to exhibit a much higher critical voltage of $V_{gs} = -210$ V, albeit with significantly higher overall leakage in comparison to the Ni/Au. This may stem from the lower barrier height at the TiN/AlGaIn interface, owing to the lower (and variable) work function of TiN in comparison to Ni/Au, or from the formation of a leaky surface layer at the interface during the initial stages of TiN growth. The NCD-gated HEMT exhibited stable gate current to only $V_{gs} = -90$ V; beyond this voltage, the device gate current steadily increased until the gate failed catastrophically at only -160 V. These devices failed as an open gate rather than a short in the case of the previous two devices. It is possible that the gate may have been etched by the ambient atmosphere due to self-heating during reverse bias stressing.

To further assess the breakdown characteristics of the Ni/Au and TiN gates, five HEMTs with each gate scheme were tested to breakdown under step-stress measurements. FIG. 5 is a table (Table II) showing breakdown voltages for Ni/Au- and TiN-gated HEMTs. The Ni/Au gates failed catastrophically at varying reverse bias, ranging from -210 V to -270 V, with an average breakdown voltage of approximately -240 V. The TiN failed at a much narrower voltage range (around -270 V), indicating that the TiN gates had both a slightly higher reverse breakdown voltage, as well as a more consistent range of reverse bias failure conditions.

Initial assessments of the time-dependent electrical stress degradation were made by holding devices at a constant gate bias of -140 V for 1 hour ($V_{ds} = 0$). This bias was selected to evaluate the stability of each gate scheme at a condition above the critical voltage that should initiate degradation (but not failure) in the reference Ni/Au devices.

Gate stability was evaluated by observing the gate current during stressing. FIG. 6 is a diagram showing turn-on (I_{ds} - V_{gs}) characteristics at $V_{ds} = 10$ V for HEMT devices with Ni/Au, TiN, and NCD gates.

Changes in the gate I-V characteristics before and after stressing were also evaluated. During this stress, the Ni/Au gate leakage at increased by nearly 225% without device failure, indicating that the gate degraded under these conditions. TiN gate leakage actually decreased to a stable value during stressing, possibly due to a self-annealing effect in the TiN during stressing. The NCD gate failed almost immediately under these conditions; this was expected given that the stress condition was significantly beyond the critical voltage identified in Figure 4.

Comparison of the pre- and post-stress gate current confirmed that permanent degradation occurred in the Ni/Au gate after stressing above the critical voltage, as the gate leakage increased

by nearly an order of magnitude after stressing. Conversely, the TiN leakage decreased as a result of the stressing, since the selected stress condition was well below the observed critical voltage for TiN. The decrease during stressing also suggests that the TiN leakage may be further reduced by annealing the gate films before testing.

5 Ni/Au-, TiN-, and NCD-gated HEMTs were successfully fabricated and characterized under static I-V testing. Stressing of the device gates under high reverse bias identified critical voltage conditions that led to degradation and catastrophic failure. Ni/Au gates exhibited a critical voltage around $V_{gs} = -120$ V, and failed catastrophically at voltages between -210 V to -270 V. TiN gates exhibited a significantly higher critical voltage of -210 V, along with much more consistent breakdown voltages around -270 V. NCD-gated HEMTs exhibited lower critical voltages of -90 V and breakdown voltages around -160 V, possibly due to gate degradation during high bias testing in the ambient atmosphere. Stressing at $V_{gs} = -140$ V (above the Ni/Au critical voltage) for one hour led to permanent degradation in the Ni/Au gates, as evidenced by higher leakage currents during and after stressing. The TiN gates improved as a result of this stress condition (below the TiN critical voltage), while the NCD gates failed almost immediately due to stressing well above their critical voltage. TiN gates are therefore expected to be more stable under high reverse bias conditions than the Ni/Au or unencapsulated NCD gates.

FIG. 7 is a diagram showing static drain current-drain voltage (I_{ds} - V_{ds}) behavior for Ni/Au, TiN, and NCD-gated HEMTs. (V_{gs} ranged from -10 V to 1 V in 1 V steps.) FIG. 8 is a diagram showing Ni/Au, TiN, and NCD gate during stressing at $V_{gs} = -140$ V for 1 hour (NCD gate failed within 60 sec of stress initiation). FIG. 9 is a diagram showing Ni/Au and TiN gate leakage currents before and after stressing at $V_{gs} = -140$ V for 1 hour. The Ni/Au gate leakage increased by nearly one order of magnitude after stressing, while the TiN leakage decreased.

11. Methods

Methods in accordance with embodiments of the present disclosure include methods wherein low atom migration metal nitride alloy material layer 108 can be deposited by a non-plasma process metal which may include, but not be limited to, atomic layer deposition, metal organic chemical vapor deposition, chemical vapor deposition, or molecular beam deposition. Methods in accordance with embodiments of the present disclosure include methods wherein low atom migration metal nitride alloy material layer 108 can be deposited by a low-plasma process metal which may include, but not be limited to, plasma assisted atomic layer deposition, metal organic chemical vapor deposition, chemical vapor deposition, or molecular beam deposition.

Methods in accordance with embodiments of the present disclosure include methods wherein low atom migration metal nitride alloy material layer 108 can be deposited by a remote-plasma process metal which may include, but not be limited to, remote plasma assisted atomic layer deposition, metal organic chemical vapor deposition, chemical vapor deposition, or molecular beam deposition.

In accordance with embodiments of the present disclosure, low atom migration metal nitride alloy material layer 108 can be deposited by methods that include, but are not limited to, atomic layer deposition, plasma assisted atomic layer deposition, or remote plasma assisted atomic layer deposition. Low atom migration metal nitride alloy material layer 108 can be annealed at a selected temperature and selected ambient. Low atom migration metal nitride alloy material layer 108 can be deposited in-situ with a semiconductor material growth system such as a III-Nitride alloy material growth system, III-V material growth system, or gallium oxide system, for example.

FIG. 10 is a flowchart of a method for creating a semiconductor device in accordance with an embodiment of the present disclosure. In step 1002, GaN is formed on a substrate. For example, in an embodiment, a GaN layer is formed on Sapphire with an N⁺ subdiffusion layer or GaN N-epi on a N⁺ Substrate. In step 1004, a dielectric layer (such as sputtered AlN, MOCVD grown AlN, CVD deposited SiO₂, PECVD SiO₂, or ALD Al₂O₃) is deposited on the GaN. In step 1006, an opening is defined in the dielectric layer by etching after a photoresist process. In step 1008, the surface is cleaned.

In step 1010, a low atom migration metal nitride alloy material layer (e.g., a TiN metal alloy material layer) is deposited (e.g., using an atomic layer deposit (ALD) technique) on the dielectric and the GaN. In optional step 1012, the low atom migration metal nitride alloy material layer (e.g., the TiN metal alloy material later) can be annealed (e.g., in the range of 100C to 900C). In step 1014, the TiN metal alloy material layer is etched (e.g., using a photoresist process). In step 1016, the ohmic contact metal to GaN is lifted off. In optional step 1018, thick metal on the surface of the ALD TiN material layer and ohmic metal layer is defined.

12. Conclusion

It is to be appreciated that the Detailed Description, and not the Abstract, is intended to be used to interpret the claims. The Abstract may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, is not intended to limit the present disclosure and the appended claims in any way.

The present disclosure has been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

The foregoing description of the specific embodiments will so fully reveal the general nature of the disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure.

Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

While various embodiments of the present disclosure have been described above, it should be understood that they have been presented by way of example only, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the disclosure. Thus, the breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:
5 a semiconductor layer; and
a low atom migration metal nitride alloy material layer coupled to the semiconductor layer, wherein the low atom migration metal nitride alloy material layer is in direct atomic contact with the semiconductor layer.
- 10 2. The semiconductor device of claim 1, wherein the low atom migration metal nitride alloy material layer is formed from TiN.
3. The semiconductor device of claim 1, wherein contact between the semiconductor layer and the low atom migration metal nitride alloy material layer forms a Schottky diode.
- 15 4. The semiconductor device of claim 3, wherein the Schottky diode comprises a TiN gate on an AlGaIn/GaN high electron mobility transistor (HEMT).
5. The semiconductor device of claim 1, wherein the semiconductor layer comprises III-Ni-
20 tride material.
6. The semiconductor device of claim 5, wherein first atoms in the low atom migration metal nitride alloy material layer have low migration into the III-Nitride material, and wherein second atoms in the III-Nitride material have low migration into the low atom migration metal
25 nitride alloy material layer.
7. The semiconductor device of claim 5, wherein the low atom migration metal nitride alloy material layer comprises:
a high work function metal nitride alloy material layer coupled to the semiconductor
30 layer; and
a low migration metal nitride alloy material layer coupled to the high work function metal nitride alloy material layer.
8. The semiconductor device of claim 1, wherein the low atom migration metal nitride alloy

material layer comprises:

a tunneling material layer at an interface between the low atom migration metal nitride alloy material layer and the semiconductor layer.

5 9. The semiconductor device of claim 5, wherein the low atom migration metal nitride alloy material layer has a vertically graded composition.

10. The semiconductor device of claim 1, wherein the low atom migration metal nitride alloy material layer is deposited by atomic layer deposition.

10

11. The semiconductor device of claim 1, wherein the low atom migration metal nitride alloy material layer is deposited using atomic layer deposition, metal organic chemical vapor deposition, chemical vapor deposition, or molecular beam deposition.

15 12. A Schottky diode, comprising:

a semiconductor layer; and

a low atom migration metal nitride alloy material layer coupled to the semiconductor layer, wherein the low atom migration metal nitride alloy material layer is in direct atomic contact with the semiconductor layer.

20

13. The Schottky diode of claim 12, wherein the low atom migration metal nitride alloy material layer is formed from TiN.

14. The Schottky diode of claim 12, wherein first atoms in the low atom migration metal nitride alloy material layer have low migration into III-Nitride material of the semiconductor layer, and wherein second atoms in the III-Nitride material have low migration into the low atom migration metal nitride alloy material layer.

25

15. The Schottky diode of claim 12, wherein the low atom migration metal nitride alloy material layer comprises:

30

a high work function metal nitride alloy material layer coupled to the semiconductor layer; and

a low migration metal nitride alloy material layer coupled to the high work function metal nitride alloy material layer.

16. The Schottky diode of claim 12, wherein the low atom migration metal nitride alloy material layer has a vertically graded composition.
- 5 17. A method of creating a semiconductor device, the method comprising:
forming a GaN layer on a substrate;
depositing a dielectric layer on the GaN layer;
defining an opening in the dielectric layer;
cleaning a surface of the dielectric layer;
10 depositing a TiN metal alloy material layer on the dielectric layer and the GaN layer;
etching a surface of the TiN metal alloy material layer; and
lifting off ohmic contact metal to the GaN layer.
18. The method of claim 17, further comprising:
15 lifting ohmic contact metal from the GaN layer.
19. The method of claim 17, further comprising:
annealing the TiN metal alloy material layer.
- 20 20. The method of claim 17, wherein the TiN metal alloy material layer is deposited using metal organic chemical vapor deposition, chemical vapor deposition, or molecular beam deposition.

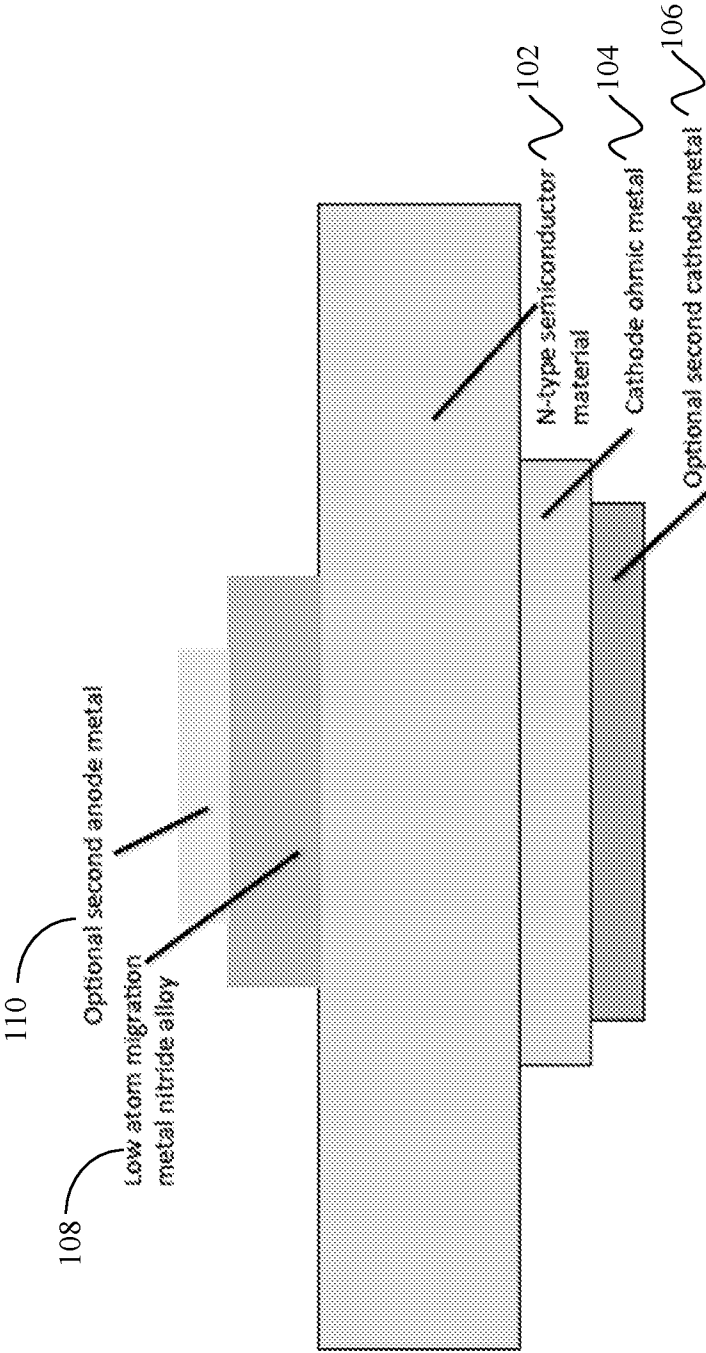


FIG. 1A

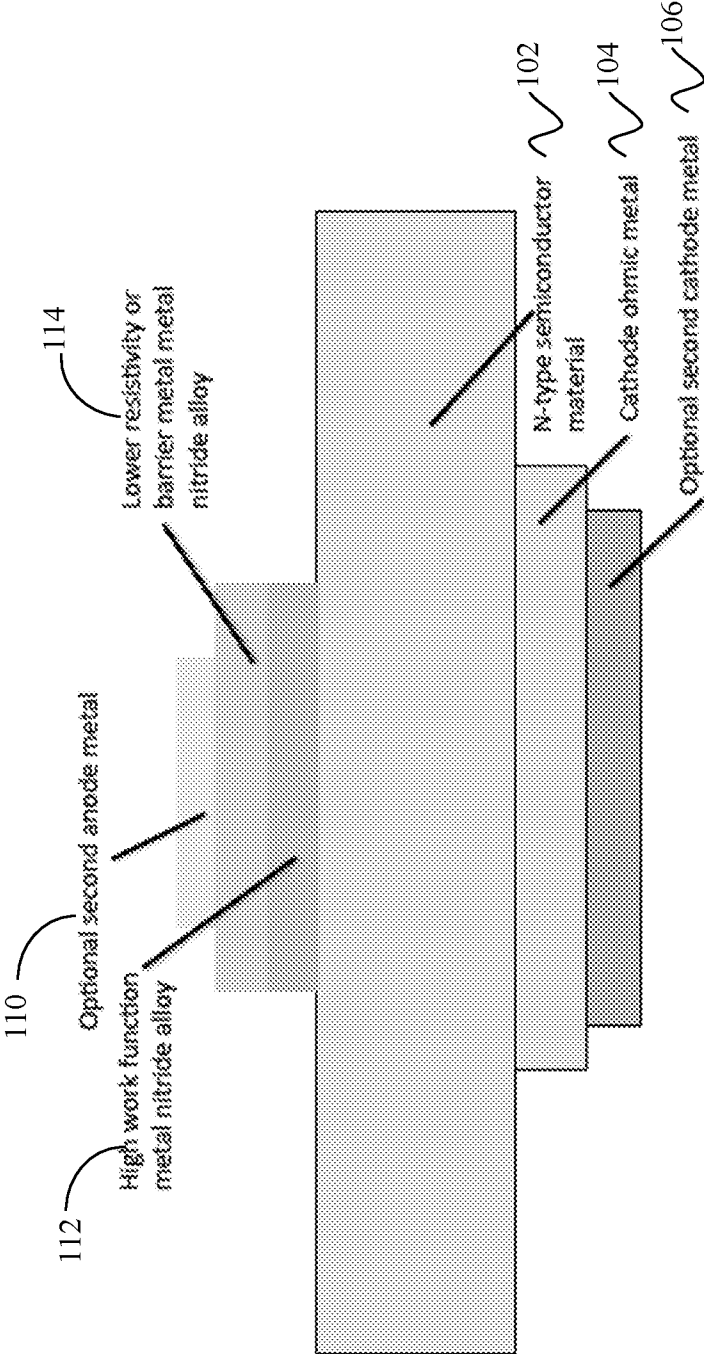


FIG. 1B

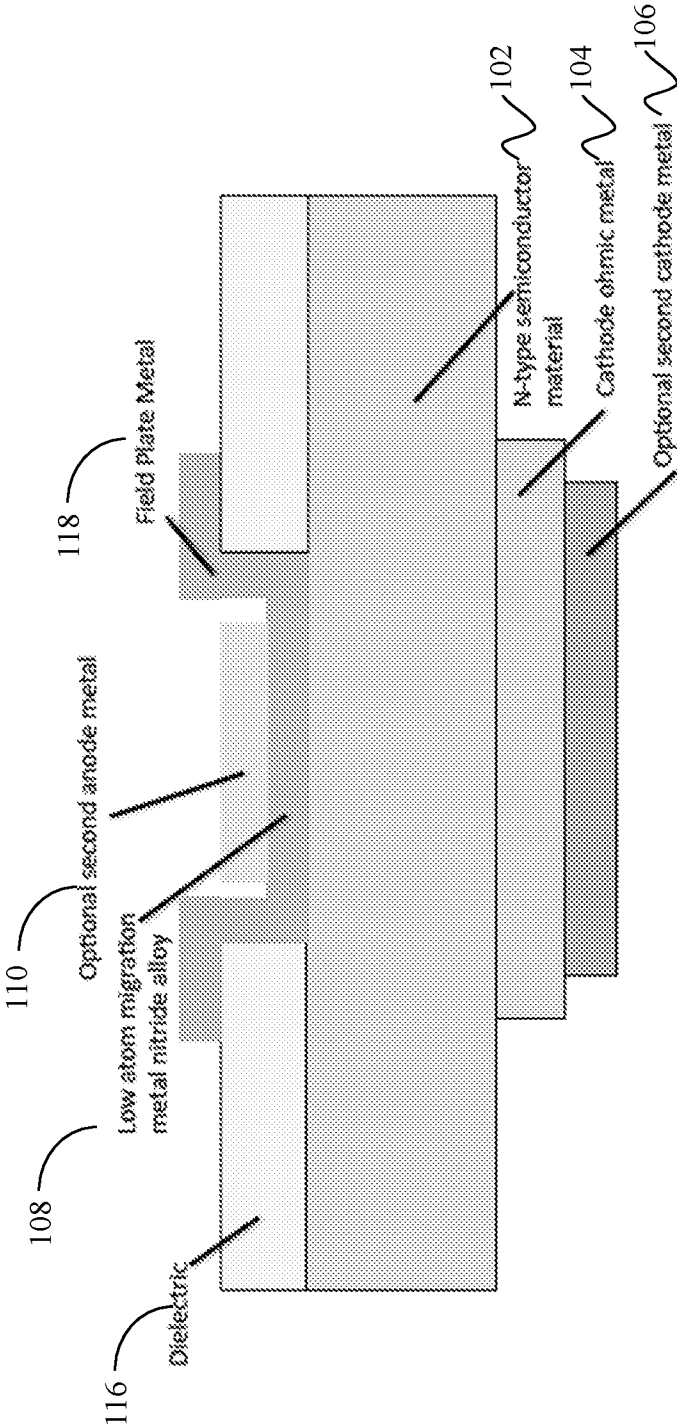


FIG. 1C

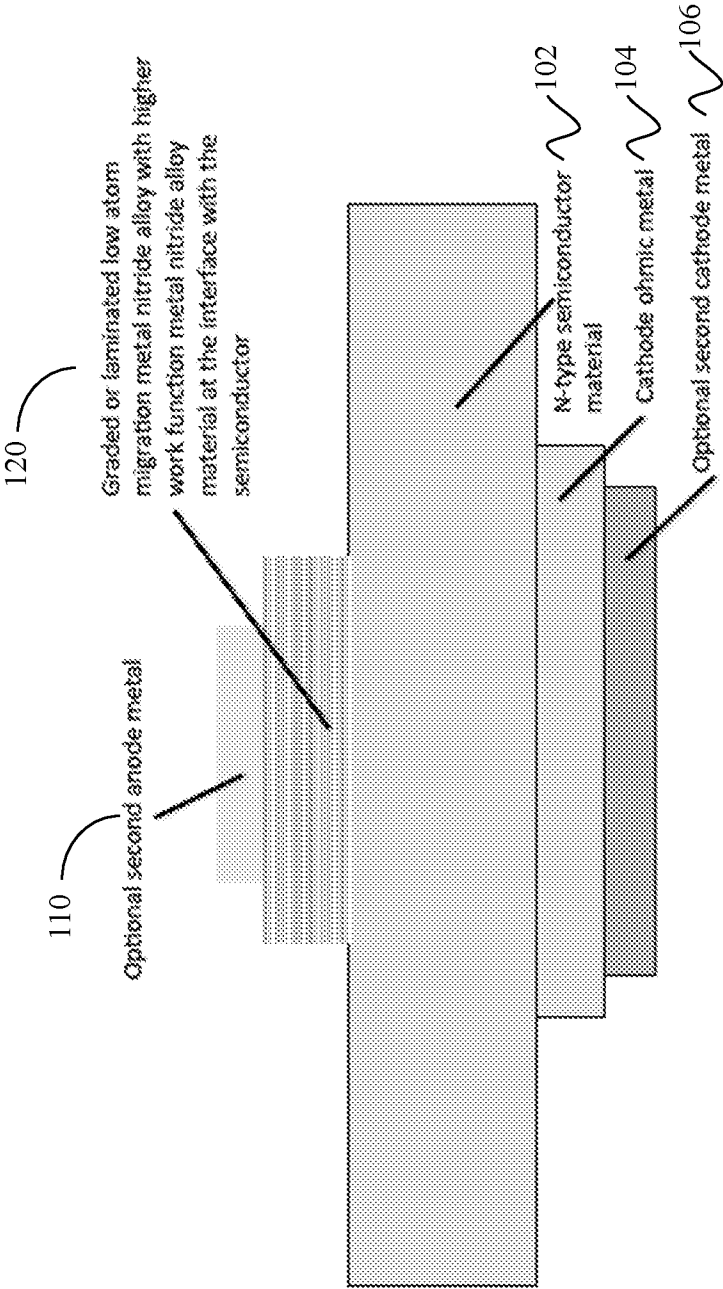


FIG. 1D

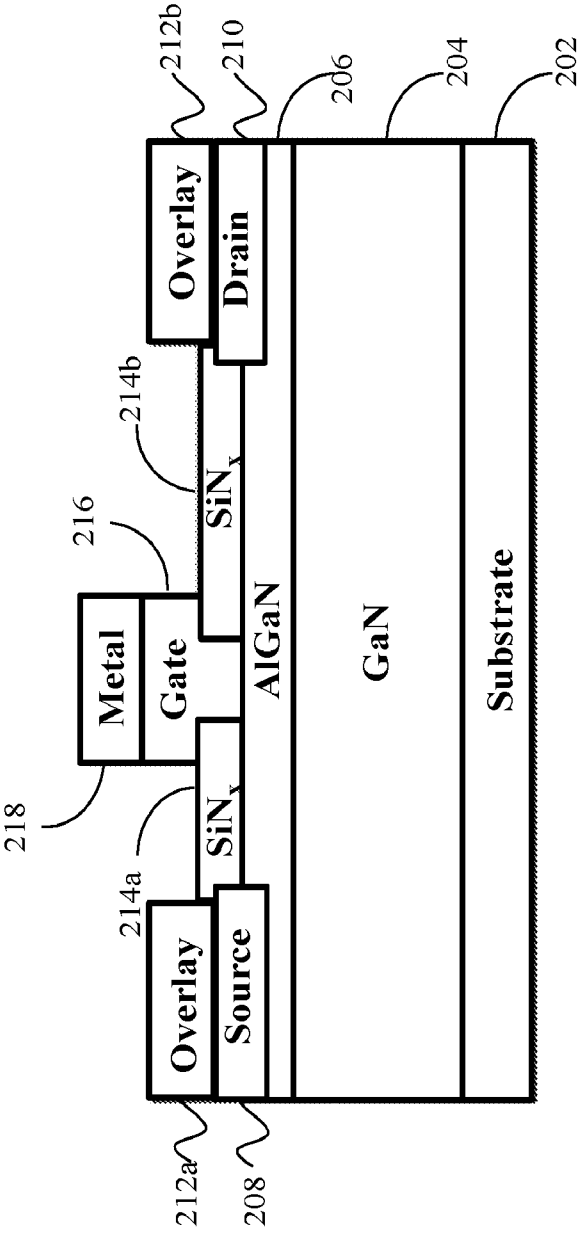


FIG. 2

TABLE I
DEVICE PARAMETERS FOR Ni/AU-, TiN-, AND NCD GATED HEMT'S

Parameter	Units	Gate Material	
		Ni/Au	TiN
V_t	V	-2.47	-2.77
$I_{off} (V_{gs} = -10V)$	mA/mm	0.179	4.88
$g_{m,max}$	mS/mm	140	159
$I_{ds,max} (V_{gs} = 1V)$	mA/mm	491	589
R_{on}	$\Omega \cdot mm$	8.61	8.10
n_s	cm^{-2}	6.76×10^{12}	7.75×10^{12}
μ_{DEG}	$cm^2/(V \cdot sec)$	1890	1950
			n/a

FIG. 3

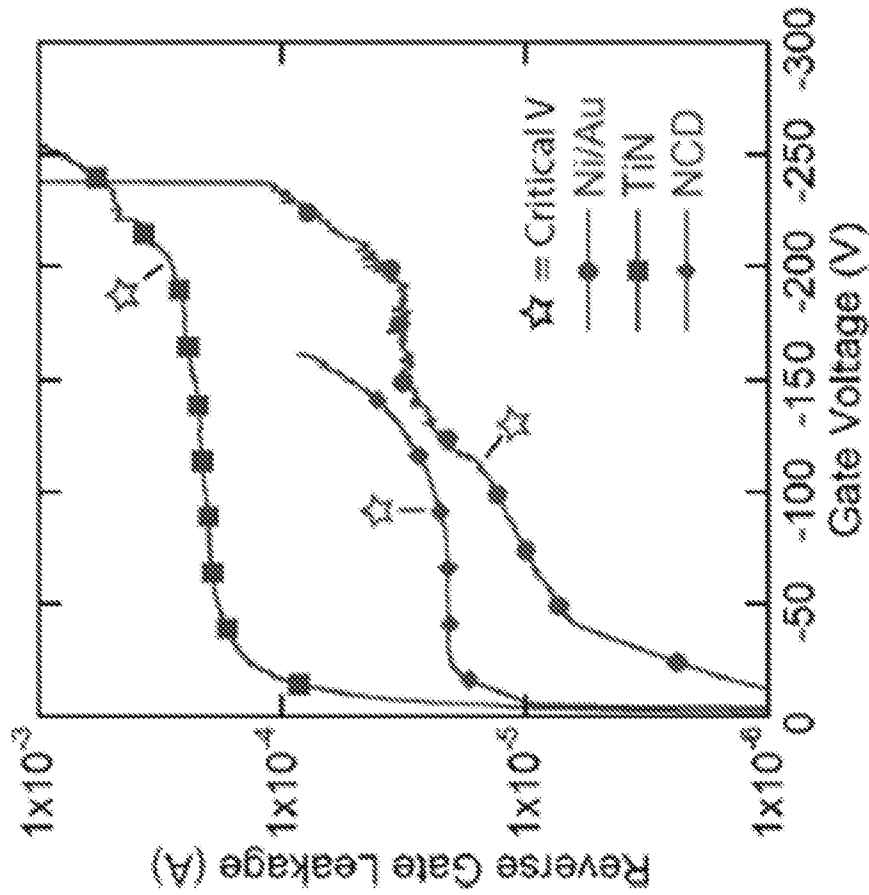


FIG. 4

TABLE II

BREAKDOWN VOLTAGES FOR Ni/AU- AND TiN-GATED HEMT'S

Gate	Reverse Breakdown Voltage (V)	
	Individual	Average (Nearest 10V)
Ni/Au	-220	-240 ± 30 V
	-250	
	-210	
	-260	
	-270	
TiN	-250	-270 ± 10 V
	-270	
	-270	
	-270	
	-270	

FIG. 5

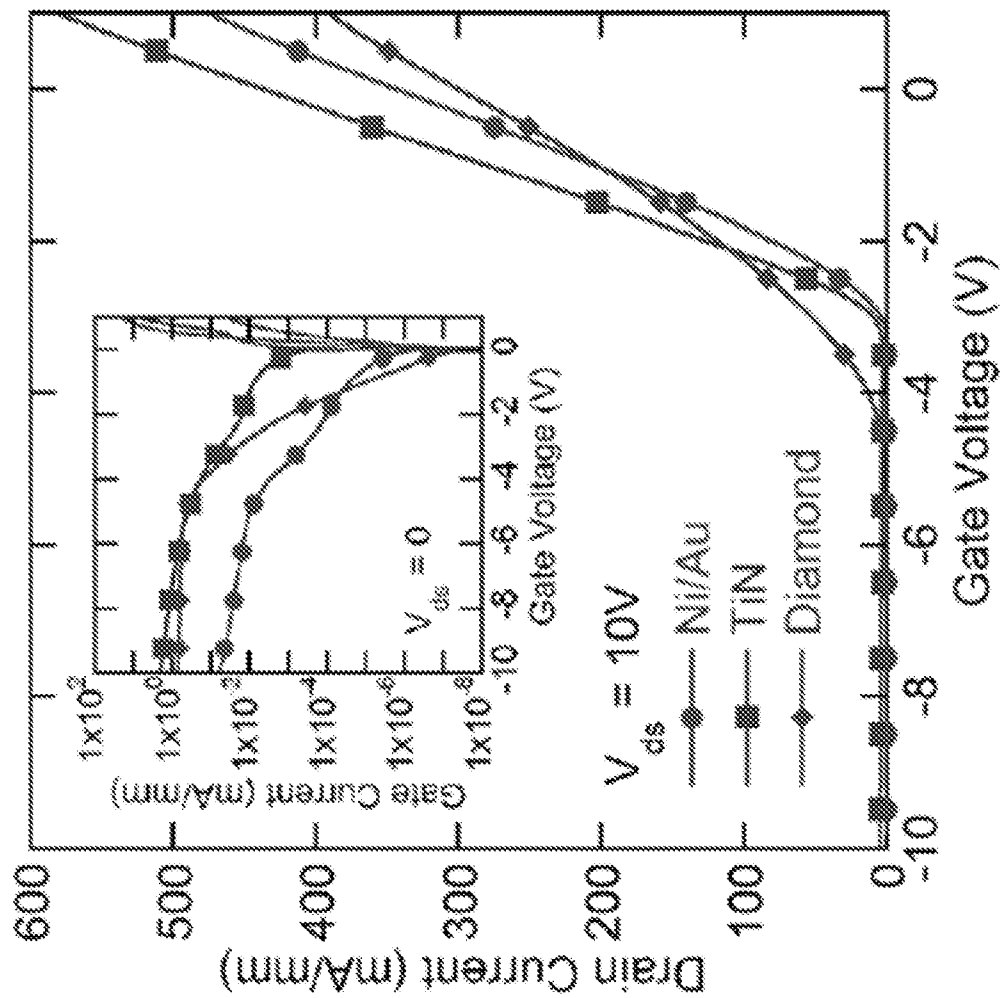


FIG. 6

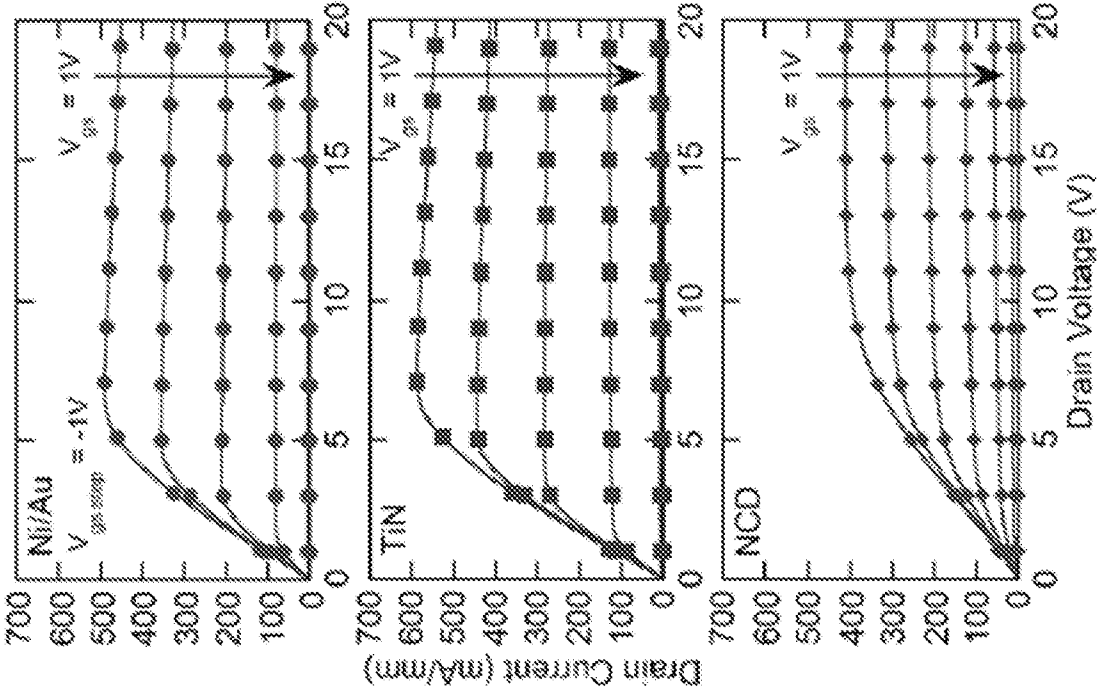


FIG. 7

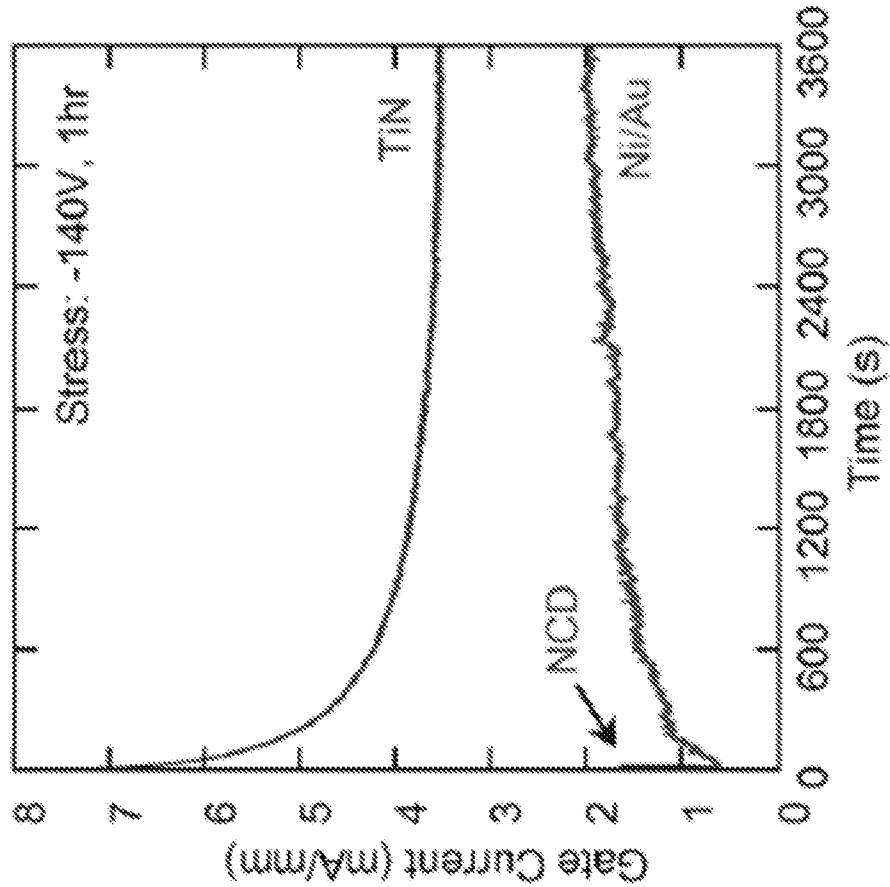


FIG. 8

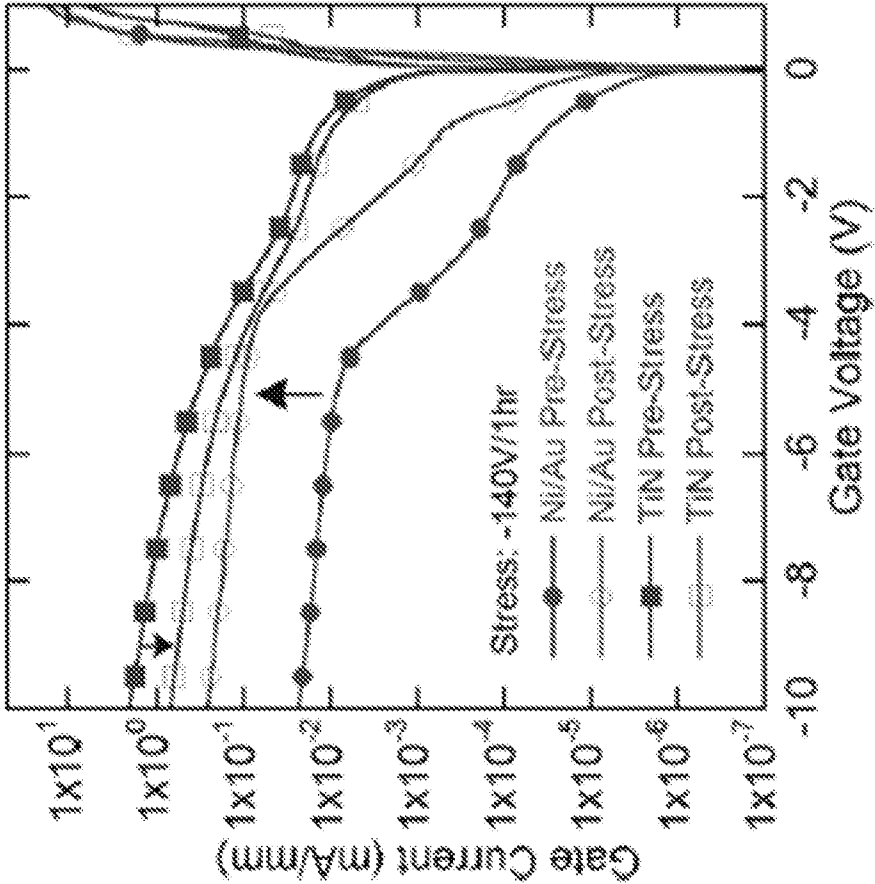


FIG. 9

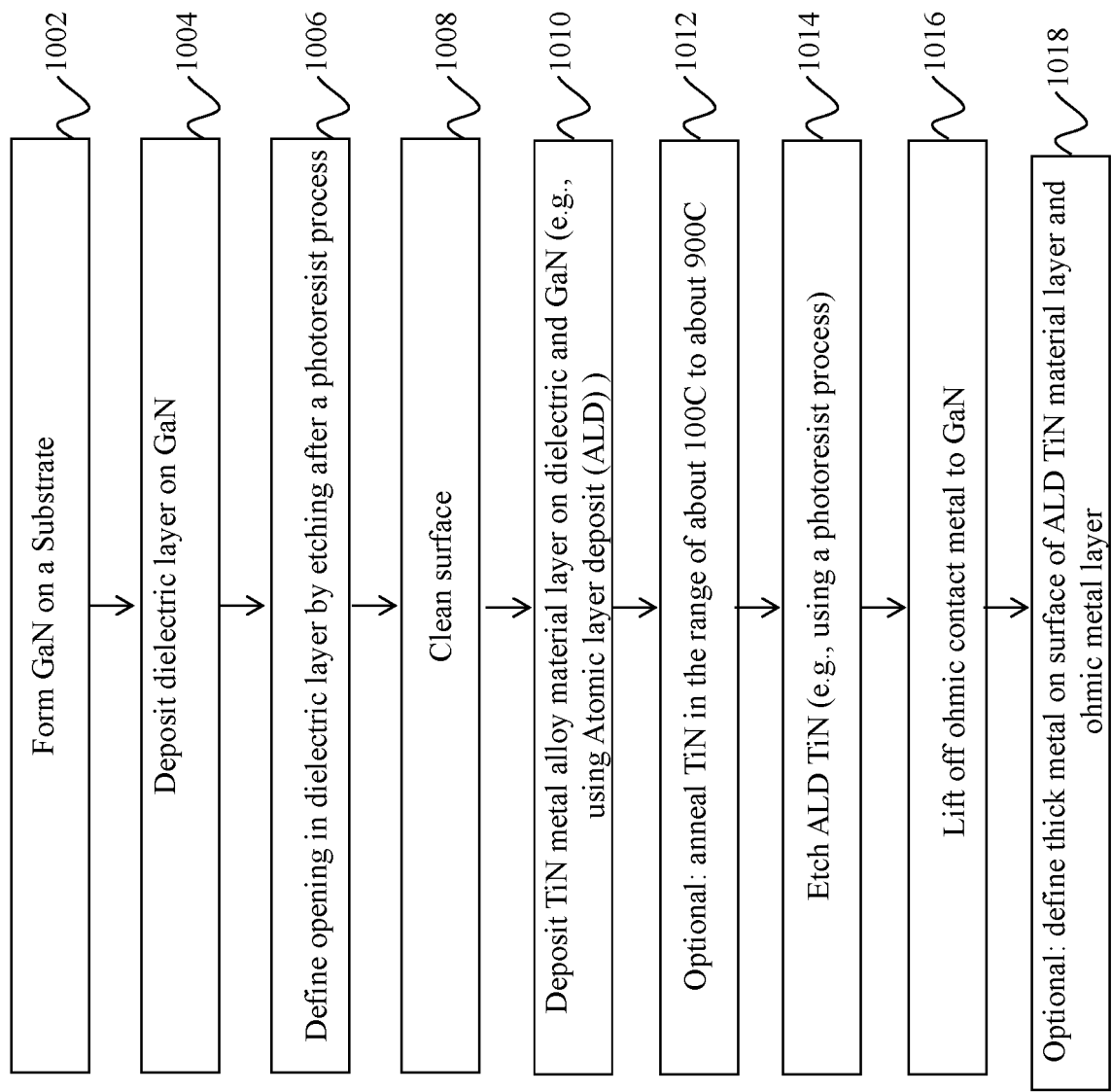


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/032927**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/47(2006.01)i, H01L 29/66(2006.01)i, H01L 29/872(2006.01)i, H01L 29/778(2006.01)i, H01L 29/49(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/47; H01L 29/778; H01L 27/095; H01L 29/72; H01L 23/48; H01L 29/20; H01L 29/417; H01L 29/812; H01L 29/66; H01L 29/872; H01L 29/49

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: schottky diode, low, migration, atom

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6262460 B1 (KALNITSKY et al.) 17 July 2001 See column 4, lines 19-25, claim 1 and figure 3.	1-16
A		17-20
X	US 2015-0102360 A1 (AVOGY, INC.) 16 April 2015 See paragraphs [0021]-[0035], [0055]-[0061], claim 1 and figures 1A-1B, 6-14.	17-19
Y		1-16, 20
Y	US 2015-0357457 A1 (RF MICRO DEVICES, INC.) 10 December 2015 See paragraphs [0017], [0025] and figure 1.	10-11, 20
A	US 2011-0227089 A1 (MIECZKOWSKI et al.) 22 September 2011 See claims 1-7 and figures 1-8.	1-20
A	US 5298784 A (GAMBINO et al.) 29 March 1994 See claims 1-8 and figures 1-4.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 July 2017 (27.07.2017)

Date of mailing of the international search report

27 July 2017 (27.07.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



Facsimile No. +82-42-481-8578

Authorized officer

KANG, Sung Chul

Telephone No. +82-42-481-8405



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/032927

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6262460 B1	17/07/2001	None	
US 2015-0102360 A1	16/04/2015	US 2014-070226 A1 US 8916871 B2	13/03/2014 23/12/2014
US 2015-0357457 A1	10/12/2015	US 9455327 B2	27/09/2016
US 2011-0227089 A1	22/09/2011	EP 2548229 A1 EP 2548229 A4 JP 2013-522906 A JP 5668133 B2 US 9142631 B2 WO 2011-115692 A1	23/01/2013 13/08/2014 13/06/2013 12/02/2015 22/09/2015 22/09/2011
US 05298784 A	29/03/1994	EP 0562996 A1 JP 06-029396 A	29/09/1993 04/02/1994