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(54) Title: SEMICONDUCTOR PACKAGING WITH INTERNAL WIRING BUS

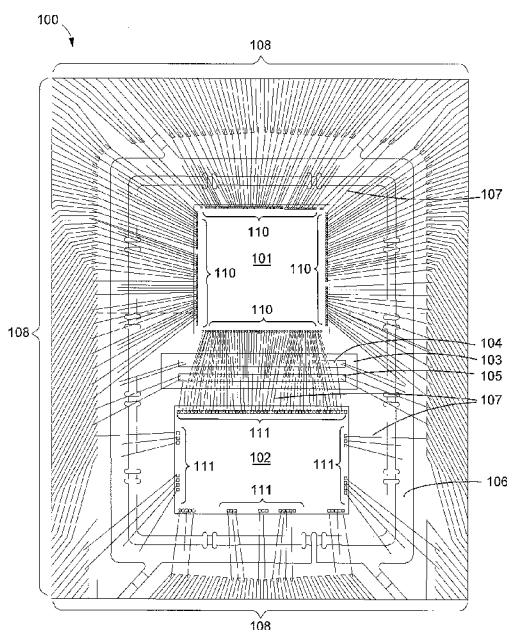


FIG. 1

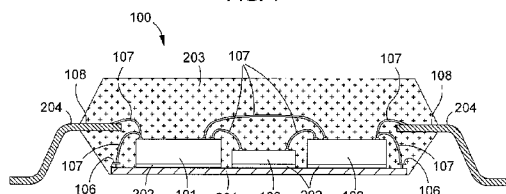


FIG. 2

(57) Abstract: A packaged semiconductor includes inner bond fingers, at least first and second semiconductor dies, and an interposer. The packaged semiconductor further includes wiring between the first and second semiconductor dies and the inner bond fingers, wiring between the interposer and the inner bond fingers, and wiring between the interposer and the first and second semiconductor dies. The wiring between the interposer and the first and second semiconductor dies thereby reduces the count of inner bond fingers needed for the wiring between the first and second semiconductor dies and the inner bond fingers. The interposer further provides indirect access to the inner bond fingers when the inner bond fingers are inaccessible by the first and second semiconductor dies.

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SEMICONDUCTOR PACKAGING WITH INTERNAL WIRING BUS

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Patent Application No. 60/912,802, filed April 19, 2007, the contents of which are hereby incorporated by reference as if fully stated herein.

Field

[0001] The present disclosure relates to a packaged semiconductor.

Background

[0002] To increase the functionality of packaged semiconductors, it is preferable to provide multiple semiconductor dies, each with different functionalities, in the same package. The different semiconductor dies are combined and connected together using gold wiring. Power is then provided to the semiconductor dies through external package pins. The external package pins are connected to inner bond fingers which are usually wire bonded to each of the semiconductor dies. However, it is sometimes difficult to provide power to each of the semiconductor dies. For example, access to the inner bond

fingers is limited due to physical limitations or interconnection process limitations, or there might not be any extra inner bond fingers available.

SUMMARY

[0003] The foregoing situation is addressed by including an interposer which provides the semiconductor dies with indirect access to inner bond fingers.

[0004] Thus, in one aspect, a packaged semiconductor includes inner bond fingers, at least first and second semiconductor dies, and an interposer. The packaged semiconductor further includes wiring between the first and second semiconductor dies and the inner bond fingers, wiring between the interposer and the inner bond fingers, and wiring between the interposer and the first and second semiconductor dies. The wiring between the interposer and the first and second semiconductor dies thereby reduces the count of inner bond fingers needed for the wiring between the first and second semiconductor dies and the inner bond fingers.

[0005] Since the interposer is internal and acts as a bridge between the first and second semiconductor dies and the inner bond fingers, the interposer further provides indirect access to the inner bond fingers when the inner bond fingers are inaccessible by the first and second semiconductor dies.

[0006] In one example embodiment, the interposer may be positioned between the first and second semiconductor dies. The inner bond fingers provide power, an electrical ground, and electrical signals to the first and second semiconductor dies through the wiring connection between the inner bond fingers and the first and second semiconductor dies. The inner bond fingers also provide power, an electrical ground, and electrical signals to the interposer through the wiring connection between the interposer and the inner bond fingers. The interposer, in turn, provides power, an electrical ground, and electrical signals to the first and second semiconductor dies, when the inner bond fingers

are inaccessible by the first and second semiconductor dies, through the wiring connection between the interposer and the first and second semiconductor dies. Thus, the first and second semiconductor dies have full access to power, an electrical ground, and electrical signals.

[0007] A more complete understanding can be obtained by reference to the following detailed description and to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a top view of a semiconductor package according to a first example embodiment of the invention.

[0009] Figure 2 is a cross-sectional view of a semiconductor package according to the first example embodiment of the invention.

[0010] Figure 3 is a top view of a semiconductor package according to a second example embodiment of the invention.

[0011] Figure 4 is a cross-sectional view of a semiconductor package according to the second example embodiment of the invention.

[0012] Figure 5A is a block diagram showing an embodiment of the invention in a hard disk drive (HDD).

[0013] Figure 5B is a block diagram of an embodiment of the invention in a digital versatile disc (DVD) drive.

[0014] Figure 5C is a block diagram of an embodiment of the invention in a high definition television (HDTV).

[0015] Figure 5D is a block diagram of an embodiment of the invention in a vehicle.

[0016] Figure 5E is a block diagram of an embodiment of the invention in a cellular or mobile phone.

[0017] Figure 5F is a block diagram of an embodiment of the invention in a set-top box.

[0018] Figure 5G is a block diagram of an embodiment of the invention in a media player.

[0019] Figure 5H is a block diagram of an embodiment of the invention in a Voice-over Internet Protocol (VoIP) player.

DETAILED DESCRIPTION

[0020] Figure 1 shows a top view of a semiconductor package 100 according to a first example embodiment of the invention. As shown in Figure 1, the semiconductor package 100 includes semiconductor dies 101 and 102, an interposer 103, an electrical ground 106, wiring 107, and inner bond fingers 108. The interposer 103 is shown to include a ground connection 104 and a power connection 105. Semiconductor dies 101 and 102 are shown to include connectors 110 and 111, respectively.

[0021] Figure 1 further shows semiconductor dies 101 and 102 connected, via connectors 110 and 111, to inner bond fingers 108, which are also called bonding fingers. The connection between semiconductor dies 101 and 102 and inner bond fingers 108 is made with wiring 107 using a wire bonding method. The wiring 107 can be, for example, gold, aluminum, or copper wiring and the wire bonding method can include either ball bonding or wedge bonding. The connection of semiconductor dies 101 and 102 to inner bond fingers 108 provides semiconductor dies 101 and 102 with power, ground, and/or signals. Furthermore, semiconductor dies 101 and 102 are also connected to the electrical ground 106 with wiring 107 using a wire bonding method. The electrical ground 106 is ring-shaped and surrounds semiconductor dies 101 and 102 to provide an additional source for ample grounding connections.

[0022] As shown in Figure 1, semiconductor dies 101 and 102 are positioned side-by-side, so that semiconductor die 101 and semiconductor die 102 can be interconnected with wiring 107 using a wire bonding method. However, neither of semiconductor dies 101 and 102 have access to inner bond fingers 108 nor the electrical ground 106 on the side of each of semiconductor dies 101 and 102 that faces the opposing semiconductor die, because each of semiconductor dies 101 and 102 physically blocks the opposing semiconductor die from accessing the inner bond fingers 108 or the electrical ground 106. Since connectors 110 and 111 on one side of both semiconductor dies 101 and 102, respectively, are blocked from accessing both inner bond fingers 108 and the electrical ground 106, semiconductor dies 101 and 102 do not have full access to power, ground, and/or signals. Furthermore, because both semiconductor dies 101 and 102 may need access to inner bond fingers 108 on all sides of each semiconductor dies 101 and 102, there are not enough inner bond fingers 108 to connect to each semiconductor die. Thus, the interposer 103 is included in the semiconductor package 100 to provide semiconductor dies 101 and 102 indirect access to inner bond fingers 108 and also to reduce the number of inner bond fingers 108 necessary for providing power.

[0023] As shown in Figure 1, the interposer 103 is positioned between semiconductor dies 101 and 102. Semiconductor dies 101 and 102 are connected to the power connection 105 and the electrical ground connection 104 of the interposer 103 with wiring 107 using a wire bonding method. The power connection 105 is connected to inner bond fingers 108 with wiring 107 and the electrical ground connection 104 is connected to the electrical ground 106 with wiring 107, both using a wire bonding method. Thus, the interposer 103 acts as a bridge for providing the semiconductor dies 101 and 102 power, an electrical ground, and/or signals, when the inner bond fingers 108 and the electrical ground 106 are inaccessible.

[0024] Since semiconductor dies 101 and 102 have full access to power, ground, and/or signals through the interposer 103, and the semiconductor dies 101 and 102 are interconnected, a packaged semiconductor is formed having different functionalities. The packaged semiconductor can be used by any electronic device, such as, for example, a

mobile phone, personal computer, or digital music player. Other embodiments are described below in connection with Figures 5A through 5H.

[0025] Semiconductor dies 101 and 102 can be formed from different wafer processing, or semiconductor dies 101 and 102 can be formed from the same wafer processing but perform different functionalities within the semiconductor package 100. For example, semiconductor dies 101 and 102 could be an application-specific integrated circuit (ASIC), flash memory, or a double data rate synchronous dynamic random access memory (DDR SDRAM). However, the semiconductor package 100 is not limited to include only these specific types of semiconductor dies; rather, the semiconductor package 100 may include other forms of semiconductor dies as required. In this embodiment, there are two semiconductor dies shown; however, in other embodiments the semiconductor package can include more than two semiconductor dies, as required to obtain a desired amount of multiple functionality for the semiconductor package.

[0026] In other embodiments, if more semiconductor dies are included, additional interposers can also be included as needed to provide access to power, ground, and/or signals to each semiconductor die. The interposer 103 can also have basic electrical functions, such as capacitance and inductance. Additionally, the interposer 103 can be a ball grid array (BGA) substrate material such as bismaleimide triazine (BT) with Cu traces/planes or Silicon dice with simple metallization.

[0027] Figure 2 will now be discussed to further illustrate the internal structure of the first example embodiment of the invention. Figure 2 shows a cross-sectional view of a semiconductor package according to the first example embodiment of the invention. As shown in Figure 2, semiconductor package 100 further includes a die pad 201, die attach material 202, mold compound 203, and external package pins 204.

[0028] As shown in Figure 2, semiconductor dies 101 and 102 are connected to inner bond fingers 108, connected to each other, and connected to the interposer 103 with wiring 107 through a wire bonding method. The inner bond fingers 108 are connected to external package pins 204 and receive power, electrical grounding, and/or signals from

the external package pins 204. As described above, the interposer 103 provides the semiconductor dies 101 and 102 power, an electrical ground, and/or signals, when the inner bond fingers 108 and the electrical ground 106 are inaccessible. Furthermore, semiconductor dies 101 and 102 are mounted to the die pad 201 using the die attach material 202. The die pad 201 can either be exposed on the bottom surface of the semiconductor package 100 as shown in Figure 2, or the die pad 201 can be exposed inside the mold compound 203. The die pad 201 is exposed for thermal regulation. Moreover, the electrical ground 106 is raised above the die pad 201 to provide easier access for wire bonding.

[0029] Figure 3 will now be discussed to illustrate a second and more complex example embodiment of the invention. Figure 3 shows a top view of a semiconductor package 300 according to this second example embodiment of the invention. As seen in Figure 3, the semiconductor package 300 includes semiconductor dies 301, 302, 303, and 304, an interposer 305, an electrical ground 306, a die pad 307, inner bond fingers 312, and wiring 313. The interposer 305 includes power connections 308 and 310 and ground connections 309 and 311. Semiconductor die 301 includes connectors 316, semiconductor die 302 includes connectors 314, and semiconductor dies 303 and 304 include connectors 315.

[0030] Semiconductor dies 301, 302, 303, and 304 can be formed from different wafer processing, or can be formed from the same wafer processing but perform different functionalities within the semiconductor package 300. For example, in Figure 3, semiconductor die 301 could be an ASIC, semiconductor die 302 could be a flash memory, and semiconductor dies 303 and 304 could both be DDR SDRAM. However, the semiconductor package 300 is not limited to include only these specific types of semiconductor dies; rather, the semiconductor package 300 may include other forms of semiconductor dies as required. In this embodiment, there are four semiconductor dies shown; however, in other embodiments the semiconductor package can include two semiconductor dies or more, as needed to provide the multiple functionalities as intended for the semiconductor package.

[0031] As shown in Figure 3, semiconductor die 301 is connected via connectors 316 to inner bond fingers 312 and the electrical ground 306 by wire bonding using wiring 313. The inner bond fingers 312 provide power, ground, and/or signals and the electrical ground 306 provides an additional source for an electrical ground. The electrical ground 306 is ring-shaped and surrounds semiconductor dies 301, 302, 303, and 304 so as to provide ample grounding connections. However, none of semiconductor dies 301, 302, 303, and 304 have access to inner bond fingers 312 nor the electrical ground 306 on the side of each of semiconductor dies 301 to 304 that face the opposing semiconductor dies, because each of semiconductor dies 301 to 304 physically blocks the opposing semiconductor dies from accessing the inner bond fingers 312 and the electrical ground 306. Since connectors 314 of semiconductor die 302, connectors 315 of semiconductor dies 303 and 304, and connectors 316 of semiconductor die 301 are blocked from accessing both inner bond fingers 312 and the electrical ground 306 on one side of each of the semiconductor dies 301 to 304, semiconductor dies 301 to 304 do not have full access to power, ground, and/or signals. In order for semiconductor dies 301 to 304 to have full access to power and an electrical ground, the interposer 305 acts as a bridge and is implemented as described below.

[0032] In this embodiment, the interposer 305 connects to the inner bond fingers 312 through a wire bonding connection between the power connections 310 and the inner bond fingers 312. The interposer 305 also connects to the electrical ground 306 through a wire bonding connection between the ground connections 311 and the electrical ground 306. The power connections 310 and the ground connections 311 are routed inside the interposer 305 to a power connection 308 and a ground connection 309, respectively. Semiconductor dies 301 and 303 are connected via connectors 316 and 315, respectively, to the interposer 305 through a wire bonding connection to power connection 308 and ground connection 309. Moreover, semiconductor die 302 is connected to semiconductor die 301 by wire bonding connectors 314 and 316 and semiconductor die 304 is connected to semiconductor die 303 by wire bonding connectors 315. Thus, through the interposer 305, semiconductor dies 301 to 304 have full access to power, as provided by the inner bond fingers 312, and full access to an electrical ground, as provided by the electrical

ground 306. [0033] Semiconductor die 301 is also connected to semiconductor die 303 by wire bonding so that all of semiconductor dies 301 to 304 are interconnected. The interposer 305 can also provide semiconductor dies 301 to 304 indirect access to electrical signals as provided by the inner bond fingers 312. The above-described connections provide a fully integrated packaged semiconductor, in which each semiconductor die is provided power, an electrical ground, and/or signals.

[0034] The embodiment as shown in Figure 3 only includes one interposer 305. However, additional interposers can be included as needed to provide access to power and ground for each semiconductor die. The interposer 305 can also have basic electrical functions, such as capacitance and inductance. Additionally, the interposer 305 can be a BGA substrate material such as BT with Cu traces/planes or Silicon die with simple metallization.

[0035] Figure 4 will now be discussed to more clearly illustrate the internal structure and interconnections of the second example embodiment of the invention. Figure 4 shows a simplified cross-sectional view of semiconductor package 300 according to the second example embodiment of the invention.

[0036] As shown in Figure 4, the semiconductor package includes semiconductor dies 301, 302, 303, and 304, an interposer 305, a die pad 307, inner bond fingers 312, wiring 313, a mold compound 401, a die attach material 402, and external package pins 403. In this embodiment, semiconductor die 302 is stacked on top of semiconductor die 301, semiconductor die 303 is stacked on top of the interposer 305, and semiconductor die 304 is stacked on top of semiconductor die 303. However, in other embodiments, the semiconductor dies can be positioned side-by-side and additional semiconductor dies can be stacked on top of each other as needed.

[0037] Semiconductor dies 301, 302, 303 and 304 are wire bonded to the inner bond fingers 312 using wiring 313. The inner bond fingers 312 are connected to external package pins 403 and receive power, electrical grounding, and/or signals from the external package pins 403. Semiconductor die 302 is wire bonded to semiconductor die

301 using wiring 313. Alternatively, semiconductor die 302 can be connected to semiconductor die 301 through the process of flip chip, which is also called Controlled Collapse Chip Connection (C4). Furthermore, semiconductor die 303 is interconnected by wire bonding with semiconductor die 301 using wiring 313. Also, both semiconductors 301 and 303 are wire bonded to the interposer 305 using wiring 313. As described above, the interposer 305 provides the semiconductor dies 301 and 303 power, an electrical ground, and/or signals, when the inner bond fingers 312 are inaccessible. Moreover, semiconductor die 304 is wire bonded to semiconductor die 303 using wiring 313. Alternatively, semiconductor die 304 can be connected to semiconductor die 303 through the process of flip chip. The interconnections between the semiconductor dies 301 to 304 and the connections to the inner bond fingers 312 provide a packaged semiconductor with multiple functionalities. In other embodiments, wire bonding can also be between the semiconductor package inner leads, E-pads, and bonding rings.

[0038] In this embodiment, the interposer 305 and semiconductor die 301 are mounted to the die pad 307 using the die attach material 402. The die pad 307 can either be exposed on the bottom surface of the semiconductor package or be exposed inside the mold compound 401 to provide thermal regulation for the semiconductor dies. Moreover, the electrical ground 306 is raised above the die pad 307 to provide easier access for wire bonding.

[0039] Generally, in all embodiments, the semiconductor package can be either a leadframe based package, such as, for example, a low-profile quad flat pack (LQFP), thin quad flat pack (TQFP), quad flat package no leads (QFN), or thin small-outline package (TSOP) or a substrate based package, such as, for example plastic ball grid array (PBGA), thin and fine-pitch ball grid array (TFBGA), or land grid array (LGA).

[0040] Referring now to Figures 5A-5H, various exemplary implementations of the present invention are shown. Referring to Figure 5A, the present invention may be embodied as a packaged semiconductor in a hard disk drive (HDD) 1500. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 5A at 1502. In some implementations, signal

processing and/or control circuit 1502 and/or other circuits (not shown) in HDD 1500 may process data, perform coding and/or encryption, perform calculations, and/or format data that is output to and/or received from a magnetic storage medium 1506.

[0041] HDD 1500 may communicate with a host device (not shown) such as a computer, mobile computing devices such as personal digital assistants, cellular phones, media or MP3 players and the like, and/or other devices via one or more wired or wireless communication links 1508. HDD 1500 may be connected to memory 1509, such as random access memory (RAM), a low latency nonvolatile memory such as flash memory, read only memory (ROM) and/or other suitable electronic data storage.

[0042] Referring now to Figure 5B, the present invention may be embodied as a packaged semiconductor in a digital versatile disc (DVD) drive 1510. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 5B at 1512, and/or mass data storage 1518 of DVD drive 1510. Signal processing and/or control circuit 1512 and/or other circuits (not shown) in DVD drive 1510 may process data, perform coding and/or encryption, perform calculations, and/or format data that is read from and/or data written to an optical storage medium 1516. In some implementations, signal processing and/or control circuit 1512 and/or other circuits (not shown) in DVD drive 1510 can also perform other functions such as encoding and/or decoding and/or any other signal processing functions associated with a DVD drive.

[0043] DVD drive 1510 may communicate with an output device (not shown) such as a computer, television or other device via one or more wired or wireless communication links 1517. DVD drive 1510 may communicate with mass data storage 1518 that stores data in a nonvolatile manner. Mass data storage 1518 may include a hard disk drive (HDD) such as that shown in Figure 5A. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". DVD drive 1510 may be connected to memory 1519, such as RAM, ROM, low latency nonvolatile memory such as flash memory, and/or other suitable electronic data storage.

[0044] Referring now to Figure 5C, the present invention may be embodied as a packaged semiconductor in a high definition television (HDTV) 1520. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 5C at 1522, a WLAN interface and/or mass data storage of the HDTV 1520. HDTV 1520 receives HDTV input signals in either a wired or wireless format and generates HDTV output signals for a display 1526. In some implementations, signal processing circuit and/or control circuit 1522 and/or other circuits (not shown) of HDTV 1520 may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other type of HDTV processing that may be required.

[0045] HDTV 1520 may communicate with mass data storage 1527 that stores data in a nonvolatile manner such as optical and/or magnetic storage devices, for example, hard disk drives and/or DVD drives. At least one HDD may have the configuration shown in Figure 5A and/or at least one DVD drive may have the configuration shown in Figure 5B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". HDTV 1520 may be connected to memory 1528 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. HDTV 1520 also may support connections with a WLAN via a WLAN interface 1529.

[0046] Referring now to Figure 5D, the present invention may be embodied as a packaged semiconductor in a control system of a vehicle 1530, a WLAN interface and/or mass data storage of the vehicle control system. In some implementations, the present invention implements a powertrain control system 1532 that receives inputs from one or more sensors 1536 such as temperature sensors, pressure sensors, rotational sensors, airflow sensors and/or any other suitable sensors and/or that generates one or more output control signals 1538 such as engine operating parameters, transmission operating parameters, braking parameters, and/or other control signals.

[0047] The present invention may also be embodied in other control systems 1540 of vehicle 1530. Control system 1540 may likewise receive signals from input sensors 1542

and/or output control signals to one or more output devices 1544. In some implementations, control system 1540 may be part of an anti-lock braking system (ABS), a navigation system, a telematics system, a vehicle telematics system, a lane departure system, an adaptive cruise control system, a vehicle entertainment system such as a stereo, DVD, compact disc and the like. Still other implementations are contemplated.

[0048] Powertrain control system 1532 may communicate with mass data storage 1546 that stores data in a nonvolatile manner. Mass data storage 1546 may include optical and/or magnetic storage devices, for example, hard disk drives and/or DVD drives. At least one HDD may have the configuration shown in Figure 5A and/or at least one DVD drive may have the configuration shown in Figure 5B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". Powertrain control system 1532 may be connected to memory 1547 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Powertrain control system 1532 also may support connections with a WLAN via a WLAN interface 1548. The control system 1540 may also include mass data storage, memory and/or a WLAN interface (all not shown).

[0049] Referring now to Figure 5E, the present invention may be embodied as a packaged semiconductor in a cellular phone 1550 that may include a cellular antenna 1551. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 5E at 1552, a WLAN interface and/or mass data storage of the cellular phone 1550. In some implementations, cellular phone 1550 includes a microphone 1556, an audio output 1558 such as a speaker and/or audio output jack, a display 1560 and/or an input device 1562 such as a keypad, pointing device, voice actuation and/or other input device. Signal processing and/or control circuits 1552 and/or other circuits (not shown) in cellular phone 1550 may process data, perform coding and/or encryption, perform calculations, format data and/or perform other cellular phone functions.

[0050] Cellular phone 1550 may communicate with mass data storage 1564 that stores data in a nonvolatile manner such as optical and/or magnetic storage devices, for

example, hard disk drives and/or DVD drives. At least one HDD may have the configuration shown in Figure 5A and/or at least one DVD drive may have the configuration shown in Figure 5B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". Cellular phone 1550 may be connected to memory 1566 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Cellular phone 1550 also may support connections with a WLAN via a WLAN interface 1568.

[0051] Referring now to Figure 5F, the present invention may be embodied as a packaged semiconductor in a set top box 1580. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 5F at 1584, a WLAN interface and/or mass data storage of the set top box 1580. Set top box 1580 receives signals from a source such as a broadband source and outputs standard and/or high definition audio/video signals suitable for a display 1588 such as a television and/or monitor and/or other video and/or audio output devices. Signal processing and/or control circuits 1584 and/or other circuits (not shown) of the set top box 1580 may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other set top box function.

[0052] Set top box 1580 may communicate with mass data storage 1590 that stores data in a nonvolatile manner. Mass data storage 1590 may include optical and/or magnetic storage devices, for example, hard disk drives and/or DVD drives. At least one HDD may have the configuration shown in Figure 5A and/or at least one DVD drive may have the configuration shown in Figure 5B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". Set top box 1580 may be connected to memory 1594 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Set top box 1580 also may support connections with a WLAN via a WLAN interface 1596.

[0053] Referring now to Figure 5G, the present invention may be embodied as a packaged semiconductor in a media player 1600. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in

Figure 5G at 1604, a WLAN interface and/or mass data storage of the media player 1600. In some implementations, media player 1600 includes a display 1607 and/or a user input 1608 such as a keypad, touchpad and the like. In some implementations, media player 1600 may employ a graphical user interface (GUI) that typically employs menus, drop down menus, icons and/or a point-and-click interface via display 1607 and/or user input 1608. Media player 1600 further includes an audio output 1609 such as a speaker and/or audio output jack. Signal processing and/or control circuits 1604 and/or other circuits (not shown) of media player 1600 may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other media player function.

[0054] Media player 1600 may communicate with mass data storage 1610 that stores data such as compressed audio and/or video content in a nonvolatile manner. In some implementations, the compressed audio files include files that are compliant with MP3 format or other suitable compressed audio and/or video formats. The mass data storage may include optical and/or magnetic storage devices, for example, hard disk drives and/or DVD drives. At least one HDD may have the configuration shown in Figure 5A and/or at least one DVD drive may have the configuration shown in Figure 5B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". Media player 1600 may be connected to memory 1614 such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. Media player 1600 also may support connections with a WLAN via a WLAN interface 1616. Still other implementations in addition to those described above are contemplated.

[0055] Referring to Figure 5H, the present invention may be embodied as a packaged semiconductor in a Voice over Internet Protocol (VoIP) player 1620 that may include an antenna 1621. The present invention may implement either or both signal processing and/or control circuits, which are generally identified in Figure 5H at 1622, a wireless interface and/or mass data storage of the VoIP player 1620. In some implementations, VoIP player 1620 includes, in part, a microphone 1624, an audio output 1625 such as a speaker and/or audio output jack, a display monitor 1626, an input device 1627 such as a

keypad, pointing device, voice actuation and/or other input devices, and a Wireless Fidelity (Wi-Fi) communication module 1628. Signal processing and/or control circuits 1622 and/or other circuits (not shown) in VoIP player 1620 may process data, perform coding and/or encryption, perform calculations, format data and/or perform other VoIP player functions.

[0056] VoIP player 1620 may communicate with mass data storage 1623 that stores data in a nonvolatile manner such as optical and/or magnetic storage devices, for example hard disk drives and/or DVD drives. At least one HDD may have the configuration shown in Figure 5A and/or at least one DVD drive may have the configuration shown in Figure 5B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". VoIP player 1620 may be connected to memory 1629, which may be a RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. VoIP player 1620 is configured to establish communications link with a VoIP network (not shown) via Wi-Fi communication module 1628.

[0057] The invention has been described above with respect to particular illustrative embodiments. It is understood that the invention is not limited to the above-described embodiments and that various changes and modifications may be made without departing from the scope of the invention.

WHAT IS CLAIMED IS:

1. A packaged semiconductor, comprising:
inner bond fingers;
at least first and second semiconductor dies;
an interposer;
wiring between said first and second semiconductor dies and said inner bond fingers;
wiring between said interposer and said inner bond fingers; and
wiring between said interposer and said first and second semiconductor dies.
2. A packaged semiconductor according to Claim 1, wherein said first and second semiconductor dies are positioned opposite each other such that said first semiconductor die prevents said second semiconductor die from having full direct access to said inner bond fingers and said second semiconductor die prevents said first semiconductor die from having full direct access to said inner bond fingers, and wherein wiring between said interposer and said first and second semiconductor dies provides indirect access to said inner bond fingers.
3. A packaged semiconductor according to Claim 1, wherein said first and second semiconductor dies are stacked on top of each other.
4. A packaged semiconductor according to Claim 1, wherein said first and second semiconductor dies are positioned side-by-side.
5. A packaged semiconductor according to Claim 1, wherein said interposer is stacked on top of either said first or second semiconductor dies.

6. A packaged semiconductor according to Claim 1, wherein said first or second semiconductor die is stacked on top of said interposer.

7. A packaged semiconductor according to Claim 1, wherein said interposer is positioned side-by-side of said first and second semiconductor dies.

8. A packaged semiconductor according to Claim 1, wherein said interposer is positioned between said first and second semiconductor dies.

9. A packaged semiconductor according to Claim 1, wherein said interposer functions as a capacitor or an inductor.

10. A packaged semiconductor according to Claim 1, comprising:
a plurality of interposers; and
a plurality of semiconductor dies,
wherein each of the plurality of interposers is positioned side-by-side with each of the other plurality of interposers, and
wherein each of the plurality of semiconductor dies is stacked on top of each of the plurality of interposers.

11. A packaged semiconductor according to Claim 10, wherein each of said plurality of interposers is positioned between each of said plurality of semiconductor dies.

12. A packaged semiconductor according to Claim 1, wherein said interposer is either a BGA substrate material or Silicon die with simple metallization.

13. A packaged semiconductor according to Claim 1, further comprising a die pad, wherein said first and second semiconductor dies and said interposer are connected to said die pad.

14. A packaged semiconductor according to Claim 13, wherein said die pad is exposed for providing thermal regulation.

15. A packaged semiconductor according to Claim 1, wherein said interposer comprises:

a first set of ground and power connections; and

a second set of ground and power connections,

wherein said first set of ground and power connections are routed to said second set of ground and power connections,

wherein said inner bond fingers are wire bonded to said first set of ground and power connections, and

wherein said first and second semiconductor dies are wire bonded to said second set of ground and power connections.

16. A method for manufacturing a semiconductor package, comprising:
mounting an interposer on a surface of a die pad;
mounting first and second semiconductor dies on said surface of said die pad;

connecting inner bond fingers and said first and second semiconductor dies with wiring;

connecting said interposer and said inner bond fingers with wiring; and

connecting said interposer and said first and second semiconductor dies with wiring.

17. A method for manufacturing a semiconductor package according to Claim 16, wherein said first and second semiconductor dies are positioned opposite each

other such that said first semiconductor die prevents said second semiconductor die from having full direct access to said inner bond fingers and said second semiconductor die prevents said first semiconductor die from having full direct access to said inner bond fingers, and wherein wiring between said interposer and said first and second semiconductor dies provides indirect access to said inner bond fingers.

18. A method for manufacturing a semiconductor package according to Claim 16, wherein said first semiconductor die is mounted to said die pad and said second semiconductor die is mounted to said first semiconductor so that said first and second semiconductor dies are stacked on top of each other.

19. A method for manufacturing a semiconductor package according to Claim 16, wherein said first and second semiconductor die are mounted to said die pad side-by-side.

20. A method for manufacturing a semiconductor package according to Claim 16, wherein said interposer is mounted to either said first or second semiconductor die so that said interposer is stacked on top of either said first or second semiconductor die.

21. A method for manufacturing a semiconductor package according to Claim 16, wherein said first or second semiconductor die is mounted to said interposer so that said first or second semiconductor die is stacked on top of said interposer.

22. A method for manufacturing a semiconductor package according to Claim 16, wherein said interposer is mounted to said die pad side-by-side with said first and second semiconductor dies.

23. A method for manufacturing a semiconductor package according to Claim 16, wherein said interposer is mounted to said die pad between said first and second semiconductor dies.

24. A method for manufacturing a semiconductor package according to Claim 16, further comprising:

mounting a plurality of interposers to said die pad; and

mounting each of a plurality of semiconductor dies to each of said plurality of interposers,

wherein said plurality of interposers are mounted to said die pad so that they are positioned side-by-side, and

wherein each of said plurality of semiconductor dies are mounted to each of said plurality of interposers so that said plurality of semiconductor dies are stacked on top of said plurality of interposers.

25. A method for manufacturing a semiconductor package according to Claim 24, wherein each of said plurality of interposers is positioned between each of said plurality of semiconductor dies.

26. A method for manufacturing a semiconductor package according to Claim 16, wherein said interposer is either a BGA substrate material or Silicon die with simple metallization.

27. A method for manufacturing a semiconductor package according to Claim 16, wherein said die pad is exposed for providing thermal regulation.

28. A method for manufacturing a semiconductor package according to Claim 16, further comprising:

connecting a first set of ground and power connections to said interposer;

connecting a second set of ground and power connections to said interposer;

routing said first set of ground and power connections to said second set of ground and power connections;

bonding said inner bond fingers to said first set of ground and power connections; and

bonding said first and second semiconductor dies to said second set of ground and power connections.

AMENDED CLAIMS**received by the International Bureau on 3 October 2008 (03.10.2008)**WHAT IS CLAIMED IS:

1. A packaged semiconductor, comprising:
inner bond fingers;
at least first and second semiconductor dies;
an interposer;
wiring between said first and second semiconductor dies and said inner
bond fingers;
wiring between said interposer and said inner bond fingers; and
wiring between said interposer and said first and second semiconductor
dies,
wherein said interposer comprises:
a first set of ground and power connections; and
a second set of ground and power connections,
wherein said first set of ground and power connections are routed
to said second set of ground and power connections,
wherein said inner bond fingers are wire bonded to said first set of
ground and power connections, and
wherein said first and second semiconductor dies are wire bonded
to said second set of ground and power connections.
2. A packaged semiconductor according to Claim 1, wherein said first and
second semiconductor dies are positioned opposite each other such that said first
semiconductor die prevents said second semiconductor die from having full direct access
to said inner bond fingers and said second semiconductor die prevents said first
semiconductor die from having full direct access to said inner bond fingers, and wherein
wiring between said interposer and said first and second semiconductor dies provides
indirect access to said inner bond fingers.

3. A packaged semiconductor according to Claim 1, wherein said first and second semiconductor dies are stacked on top of each other.

4. A packaged semiconductor according to Claim 1, wherein said first and second semiconductor dies are positioned side-by-side.

5. A packaged semiconductor according to Claim 1, wherein said interposer is stacked on top of either said first or second semiconductor dies.

6. A packaged semiconductor according to Claim 1, wherein said first or second semiconductor die is stacked on top of said interposer.

7. A packaged semiconductor according to Claim 1, wherein said interposer is positioned side-by-side of said first and second semiconductor dies.

8. A packaged semiconductor according to Claim 1, wherein said interposer is positioned between said first and second semiconductor dies.

9. A packaged semiconductor according to Claim 1, wherein said interposer functions as a capacitor or an inductor.

10. A packaged semiconductor according to Claim 1, comprising:
a plurality of interposers; and
a plurality of semiconductor dies,
wherein each of the plurality of interposers is positioned side-by-side with each of the other plurality of interposers, and
wherein each of the plurality of semiconductor dies is stacked on top of each of the plurality of interposers.

11. A packaged semiconductor according to Claim 10, wherein each of said plurality of interposers is positioned between each of said plurality of semiconductor dies.

12. A packaged semiconductor according to Claim 1, wherein said interposer is either a BGA substrate material or Silicon die with simple metallization.

13. A packaged semiconductor according to Claim 1, further comprising a die pad, wherein said first and second semiconductor dies and said interposer are connected to said die pad.

14. A packaged semiconductor according to Claim 13, wherein said die pad is exposed for providing thermal regulation.

16. A method for manufacturing a semiconductor package, comprising:
mounting an interposer on a surface of a die pad;
mounting first and second semiconductor dies on said surface of said die pad;

connecting inner bond fingers and said first and second semiconductor dies with wiring;

connecting said interposer and said inner bond fingers with wiring;
connecting said interposer and said first and second semiconductor dies with wiring;

connecting a first set of ground and power connections to said interposer;
connecting a second set of ground and power connections to said interposer;

routing said first set of ground and power connections to said second set of ground and power connections;

bonding said inner bond fingers to said first set of ground and power connections; and

bonding said first and second semiconductor dies to said second set of ground and power connections.

17. A method for manufacturing a semiconductor package according to Claim 16, wherein said first and second semiconductor dies are positioned opposite each other such that said first semiconductor die prevents said second semiconductor die from having full direct access to said inner bond fingers and said second semiconductor die prevents said first semiconductor die from having full direct access to said inner bond fingers, and wherein wiring between said interposer and said first and second semiconductor dies provides indirect access to said inner bond fingers.

18. A method for manufacturing a semiconductor package according to Claim 16, wherein said first semiconductor die is mounted to said die pad and said second semiconductor die is mounted to said first semiconductor so that said first and second semiconductor dies are stacked on top of each other.

19. A method for manufacturing a semiconductor package according to Claim 16, wherein said first and second semiconductor die are mounted to said die pad side-by-side.

20. A method for manufacturing a semiconductor package according to Claim 16, wherein said interposer is mounted to either said first or second semiconductor die so that said interposer is stacked on top of either said first or second semiconductor die.

21. A method for manufacturing a semiconductor package according to Claim 16, wherein said first or second semiconductor die is mounted to said interposer so that said first or second semiconductor die is stacked on top of said interposer.

22. A method for manufacturing a semiconductor package according to Claim 16, wherein said interposer is mounted to said die pad side-by-side with said first and second semiconductor dies.

23. A method for manufacturing a semiconductor package according to Claim 16, wherein said interposer is mounted to said die pad between said first and second semiconductor dies.

24. A method for manufacturing a semiconductor package according to Claim 16, further comprising:

mounting a plurality of interposers to said die pad; and

mounting each of a plurality of semiconductor dies to each of said plurality of interposers,

wherein said plurality of interposers are mounted to said die pad so that they are positioned side-by-side, and

wherein each of said plurality of semiconductor dies are mounted to each of said plurality of interposers so that said plurality of semiconductor dies are stacked on top of said plurality of interposers.

25. A method for manufacturing a semiconductor package according to Claim 24, wherein each of said plurality of interposers is positioned between each of said plurality of semiconductor dies.

26. A method for manufacturing a semiconductor package according to Claim 16, wherein said interposer is either a BGA substrate material or Silicon die with simple metallization.

27. A method for manufacturing a semiconductor package according to Claim 16, wherein said die pad is exposed for providing thermal regulation.

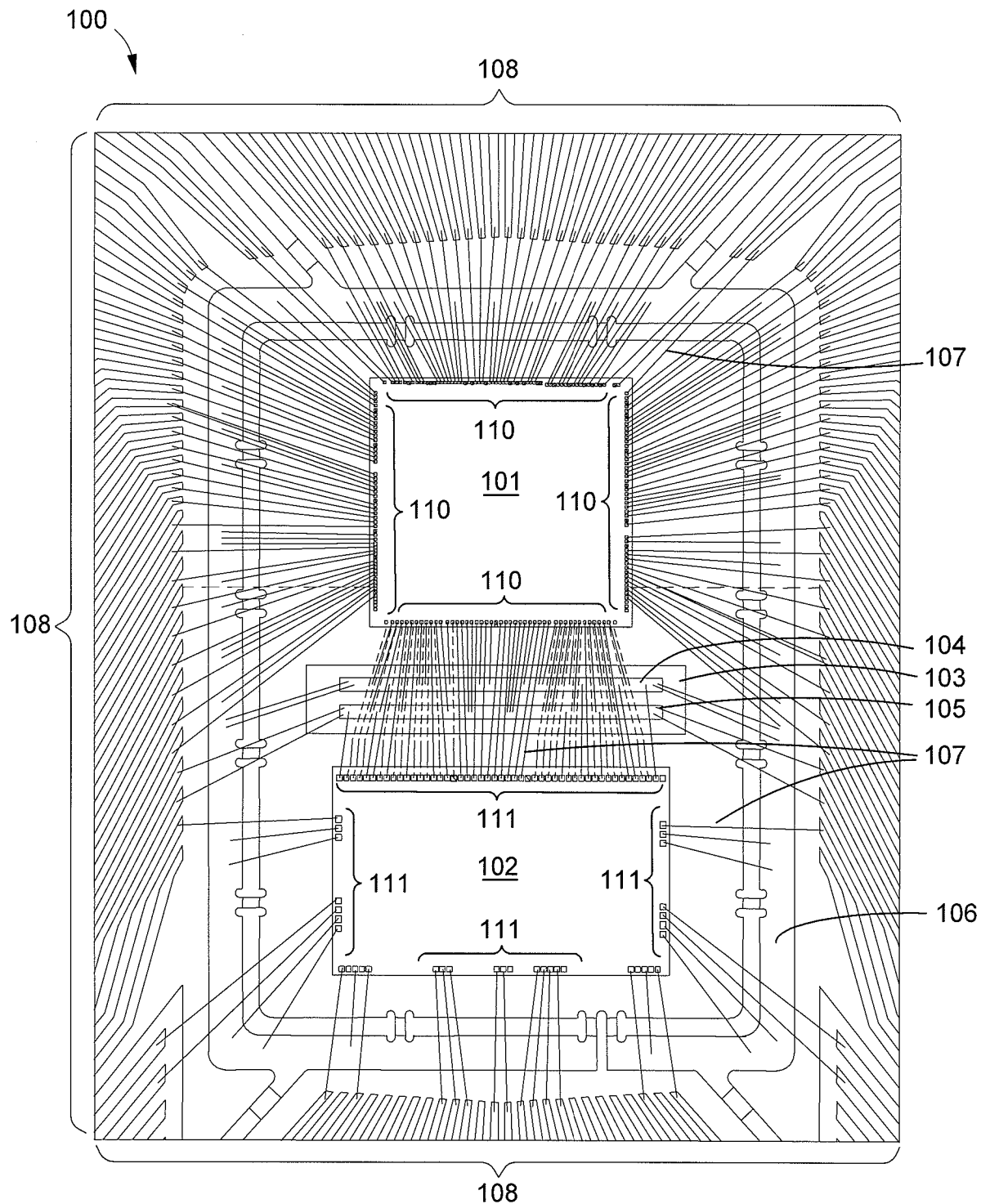


FIG. 1

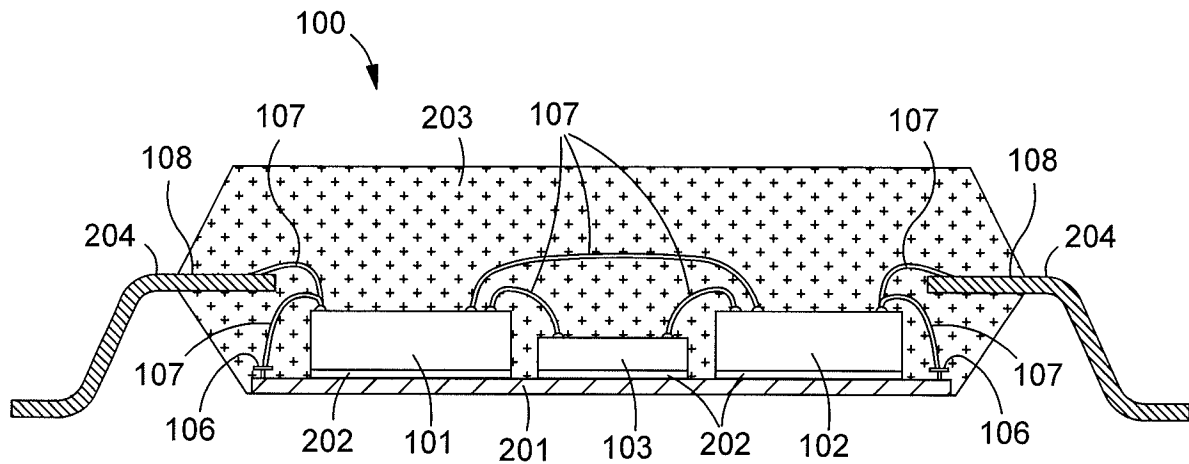


FIG. 2

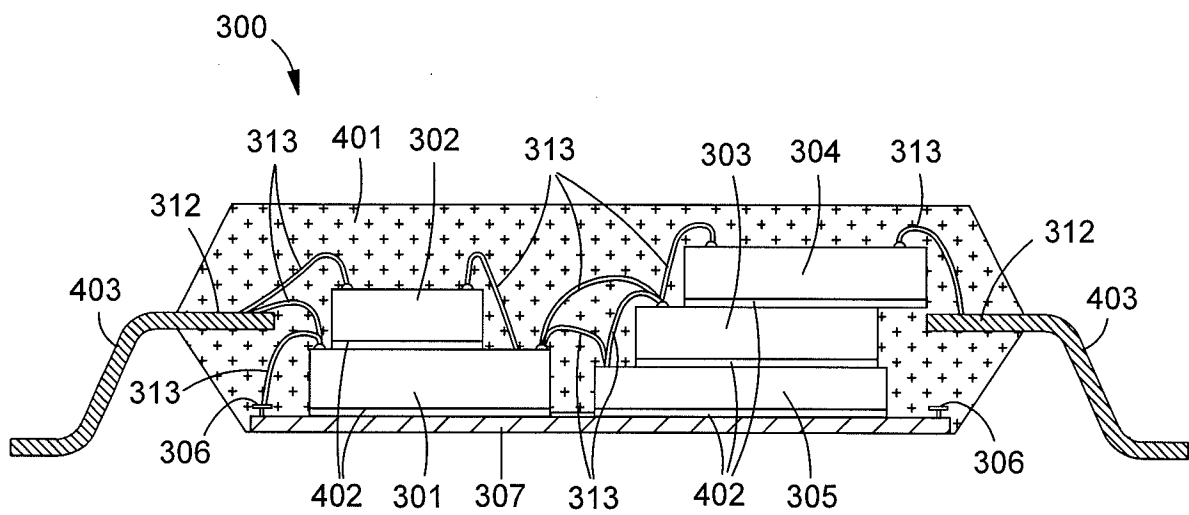


FIG. 4

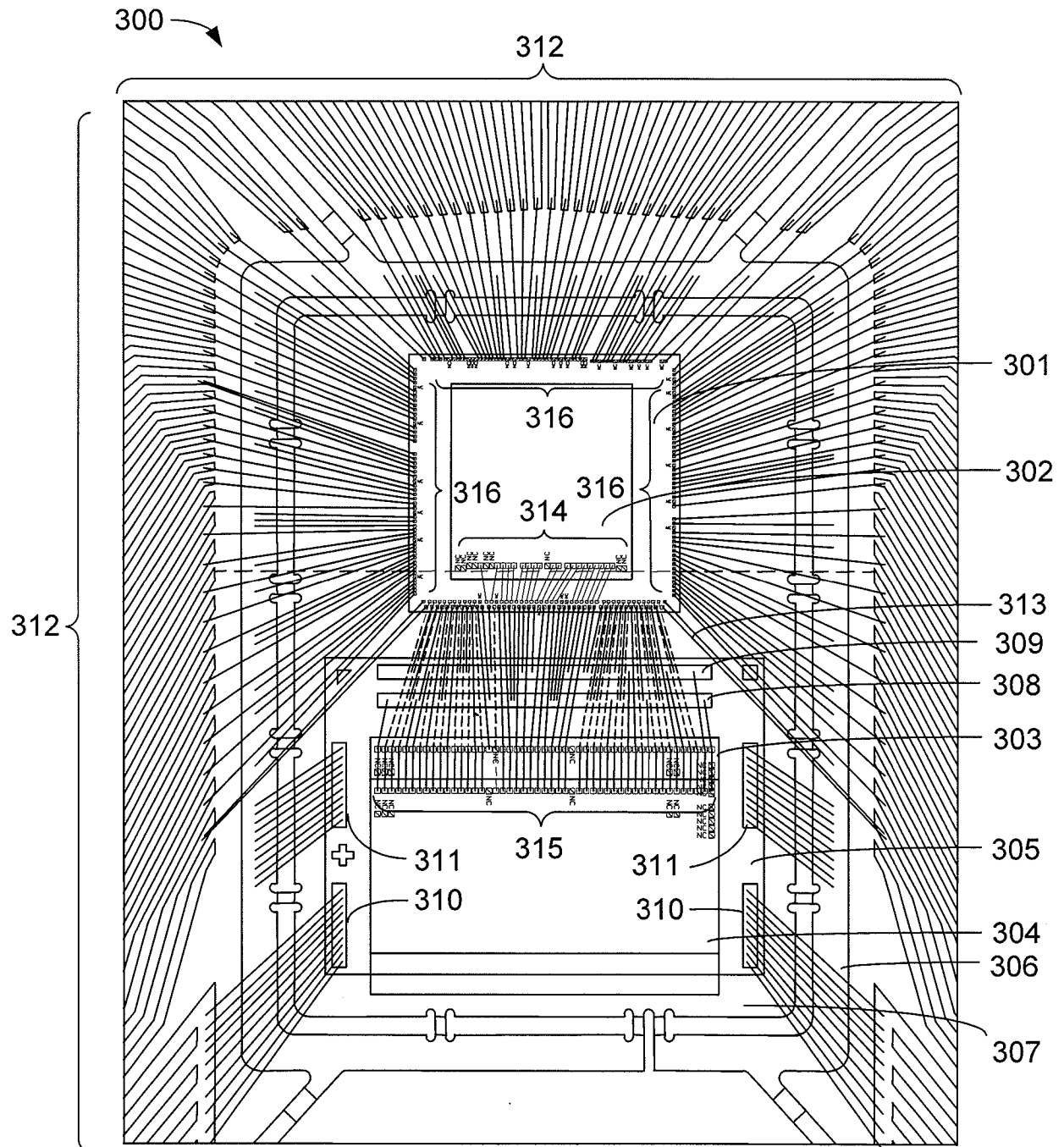


FIG. 3

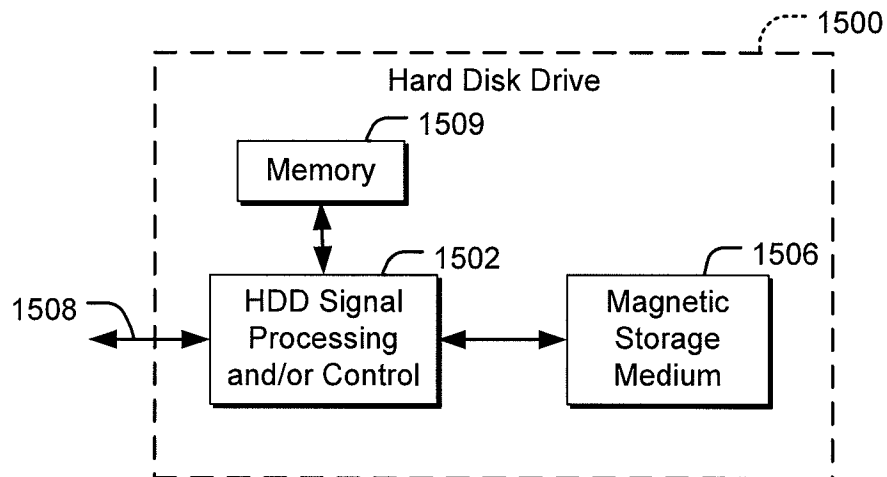


FIG. 5A

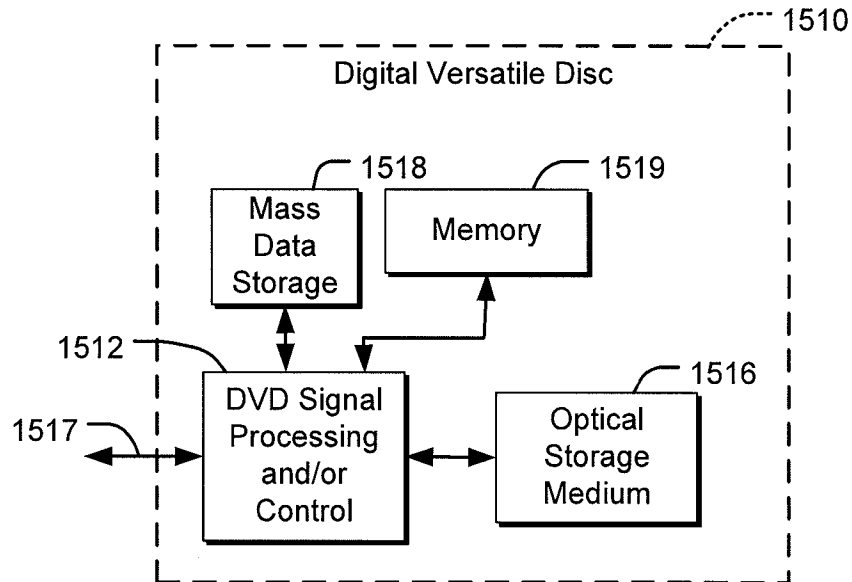


FIG. 5B

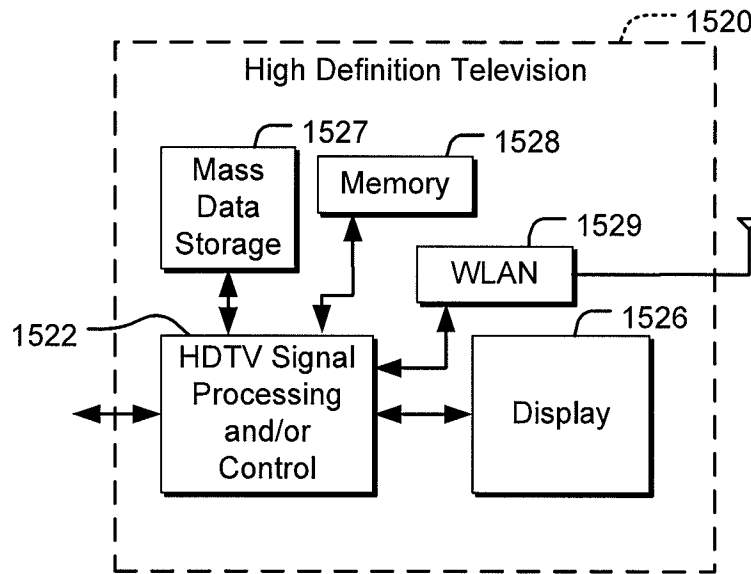


FIG. 5C

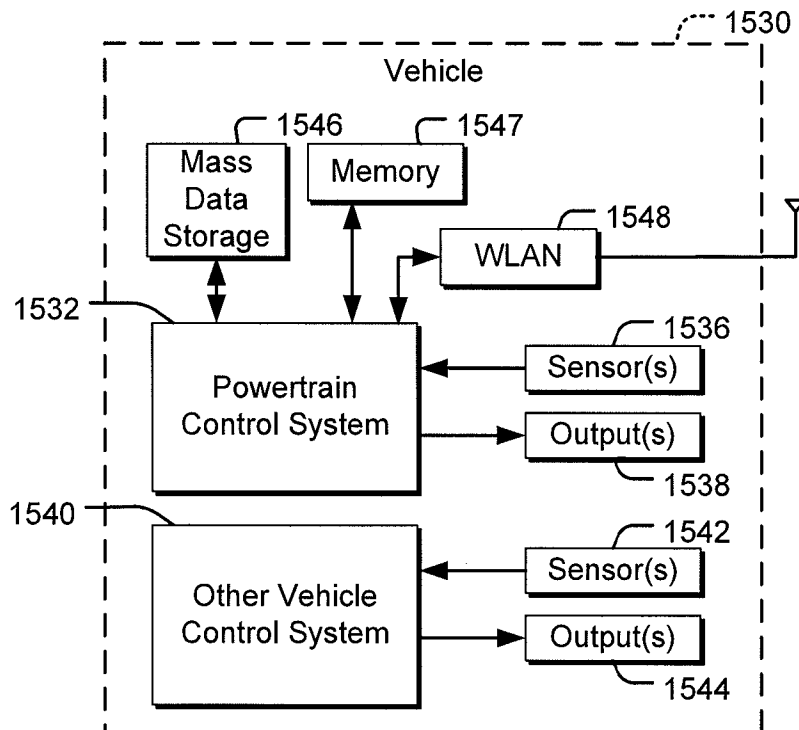


FIG. 5D

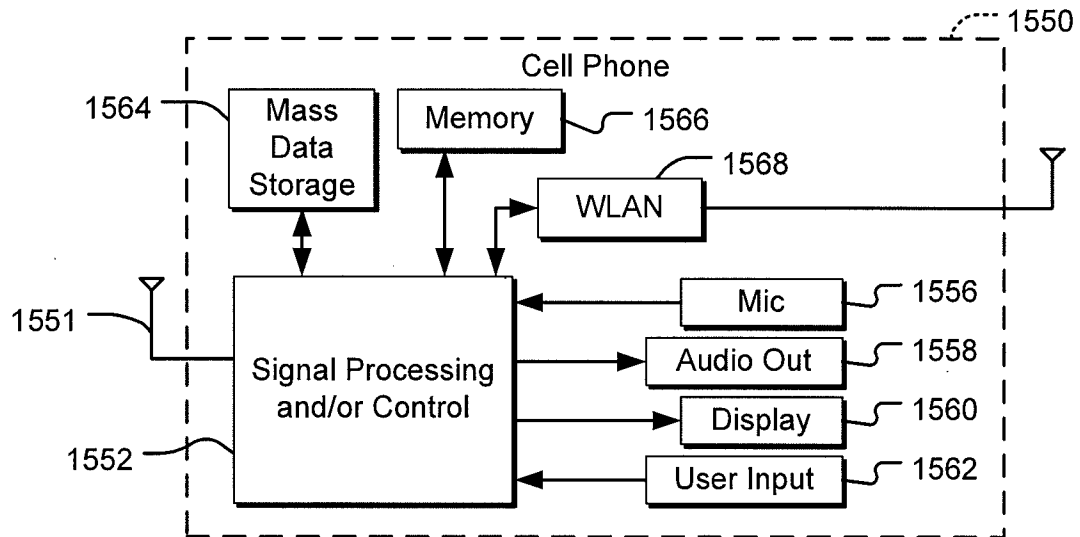


FIG. 5E

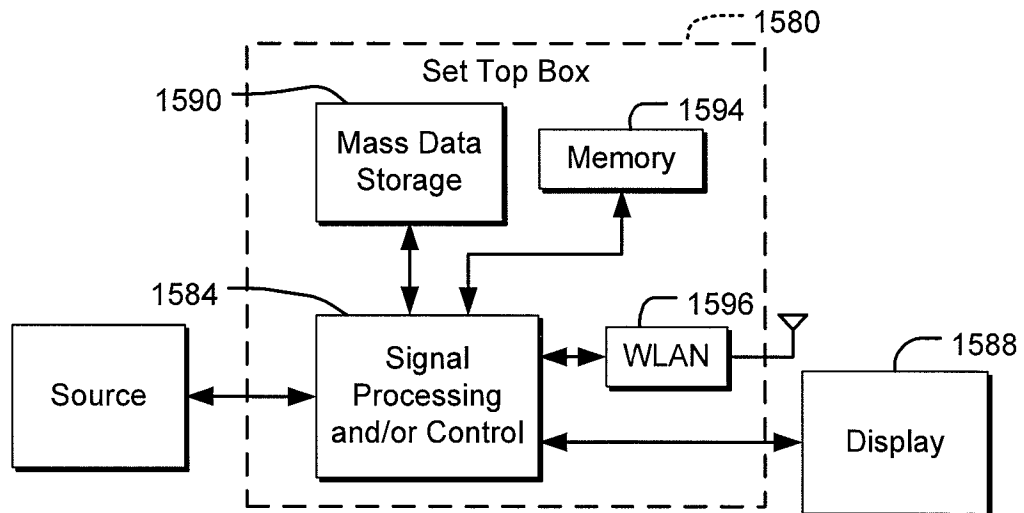


FIG. 5F

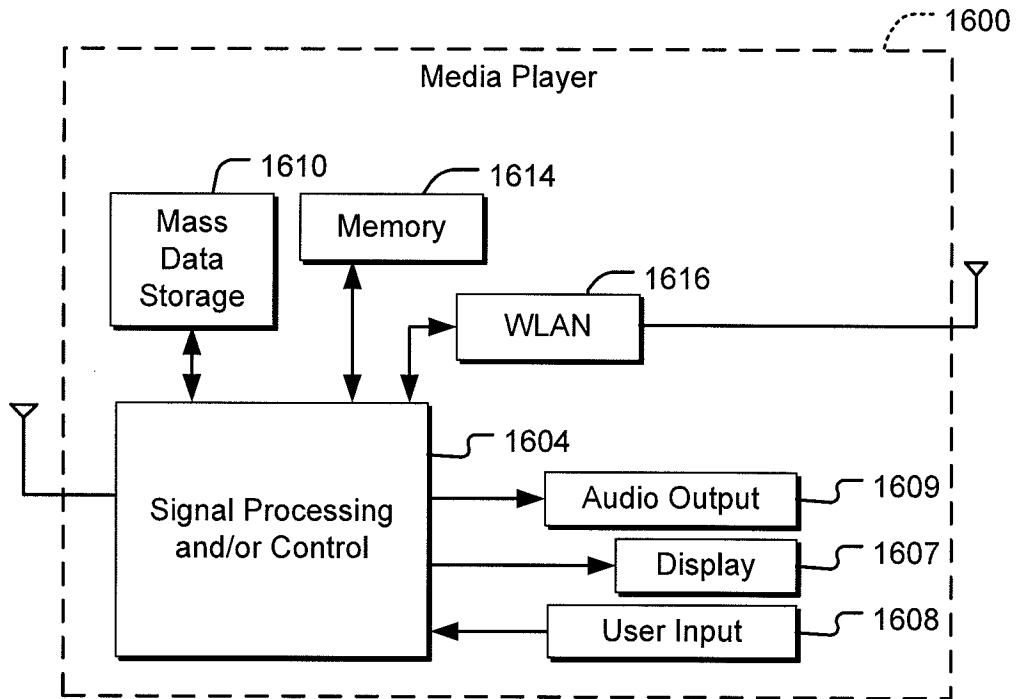


FIG. 5G

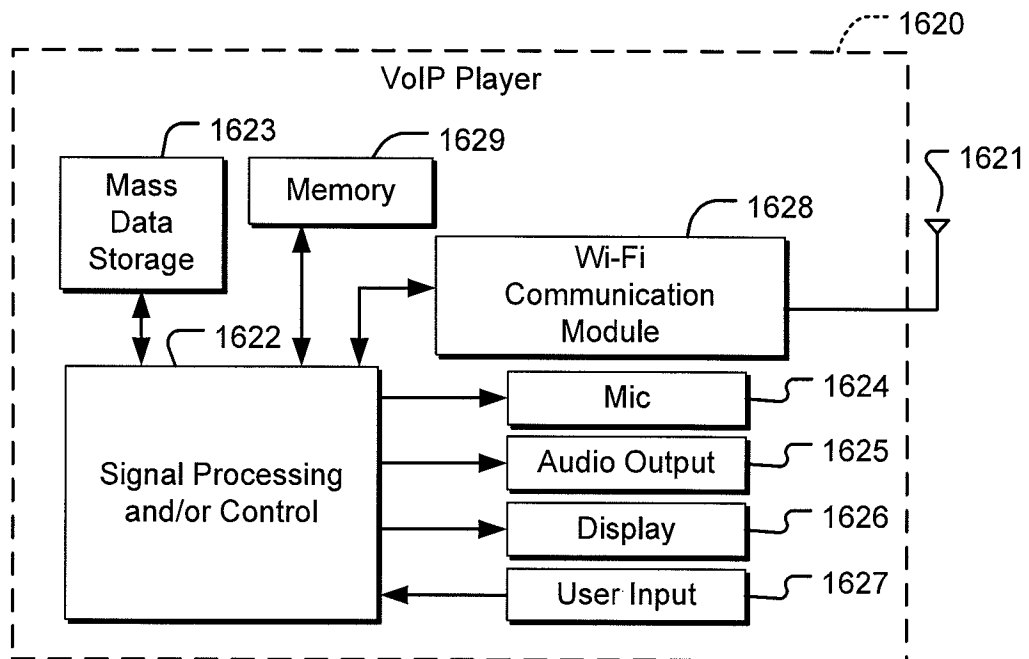


FIG. 5H

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/060932

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/50 H01L23/495

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 715 147 A (NAGANO JUNYA [JP]) 3 February 1998 (1998-02-03)	1,2,4-8, 10, 12-14, 16,17, 19-24, 26,27
Y	figures 1,5	9,15,28
X	WO 2004/090977 A (IXYS SEMICONDUCTOR GMBH [DE]; LINDEMANN ANDREAS [DE]) 21 October 2004 (2004-10-21) figure 1	1,2,4-6, 12,16, 17, 19-21,26

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

& document member of the same patent family

Date of the actual completion of the international search

24 July 2008

Date of mailing of the international search report

06/08/2008

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/060932

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 2005/253278 A1 (LAM KEN M [US] ET AL) 17 November 2005 (2005-11-17) figures 3,4	1-3,5,6, 11-14, 16-18, 20,21, 25-27
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International application No

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