A cmos device comprising an nmos transistor with recessed drain and source areas and a pmos transistor having a silicon/germanium material in the drain and source

Title of the Invention:

A recessed transistor configuration may be provided selectively for one type of transistor (150B), such as N-channel transistors, thereby enhancing

strain-inducing efficiency and series resistance, while a substantially planar configuration or raised drain and source configuration may be provided for other transistors (150A), such as P-channel transistors, which may also include a strained semiconductor alloy (157), while nevertheless providing a high degree of compatibility with CMOS techniques. For this purpose, an appropriate masking regime may be provided to efficiently cover the gate electrode (151) of one transistor type (150A, 150B) during the formation of the corresponding recesses (107, 112), while completely covering the other type of transistor (150A, 150B).