



(51) International Patent Classification:

H03F 1/02 (2006.01) H03F 3/68 (2006.01)
H03F 3/24 (2006.01)

(21) International Application Number:

PCT/US20 12/068501

(22) International Filing Date:

7 December 2012 (07.12.2012)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

13/3 13,971 7 December 2011 (07.12.2011) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:

US 13/31 3,971 (CON)
Filed on 7 December 2011 (07.12.2011)

(71) Applicant: TEXAS INSTRUMENTS INCORPORATED [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant (for JP only): TEXAS INSTRUMENTS JAPAN LIMITED [JP/JP]; 24-1, Nishi-Shinjuku 6-chome, Shinjuku-ku, Tokyo 160-8366 (JP).

(72) Inventors: HEZAR, Rahmi; 1847 Nueces Dr., Allen, TX 75013 (US). DING, Lei; 4512 Tuscany Dr., Plano, TX 75093 (US). HUR, Joonhoi; 15190 Prestonwood Blvd. #926, Dallas, TX 75248 (US). HAROUN, Baher, S.; 906 Pampa Dr., Allen, TX 75013 (US).

(74) Agents: FRANZ, Warren L. et al; Texas Instruments Incorporated, Deputy General Patent Counsel, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

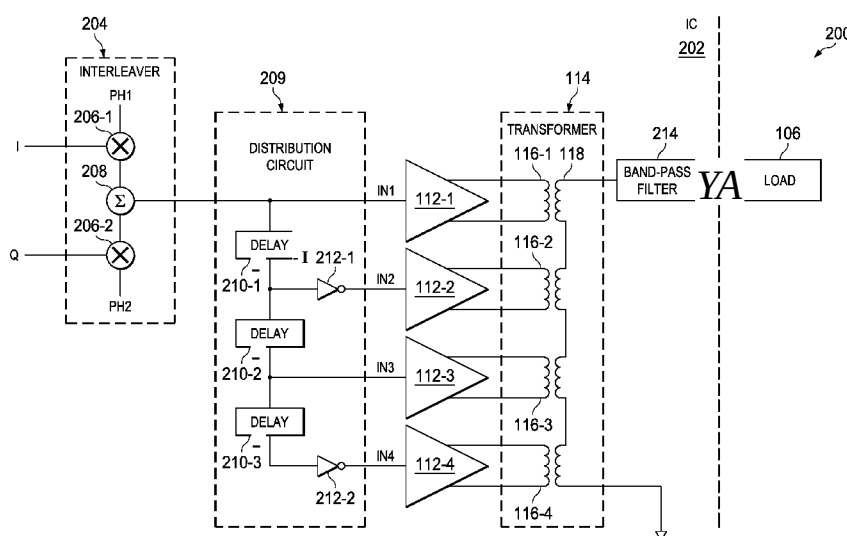
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.1 7(H))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.1 7(in))

[Continued on nextpage]

(54) Title: TRANSFORMER POWER COMBINER WITH FILTER RESPONSE



(57) **Abstract:** A method for generating an amplified radio frequency (RF) signal is provided. In-phase (I) and quadrature (Q) signals are received and interleaved by an interleaver (204) to generate a time-interleaved signal. Delayed time-interleaved signals are then generated by a distribution circuit (209) from the time interleaved signal, and each of the delayed time-interleaved signals (IN1, IN2, IN3, IN4) is amplified by an amplifier (112-1, 112-2, 112-3, 112-4) to generate a plurality of amplified signals. The amplified signals are then combined at a transformer (114) and by way of a filter (214) generate a filtered response with the transformer.

**Published:**

— with international search report (Art. 21(3))

— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

TRANSFORMER POWER COMBINER WITH FILTER RESPONSE

[0001] This relates generally to transformer power combiners and, more particularly, to transformer power combiners with a filter response.

BACKGROUND

[0002] FIG. 1 shows an example of a conventional radio frequency (RF) transmitter 200 can be seen. As shown in this example, RF circuitry is included on an integrated circuit (IC) 102 that uses a transformer combiner to generate the desired power. The scheme employed by the IC 102 is a polar modulation scheme, which uses a polar modulator 108 to decompose in-phase (I) and quadrature (Q) signals into amplitude and phase. The phase information is provided to the power amplifiers 112-1 to 112-4 (PAs), which are digital PAs, and the amplitude information is provided to the power controller 110, which controls the power output of each of PAs 112-1 to 112-4. Since each of the PAs 112-1 to 112-4 receive the same signal and the respective outputs are applied to primary windings 116-1 to 116-4 of transformer 114, the power from each "branch" can be added together by secondary winding 108 to generate an output signal for IC 102. Depending on the amount of deliverable power desired, the number of PAs 112-1 to 112-4 can be increased or decreased.

[0003] One issue with this transmitter 100 is that there is no filter response introduced that allows for any analog filtering. The usual reason is that phase modulation is very sensitive, and introduction of predistortion to induce a filter response would create a mismatch between the power controller 110 and the PAs 112-1 to 112-4. As a result, an off-chip band-pass filter 104 is provided between the IC 102 and load 106 (which may be an antenna and matching circuitry). Other conventional RF transmitter also have similar drawbacks. For example, quadrature modulators usually includes an off-chip PA, and Linear Amplification with Nonlinear Components (LENC) transmitters usually include off-chip Wilkinson combiners and band-pass filters. Thus, there is a need for an improved RF transmitter.

[0004] Some example of other conventional systems are: Haldi et al., "A 5.8 GHz 1 V Linear Power Amplifier Using a Novel On-Chip Transformer Power Combiner in Standard 90

nm CMOS," IEEE J. of Solid-State Circuits, Vol. 43, No. 5, May 2008, pp. 1054-1063; Lai et al, "A IV 17.9dBm 60GHz Power Amplifier in Standard 65nm CMOS," 2010 IEEE Intl. Solid-State Circuits Conf. (ISSCC), Feb. 10, 2010, pp. 424-425; Chang et al, "A 77 GHz Power Amplifier Using Transformer-Based Power Combiner in 90 nm CMOS," 2010 IEEE Custom Integrated Circuits Conf. (CICC), Sept. 19-22, 2010, pp. 1-4; Kim et al, "A Linear Multi-Mode CMOS Power Amplifier With Discrete Resizing and Concurrent Power Combining Structure," IEEE J. of Solid-State Circuits, Vol. 46, No. 5, May 2011; and U.S. Patent No. 7,777,570.

SUMMARY

[0005] An embodiment provides an apparatus including an interleaver that is configured to receive an in-phase (I) signal and a quadrature (Q) signal; a distribution circuit that is coupled to the interleaver; a plurality of power amplifiers (PAs), wherein each PA is coupled to the distribution circuit; and a transformer having a plurality of primary windings and a secondary winding, wherein each primary winding is coupled to at least one of the PAs, and wherein the distribution circuit introduces at least one of a plurality of delays between the output of the interleaver and each PA so as to generate a filter response with the transformer.

[0006] In accordance with an embodiment, the distribution circuit further comprises: a plurality of channels, wherein each channel is coupled to at least one of the PAs; and a plurality of delay circuits, wherein each delay circuit is coupled between at least two of the channels.

[0007] In accordance with an embodiment, the plurality of channels further comprises a first set of channels and a second set of channels that are interleaved with one another, and wherein each channel from the second set of channels further comprises an inverter.

[0008] In accordance with an embodiment, the interleaver further comprises: a first mixer that is configured to receive the I signal and a first interleaving signal; a second mixer that is configured to receive the Q signal and a second interleaving signal; and a combiner that is coupled to the first mixer, the second mixer, and the distribution circuit.

[0009] In accordance with an embodiment, the apparatus further comprises a band-pass filter that is coupled to the secondary winding of the transformer.

[0010] In accordance with an embodiment, the first and second interleaving signals are 90° out-of-phase.

[0011] In accordance with an embodiment, a method is provided. The method comprises receiving I and Q signals; interleaving the I and Q signals so as to generate a time-interleaved

signal; generating a plurality of delayed time-interleaved signals from the time interleaved signal; amplifying each of the delayed time-interleaved signals so as to generate a plurality of amplified signals; and combining the amplified signals with a transformer, wherein the delayed time-interleaved signals are arranged to generate a filter response with the transformer.

[0012] In accordance with an embodiment, the step of generating further comprises: delaying the time-interleaved signal by a first amount to generate a first delayed time-interleaved signal from the plurality of delayed time-interleaved signals; delaying the time-interleaved signal by a second amount to generate a second delayed time-interleaved signal from the plurality of delayed time-interleaved signals, wherein the second amount is the sum of the first amount and a predetermined delay; delaying the time-interleaved signal by a third amount to generate a third delayed time-interleaved signal from the plurality of delayed time-interleaved signals, wherein the third amount is the sum of the second amount and the predetermined delay; and delaying the time-interleaved signal by a fourth amount to generate a fourth delayed time-interleaved signal from the plurality of delayed time-interleaved signals, wherein the fourth amount is the sum of the third amount and the predetermined delay.

[0013] In accordance with an embodiment, the step of interleaving further comprises: mixing the I signal with a first interleaving signal; mixing the Q signal with a second interleaving signal; and combining the mixed I and Q signals to generate the time-interleaved signal.

[0014] In accordance with an embodiment, the steps of mixing and combining the mixed I and Q signals further comprise: outputting, during a first period of the first and second interleaving signals, the I signal; outputting, during a second period of the first and second interleaving signals, the Q signal; outputting, during a third period of the first and second interleaving signals, an inverse of the I signal; and outputting, during a fourth period of the first and second interleaving signals, an inverse of the Q signal.

[0015] In accordance with an embodiment, the steps of delaying the time-interleaved signal by the second amount and delaying the time-interleaved signal by the fourth amount further comprise: delaying and inverting the time-interleaved signal by the second amount to generate the second delayed time-interleaved signal; and delaying and inverting the time-interleaved signal by the fourth amount to generate the third delayed time-interleaved signal.

[0016] In accordance with an embodiment, an apparatus is provided. The apparatus comprises an interleaver that is configured to receive an I signal and a Q signal; a distribution circuit that is coupled to the interleaver so as to generate first, second, third, and fourth delayed time-interleaved signals; a first PA that is coupled to the distribution circuit so as to receive the first delayed time-interleaved signal; a second PA that is coupled to the distribution circuit so as to receive the second delayed time-interleaved signal; a third PA that is coupled to the distribution circuit so as to receive the third delayed time-interleaved signal; a fourth PA that is coupled to the distribution circuit so as to receive the fourth delayed time-interleaved signal; a transformer having a first primary winding, a second primary winding, a third primary winding, a fourth primary winding, and a secondary winding, wherein the first primary winding is coupled to the first PA, and wherein the second primary winding is coupled to the second PA, and wherein the third primary winding is coupled to the third PA, and wherein the fourth primary winding is coupled to the fourth PA, and wherein the first, second, third, and fourth delayed time-interleaved signals are introduced so as to generate a filter response with the transformer.

[0017] In accordance with an embodiment, the distribution circuit further comprises: a first channel that is coupled between the interleaver and the first PA; a first delay circuit that is coupled to the interleaver; a second channel that is coupled between the first delay circuit and the second PA; a second delay circuit that is coupled to the first delay circuit; a third channel that is coupled between the second delay circuit and the third PA; a third delay circuit that is coupled to the second delay circuit; and a fourth channel that is coupled between the third delay circuit and the fourth PA.

[0018] In accordance with an embodiment, the second and fourth channels further comprise first and second inverters, respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. 1 is a diagram of an example of a conventional RF transmitter;

[0020] FIG. 2 is a diagram of an example of an RF transmitter in accordance with an embodiment;

[0021] FIG. 3 is an example of a timing diagram depicting the operation of the interleaver and distribution circuit of FIG. 2; and

[0022] FIG. 4 is a diagram of the filter response of the transmitter of FIG. 2.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0023] FIG. 2 shows an example of an RF transmitter 200 in accordance with an example embodiment. As shown, the transmitter includes transformer 114 and PAs 112-1 to 112-4, similar to system 100. In this example, four PAs 112-1 to 112-4 are shown for the sake of illustration, but depending on the desired output power the number can be increased or decreased. Transmitter 200, however, does not operate based on polar modulation but, instead, operates as a time-interleaved pulse width modulation (PWM) transmitter. To do this, the I and Q signals are upsampled at a rate of four times the center frequency F_c . The interleaver 204 (which generally comprises mixers 206-1 and 206-2 and combiner or adder 208) then interleaves the I and Q signals into a single stream using interleaving signals PHI and PH2. The distribution circuit 209 (which generally comprises delay circuits 210-1 to 210-3 and inverters 212-1 and 212-2) then distributes the interleaved stream to PAs 112-1 to 112-4, where, in this example, there is a channel for each of the PAs 112-1 to 112-4. The distribution circuit 209 also introduces a delay for each channel generating signals IN1 to IN4 that would create a filter response with the transformer 114 (namely, an analog finite impulse response). Since a filter response is created or introduced with transformer 114, an on-chip band-pass filter 214 can be used instead of an off-chip band-pass filter (i.e., 104), reducing cost.

[0024] To illustrate the operation of transmitter, a timing diagram is shown in FIG. 3. As shown in this example, the interleaving signals PHI and PH2 have a cycle of $0 \rightarrow 1 \rightarrow 0 \rightarrow -1 \rightarrow 0$ and are 90° out-of-phase with one another. In period T1, signals PHI and PH2 are 1 and 0, respectively, which allows the I signal to be provided as signal IN1 (with the channel for PA 112-1 having a nominal delay). In period T2, signals PHI and PH2 are 0 and 1, respectively, allowing the Q signal to be provided as signal IN1. In period T3, signals PHI and PH2 are -1 and 0, respectively, allowing an inverse of the I signal to be provided as signal IN1. Additionally, because of the use of delay circuit 210-1 (which is generally a $\frac{1}{2}$ cycle delay but the length of the delay is usually related to the upsample rate and/or the number of PAs), the channel for PA 112-2 receives the I signal from period T1, which is then inverted by inverter 212-1 and provided as signal IN2. Similarly, for period T4, an inverse of the Q signal is provided as signals IN1 and IN2, and a similar result is shown for periods T5 to T10 for signals IN1 to IN4. As should be apparent, the structure of the distribution circuit 209 (which is similar to the construction for a finite impulse response (FIR) filter) and the timings for the interleaving

signals PHI and PH2, the signals IN1 to IN4 are the same or are "aligned." This creates notches at certain frequencies (as shown, for example, in FIG. 4 with notches at $F_c/2$, $3F_c/2$, and $2F_c$), which is the filter response created with transformer 114.

[0025] As a result of employing the interleaver 204 and distribution circuit 209 in a manner so as to create a filter response with transformer 114, several advantages can be realized. A complete on-chip combining of the I and Q signals along with parallel PAs 112-1 to 112-4 through a transformer 114 to increase the total output power is also achieved. As an example, if individual PAs 112-1 to 112-4 can deliver 250mW of power, the combined power output can be 1W with fully integrated solution. The filter response with transformer 114 also provides a sufficient amount of suppression that relaxes requirements for analog band-pass filter 214 following the transformer 114, allowing for an on-chip implementation with a low Q-factor. Additionally, adding more parallel PAs (greater than the four shown) to reach higher output power creates more room to improve the filter response of the transformer with more notch locations and better stop-band attenuation. Moreover, the fully digital transmitter architecture allows flexibility to adjust out-of-band noise and image cancellation using different PWM schemes to meet the spectral mask requirements without using external off-chip components.

[0026] Those skilled in the art to which the invention relates will appreciate that changes may be made to the described embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:
an interleaver that is configured to receive an in-phase (I) signal and a quadrature (Q) signal;
a distribution circuit that is coupled to the interleaver;
a plurality of power amplifiers (PAs), wherein each PA is coupled to the distribution circuit; and
a transformer having a plurality of primary windings and a secondary winding, wherein each primary winding is coupled to at least one of the PAs, and wherein the distribution circuit introduces at least one of a plurality of delays between the output of the interleaver and each PA so as to generate a filter response with the transformer.
2. The apparatus of Claim 1, wherein the distribution circuit further comprises:
a plurality of channels, wherein each channel is coupled to at least one of the PAs; and
a plurality of delay circuits, wherein each delay circuit is coupled between at least two of the channels.
3. The apparatus of Claim 2, wherein the plurality of channels further comprises a first set of channels and a second set of channels that are interleaved with one another, and wherein each channel from the second set of channels further comprises an inverter.
4. The apparatus of Claim 3, wherein the interleaver further comprises:
a first mixer that is configured to receive the I signal and a first interleaving signal;
a second mixer that is configured to receive the Q signal and a second interleaving signal;
and
a combiner that is coupled to the first mixer, the second mixer, and the distribution circuit.

5. The apparatus of Claim 4, wherein the apparatus further comprises a band-pass filter that is coupled to the secondary winding of the transformer.

6. The apparatus of Claim 5, wherein the first and second interleaving signals are 90° out-of-phase.

7. A method comprising:
receiving I and Q signals;
interleaving the I and Q signals so as to generate a time-interleaved signal;
generating a plurality of delayed time-interleaved signals from the time interleaved signal;
amplifying each of the delayed time-interleaved signals so as to generate a plurality of amplified signals; and
combining the amplified signals with a transformer, wherein the delayed time-interleaved signals are arranged to generate a filter response with the transformer.

8. The method of Claim 7, wherein the step of generating further comprises:
delaying the time-interleaved signal by a first amount to generate a first delayed time-interleaved signal from the plurality of delayed time-interleaved signals;
delaying the time-interleaved signal by a second amount to generate a second delayed time-interleaved signal from the plurality of delayed time-interleaved signals, wherein the second amount is the sum of the first amount and a predetermined delay;
delaying the time-interleaved signal by a third amount to generate a third delayed time-interleaved signal from the plurality of delayed time-interleaved signals, wherein the third amount is the sum of the second amount and the predetermined delay; and
delaying the time-interleaved signal by a fourth amount to generate a fourth delayed time-interleaved signal from the plurality of delayed time-interleaved signals, wherein the fourth amount is the sum of the third amount and the predetermined delay.

9. The method of Claim 8, wherein the step of interleaving further comprises:
mixing the I signal with a first interleaving signal;

mixing the Q signal with a second interleaving signal; and
combining the mixed I and Q signals to generate the time-interleaved signal.

10. The method of Claim 9, wherein the steps of mixing and combining the mixed I and Q signals further comprise:

outputting, during a first period of the first and second interleaving signals, the I signal;
outputting, during a second period of the first and second interleaving signals, the Q signal;

outputting, during a third period of the first and second interleaving signals, an inverse of the I signal; and

outputting, during a fourth period of the first and second interleaving signals, an inverse of the Q signal.

11. The method of Claim 10, wherein the steps of delaying the time-interleaved signal by the second amount and delaying the time-interleaved signal by the fourth amount further comprise:

delaying and inverting the time-interleaved signal by the second amount to generate the second delayed time-interleaved signal; and

delaying and inverting the time-interleaved signal by the fourth amount to generate the third delayed time-interleaved signal.

12. An apparatus comprising:

an interleaver that is configured to receive an I signal and a Q signal;

a distribution circuit that is coupled to the interleaver so as to generate first, second, third, and fourth delayed time-interleaved signals;

a first PA that is coupled to the distribution circuit so as to receive the first delayed time-interleaved signal;

a second PA that is coupled to the distribution circuit so as to receive the second delayed time-interleaved signal;

a third PA that is coupled to the distribution circuit so as to receive the third delayed time-interleaved signal;

a fourth PA that is coupled to the distribution circuit so as to receive the fourth delayed time-interleaved signal;

a transformer having a first primary winding, a second primary winding, a third primary winding, a fourth primary winding, and a secondary winding, wherein the first primary winding is coupled to the first PA, and wherein the second primary winding is coupled to the second PA, and wherein the third primary winding is coupled to the third PA, and wherein the fourth primary winding is coupled to the fourth PA, and wherein the first, second, third, and fourth delayed time-interleaved signals are introduced so as to generate a filter response with the transformer.

13. The apparatus of Claim 12, wherein the distribution circuit further comprises:

a first channel that is coupled between the interleaver and the first PA;

a first delay circuit that is coupled to the interleaver;

a second channel that is coupled between the first delay circuit and the second PA;

a second delay circuit that is coupled to the first delay circuit;

a third channel that is coupled between the second delay circuit and the third PA;

a third delay circuit that is coupled to the second delay circuit; and

a fourth channel that is coupled between the third delay circuit and the fourth PA.

14. The apparatus of Claim 13, wherein the second and fourth channels further comprise first and second inverters, respectively.

15. The apparatus of Claim 14, wherein the interleaver further comprises:

a first mixer that is configured to receive the I signal and a first interleaving signal;

a second mixer that is configured to receive the Q signal and a second interleaving signal;

and

a combiner that is coupled to the first mixer, the second mixer, and the distribution circuit.

16. The apparatus of Claim 15, wherein the apparatus further comprises a band-pass filter that is coupled to the secondary winding of the transformer.

17. The apparatus of Claim 16, wherein the first and second interleaving signals are 90° out-of-phase.

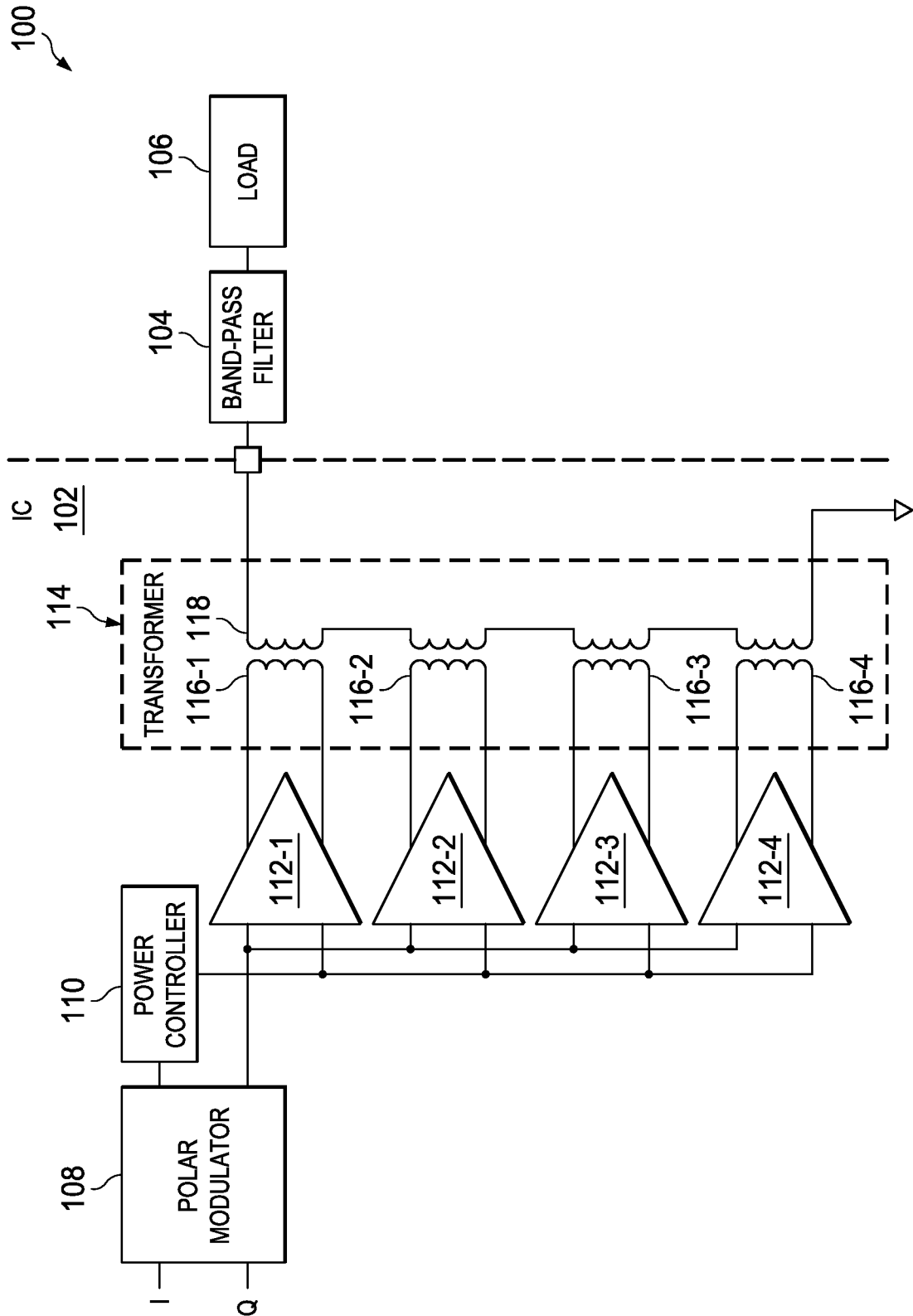


FIG. 1
(PRIOR ART)

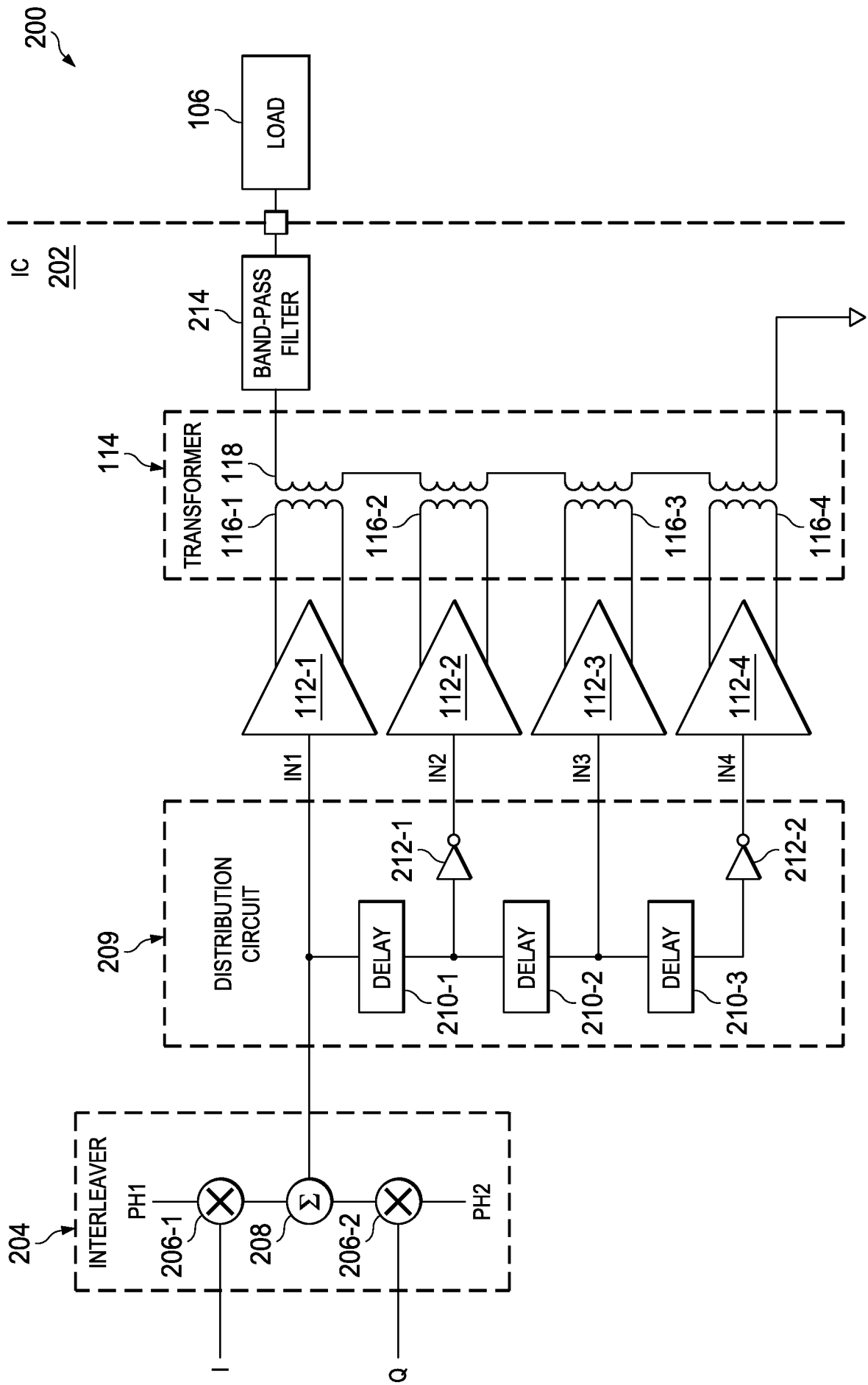


FIG. 2

3/3

FIG. 3

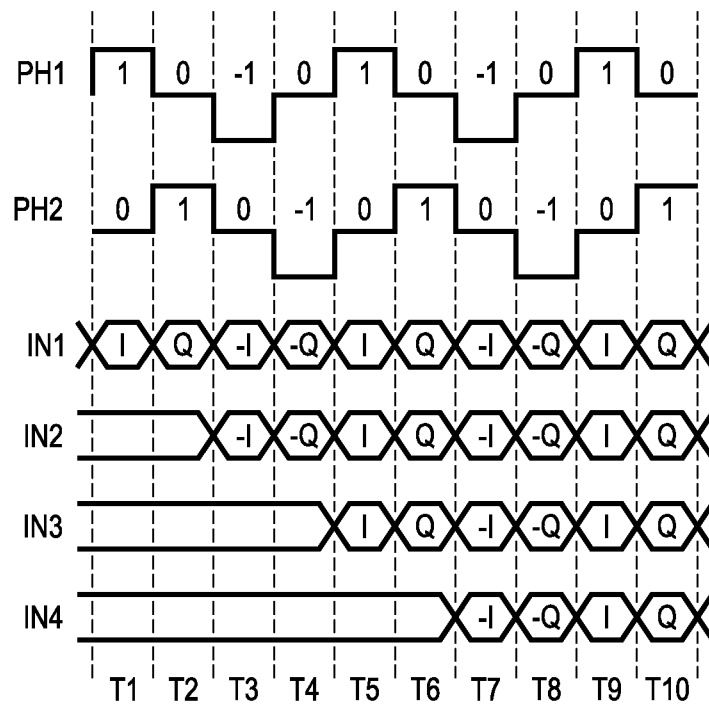
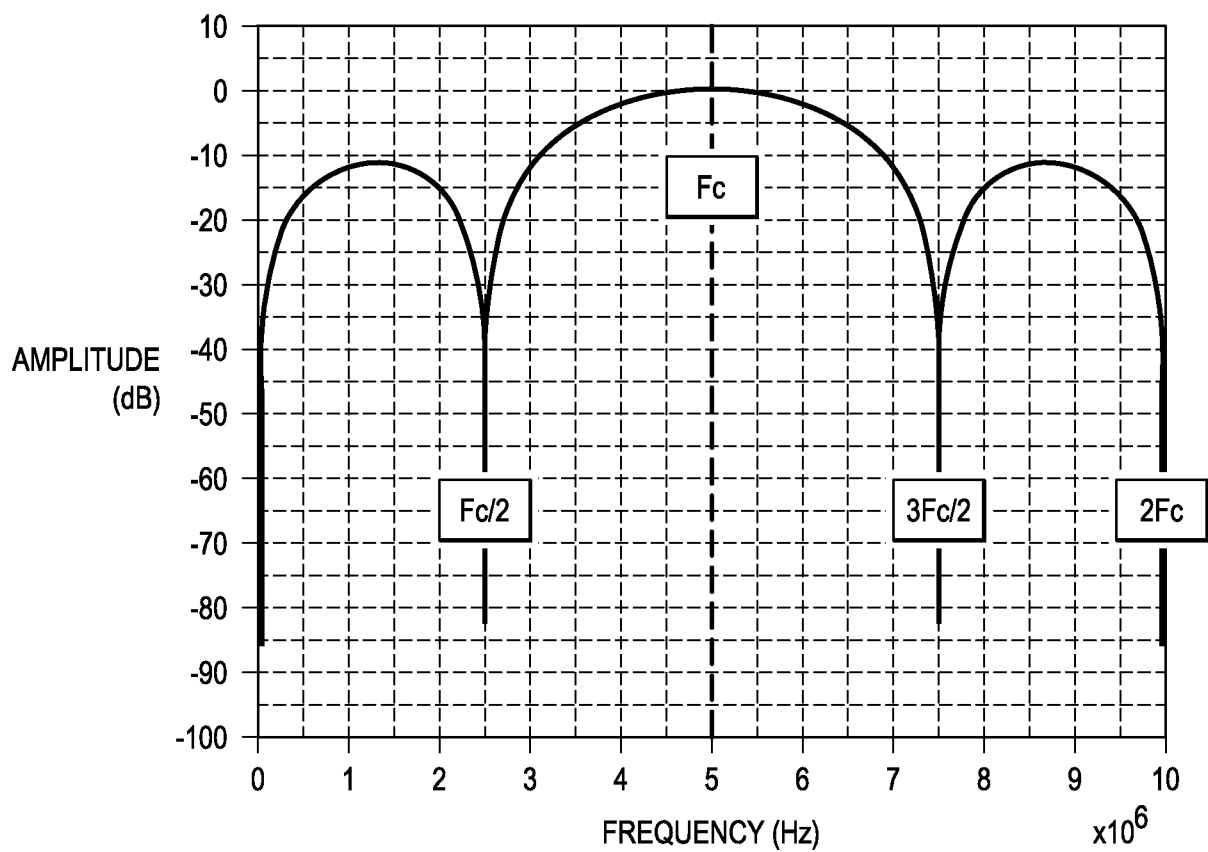


FIG. 4



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/068501**A. CLASSIFICATION OF SUBJECT MATTER****H03F 1/02(2006.01)i, H03F 3/24(2006.01)1, H03F 3/68(2006.01)1**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F 1/02; H04L 27/00; H04L 27/36; H03F 3/26; H04L 27/20; H04B 1/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: interleaver, modulation, RF, in-phase (I), quadrature (Q), phase delay, power amplifier, transformer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 2011-0050344 A1 (HE XIN et al.) 03 March 2011 See abstract, paragraphs [0024] -[0031], claims 1, 6, 9, and figure 3.	1-2, 7-10, 12-13 3-6, 11, 14-17
Y	US 2007-0201581 A1 (P00JAN WAGH et al.) 30 August 2007 See abstract, paragraphs [0012] -[0016], claim 1, figure 1.	1-2, 7-10, 12-13
A	US 2011-0129037 A1 (STASZEWSKI BOGDAN et al.) 02 June 2011 See abstract, paragraphs [0069] -[0074], claims 1-3, and figures 1, 5, 7-8.	1-17
A	US 7221915 B2 (JEFFREY WILLIAM TRIPP et al.) 22 May 2007 See abstract, column 7, line 17 ~ column 8, line 2, claims 1, 8, and figure 3a.	1-17
A	US 5638401 A (JONES; MARK A.) 10 June 1997 See abstract, column 4, line 8 ~ line 44, claims 1-2, and figure 3.	1-17

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28 March 2013 (28.03.2013)

Date of mailing of the international search report

29 March 2013 (29.03.2013)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan
City, 302-70 1, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

KIM, Sung Gon

Telephone No. 82-42-481-8746



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2012/068501

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011-0050344 A1	03,03,2011	AT 527758 T CN 102007699 A EP 2266208 A2 EP 2266208 B1 US 8237503 B2 WO 2009- 113000 A2 WO 2009- 113000 A3	15 . 10 . 2011 06 . 04 . 2011 29 . 12 . 2010 05 . 10 . 2011 07 . 08 . 2012 17 . 09 . 2009 05 . 11 . 2009
US 2007-020158 1 A1	30,08,2007	None	
US 2011-0129037 A1	02,06,2011	EP 2333950 A2	15 . 06 . 2011
US 722 19 15 B2	22,05,2007	AU 2003-275477 A1 US 2004-0266359 A1 WO 2004-034566 A1	04 . 05 . 2004 30 . 12 . 2004 22 . 04 . 2004
US 563840 1 A	10,06,1997	CN 1126301 CO CN 1173253 AO EP 0807344 A1 EP 0807344 A1 EP 0807344 B1 JP 10-5 13323 A KR 10- 1998-070 1845 A WO 96-24205 A1	29 . 10 . 2003 11 . 02 . 1998 19 . 11 . 1997 02 . 01 . 2004 02 . 04 . 2008 15 . 12 . 1998 25 . 06 . 1998 08 . 08 . 1996