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(54) **Title**: CASCADED PACKED U-CELL MULTILEVEL INVERTER

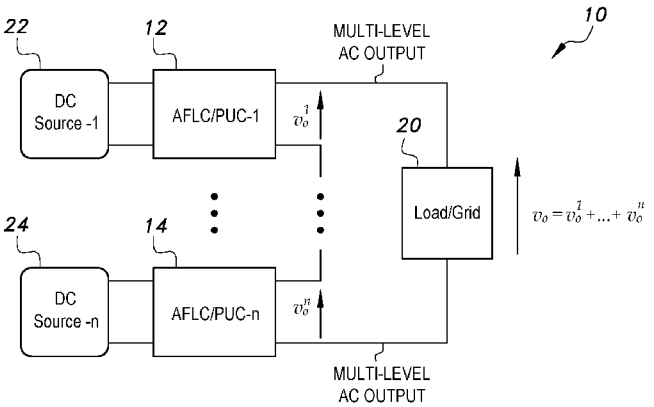


FIG. 1

(57) **Abstract**: The cascaded packed U-cell multilevel inverter (10) is a power converter for transforming direct current (DC) power to alternating current (AC) power with variable voltage magnitude and variable frequency output. The cascaded packed U-cell multilevel inverter (10) includes a first packed U-cell (PUC) multilevel inverter (12) and at least one sequential packed U-cell multilevel inverter (14) connected in cascade to the first packed U-cell multilevel inverter (12), i.e., the cascaded packed U-cell multilevel inverter (10) is formed by cascading two or more PUC multilevel inverter units (12, 14). Preferably, each PUC multilevel inverter is a 7-level inverter including a DC link capacitor adapted for connection to a separate independent DC power source (22, 24) and a flying capacitor clamping the multilevel inverter to one-third of the voltage of the corresponding power source.

WO 2017/152181 A1

CASCADED PACKED U-CELL MULTILEVEL INVERTER

TECHNICAL FIELD

The present invention relates to power converters, and particularly to a power converter for transforming direct current (DC) power to alternating current (AC) power with variable voltage magnitude and variable frequency output using a cascade of packed U-cell (PUC) multilevel inverters.

BACKGROUND ART

Multilevel inverters are commonly used as an interface in renewable energy generation systems, such as solar photovoltaic (PV) applications. Multilevel inverters are also commonly used in medium voltage and high power motor drive systems, such as those found in electric and hybrid vehicles. The wide usage of multilevel inverters is due to a number of desirable properties, such as reduced voltage stress on power semiconductor switches, reduced voltage harmonics, reduced $\frac{dv}{dt}$, reduced electromagnetic interference, and a comparatively higher efficiency. However, in higher voltage and high power applications, the switching frequency and device ratings of conventional multilevel inverters are limited.

Although a wide variety of multilevel topologies are available, the most common topologies for multilevel inverters are neutral point clamped (NPC), flying capacitor (FLC), and cascaded H-bridge (CHB). These topologies each suffer from numerous drawbacks. The NPC inverter, for example, is inefficient when it comes to balancing of the neutral point. Ordinarily, the neutral point should be precisely controlled at zero voltage but, due to an asymmetrical switching of the power switches in NPC inverters, the neutral point is not maintained at zero. In order to maintain zero potential, a modified pulse width modulation (PWM) technique must be applied, making control complex. A similar problem exists in FLC inverters, where the zero voltage is obtained by equally charging and discharging the two clamping capacitors using a modified PWM technique. The inherent problem in CHB inverters is the requirement that isolated DC sources must be used.

Thus, a cascaded packed U-cell multilevel inverter solving the aforementioned problems is desired.

DISCLOSURE OF INVENTION

The cascaded packed U-cell multilevel inverter is a power converter for transforming direct current (DC) power to alternating current (AC) power with variable voltage magnitude and variable frequency output. The cascaded packed U-cell multilevel inverter includes a first packed U-cell (PUC) multilevel inverter and at least one sequential packed U-cell multilevel inverter connected in cascade to the first packed U-cell multilevel inverter; i.e., the cascaded packed U-cell multilevel inverter is formed by cascading two or more PUC multilevel inverter units. Preferably, each PUC multilevel inverter is a 7-level inverter including a DC link capacitor adapted for connection to a separate independent DC power source and a flying capacitor clamping the multilevel inverter to one-third of the voltage of the corresponding power source. The voltage developed over the DC link capacitors for the first packed U-cell multilevel inverter and the second packed U-cell multilevel inverter(s) may have a voltage ratio of 4:1, such that thirty-one output voltage levels are selectively obtained. Alternatively, the voltage developed over the DC link capacitors for the first PUC multilevel inverter and the second PUC multilevel inverter(s) may have a voltage ratio of 7:1, such that forty-nine output voltage levels are selectively obtained.

These and other features of the present invention will become readily apparent upon further review of the following specification and drawings.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a block diagram illustrating a cascaded packed U-cell multilevel inverter according to the present invention.

Fig. 2 is a schematic diagram of a single packed U-cell (PUC) multilevel inverter used in the cascaded packed U-cell multilevel inverter according to the present invention.

Fig. 3 illustrates the eight distinct switching states available for the single packed U-cell (PUC) multilevel inverter of Fig. 2.

Fig. 4 is a schematic diagram illustrating the cascaded packed U-cell multilevel inverter according to the present invention.

Fig. 5A illustrates the switching pattern for a first packed U-cell multilevel inverter of the cascaded packed U-cell multilevel inverter.

Fig. 5B illustrates the switching pattern for a second packed U-cell multilevel inverter of the cascaded packed U-cell multilevel inverter.

Fig. 6 is a block diagram illustrating the cascaded packed U-cell multilevel inverter integrated into an exemplary solar photovoltaic (PV)/direct current (DC) power system.

Fig. 7 is a schematic diagram illustrating the cascaded packed U-cell multilevel inverter with an associated control system.

Fig. 8 schematically illustrates a conventional prior art 31-level inverter.

Fig. 9A shows load voltage, load current and inverter terminal voltage for a simulated cascaded packed U-cell multilevel inverter according to the present invention.

Fig. 9B compares simulated voltage output for a first packed U-cell multilevel inverter of the cascaded packed U-cell multilevel inverter against simulated voltage output for a second packed U-cell multilevel inverter of the cascaded packed U-cell multilevel inverter and simulated overall terminal voltage for the cascaded packed U-cell multilevel inverter according to the present invention.

Fig. 9C is a graph showing DC bus voltages and flying capacitor voltages for the simulated cascaded packed U-cell multilevel inverter.

Fig. 9D is a graph showing the carrier signal and modulation signal for the simulated cascaded packed U-cell multilevel inverter.

Fig. 10A is a graph showing voltage output of the cascaded packed U-cell multilevel inverter with a 31-level output.

Fig. 10B is a graph showing voltage output of the cascaded packed U-cell multilevel inverter with a 25-level output.

Fig. 10C is a graph showing voltage output of the cascaded packed U-cell multilevel inverter with a 19-level output.

Fig. 10D is a graph showing voltage output of the cascaded packed U-cell multilevel inverter with a 13-level output.

Fig. 10E shows the results of a harmonic analysis on the terminal voltage of the cascaded packed U-cell multilevel inverter according to the present invention.

Fig. 11A shows the results of measured DC supply and flying capacitor voltages for the cascaded packed U-cell multilevel inverter according to the present invention.

Fig. 11B shows the results of the measured load voltage for the cascaded packed U-cell multilevel inverter according to the present invention.

Fig. 11C shows the results of the measured cross-resistor current and terminal voltage for the cascaded packed U-cell multilevel inverter according to the present invention.

Fig. 11D compares the outputs of a first packed U-cell multilevel inverter and a second packed U-cell multilevel inverter of the cascaded packed U-cell multilevel inverter, and further compared against overall output of the cascaded packed U-cell multilevel inverter.

Fig. 11E shows the results of measured voltages across switch pairs of the first packed U-cell multilevel inverter of the cascaded packed U-cell multilevel inverter.

Fig. 11F shows the results of measured voltages across switch pairs of the second packed U-cell multilevel inverter of the cascaded packed U-cell multilevel inverter.

Fig. 12A shows experimental results of the measured spectrum of load voltage of the cascaded packed U-cell multilevel inverter.

Fig. 12B shows experimental results of the measured spectrum of load current of the cascaded packed U-cell multilevel inverter.

Fig. 13A shows the results of measured output voltages of the cascaded packed U-cell multilevel inverter for 31-level output.

Fig. 13B shows the results of measured output voltages of the cascaded packed U-cell multilevel inverter for 25-level output.

Fig. 13C shows the results of measured output voltages of the cascaded packed U-cell multilevel inverter for 19-level output.

Fig. 13D shows the results of measured output voltages of the cascaded packed U-cell multilevel inverter for 13-level output.

Fig. 14A shows the results of measured DC supply and flying capacitor voltages of an alternative cascaded packed U-cell multilevel inverter with a 49-level output.

Figs. 14B and 14C show the results of measured load voltage and current across a resistor, as well as terminal voltage, for the alternative cascaded packed U-cell multilevel inverter with a 49-level output.

Fig. 14D shows the results of the measured output of first and second cascaded packed U-cell multilevel inverters, as well as the overall output of the alternative cascaded packed U-cell multilevel inverter with a 49-level output.

Fig. 14E shows the results of the measured voltages across the switches of the first packed U-cell multilevel inverter of the alternative cascaded packed U-cell multilevel inverter with a 49-level output.

Fig. 14F shows the results of the measured voltages across the switches of the second packed U-cell multilevel inverter of the alternative cascaded packed U-cell multilevel inverter with a 49-level output.

Fig. 14G shows the results of the measured terminal voltage and grid/load voltage of the alternative cascaded packed U-cell multilevel inverter with a 49-level output.

Fig. 15A shows the results of a harmonic analysis of the load current of the alternative cascaded packed U-cell multilevel inverter with a 49-level output.

Fig. 15B shows the results of a harmonic analysis of the terminal voltage of the alternative cascaded packed U-cell multilevel inverter with a 49-level output.

Fig. 16A shows the measured output voltages for the alternative cascaded packed U-cell multilevel inverter with a 49-level output.

Fig. 16B shows a magnified view of the output's positive cycle from the output of Fig. 16A.

Fig. 16C shows the output voltages for a further alternative cascaded packed U-cell multilevel inverter with a 43-level output.

Fig. 16D shows the output voltages for another alternative cascaded packed U-cell multilevel inverter with a 37-level output.

Similar reference characters denote corresponding features consistently throughout the attached drawings.

BEST MODES FOR CARRYING OUT THE INVENTION

The cascaded packed U-cell multilevel inverter 10 is a power converter for transforming direct current (DC) power to alternating current (AC) power with variable voltage magnitude and variable frequency output. As shown in Fig. 1, the cascaded packed U-cell multilevel inverter 10 includes a first asymmetrical flying capacitor (AFLC) or packed U-cell (PUC) multilevel inverter (AFLC/PUC-1) 12 and at least one asymmetrical flying capacitor (AFLC) or packed U-cell (PUC) multilevel inverter 14 connected in cascade to the first packed U-cell multilevel inverter 12, i.e., the cascaded packed U-cell multilevel inverter 10 is formed by cascading two or more PUC multilevel inverter units. In Fig. 1, AFLC/PUC-n represents the *n*-th asymmetrical flying capacitor (AFLC) or packed U-cell (PUC) multilevel inverter 14 in a cascade of n AFLC/PUCs.

A single packed U-cell multilevel inverter 16 is show in Fig. 2. As shown, each PUC multilevel inverter 16 is, preferably, a 7-level inverter including six power switching devices,

a DC link capacitor adapted for connection to a separate independent DC power source and a flying capacitor clamping the multilevel inverter to one-third of the voltage of the corresponding power source. The DC link can be obtained from a solar photovoltaic module, a standard AC/DC converter or the like. In Fig. 2, PUC multilevel inverter 16 is shown as having six power switching devices S1, S2, S3, S1', S2' and S3'. Here, the clamping capacitor or flying capacitor voltage V_1 is one-third of the DC link voltage V_2. The switches S1, S2, S3, S1', S2' and S3' may be MOSFETs, IGBTs or the like. Switch pairs S1, S1'; S2, S2'; and S3, S3' are complimentary in operation.

As shown in Fig. 3, for a flying capacitor voltage tied to one-third of the DC link voltage, $\frac{1}{3}V_{DC}$, where V_{DC} is the DC link voltage, eight switching states are possible (shown in Fig. 3 as set 100): V_{DC} (State 1), $\frac{1}{3}V_{DC}$ (State 2), 0 (State 3), $-\frac{2}{3}V_{DC}$ (State 4), $\frac{2}{3}V_{DC}$ (State 5), 0 (State 6), $-\frac{1}{3}V_{DC}$ (State 7), and $-V_{DC}$ (State 8). The two zero states (States 3 and 6) are referred to as "redundant states". This is achieved when the load is short circuited by three main switching devices or three complimentary switching devices being turned on simultaneously.

The voltage developed over the DC link capacitors for the first packed U-cell multilevel inverter 12 and a second packed U-cell multilevel inverter 14, with the two units each generating 7-level output, may have a voltage ratio of 4:1 (or 1:4), such that thirty-one output voltage levels are selectively obtained. Here, the thirty-one overall output phase voltage levels are achieved when the two PUC inverters 12, 14 are supplied from two isolated DC sources 22, 24, respectively. The two cascaded units 12, 14 can be supplied from two isolated supplies, such as, for example, two solar photovoltaic (PV) arrays with a voltage ratio of 1:4 or 4:1. If the ratio of the two isolated DC supplies 22, 24 is changed then the number of output voltage levels is also changed. For example, when the ratio of the two isolated sources 22, 24 are 1:2 or 2:1, then 15 output phase voltage levels can be achieved. When the voltage developed over the DC link capacitors for the first PUC multilevel inverter 12 and the second PUC multilevel inverter 14 has a voltage ratio of 7:1, forty-nine output voltage levels are selectively obtained.

The two PUC inverters 12, 14 can be controlled using level or phase-shifted multicarrier pulse width modulation techniques. A higher number of voltage levels gives rise to lower $\frac{dv}{dt}$, lower electromagnetic interference, lower switching losses and higher conversion efficiency. This remains true for any number of output phases, such as, for

example, three-phase or five-phase outputs, which can be achieved by cascading identical PUC inverter units. The cascaded packed U-cell multilevel inverter 10 may be used in a wide variety of applications, such as solar PV for supplying power to a utility grid, variable speed drives, electric vehicles, HVDC, in power systems, etc. The cascaded packed U-cell multilevel inverter 10 produces output voltage in several steps, depending upon the number of levels. For example, a five level output requires five steps. As the number of steps grows, the waveform grows closer to being sinusoidal. The ideal waveform is a pure sine wave, which is not realistically possible when generated using power electronic devices.

A neutral point clamped (NPC) 7-level inverter uses a single DC power source, ten power switches, six DC link capacitors and eight clamping diodes. The NPC 7-level inverter includes a total of 25 separate components with a very high level of control complexity. A flying capacitor converter (FLC) 7-level inverter also uses a single DC power source, ten power switches, six DC link capacitors and four clamping capacitors. The FLC 7-level inverter includes a total of 21 separate components, also with a very high level of control complexity. The cascaded H-bridge (CHB) 7-level inverter uses two DC power sources, twelve power switches, and three DC link capacitors. The CHB 7-level inverter includes a total of 17 separate components, with a low level of control complexity. By comparison, the present cascaded packed U-cell multilevel inverter 10 uses a single DC power source, only six power switches, only one DC link capacitor and only one clamping capacitor. The cascaded packed U-cell multilevel inverter 10 includes a total of only nine separate components with a moderate level of control complexity.

For purposes of simplification, the following analysis largely focuses on only two cascaded PUC inverters. It should be understood that the following is intended to be extended to *n* PUC inverts with different ratios of the DC link voltages. As noted above, a single PUC inverter produces three positive output voltage levels and three negative voltage levels, while one level is zero. Thus, if one inverter unit is kept at one voltage level and the other PUC inverter unit is switched in such a way as to generate all seven voltage levels, when the outputs of the two units are added, the number of output voltage levels can be increased. It is important to note that the total number of output voltage levels will greatly depend upon the ratio of the two DC link voltages. Considering one DC link voltage, V_{DC1}, and a second DC link voltage, V_{DC2}, then a 1:1 ratio of V_{DC1}: V_{DC2} yields 13 output voltage levels. Similarly, a V_{DC1}: V_{DC2} ratio of 1:2 yields 19 output voltage levels. A V_{DC1}: V_{DC2} ratio of 1:3 yields 25 output voltage levels, a V_{DC1}: V_{DC2} ratio of 1:4 yields 31 output voltage

levels, a V_{DC1}: V_{DC2} ratio of 1:5 yields 37 output voltage levels, a V_{DC1}: V_{DC2} ratio of 1:6 yields 43 output voltage levels, and a V_{DC1}: V_{DC2} ratio of 1:7 yields 49 output voltage levels.

From the above, it can be seen that, in general, for a number of positive or negative levels, p, p^0: $p^0 + p^1$: $p^0 + p^1 + p^2$: $p^0 + p^1 + p^2 + p^3$: $p^0 + p^1 + p^2 + p^3 + p^4$ yields $1V_{DC}$: $4V_{DC}$: $16V_{DC}$: $64V_{DC}$: $256V_{DC}$ for $p = 3$ (i.e., the number of positive or negative levels in a single PUC inverter unit). In a single stage PUC, only 3^0 positive or negative levels are achieved. Thus, if the flying capacitance voltage is maintained at $\frac{1}{3}V_{DC}$, then the maximum number of voltage levels that can be achieved is 7. As noted above, the seven levels are V_{DC}, $\frac{1}{3}V_{DC}$, and $\frac{2}{3}V_{DC}$ in the positive half-cycle, and $-V_{DC}$, $-\frac{1}{3}V_{DC}$, and $-\frac{2}{3}V_{DC}$ in the negative half-cycle, along with the zero voltage level. This single stage PUC will switch at a relatively high switching frequency (about 2 to 10 kHz). However, as indicated below in Table 1, two cascaded PUC inverters will include one switching at high frequency (about 2 to 10 kHz) and the other switching at a lower frequency.

In the exemplary case of solar PV applications, the lower switching frequency inverter unit will switch at eight times the grid frequency (8 X 50 = 400 Hz). The second cascaded PUC stage will produce all of its seven levels with low frequency switching. The inverter, which operates at the higher frequency, should operate at low voltages and repeat all of its four levels (V_{DC}, $\frac{1}{3}V_{DC}$, $\frac{2}{3}V_{DC}$, 0) on every step of the low frequency inverter unit. Thus, overall, 31-levels can be achieved in two cascaded PUC inverters. Further, if three PUC modules are cascaded, then two modules at low voltage ($1V_{DC}$: $4V_{DC}$) will switch at a high frequency, and the third PUC inverter ($16V_{DC}$) will be at a low frequency. The number of voltage levels that can be achieved is increased to 127 in this case. In general, for *n* cascaded cells, or modules, the required DC bus voltages follow the progression $1: 4^1: 4^2: 4^3: 4^4: \ldots : 4^n$. Here, the respective maximum achievable voltage levels, *L*, is given by $L = 2 \times 4^n - 1$.

When two units are cascaded, superimposing the seven levels of one inverter on the seven levels of another cascaded unit, the number of output voltage level can be increased to 49. The inverter operating at high frequency should then operate at low voltages and repeat all seven levels (V_{DC}, $\frac{1}{3}V_{DC}$, $\frac{2}{3}V_{DC}$, 0, $-V_{DC}$, $-\frac{1}{3}V_{DC}$, $-\frac{2}{3}V_{DC}$) on every step of the low frequency inverter unit. Thus, 49 overall levels can be achieved with two cascaded PUC inverters. Furthermore, if three PUC modules are cascaded, two modules which are at low voltages ($1V_{DC}$:$7V_{DC}$) will switch at high frequencies at 960 Hz and 700 Hz, respectively,

and the third ($49V_{DC}$) will be at a low frequency of 350 Hz. The number of voltage levels achieved is drastically increased to 343. The generalized formula for cascading n modules at the required DC bus voltages is $1: 7^1: 7^2: 7^3: 7^4: \ldots : 7^n$ and the respective maximum achievable voltage levels L is then $L = 7^n$.

If the ratio of V_{DC1} and V_{DC2} is increased further, the number of levels can be further increased, however, the step size of the level will not be uniform. Thus, it is preferred to keep the ratio to 1:4 or 4:1, where the output number of levels is 31 (in the case of two units of cascading PUC inverters). Fig. 4 shows two such PUC inverters 12, 14 cascaded and connected across the common load.

Table 1: Possible Switching Combinations For 31 Level Output

Level	Inverter 1 (V_{DC1})			Inverter 1 Output	Inverter 2 (V_{DC2})			Inverter 2 Output	Inverter Output
	S1	S2	S3		S4	S5	S6		
1	1	0	0	V_{DC1}	1	0	0	V_{DC2}	$V_{DC1} + V_{DC2}$
2	1	0	1	$\frac{2}{3}V_{DC1}$	1	0	0	V_{DC2}	$\frac{2}{3}V_{DC1} + V_{DC2}$
3	1	1	0	$\frac{1}{3}V_{DC1}$	1	0	0	V_{DC2}	$\frac{1}{3}V_{DC1} + V_{DC2}$
4	1	1	1	0	1	0	0	V_{DC2}	V_{DC2}
5	1	0	0	V_{DC1}	1	0	1	$\frac{2}{3}V_{DC2}$	$V_{DC1} + \frac{2}{3}V_{DC2}$
6	1	0	1	$\frac{2}{3}V_{DC1}$	1	0	1	$\frac{2}{3}V_{DC2}$	$\frac{2}{3}V_{DC1} + \frac{2}{3}V_{DC2}$
7	1	1	0	$\frac{1}{3}V_{DC1}$	1	0	1	$\frac{2}{3}V_{DC2}$	$\frac{1}{3}V_{DC1} + \frac{2}{3}V_{DC2}$
8	1	1	1	0	1	0	1	$\frac{2}{3}V_{DC2}$	$\frac{2}{3}V_{DC2}$
9	1	0	0	V_{DC1}	1	1	0	$\frac{1}{3}V_{DC2}$	$V_{DC1} + \frac{1}{3}V_{DC2}$
10	1	0	1	$\frac{2}{3}V_{DC1}$	1	1	0	$\frac{1}{3}V_{DC2}$	$\frac{2}{3}V_{DC1} + \frac{1}{3}V_{DC2}$
11	1	1	0	$\frac{1}{3}V_{DC1}$	1	1	0	$\frac{1}{3}V_{DC2}$	$\frac{1}{3}V_{DC1} + \frac{1}{3}V_{DC2}$
12	1	1	1	0	1	1	0	$\frac{1}{3}V_{DC2}$	$\frac{1}{3}V_{DC2}$
13	1	0	0	V_{DC1}	1	1	1	0	V_{DC1}
14	1	0	1	$\frac{2}{3}V_{DC1}$	1	1	1	0	$\frac{2}{3}V_{DC1}$
15	1	1	0	$\frac{1}{3}V_{DC1}$	1	1	1	0	$\frac{1}{3}V_{DC1}$
16	1	1	1	0	1	1	1	0	0
16	0	0	0	0	0	0	0	0	0

17	0	0	1	$-\frac{1}{3}V_{DC1}$	0	0	0	0	$-\frac{1}{3}V_{DC1}$
18	0	1	0	$-\frac{2}{3}V_{DC1}$	0	0	0	0	$-\frac{2}{3}V_{DC1}$
19	0	1	1	$-V_{DC1}$	0	0	0	0	$-V_{DC1}$
20	0	0	0	0	0	0	1	$-\frac{1}{3}V_{DC2}$	$-\frac{1}{3}V_{DC2}$
21	0	0	1	$-\frac{1}{3}V_{DC1}$	0	0	1	$-\frac{1}{3}V_{DC2}$	$-\frac{1}{3}V_{DC1}-\frac{1}{3}V_{DC2}$
22	0	1	0	$-\frac{2}{3}V_{DC1}$	0	0	1	$-\frac{1}{3}V_{DC2}$	$-\frac{2}{3}V_{DC1}-\frac{1}{3}V_{DC2}$
23	0	1	1	$-V_{DC1}$	0	0	1	$-\frac{1}{3}V_{DC2}$	$-V_{DC1}-\frac{1}{3}V_{DC2}$
24	0	0	0	0	0	1	0	$-\frac{2}{3}V_{DC2}$	$-\frac{2}{3}V_{DC2}$
25	0	0	1	$-\frac{1}{3}V_{DC1}$	0	1	0	$-\frac{2}{3}V_{DC2}$	$-\frac{1}{3}V_{DC1}-\frac{2}{3}V_{DC2}$
26	0	1	0	$-\frac{2}{3}V_{DC1}$	0	1	0	$-\frac{2}{3}V_{DC2}$	$-\frac{2}{3}V_{DC1}-\frac{2}{3}V_{DC2}$
27	0	1	1	$-V_{DC1}$	0	1	0	$-\frac{2}{3}V_{DC2}$	$-V_{DC1}-\frac{2}{3}V_{DC2}$
28	0	0	0	0	0	1	1	$-V_{DC2}$	$-V_{DC2}$
29	0	0	1	$-\frac{1}{3}V_{DC1}$	0	1	1	$-V_{DC2}$	$-\frac{1}{3}V_{DC1}-V_{DC2}$
30	0	1	0	$-\frac{2}{3}V_{DC1}$	0	1	1	$-V_{DC2}$	$-\frac{2}{3}V_{DC1}-V_{DC2}$
31	0	1	1	$-V_{DC1}$	0	1	1	$-V_{DC2}$	$-V_{DC1}-V_{DC2}$

It can be seen in Table 1 above that fifteen positive levels and fifteen negative levels are generated, while two states are shown with zero voltage (i.e., State 16). The zero state has one degree of redundancy. The switching diagram for half of the switching period is shown in Figs. 5A and 5B. It should be noted that the switching frequency of each switch are unique. With regard to the first inverter (Fig. 5A), the switching frequency of switches S2, S2' is 14 times higher than that of switches S1, S1'. The switching frequency of switches S3, S3' is 28 times higher than that of switches S1, S1'. The top two switches in the configuration of Fig. 4 do not switch in half of the switching period, while the middle two switches make seven switching transitions (i.e., on and off), and the bottom two switches make 14 switching transitions in the same half switching period. With regard to Fig. 5B, it can be seen that the switching frequency of switches S5, S5' is twice the switching frequency of switches S4, S4'. The switching frequency of switches S6, S6' is three times that of

switches S4, S4'. The top two switches (S4, S4') do not switch in the half cycle, the middle switches (S5, S5') switch only once, and the bottom switches (S6, S6') switch three times.

When comparing the switching of the two cascaded inverters, it can be seen that the total number of switches in one switching period of inverter 1 is 44, while inverter 2 only switches 13 times in one switching period. It is important to note that the switching frequency of inverter 2 is significantly lower than that of inverter 1. This is a notable advantage since, for high power applications, inverter 2 can use gate turn-off thyristors (GTOs) or thyristors and, similarly, the top switches of inverter 1 can also be GTOs or thyristor.

The PUC inverter with the higher DC link voltage will be switched at the lower frequency in order to keep the switching losses to a minimum. Each of the PUC inverters can be controlled using simple multicarrier level shifted and/or phase shifted pulse width modulation (PWM) techniques. Standard available multicarrier PWM techniques can be employed, such as phase disposed (PD) PWM, alternative phase opposed disposed (APOD) PWM, or phase opposed disposed (POD) PWM.

Table 2: Possible Switching Combinations For 49 Level Output

Level	Inverter 1 (V_{DC1})			Inverter 1 Output	Inverter 2 (V_{DC2})			Inverter 2 Output	Inverter Output
	S1	S2	S3		S4	S5	S6		
1	1	0	0	V_{DC1}	1	0	0	V_{DC2}	$V_{DC1}+V_{DC2}$
2	1	0	1	$\frac{2}{3}V_{DC1}$	1	0	0	V_{DC2}	$\frac{2}{3}V_{DC1}+V_{DC2}$
3	1	1	0	$\frac{1}{3}V_{DC1}$	1	0	0	V_{DC2}	$\frac{1}{3}V_{DC1}+V_{DC2}$
4	1	1	1	0	1	0	0	V_{DC2}	V_{DC2}
4	0	0	0	0	1	0	0	V_{DC2}	V_{DC2}
5	0	0	1	$-\frac{1}{3}V_{DC1}$	1	0	0	V_{DC2}	$-\frac{1}{3}V_{DC1}+V_{DC2}$
6	0	1	0	$-\frac{2}{3}V_{DC1}$	1	0	0	V_{DC2}	$-\frac{2}{3}V_{DC1}+V_{DC2}$
7	0	1	1	$-V_{DC1}$	1	0	0	V_{DC2}	$-V_{DC1}+V_{DC2}$
8	1	0	0	V_{DC1}	1	0	1	$\frac{2}{3}V_{DC2}$	$V_{DC1}+\frac{2}{3}V_{DC2}$
9	1	0	1	$\frac{2}{3}V_{DC1}$	1	0	1	$\frac{2}{3}V_{DC2}$	$\frac{2}{3}V_{DC1}+\frac{2}{3}V_{DC2}$
10	1	1	0	$\frac{1}{3}V_{DC1}$	1	0	1	$\frac{2}{3}V_{DC2}$	$\frac{1}{3}V_{DC1}+\frac{2}{3}V_{DC2}$
11	1	1	1	0	1	0	1	$\frac{2}{3}V_{DC2}$	$\frac{2}{3}V_{DC2}$

11	0	0	0	0	1	0	1	$\frac{2}{3}V_{DC2}$	$\frac{2}{3}V_{DC2}$
12	0	0	1	$-\frac{1}{3}V_{DC1}$	1	0	1	$\frac{2}{3}V_{DC2}$	$-\frac{1}{3}V_{DC1}+\frac{2}{3}V_{DC2}$
13	0	1	0	$-\frac{2}{3}V_{DC1}$	1	0	1	$\frac{2}{3}V_{DC2}$	$-\frac{2}{3}V_{DC1}+\frac{2}{3}V_{DC2}$
14	0	1	1	$-V_{DC1}$	1	0	1	$\frac{2}{3}V_{DC2}$	$-V_{DC1}+\frac{2}{3}V_{DC2}$
15	1	0	0	V_{DC1}	1	1	0	$\frac{1}{3}V_{DC2}$	$V_{DC1}+\frac{1}{3}V_{DC2}$
16	1	0	1	$\frac{2}{3}V_{DC1}$	1	1	0	$\frac{1}{3}V_{DC2}$	$\frac{2}{3}V_{DC1}+\frac{1}{3}V_{DC2}$
17	1	1	0	$\frac{1}{3}V_{DC1}$	1	1	0	$\frac{1}{3}V_{DC2}$	$\frac{1}{3}V_{DC1}+\frac{1}{3}V_{DC2}$
18	1	1	1	0	1	1	0	$\frac{1}{3}V_{DC2}$	$\frac{1}{3}V_{DC2}$
18	0	0	0	0	1	1	0	$\frac{1}{3}V_{DC2}$	$\frac{1}{3}V_{DC1}$
19	0	0	1	$-\frac{1}{3}V_{DC1}$	1	1	0	$\frac{1}{3}V_{DC2}$	$-\frac{1}{3}V_{DC1}+\frac{1}{3}V_{DC2}$
20	0	1	0	$-\frac{2}{3}V_{DC1}$	1	1	0	$\frac{1}{3}V_{DC2}$	$-\frac{2}{3}V_{DC1}+\frac{1}{3}V_{DC2}$
21	0	1	1	$-V_{DC1}$	1	1	0	$\frac{1}{3}V_{DC2}$	$-V_{DC1}+\frac{1}{3}V_{DC2}$
22	1	0	0	V_{DC1}	1	1	1	0	V_{DC1}
23	1	0	1	$\frac{2}{3}V_{DC1}$	1	1	1	0	$\frac{2}{3}V_{DC1}$
24	1	1	0	$\frac{1}{3}V_{DC1}$	1	1	1	0	$\frac{1}{3}V_{DC1}$
25	1	1	1	0	1	1	1	0	0
25	0	0	0	0	0	0	0	0	0
26	0	0	1	$-\frac{1}{3}V_{DC1}$	0	0	0	0	$-\frac{1}{3}V_{DC1}$
27	0	1	0	$-\frac{2}{3}V_{DC1}$	0	0	0	0	$-\frac{2}{3}V_{DC1}$
28	0	1	1	$-V_{DC1}$	0	0	0	0	$-V_{DC1}$
29	1	0	0	V_{DC1}	0	0	1	$-\frac{1}{3}V_{DC2}$	$V_{DC1}-\frac{1}{3}V_{DC2}$
30	1	0	1	$\frac{2}{3}V_{DC1}$	0	0	1	$-\frac{1}{3}V_{DC2}$	$\frac{2}{3}V_{DC1}-\frac{1}{3}V_{DC2}$
31	1	1	0	$\frac{1}{3}V_{DC1}$	0	0	1	$-\frac{1}{3}V_{DC2}$	$\frac{1}{3}V_{DC1}-\frac{1}{3}V_{DC2}$
32	1	1	1	0	0	0	1	$-\frac{1}{3}V_{DC2}$	$-\frac{1}{3}V_{DC2}$
32	0	0	0	0	0	0	1	$-\frac{1}{3}V_{DC2}$	$-\frac{1}{3}V_{DC2}$

33	0	0	1	$-\frac{1}{3}V_{DC1}$	0	0	1	$-\frac{1}{3}V_{DC2}$	$-\frac{1}{3}V_{DC1}-\frac{1}{3}V_{DC2}$
34	0	1	0	$-\frac{2}{3}V_{DC1}$	0	0	1	$-\frac{1}{3}V_{DC2}$	$-\frac{2}{3}V_{DC1}-\frac{1}{3}V_{DC2}$
35	0	1	1	$-V_{DC1}$	0	0	1	$-\frac{1}{3}V_{DC2}$	$-V_{DC1}-\frac{1}{3}V_{DC2}$
36	1	0	0	V_{DC1}	0	1	0	$-\frac{2}{3}V_{DC2}$	$V_{DC1}-\frac{2}{3}V_{DC2}$
37	1	0	1	$\frac{2}{3}V_{DC1}$	0	1	0	$-\frac{2}{3}V_{DC2}$	$\frac{2}{3}V_{DC1}-\frac{2}{3}V_{DC2}$
38	1	1	0	$\frac{1}{3}V_{DC1}$	0	1	0	$-\frac{2}{3}V_{DC2}$	$\frac{1}{3}V_{DC1}-\frac{2}{3}V_{DC2}$
39	1	1	1	0	0	1	0	$-\frac{2}{3}V_{DC2}$	$-\frac{2}{3}V_{DC2}$
40	0	0	1	0	0	1	0	$-\frac{2}{3}V_{DC2}$	$-\frac{2}{3}V_{DC2}$
41	0	1	0	$-\frac{2}{3}V_{DC1}$	0	1	0	$-\frac{2}{3}V_{DC2}$	$-\frac{2}{3}V_{DC1}-\frac{2}{3}V_{DC2}$
42	0	1	1	$-V_{DC1}$	0	1	0	$-\frac{2}{3}V_{DC2}$	$-V_{DC1}-\frac{2}{3}V_{DC2}$
43	1	0	0	V_{DC1}	0	1	0	$-V_{DC2}$	$V_{DC1}-V_{DC2}$
44	1	0	1	$\frac{2}{3}V_{DC1}$	0	1	1	$-V_{DC2}$	$\frac{2}{3}V_{DC1}-V_{DC2}$
45	1	1	0	$\frac{1}{3}V_{DC1}$	0	1	1	$-V_{DC2}$	$\frac{1}{3}V_{DC1}-V_{DC2}$
46	1	1	1	0	0	1	1	$-V_{DC2}$	$-V_{DC2}$
46	0	0	0	0	0	1	1	$-V_{DC2}$	$-V_{DC2}$
47	0	0	1	$-\frac{1}{3}V_{DC1}$	0	1	1	$-V_{DC2}$	$-\frac{1}{3}V_{DC1}-V_{DC2}$
48	0	1	0	$-\frac{2}{3}V_{DC1}$	0	1	1	$-V_{DC2}$	$-\frac{2}{3}V_{DC1}-V_{DC2}$
49	0	1	1	$-V_{DC1}$	0	1	1	$-V_{DC2}$	$-V_{DC1}-V_{DC2}$

It can be seen in Table 2 above that 24 positive levels and 24 negative levels are created (for the 49 level case), while two states are shown for zero voltage (state 16). The zero state has one degree of redundancy and six states each have one degree of redundancy.

The results below are shown for a case based on the PD PWM technique for both PUC inverters. In order to clamp the capacitor voltage to one-third of their respective DC links, a closed-loop control is adopted. Referring to overall system 50 of Fig. 6, five voltage sensors one current sensor are employed. The voltage sensors sense the two DC link voltages and the two flying capacitor voltages across the capacitors. One AC voltage sensor is used to sense the magnitude and frequency of the grid/load voltage in order to synchronize the generated voltage. A current sensor is used to sense the load current used in the current

control loop. The control code can be operated on a control platform, such as a digital signal processor (DSP), a microcontroller, exemplary field-programmable gate array (FPGA) 36 or the like. The FPGA 36 or the like may be linked to a hosting computer, such as personal computer 30 or the like, allowing the control code to be written in an appropriate coding language, such as C/C++, Matlab/Simulink, VHSIC hardware description language (VHDL) or the like. FPGA 36 generates appropriate gating signals that are fed to a gate driver circuit 38. The gate drive circuit 38 then switches the power converters 12, 14 accordingly. Feedback is fed back into FPGA 36 by analog-digital (A/D) converters 32, 34 or the like.

In the control system shown in Fig. 7, in either grid-connected, off-grid or electric drive systems, the power converter 10 has to control the power injection such as, for example, reactive control and real power control. In order to achieve this, the converter is modeled in the dq-plane, and then a suitable controller is designed for tracking the reference. The control objectives are balancing the flying capacitor voltage (i.e., holding at one-third of the DC link, as indicated at 60 and 62 in Fig. 7) and controlling load or grid current to be sinusoidal.

The controller compensates the flying capacitor voltage with the inverter current. This is achieved by proportional integral (PI) controllers 64, 66, which minimize the constant error between the reference and the actual signals. Since there are two cascaded AFLC/PUC modules, both flying capacitor voltages will charge and discharge with the same load or grid current. Thus, the error signals of both modules are added to get the desired current reference error signal. To have control over the reactive and real power, control is required for the phase angle between the output voltage and current. This is performed by first sensing the voltage signal and generating a unit synchronizing vector (performed by unit synchronizer 68 in Fig. 7), and then, for a lagging reactive power delay, the unit synchronizing vector is set between 0° and 90°. Next, for a leading reactive power delay, the unit synchronizing vector is set between 180° and 270°. However, here, only unity power is selected, leading to the current reference error signal being further multiplied by the unit synchronizing vector to get the actual current reference (shown at 70 in Fig. 7). This is compared with the actual sensed signal (at 72 in Fig. 7) and this final error is minimized by PI controller 74. PI controller 74 is responsible for system dynamic response and stability in loaded conditions, since it directly affects load current.

The controller is designed for $\omega = 10$ rad/sec and $\varepsilon = 1$ (i.e., critically damped). For this value of ε, the equivalent value of phase margin is 75°. For determining the values of K_p and K_i, the open loop transfer function of the system is first written and then the gain and

phase margin conditions are applied (indicated at 76 in Fig. 7). The transfer function of the system is given by:

$$G_1(s) = \left(K_{p1} + \frac{K_{i1}}{s}\right) \times \left(\frac{1}{sC_1}\right) \quad (1)$$

$$G_2(s) = \left(K_{p2} + \frac{K_{i2}}{s}\right) \times \left(\frac{1}{sC_2}\right) \quad (2)$$

$$G_3(s) = \left(K_{p3} + \frac{K_{i3}}{s}\right) \times \left(\frac{1}{R+sL}\right), \quad (3)$$

where C_1 is the capacitance of the flying capacitor of the first module 78, C_2 is the capacitance of the flying capacitor of the second module 80, R is the load resistance, and L is the load inductance.

For purposes of comparison, Fig. 8 illustrates a prior art 31-level PUC 200. The prior art 31-level PUC 200 includes three U-cells 202, 204, 206 connected across load 220. As shown, two additional flying capacitors must be added to the 7-level PUC in order to achieve 31-levels. Thus, for 31-level PUC 200, there are a total of four capacitors used for one DC link, along with three flying capacitors 208, 210, 212, and the total number of power switching devices is ten. By comparison, the present cascaded packed U-cell multilevel inverter 10 utilizes four capacitors, two DC links, two flying capacitors, and the total number of power switching devices is twelve. 31-level PUC 200 has a control which is highly complex when compared to that of cascaded packed U-cell multilevel inverter 10. Additionally, 31-level PUC 200 requires four PI controllers and their tuning will be relatively difficult. If any of the four PI controllers does not function properly, it will be extremely difficult to debug the control system. Further, the switching frequency will necessarily be much higher than that of the present cascaded packed U-cell multilevel inverter 10.

Cascaded packed U-cell multilevel inverter 10 was simulated using Matlab/Simulink. In the simulation, the first link voltage was 60 V, the second link voltage was 240 V, the first DC link capacitor value was 4700 µF, the second DC link capacitor value was 4700 µF, the first flying capacitor value was 2200 µF, the second flying capacitor value was 2200 µF, the load parameters were 100 Ω and 200 µH, and the switching frequency was 2 KHz. The simulation results are presented in Figs. 9A-9D and Figs. 10A-10D. Successful cascading can be clearly seen with a 31-level voltage output. It can be further seen that one unit is operating at a higher switching frequency than the other. The low switching frequency inverter is supplied with a higher DC link voltage, i.e., four times higher than the high frequency switched inverter unit. The flying capacitor voltages are seen to be perfectly balanced at one-third of their respective DC link voltages. The output voltages are also

shown for different DC link voltage ratios, including 1:1, 1:2 and 1:3. The harmonic spectrum of the output 31-level voltage is shown in Fig. 10A, which is clearly shown to be a clean waveform without any harmonic components.

An experimental cascaded packed U-cell multilevel inverter according to the present invention was also constructed. The first link voltage was 16 V, the second link voltage was 64 V, the first flying capacitor voltage was 5.33 V, the second flying capacitor voltage was 21.33 V, the first flying capacitor value was 2.2 mF, the second flying capacitor value was 2.2 mF, the load parameters were 10 Ω and 25 mH, and the switching frequency was 2 KHz. The experimental results are shown in Figs. 11A-11F, Figs. 12A and 12B, and Figs.13A-13D. It can be clearly seen that the output voltage formed by cascading of the two PUC units achieves the desired 31 levels. The flying capacitor DC voltages are fixed at one-third of their respective DC link voltages. The load voltage and currents are perfectly sinusoidal. The individual outputs of the two PUCs are shown with a higher switching frequency, while the other is shown at a very low switching frequency. The voltage across each pair of IGBT switches is also shown. It is clearly seen that the six pairs of power switches have different switching frequencies. The spectrum of load voltage and load current shown in Figs. 12A and 12B shows a very low total harmonic distortion (THD) recorded for both voltage and current.

An experimental cascaded packed U-cell multilevel inverter according to the present invention was also constructed for a 49 level output; i.e., a DC link voltage ratio of 1:7. In this 49 level output case, the first link voltage was 15 V, the second link voltage was 105 V, the first flying capacitor voltage was 5.0 V, the second flying capacitor voltage was 35.0 V, the first flying capacitor value was 2.2 mF, the second flying capacitor value was 2.2 mF, the load parameters were 10 Ω and 0.78 mH, and the switching frequency was 1 KHz. The experimental results are shown in Figs. 14A-14G, Figs. 15A and 15B, and Figs.16A-16D. It can be seen that the output voltage is formed by cascading of the two units to achieve the 49 level output. The capacitor DC voltages are fixed at one-third of their respective DC link voltages. The load voltage and currents are perfectly sinusoidal. The individual outputs of the two PUCs can be seen to have a higher switching frequency, while the other is at a very low switching frequency. The voltage across each pair of IGBTs is also shown. Here, it can be seen that the six pairs of power switches have different switching frequencies. With regard to the inverter terminal voltage and grid/load voltage illustrated in Fig. 14G, it can be seen that the overall load of the cascaded packed U-cell multilevel inverter is relatively small.

The spectra of the load voltage and the load current are shown in Figs. 15A and 15B, respectively. A very low THD was recorded for both voltage and current, as shown. Specifically, Fig. 15A shows the results of the harmonic analysis of the load current with only a 0.8% THD, and Fig. 15B shows the results of the harmonic analysis of the terminal voltage at only 2.4% THD. Fig. 16A shows the output voltages for a DC link voltage ratio of 1:7. Fig. 16B shows a magnified view of the output's positive cycle for the 49 level output. Fig. 16C shows the output voltages for a DC link voltage ratio of 1:6 (i.e., a 43 level output), and Fig. 16D shows the output voltages for a DC link voltage ratio of 1:5 (i.e., a 37 level output).

It is to be understood that the present invention is not limited to the embodiments described above, but encompasses any and all embodiments within the scope of the following claims.

CLAIMS

We claim:

1. A cascaded packed U-cell multilevel inverter, comprising:

a first packed U-cell multilevel inverter; and

at least one sequential packed U-cell multilevel inverter connected in cascade to the first packed U-cell multilevel inverter.

2. The cascaded packed U-cell multilevel inverter as recited in claim 1, wherein said at least one sequential packed U-cell multilevel inverter consists of a single second packed U-cell multilevel inverter.

3. The cascaded packed U-cell multilevel inverter as recited in claim 2, wherein both the first packed U-cell multilevel inverter and the second packed U-cell multilevel inverter are 7-level inverters.

4. The cascaded packed U-cell multilevel inverter as recited in claim 3, wherein both the first packed U-cell multilevel inverter and the second packed U-cell multilevel inverter comprise a DC link capacitor adapted for connection to separate, independent DC power sources.

5. The cascaded packed U-cell multilevel inverter as recited in claim 4, wherein both the first packed U-cell multilevel inverter and the second packed U-cell multilevel inverter comprise a flying capacitor clamping the multilevel inverter to one-third of the voltage of the corresponding power source.

6. The cascaded packed U-cell multilevel inverter as recited in claim 5, wherein the voltage developed over the DC link capacitors for the first packed U-cell multilevel inverter and the second packed U-cell multilevel inverter have a voltage ratio of 4:1, whereby thirty-one output voltage levels are selectively obtained.

7. The cascaded packed U-cell multilevel inverter as recited in claim 6, wherein each of the first and second packed U-cell multilevel inverters further comprise three pairs of power switches.

8. A cascaded packed U-cell multilevel inverter, comprising:

a first packed U-cell multilevel inverter; and

a second packed U-cell multilevel inverter connected in cascade to the first packed U-cell multilevel inverter, wherein each of said first and second packed U-cell multilevel inverters are 7-level inverters comprising a DC link capacitor adapted for connection to a unique independent DC power source, a flying capacitor clamping the respective packed U-cell multilevel inverter to one-third of the voltage of the corresponding DC power source, and three pairs of power switches.

9. The cascaded packed U-cell multilevel inverter as recited in claim 8, wherein the voltage developed over the DC link capacitors for the first packed U-cell multilevel inverter and the second packed U-cell multilevel inverter have a voltage ratio of 4:1, whereby thirty-one output voltage levels are selectively obtained.

10. The cascaded packed U-cell multilevel inverter as recited in claim 8, wherein the voltage developed over the DC link capacitors for the first packed U-cell multilevel inverter and the second packed U-cell multilevel inverter have a voltage ratio of 7:1, whereby 49 output voltage levels are selectively obtained.

11. The cascaded packed U-cell multilevel inverter as recited in claim 8, further comprising a third packed U-cell multilevel inverter connected in cascade to the first and second packed U-cell multilevel inverters, whereby 343 output voltage levels are selectively obtained.

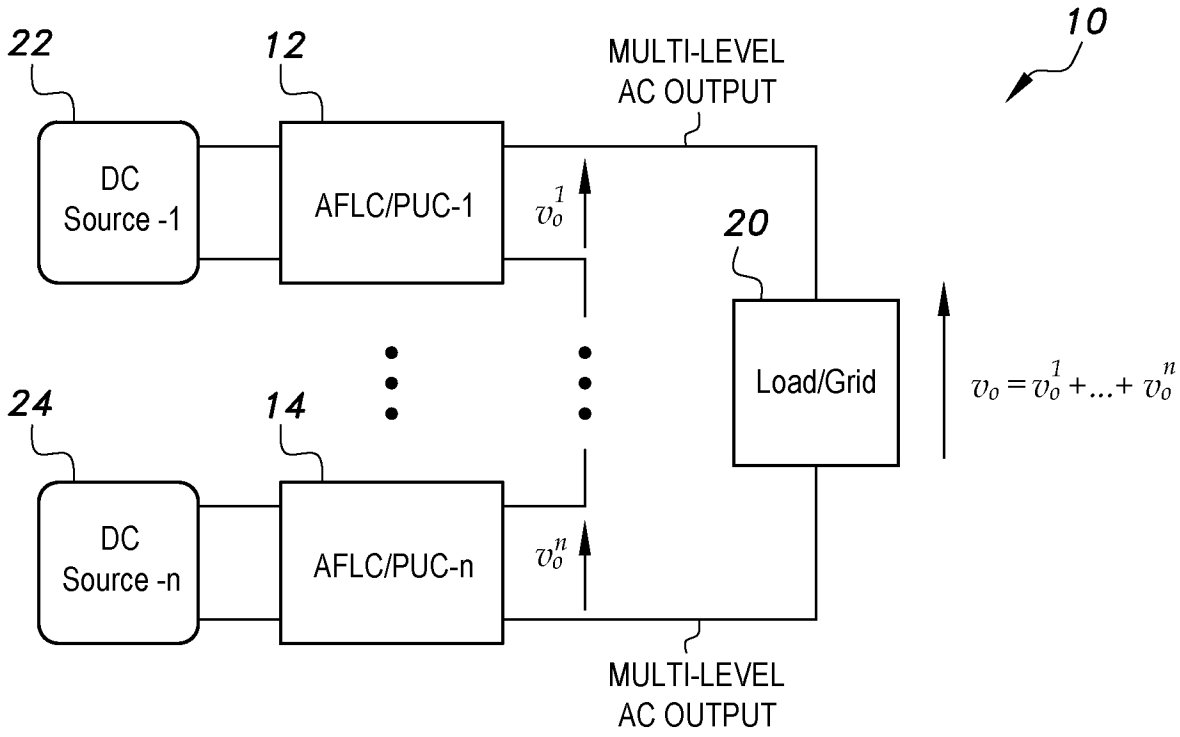

10
22
12
MULTI-LEVEL
AC OUTPUT
DC
Source -1
AFLC/PUC-1
v_o^1
20
Load/Grid
$v_o = v_o^1 + ... + v_o^n$
24
14
DC
Source -n
AFLC/PUC-n
v_o^n
MULTI-LEVEL
AC OUTPUT

FIG. 1

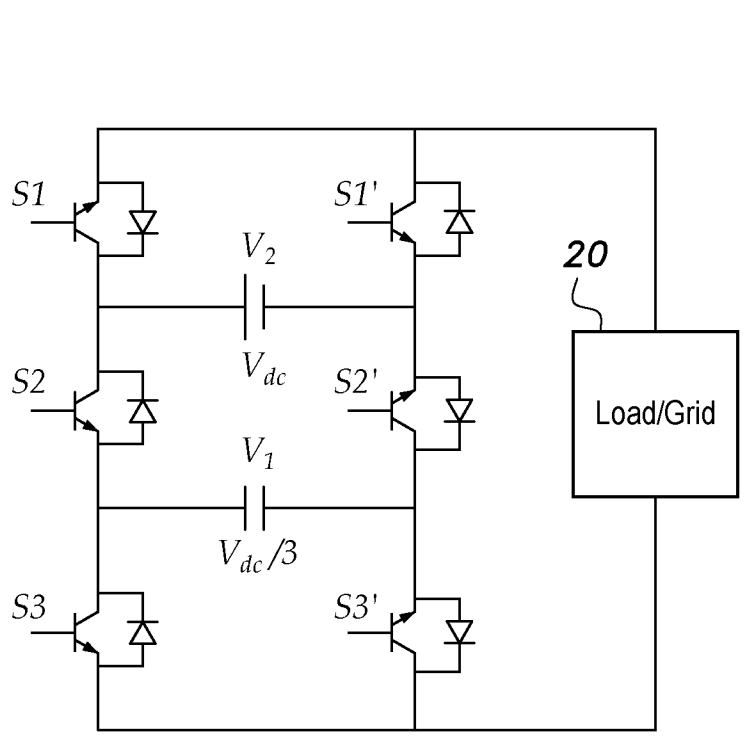

16
S1
S1'
V_2
20
V_{dc}
S2
S2'
Load/Grid
V_1
$V_{dc}/3$
S3
S3'

FIG. 2

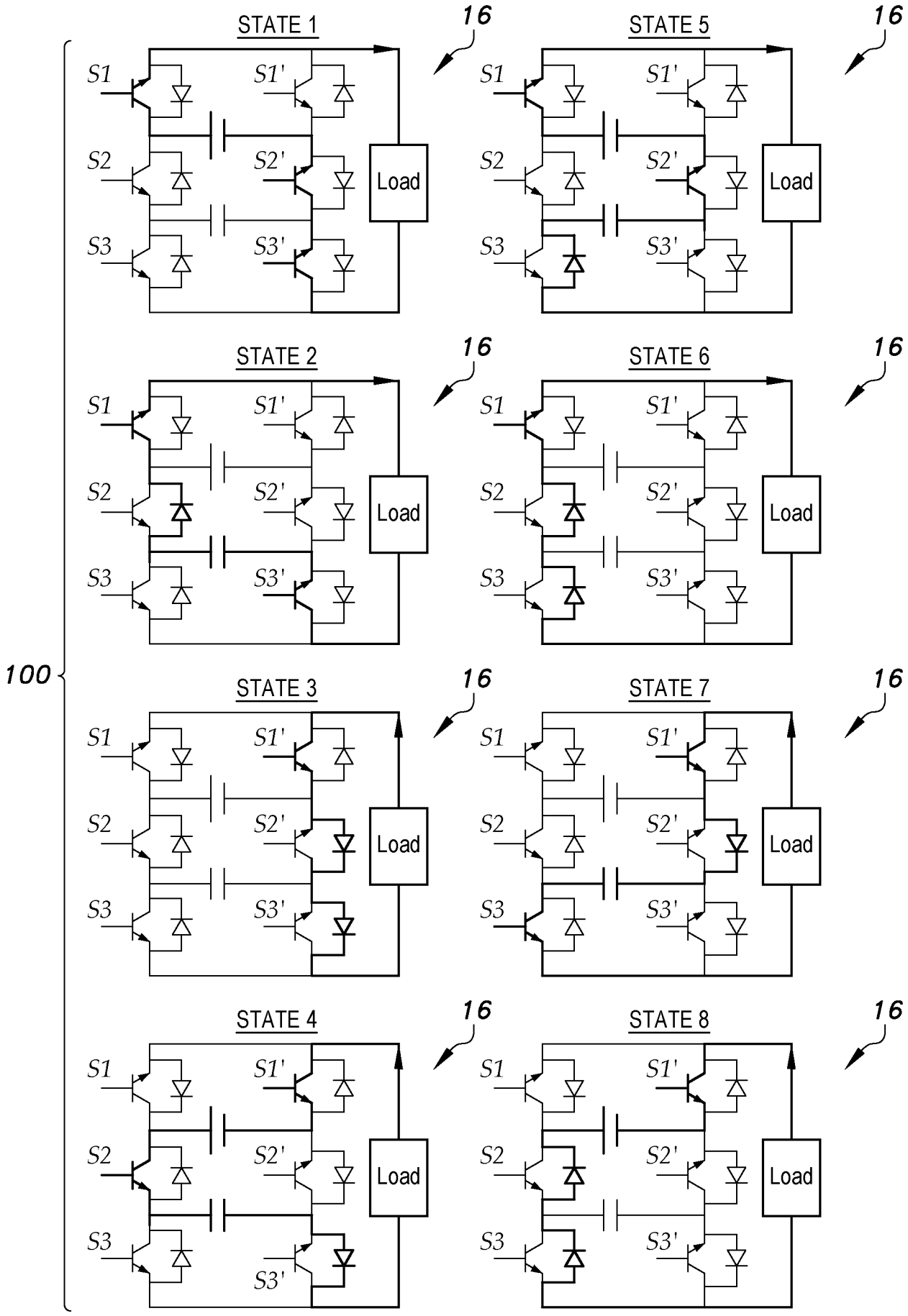

100
STATE 1
STATE 2
STATE 3
STATE 4
STATE 5
STATE 6
STATE 7
STATE 8
16
S1
S1'
S2
S2'
S3
S3'
Load

FIG. 3

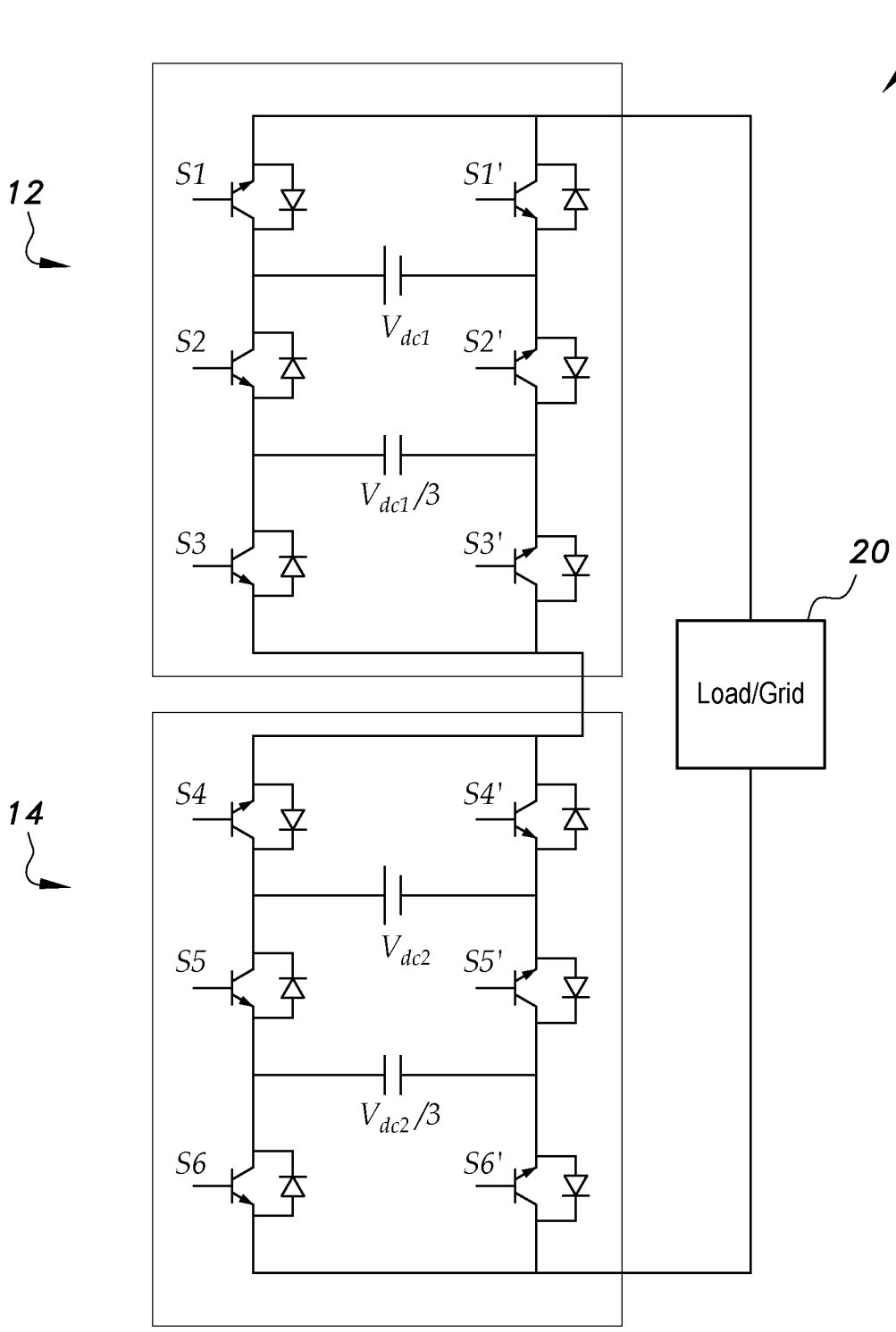

10
12
S1
S1'
S2
S2'
S3
S3'
V_{dc1}
$V_{dc1}/3$
20
Load/Grid
14
S4
S4'
S5
S5'
S6
S6'
V_{dc2}
$V_{dc2}/3$

FIG. 4

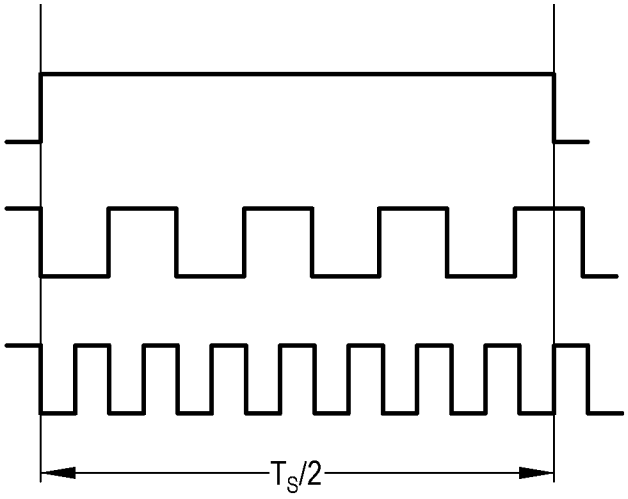


FIG. 5A

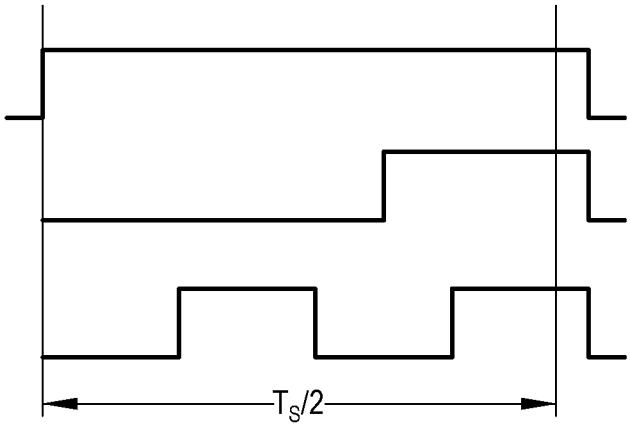


FIG. 5B

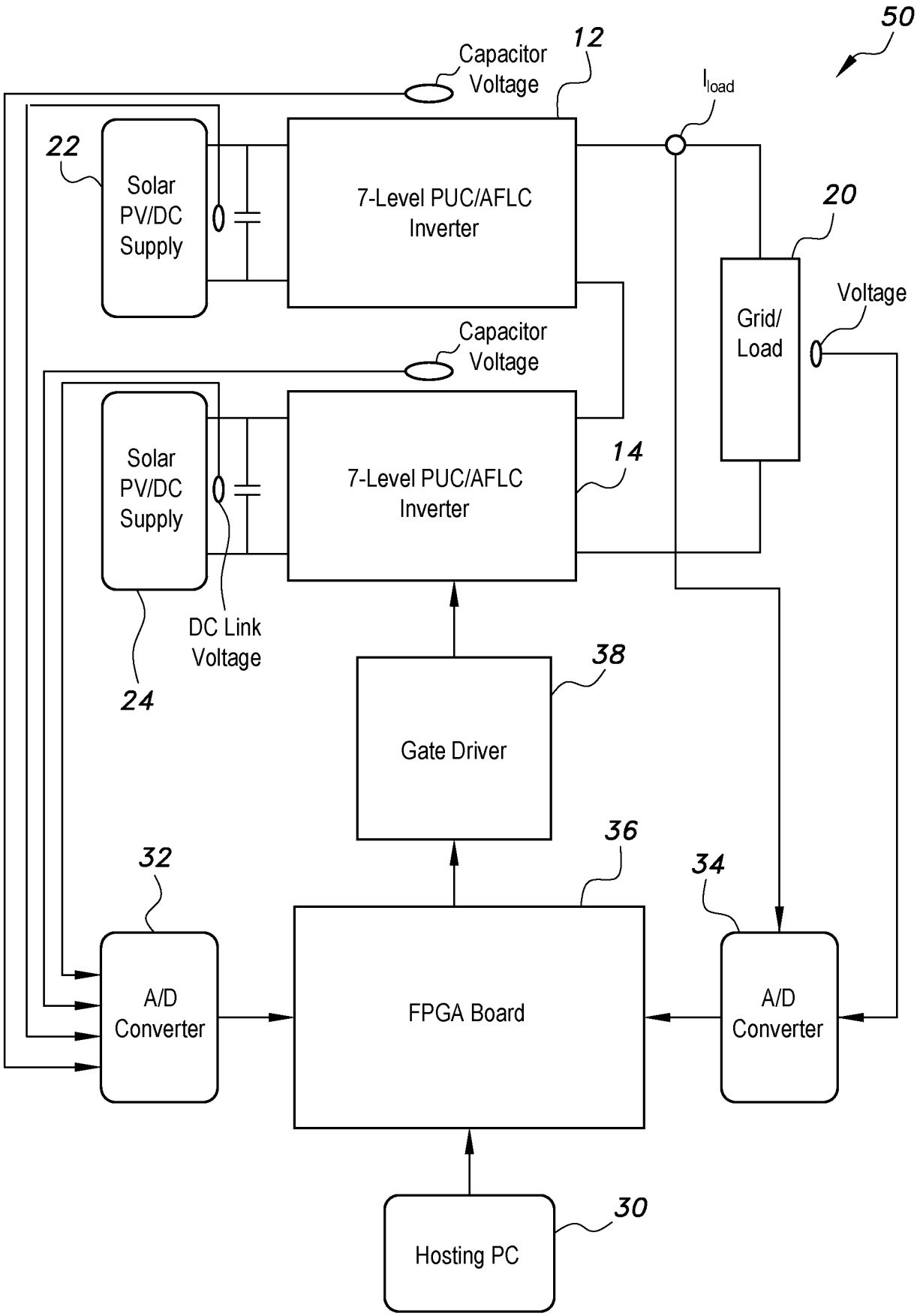

50
12
Capacitor Voltage
I_{load}
22
Solar PV/DC Supply
7-Level PUC/AFLC Inverter
20
Grid/ Load
Voltage
Capacitor Voltage
Solar PV/DC Supply
7-Level PUC/AFLC Inverter
14
DC Link Voltage
24
38
Gate Driver
36
32
34
A/D Converter
FPGA Board
A/D Converter
30
Hosting PC

FIG. 6

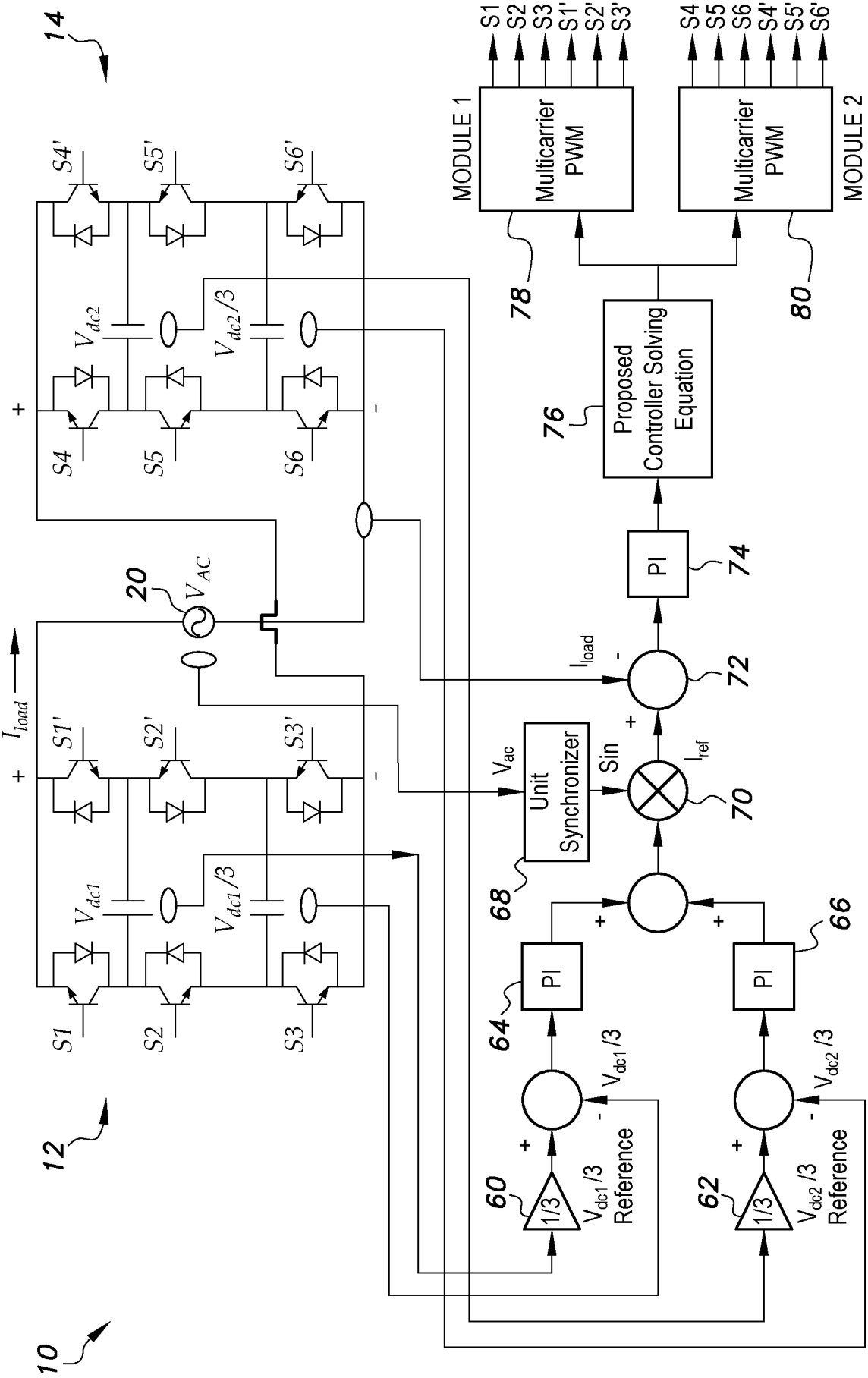
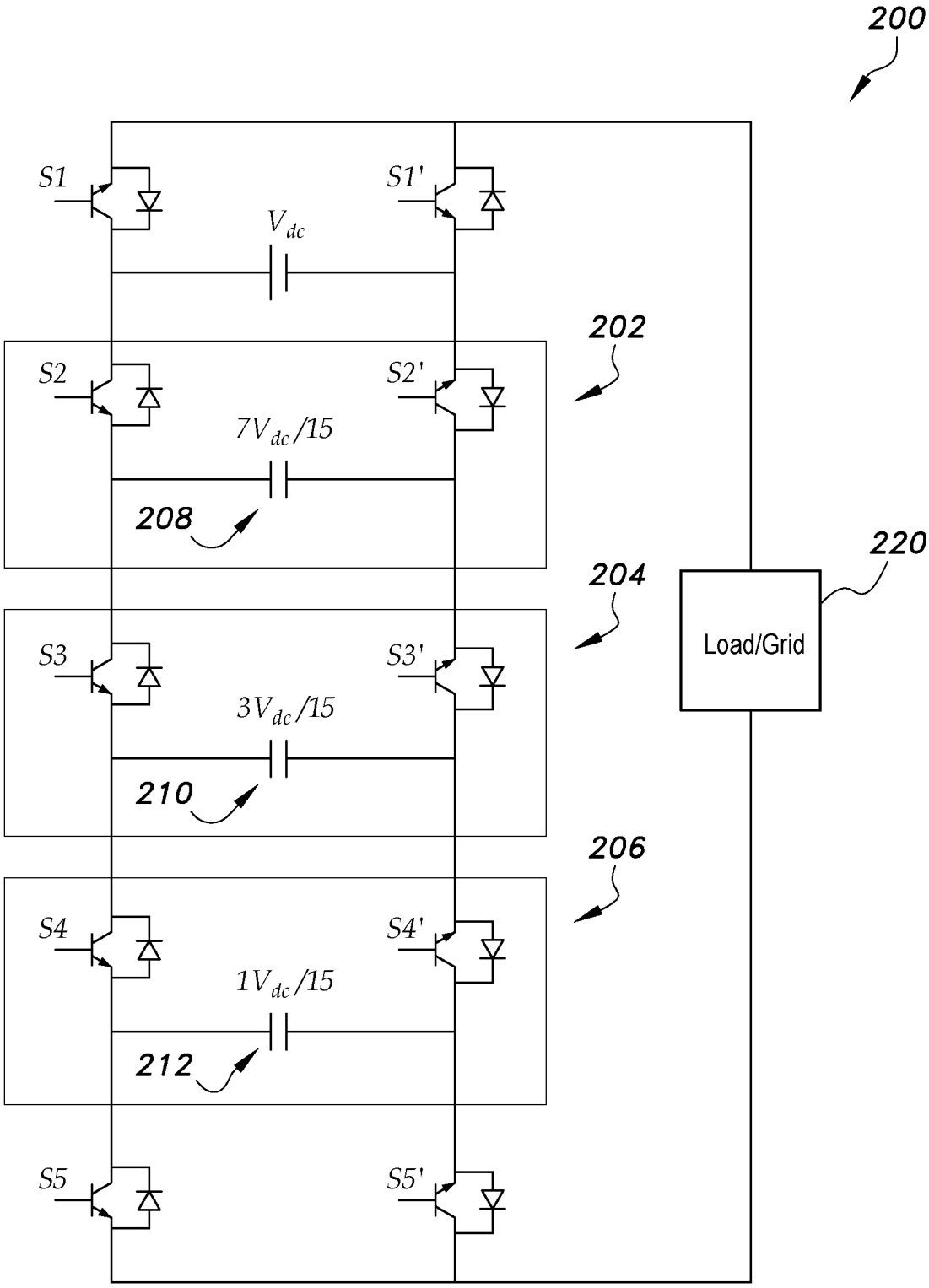

10
12
14
20
V_{AC}
I_{load}
V_{dc1}
V_{dc2}
$V_{dc1}/3$
$V_{dc2}/3$
S1
S2
S3
S4
S5
S6
S1'
S2'
S3'
S4'
S5'
S6'
MODULE 1
MODULE 2
Multicarrier PWM
Multicarrier PWM
78
80
Proposed Controller Solving Equation
76
PI
74
72
70
Unit Synchronizer
V_{ac}
Sin
I_{ref}
68
PI
64
PI
66
60
62
1/3
$V_{dc1}/3$ Reference
$V_{dc2}/3$ Reference

FIG. 7



PRIOR ART

FIG. 8

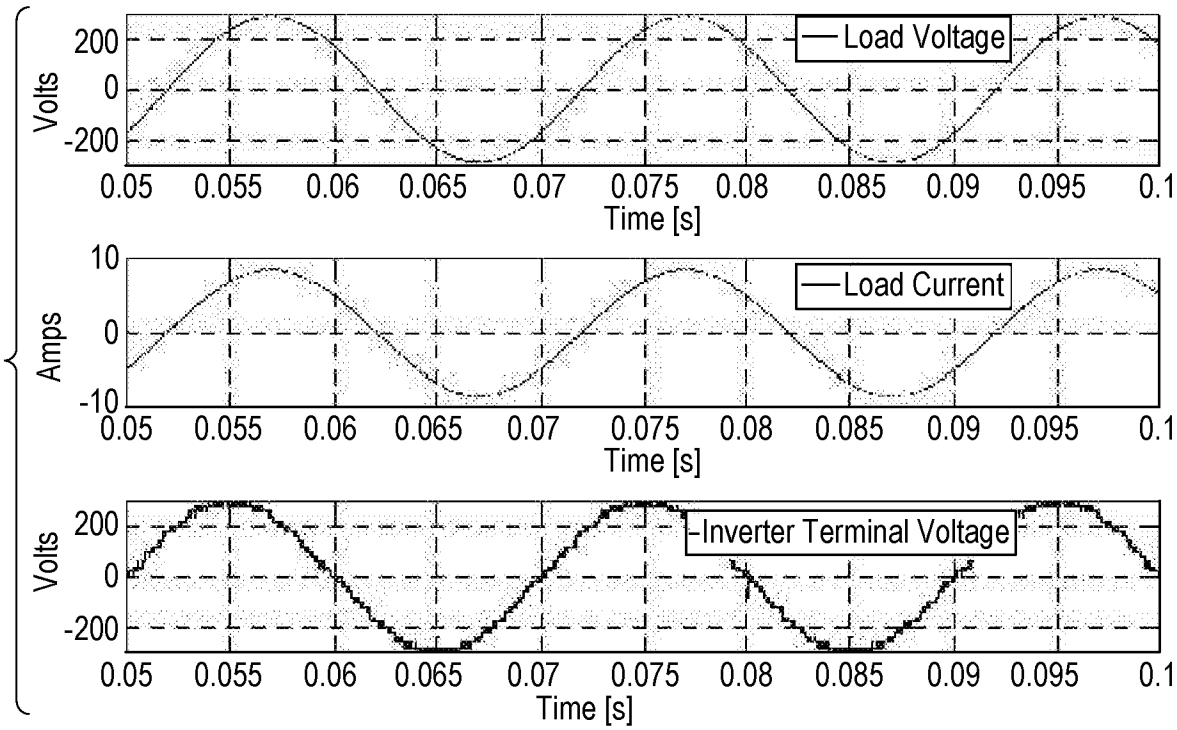

Load Voltage
Volts
200
0
-200
0.05 0.055 0.06 0.065 0.07 0.075 0.08 0.085 0.09 0.095 0.1
Time [s]
Load Current
Amps
10
0
-10
0.05 0.055 0.06 0.065 0.07 0.075 0.08 0.085 0.09 0.095 0.1
Time [s]
Inverter Terminal Voltage
Volts
200
0
-200
0.05 0.055 0.06 0.065 0.07 0.075 0.08 0.085 0.09 0.095 0.1
Time [s]

FIG. 9A

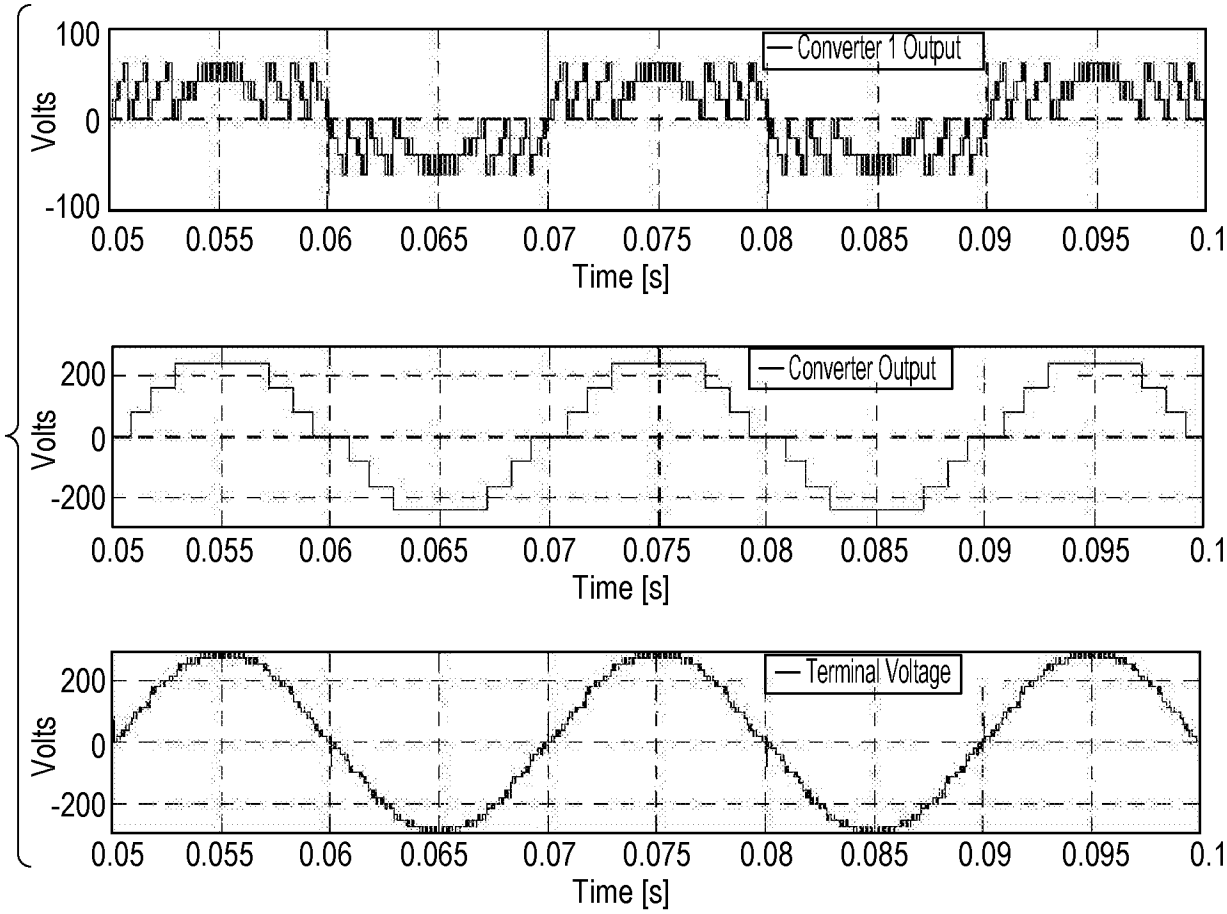

Converter 1 Output
Volts
100
0
-100
0.05 0.055 0.06 0.065 0.07 0.075 0.08 0.085 0.09 0.095 0.1
Time [s]
Converter Output
Volts
200
0
-200
0.05 0.055 0.06 0.065 0.07 0.075 0.08 0.085 0.09 0.095 0.1
Time [s]
Terminal Voltage
Volts
200
0
-200
0.05 0.055 0.06 0.065 0.07 0.075 0.08 0.085 0.09 0.095 0.1
Time [s]

FIG. 9B

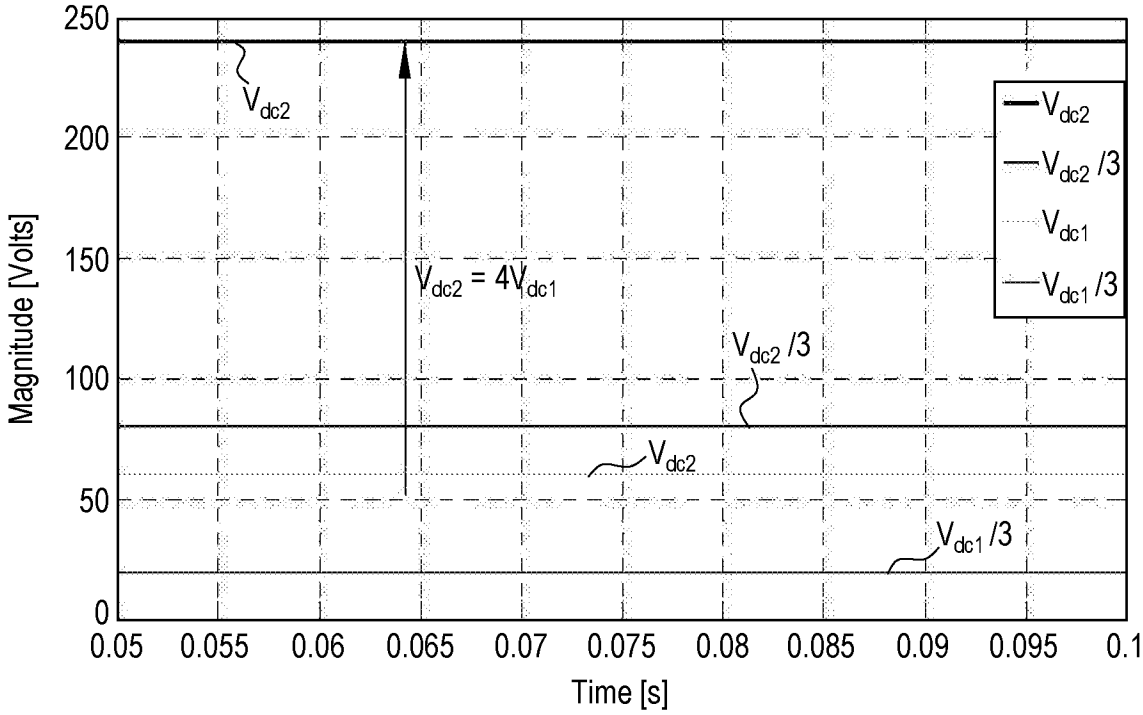

250
200
150
100
50
0
Magnitude [Volts]
0.05
0.055
0.06
0.065
0.07
0.075
0.08
0.085
0.09
0.095
0.1
Time [s]
V_{dc2}
$V_{dc2} = 4V_{dc1}$
V_{dc2} /3
V_{dc2}
V_{dc1} /3
V_{dc2}
V_{dc2} /3
V_{dc1}
V_{dc1} /3

FIG. 9C

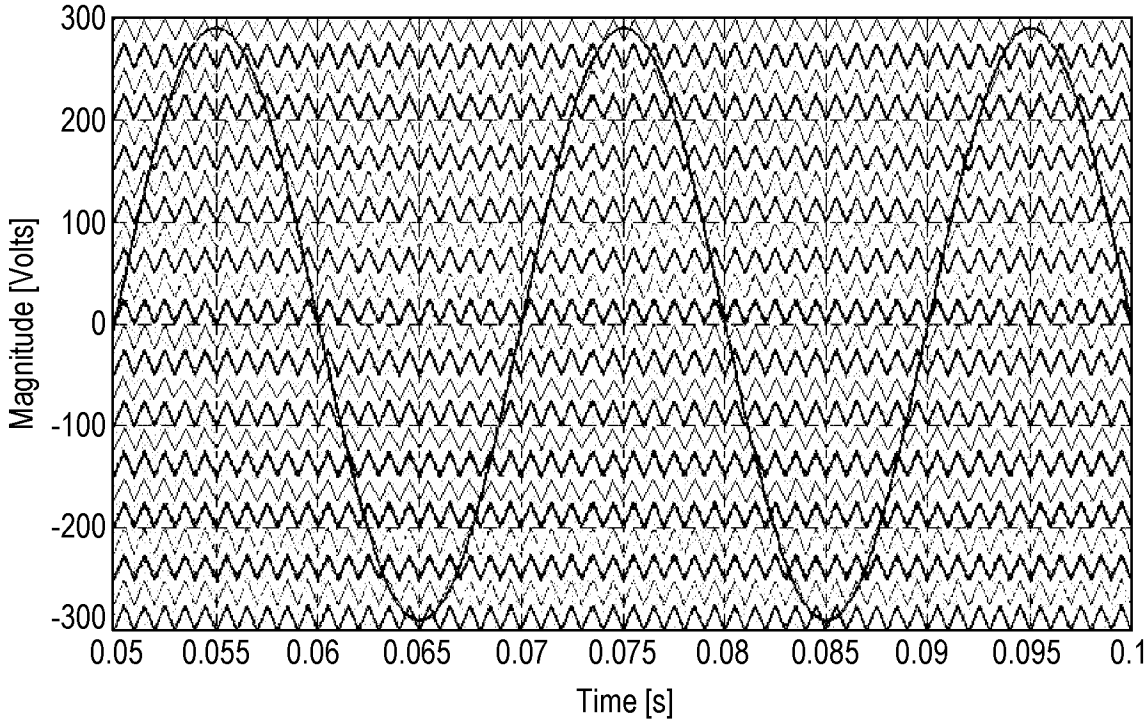

300
200
100
0
-100
-200
-300
Magnitude [Volts]
0.05
0.055
0.06
0.065
0.07
0.075
0.08
0.085
0.09
0.095
0.1
Time [s]

FIG. 9D

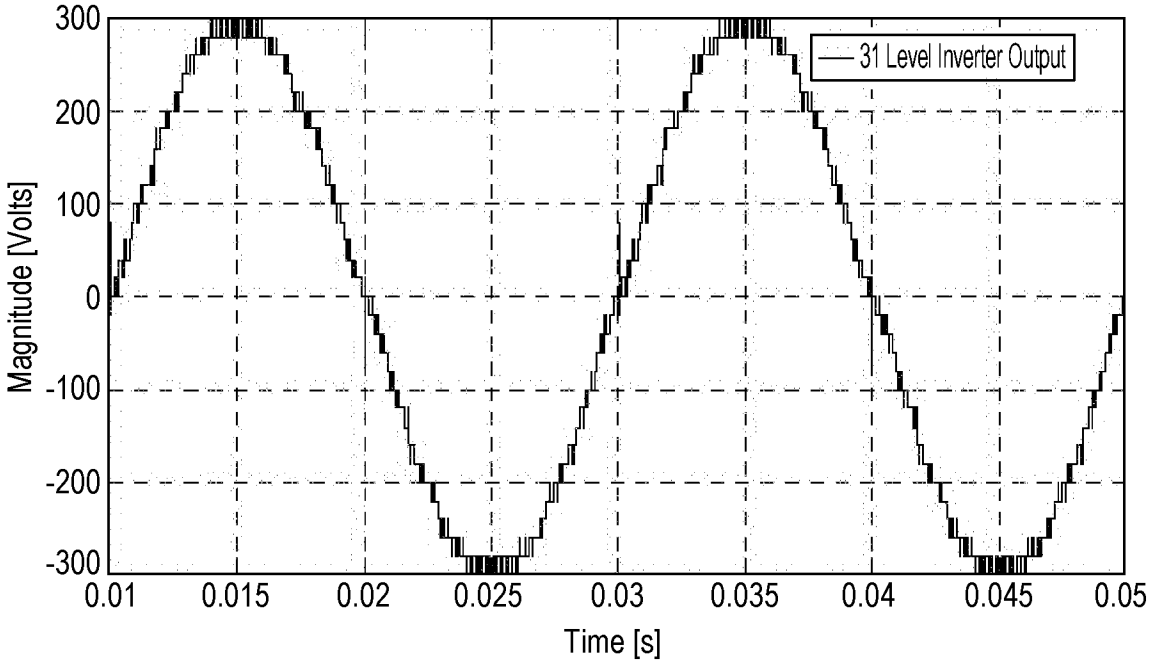


FIG. 10A

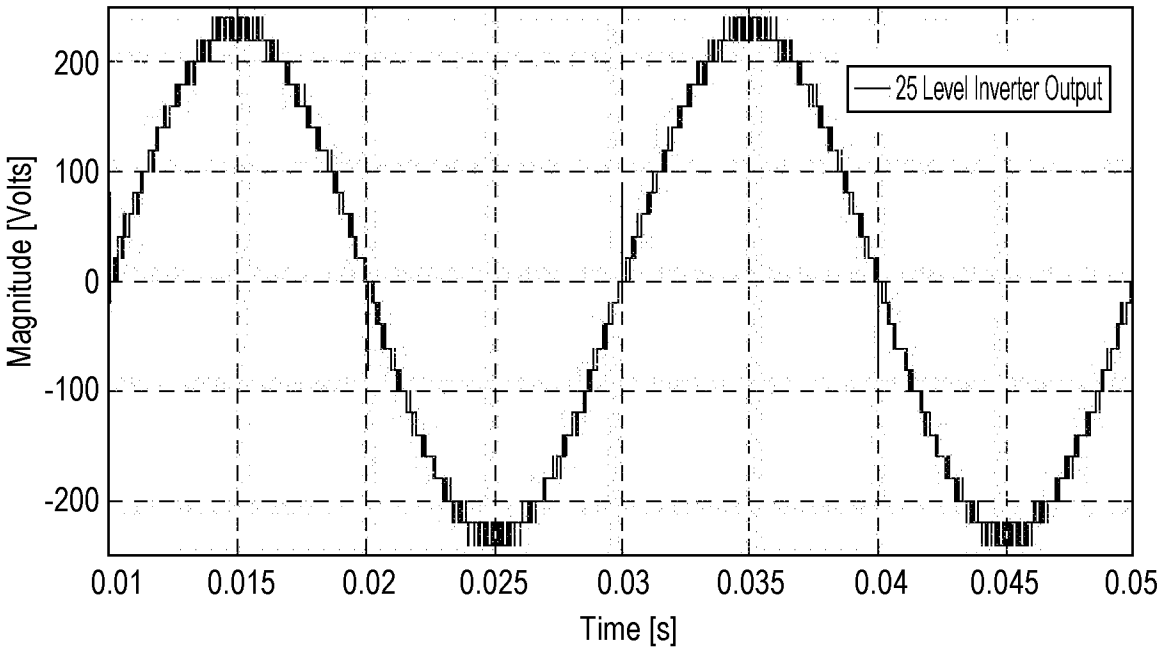


FIG. 10B

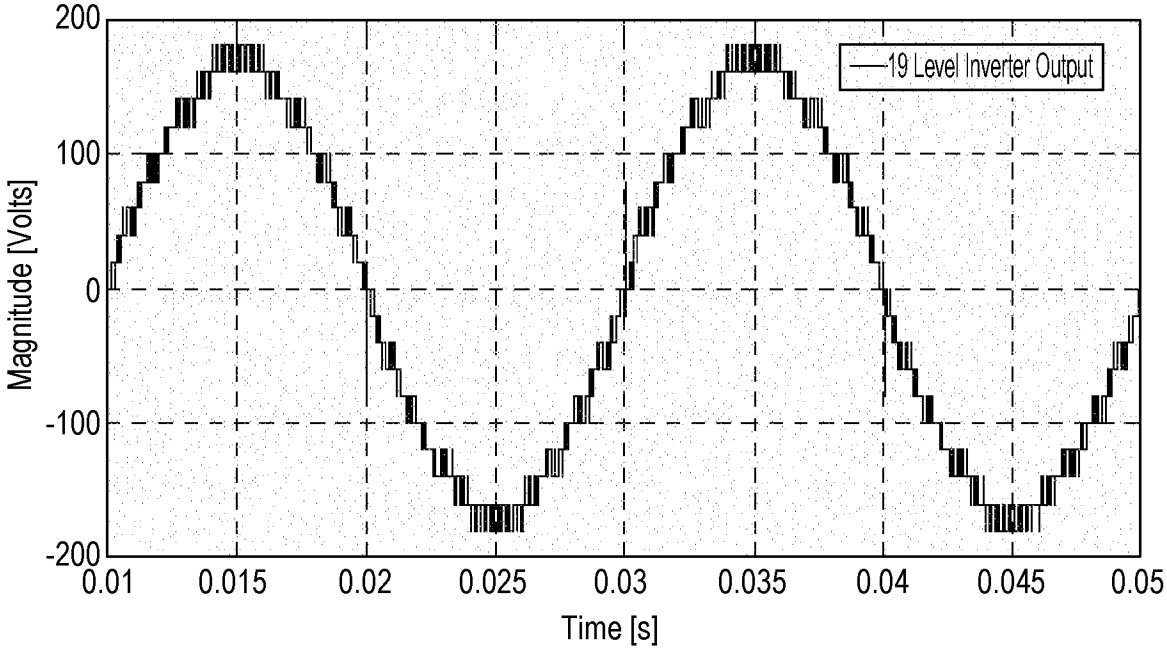


FIG. 10C

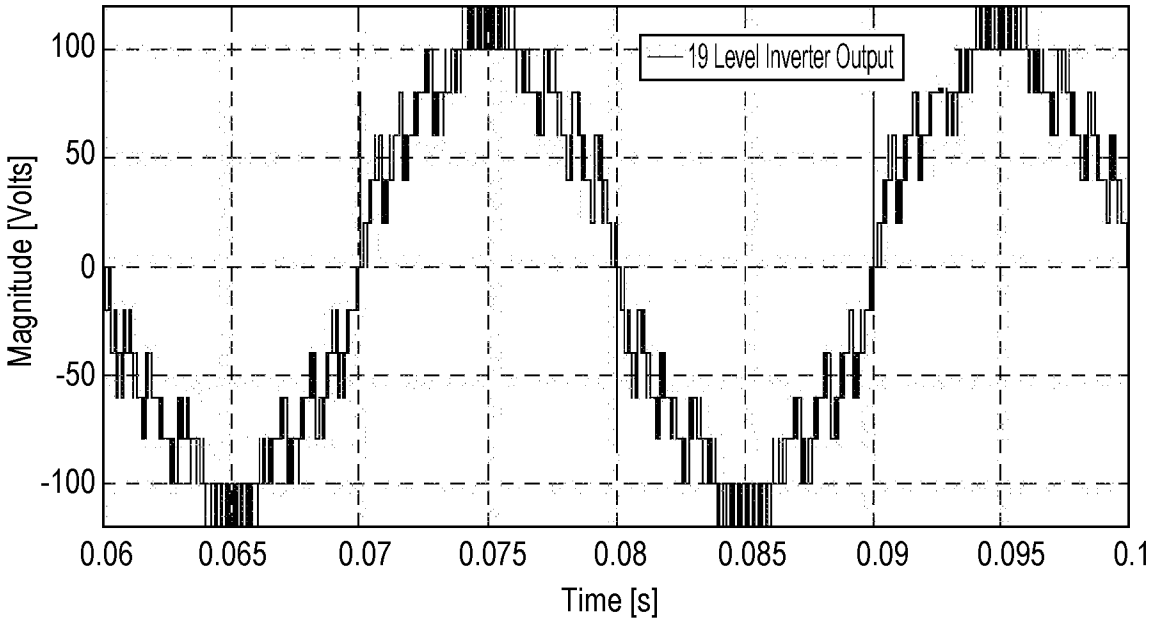


FIG. 10D

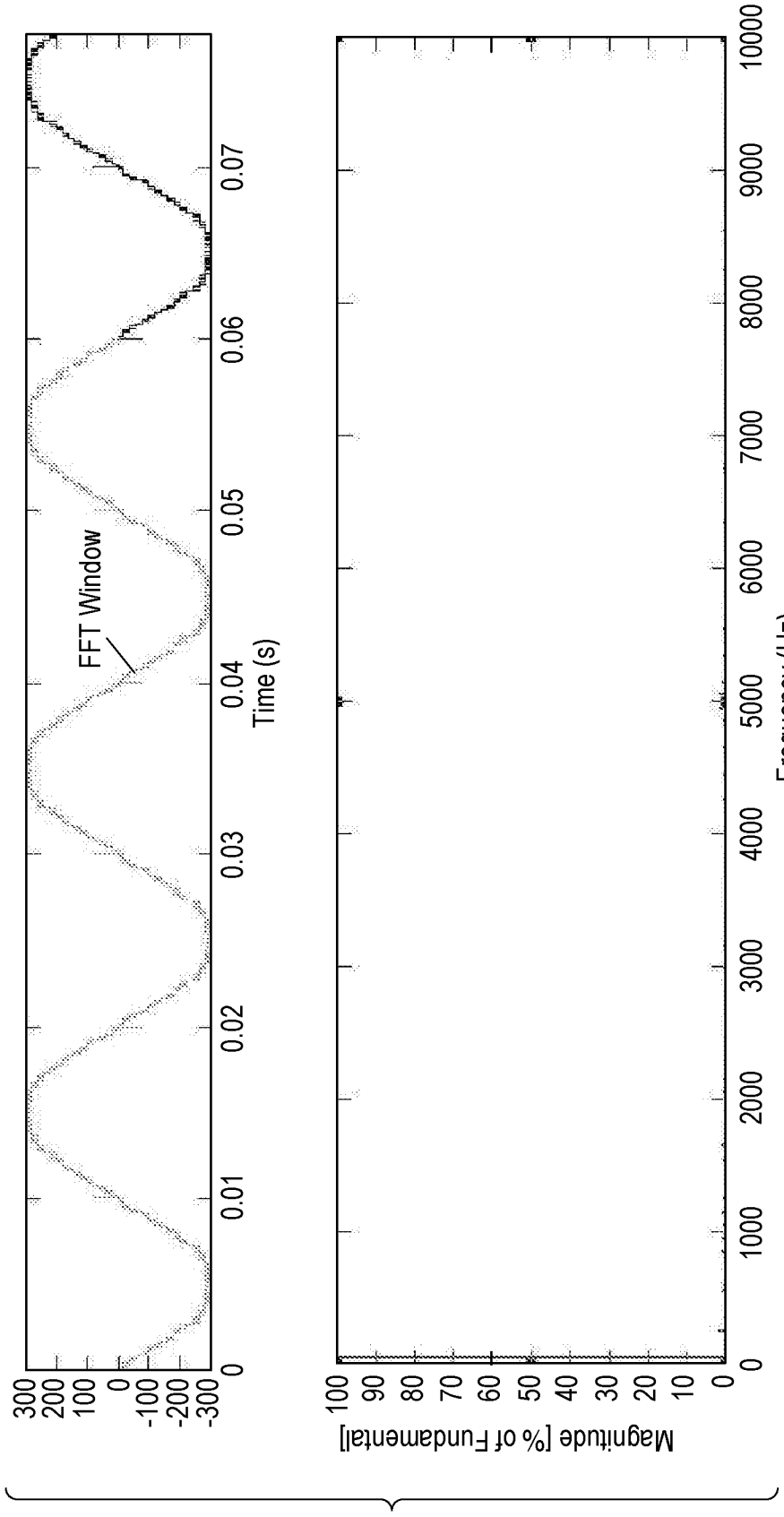

300
200
100
0
-100
-200
-300
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
Time (s)
FFT Window
100
90
80
70
60
50
40
30
20
10
0
Magnitude [% of Fundamental]
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000
Frequency (Hz)

FIG. 10E

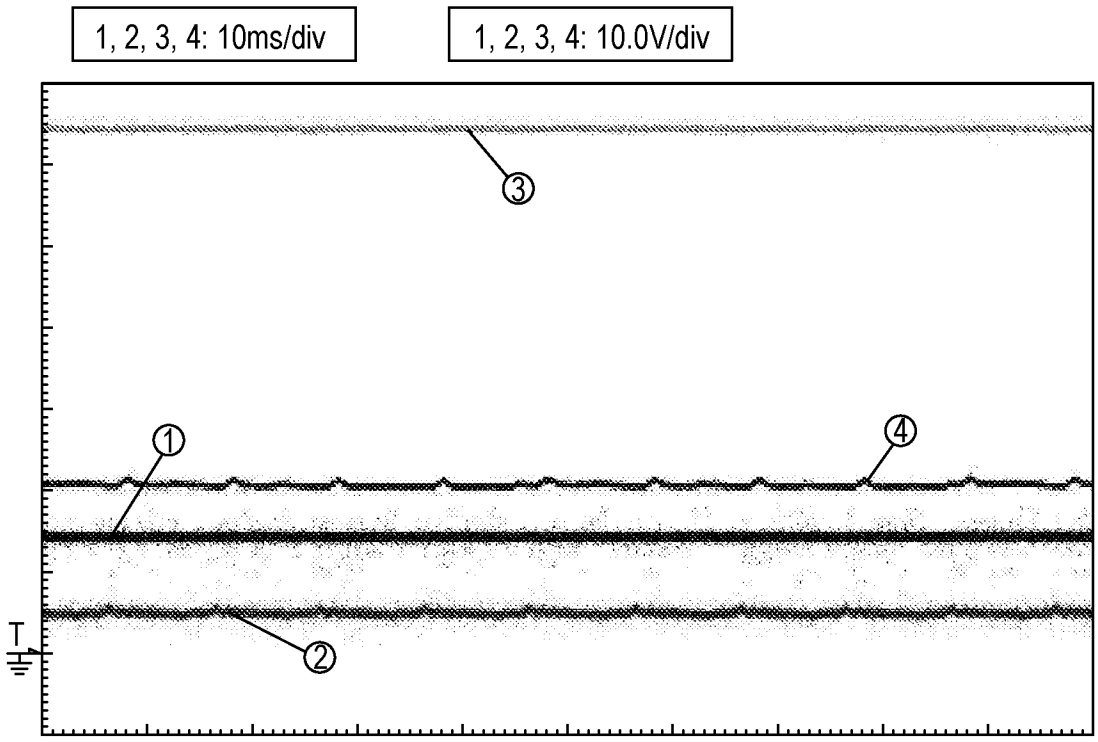


FIG. 11A

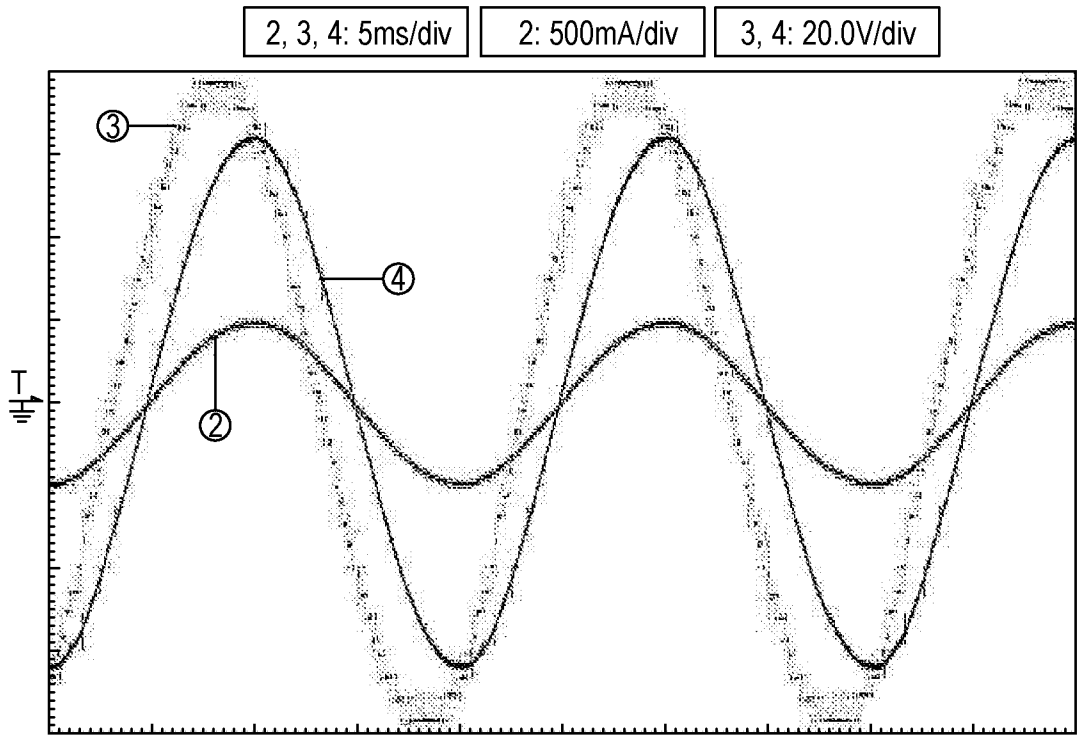


FIG. 11B

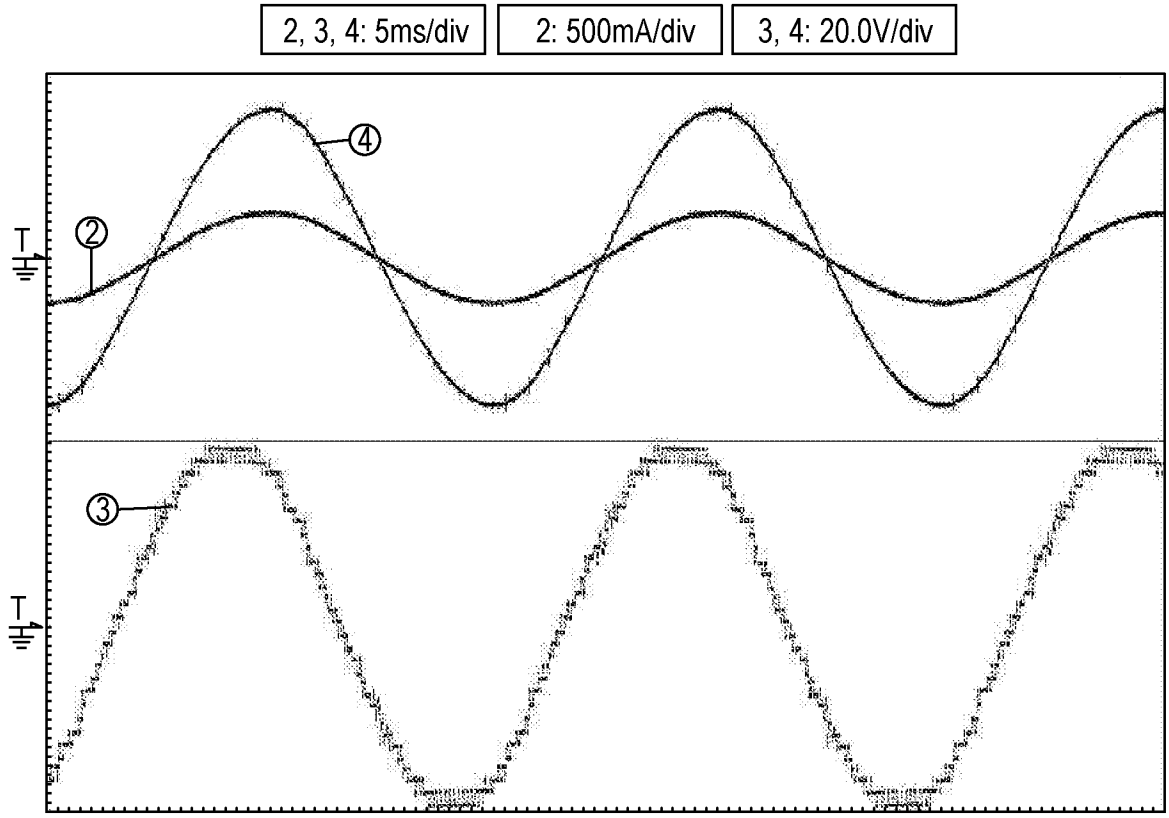


FIG. 11C

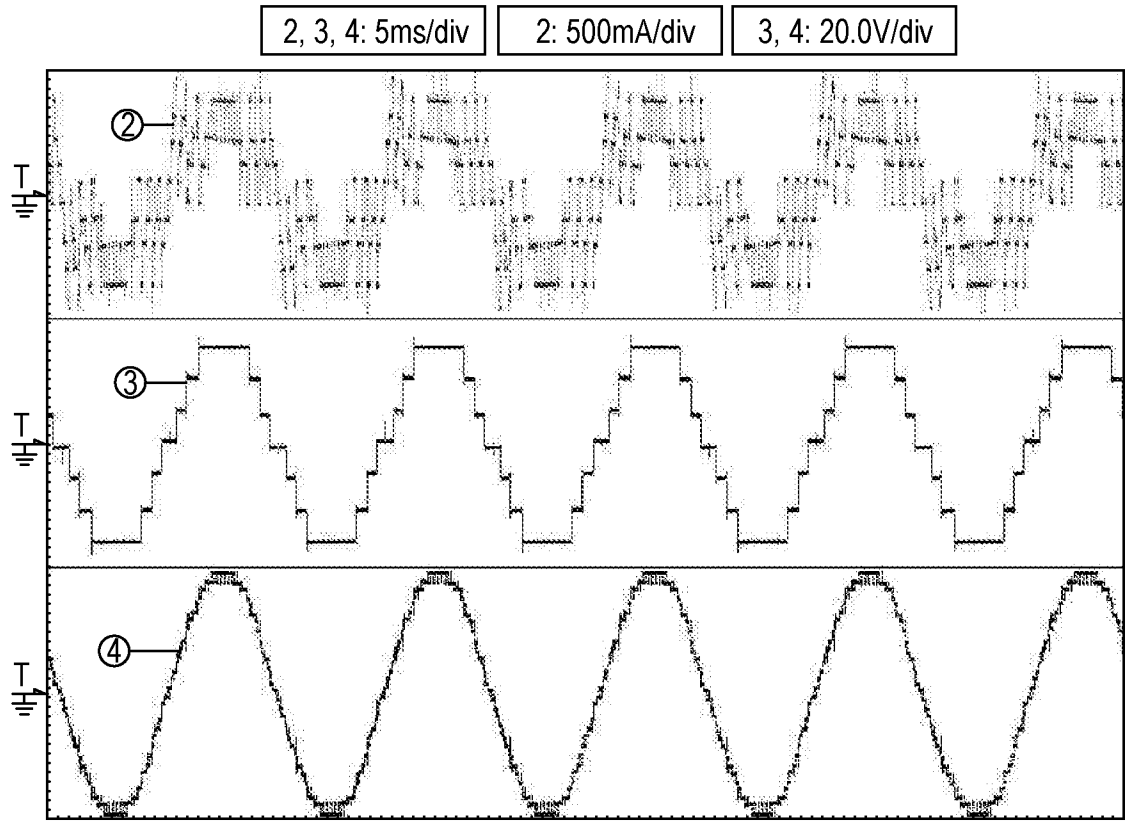


FIG. 11D

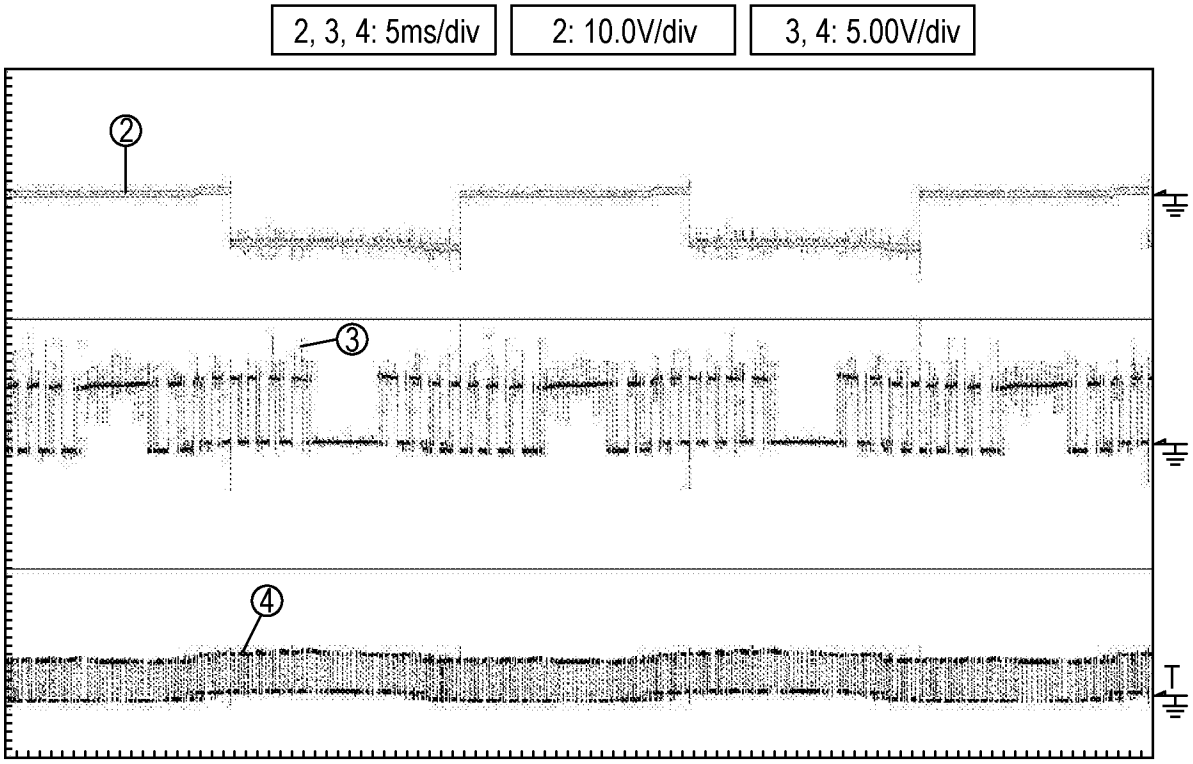


FIG. 11E

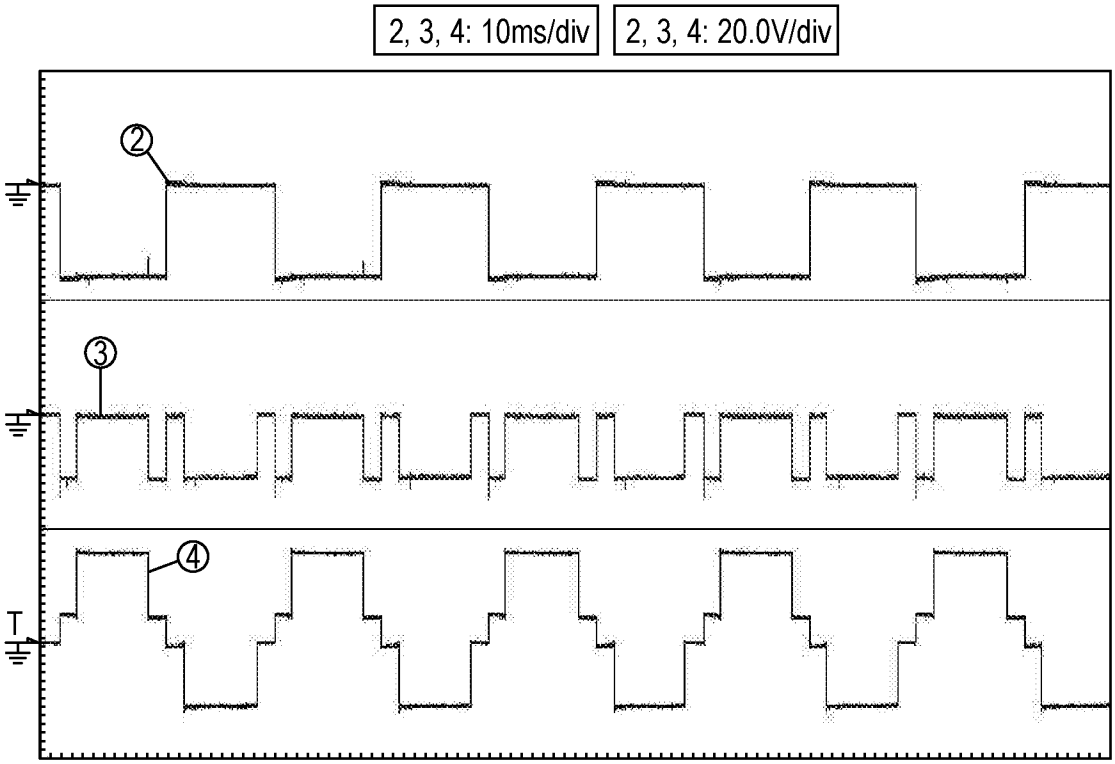


FIG. 11F

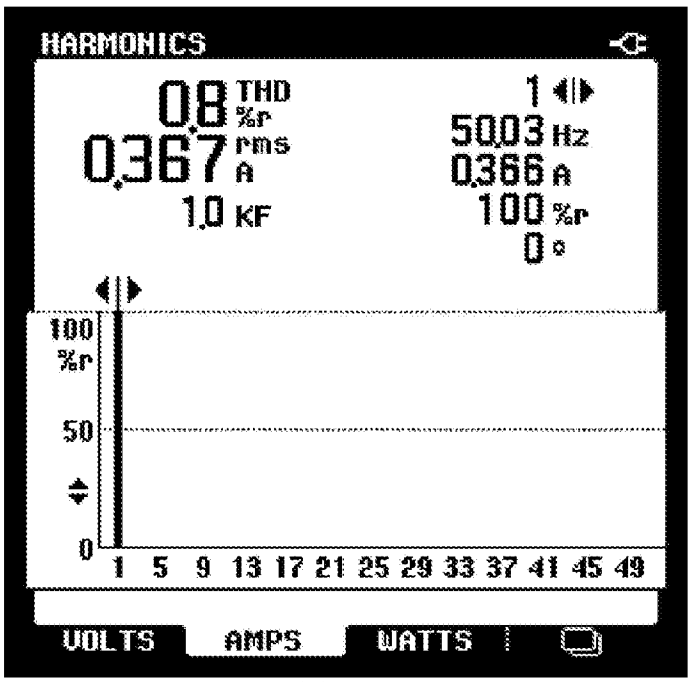


FIG. 12A

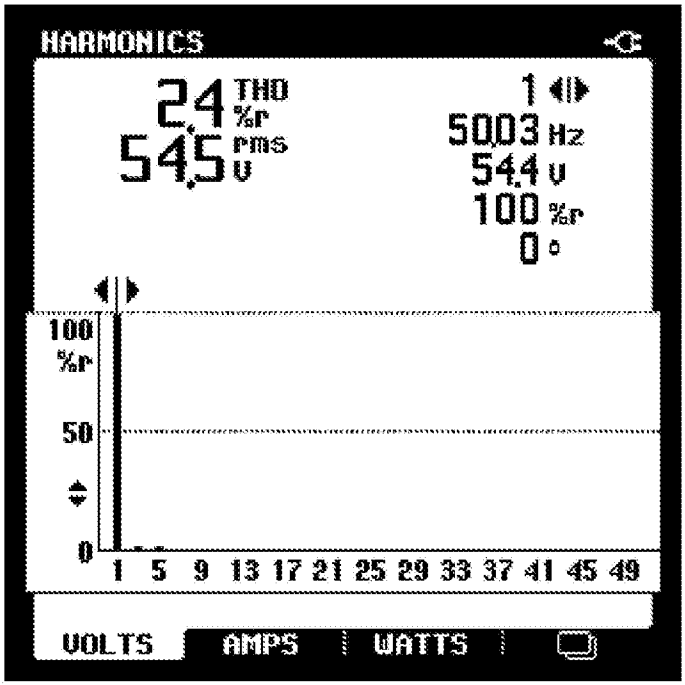


FIG. 12B

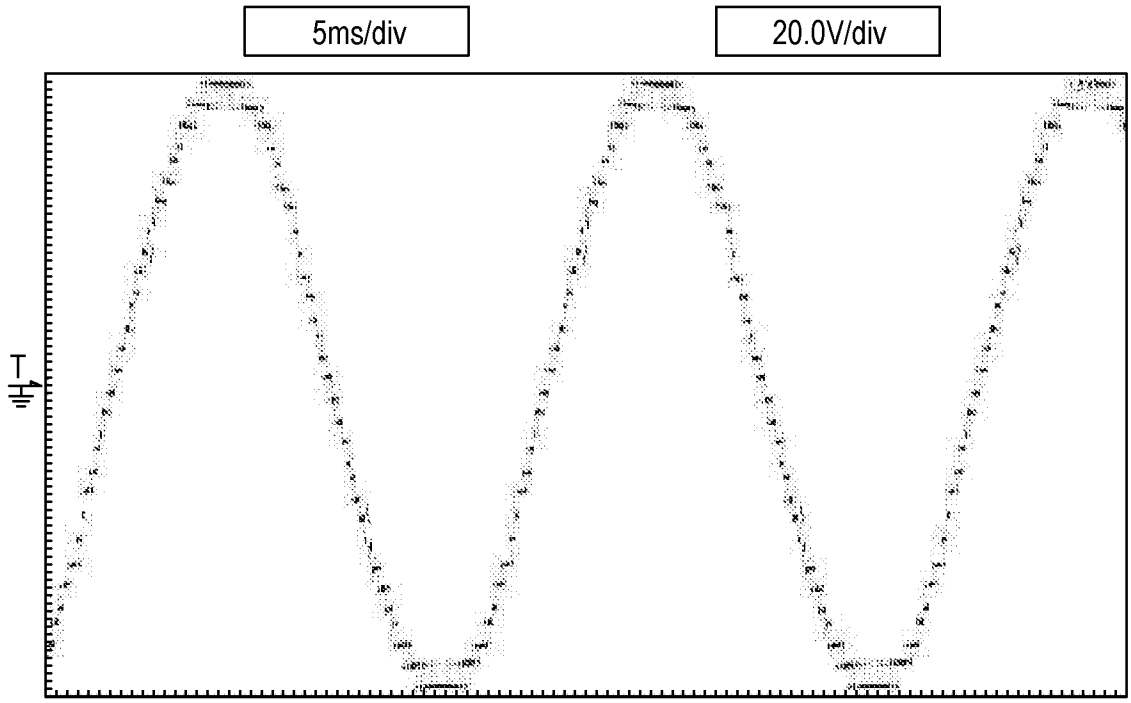


FIG. 13A

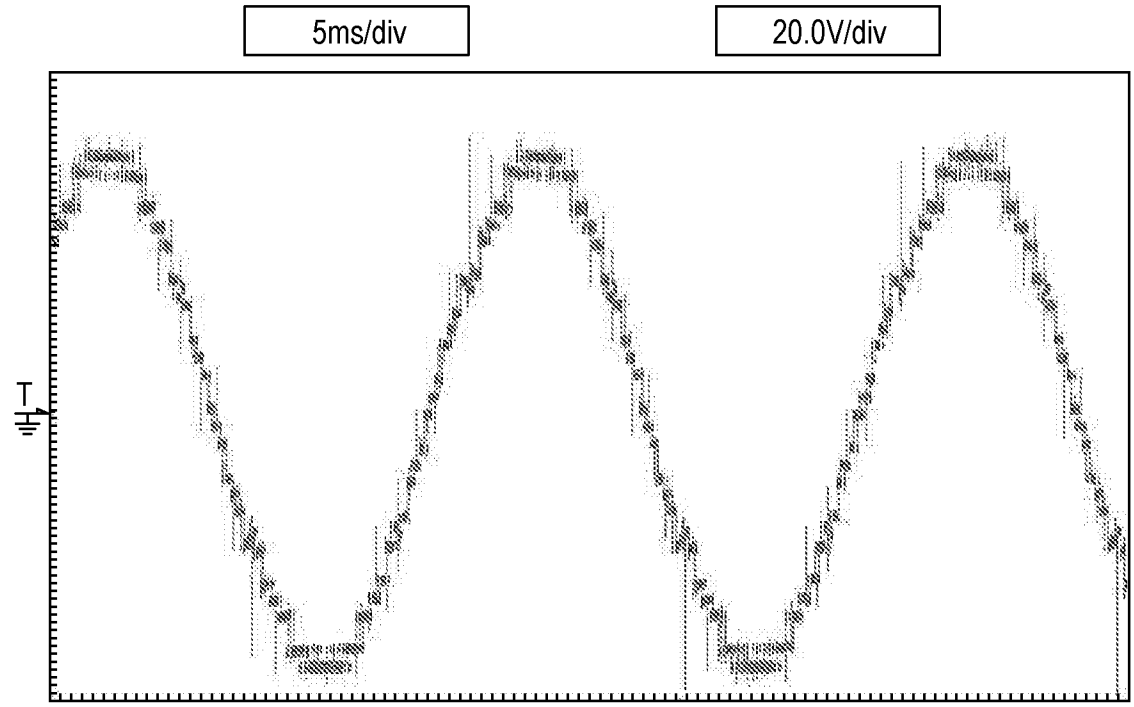


FIG. 13B

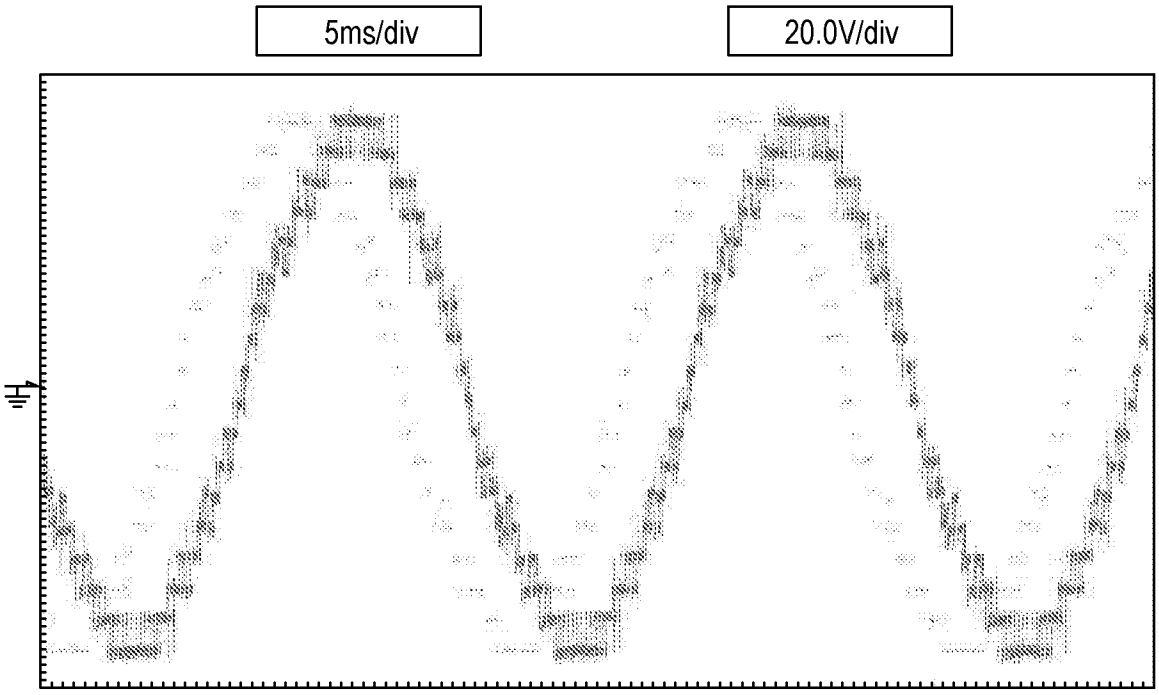


FIG. 13C

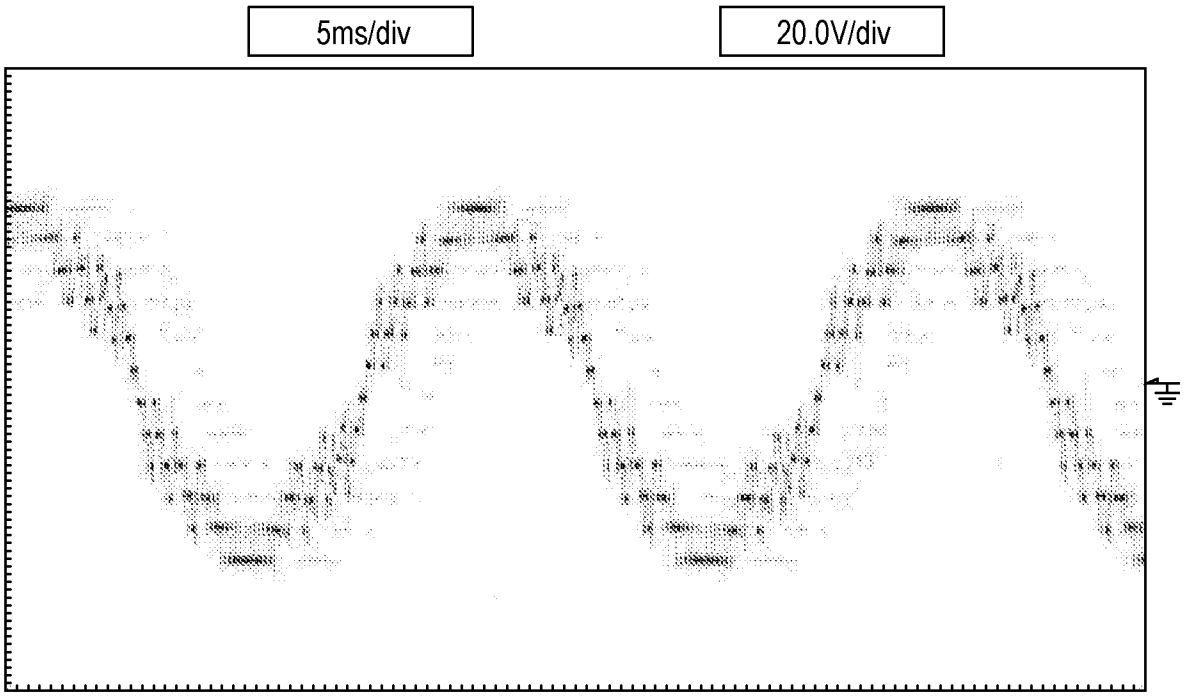


FIG. 13D

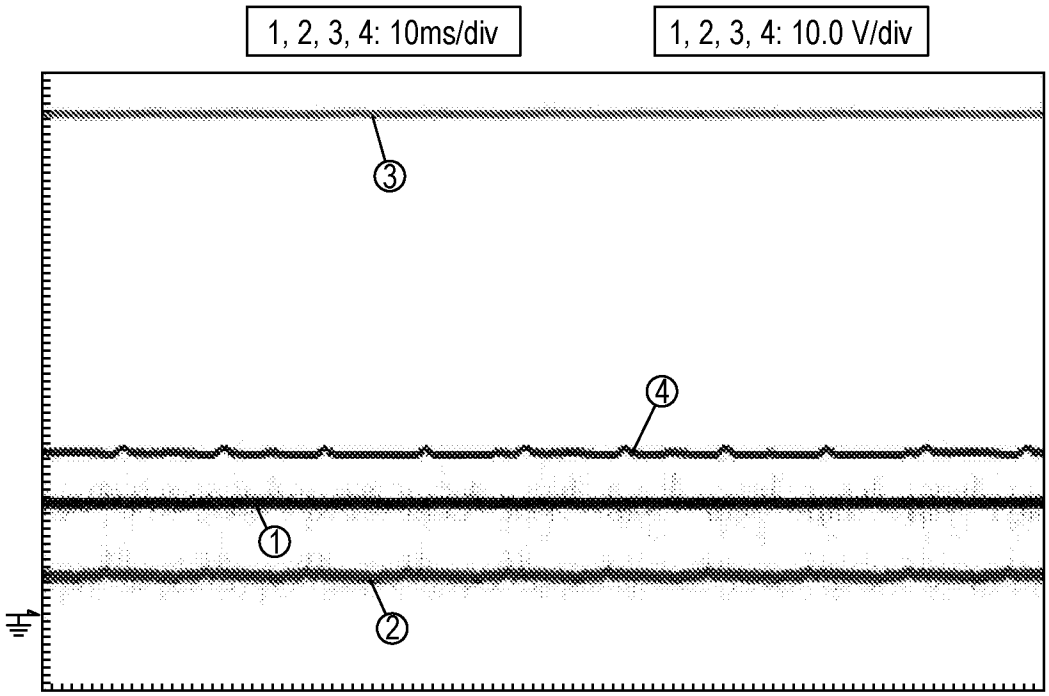


FIG. 14A

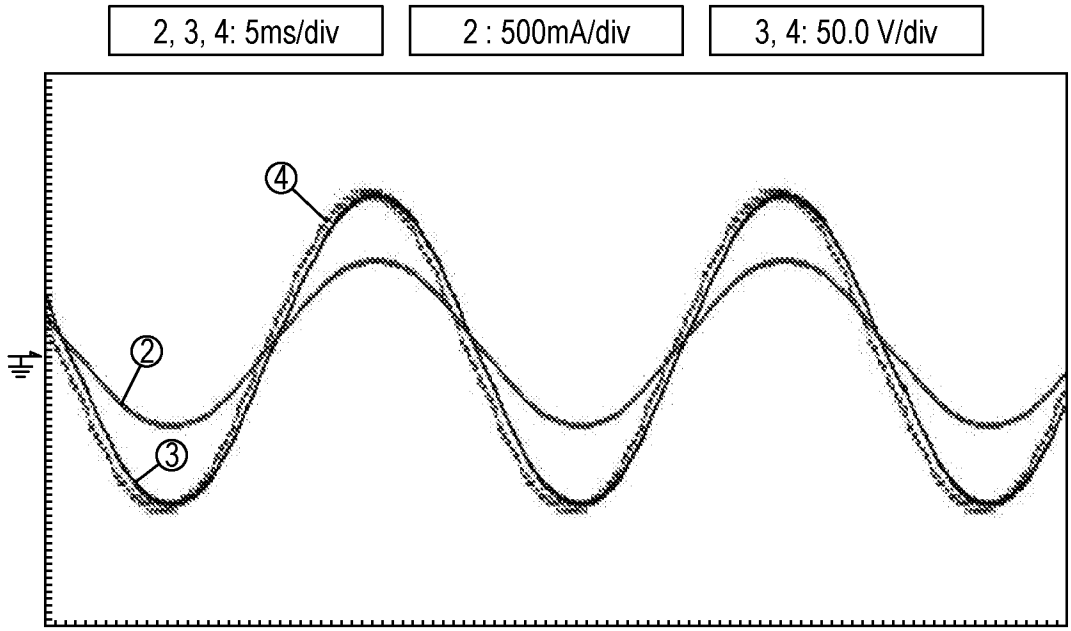


FIG. 14B

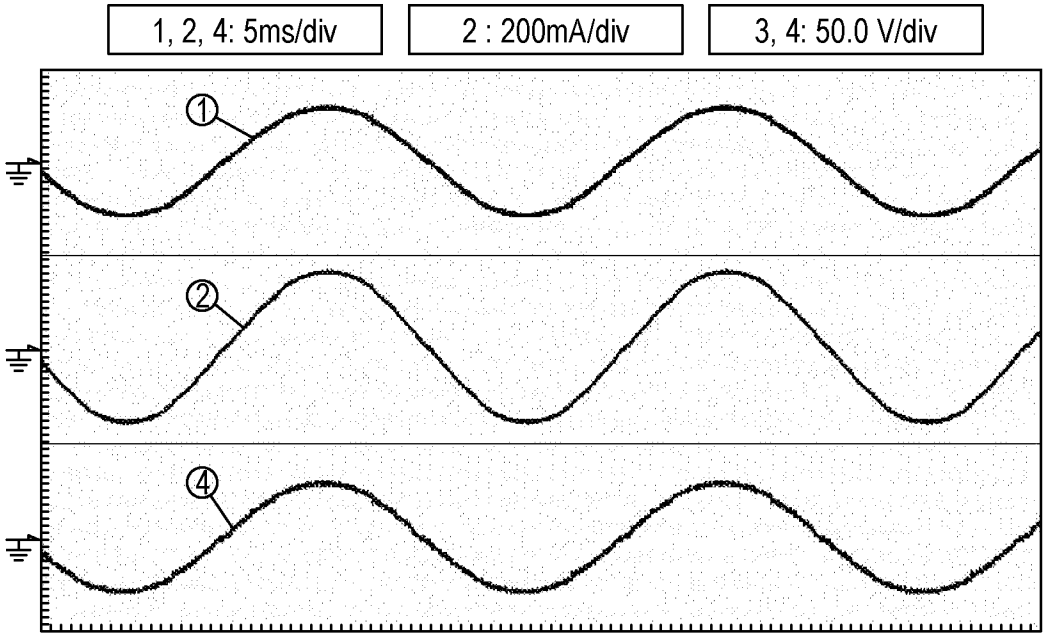


FIG. 14C

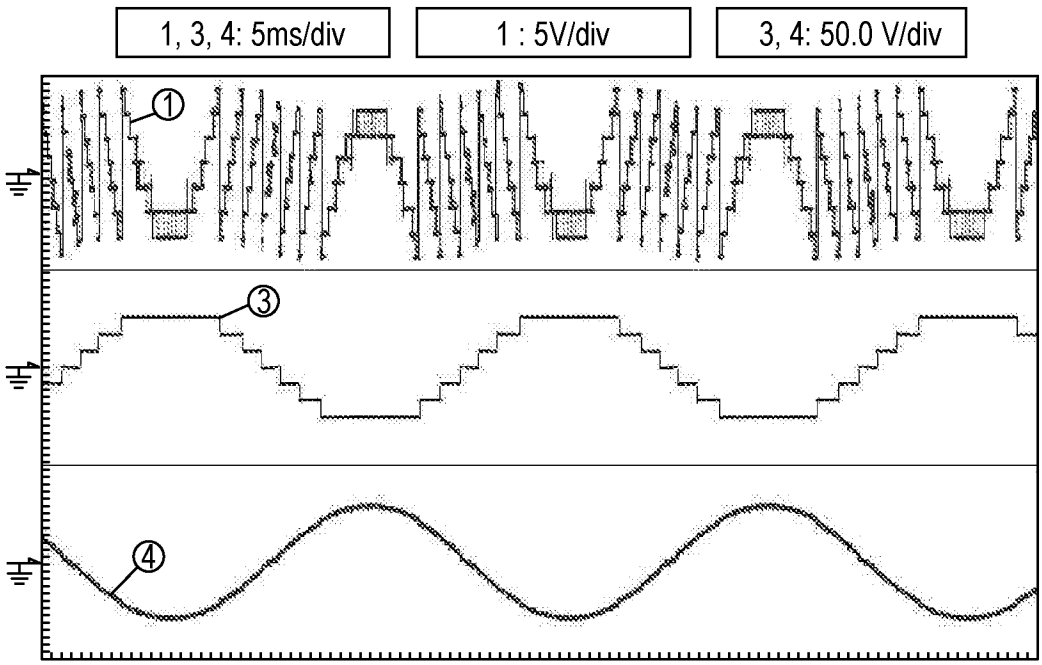


FIG. 14D

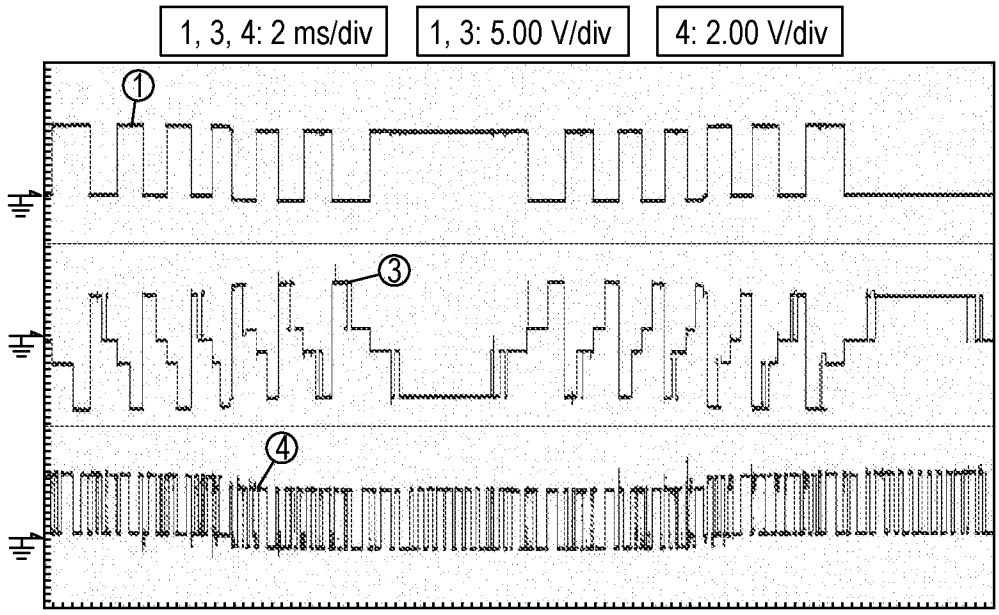


FIG. 14E

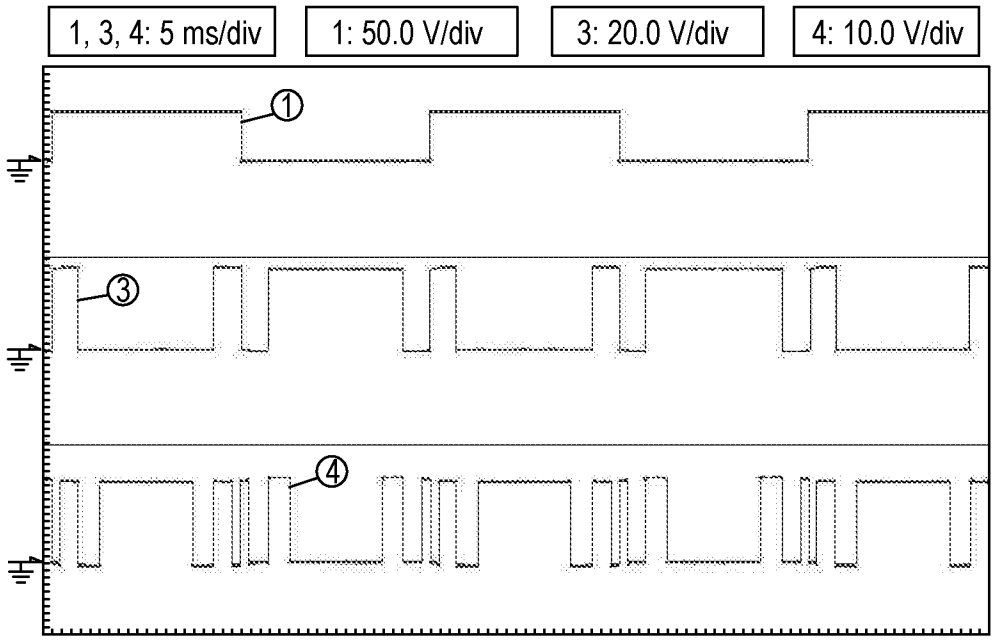


FIG. 14F

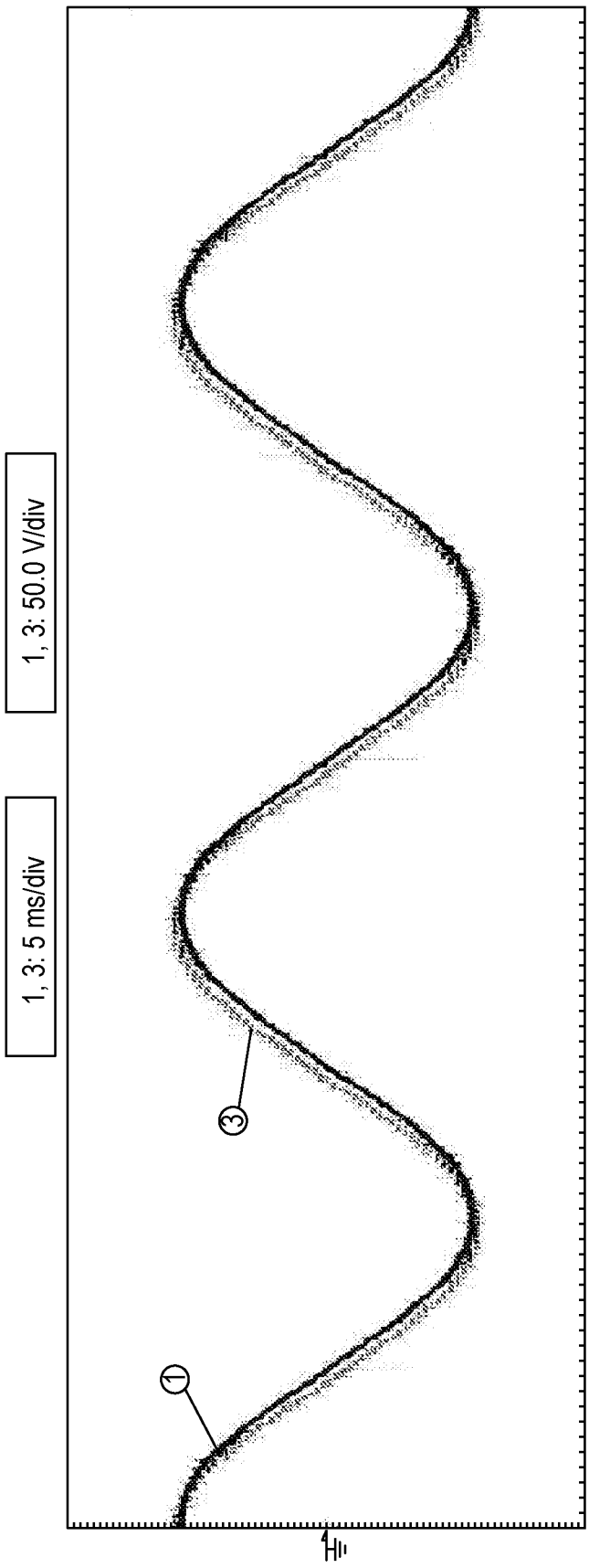


FIG. 14G

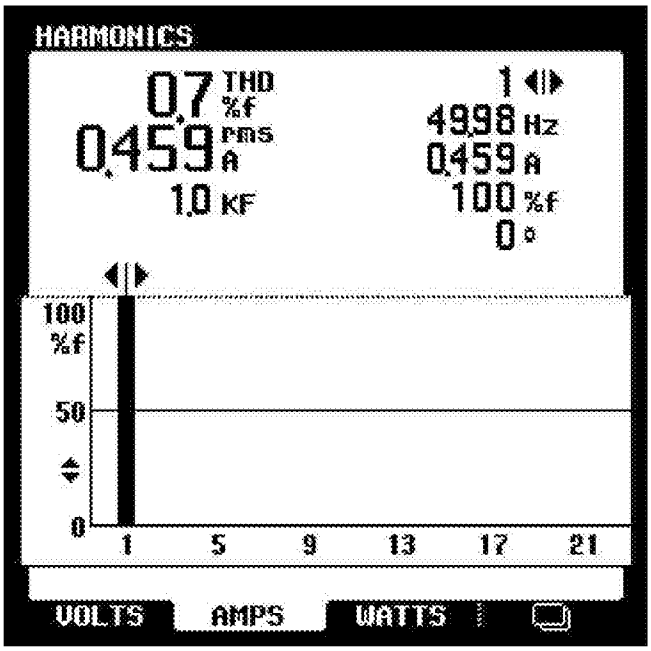


FIG. 15A

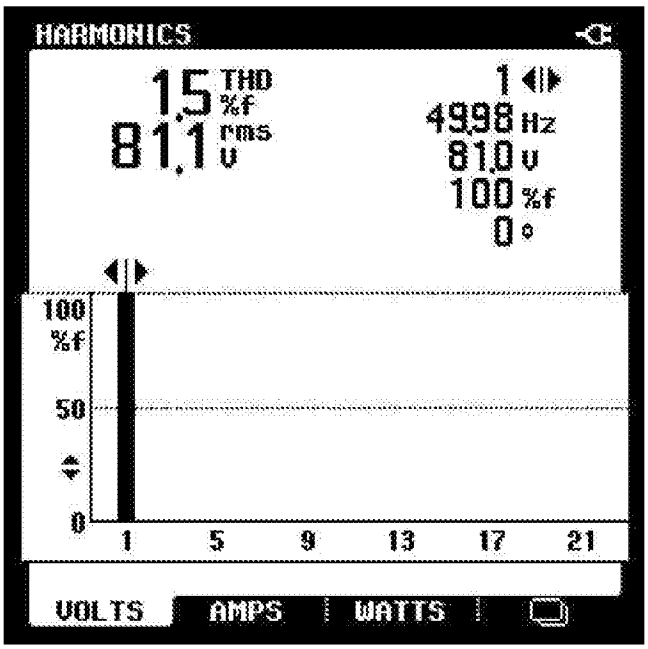


FIG. 15B

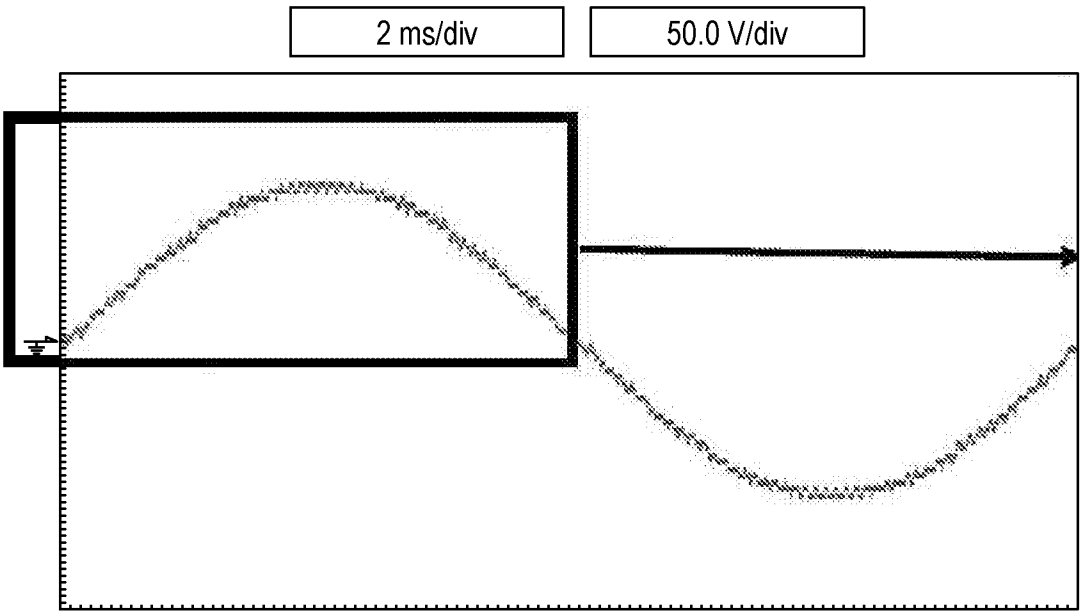


FIG. 16A

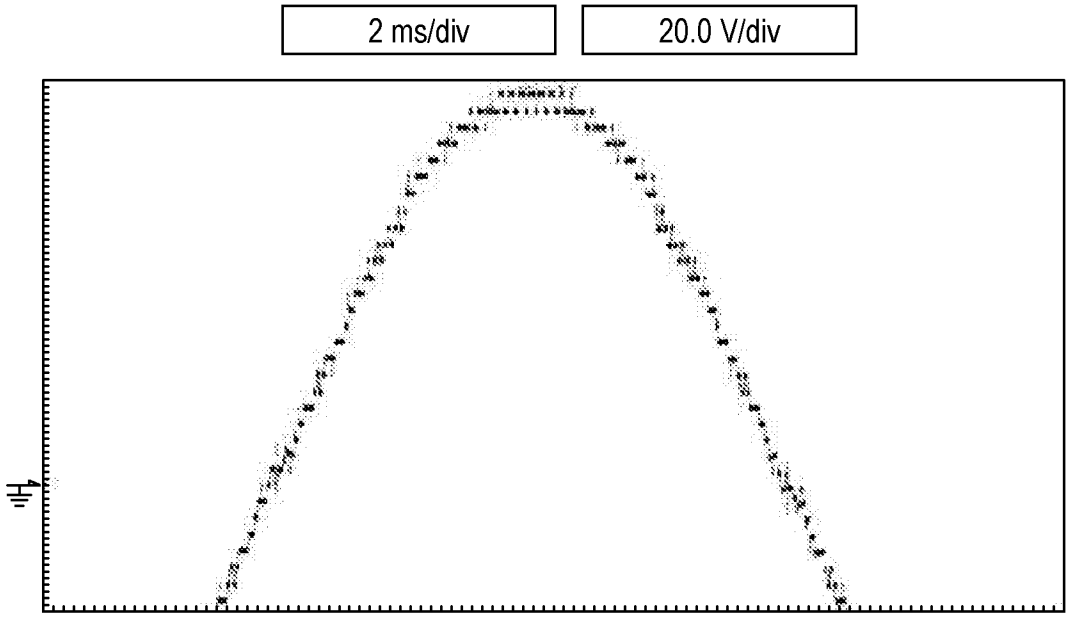


FIG. 16B

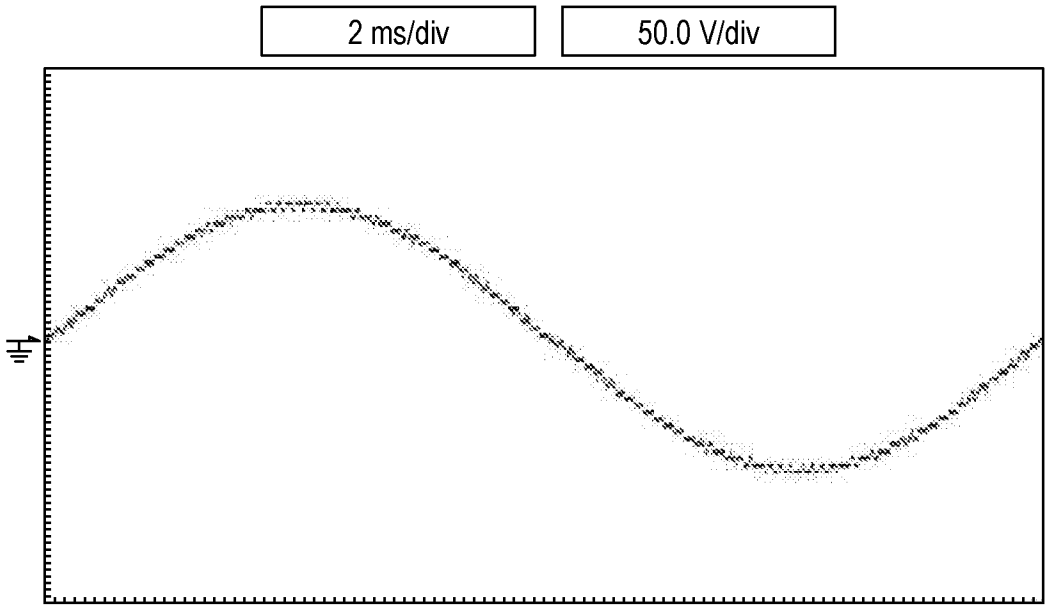


FIG. 16C

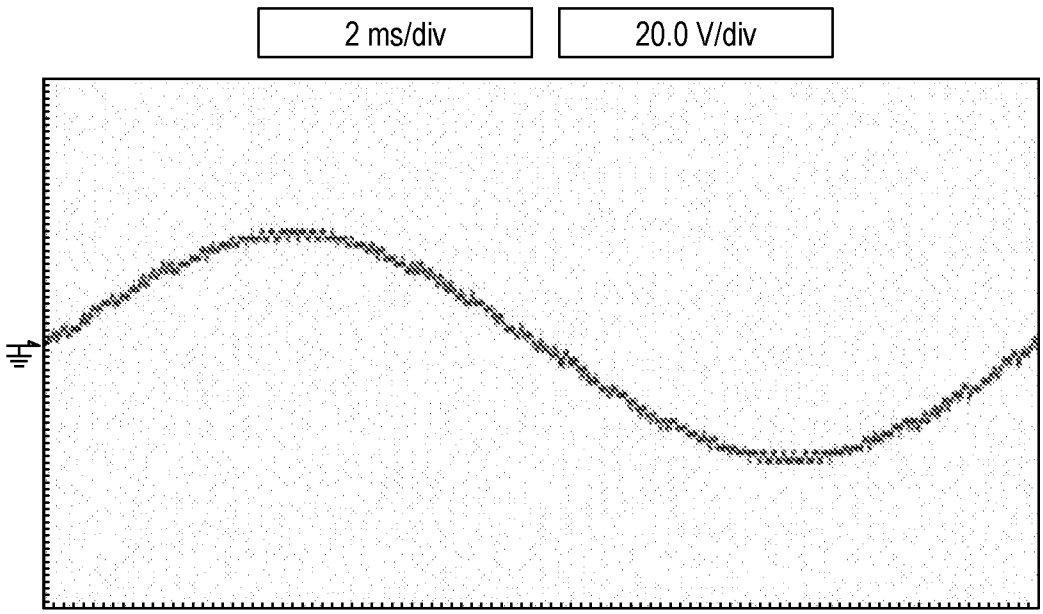


FIG. 16D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/020967

A. CLASSIFICATION OF SUBJECT MATTER

H02M 7/483(2007.01)i, H02J 3/38(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M 7/483; H05B 33/08; H02M 5/458; H02M 1/42; H02M 7/48; H02J 3/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: power, inverter, packed U-cell, multilevel, cascade, voltage, capacitor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	M.GOWTHAM et al, `A Seven Level Packed U Cell (Puc) Multilevel Inverter For Photovoltaic System`, International Journal of Applied Engineering Research, 2015, Vol. 10, No. 6, pages 15237-15250 See pages 15239-15241 and figures 2-4.	1-11
Y	JOSE RODRIGUEZ et al., `Multilevel Inverters: A Survey of Topologies, Controls, and Applications`, IEEE Transactions on Industrial Electronics, August 2002, Vol. 49, No. 4, pages 724-738 See pages 726-729 and figures 3-4.	1-11
A	US 2014-0346962 A1 (THE REGENTS OF THE UNIVERSITY OF CALIFORNIA) 27 November 2014 See claims 1-8 and figures 1-4.	1-11
A	US 2014-0268928 A1 (LIXIANG WEI et al.) 18 September 2014 See claims 1-5 and figures 1-4.	1-11
A	JP 2013-055830 A (CHIBA UNIV.) 21 March 2013 See paragraphs 10-22 and figures 1-5.	1-11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 May 2017 (29.05.2017)	**29 May 2017 (29.05.2017)**

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Telephone No. +82-42-481-3463

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/020967

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014-0346962 A1	27/11/2014	US 9295116 B2	22/03/2016
		WO 2013-086445 A1	13/06/2013
US 2014-0268928 A1	18/09/2014	CN 104065280 A	24/09/2014
		EP 2782240 A2	24/09/2014
		EP 2782240 A3	29/10/2014
		MX 2014003241 A	25/03/2015
		US 2016-0111967 A1	21/04/2016
		US 9240731 B2	19/01/2016
JP 2013-055830 A	21/03/2013	JP 5927640 B2	01/06/2016