

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization

International Bureau



(10) International Publication Number

WO 2014/055935 A1

(43) International Publication Date

10 April 2014 (10.04.2014)

(51) International Patent Classification:

H01L 21/66 (2006.01)

(21) International Application Number:

PCT/US2013/063556

(22) International Filing Date:

4 October 2013 (04.10.2013)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

61/710,668 5 October 2012 (05.10.2012) US

(71) Applicant: FEI COMPANY [US/US]; 5350 NE Dawson Creek Dr., Hillsboro, Oregon 97124 (US).

(72) Inventors: BLACKWOOD, Jeffrey; 3203 SE 75th Ave, Portland, Oregon 97206 (US). LEE, Sang Hoon; 1053 NE Orenco Station Pkwy, #D320, Hillsboro, Oregon 97124 (US). SCHMIDT, Michael; 1003 SE Hacienda Lane, Gresham, Oregon 97080 (US). STONE, Stacey; 795 SW Sosa Place, Beaverton, Oregon 97006 (US). HOLLAND, Karey; 22855 NW Dairy Creek Rd, North Plains, Oregon 97133 (US).

(74) Agent: SCHEINBERG, Michael, O.; Scheinberg & Associates, PC, PO Box 164140, Austin, Texas 78716 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) Title: MULTIDIMENSIONAL STRUCTURAL ACCESS

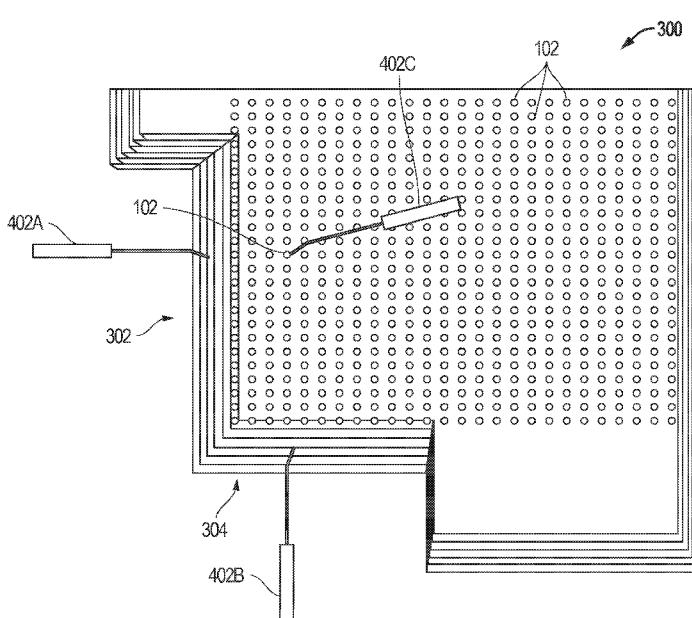


FIG. 4

(57) Abstract: Multiple planes within the sample are exposed from a single perspective for contact by an electrical probe. The sample can be milled at a non-orthogonal angle to expose different layers as sloped surfaces. The sloped edges of multiple, parallel conductor planes provide access to the multiple levels from above. The planes can be accessed, for example, for contacting with an electrical probe for applying or sensing a voltage. The level of an exposed layer to be contacted can be identified, for example, by counting down the exposed layers from the sample surface, since the non-orthogonal mill makes all layers visible from above. Alternatively, the sample can be milled orthogonally to the surface, and then tilted and/or rotated to provide access to multiple levels of the device. The milling is preferably performed away from the region of interest, to provide electrical access to the region while minimizing damage to the region.

## Multidimensional Structural Access

### Technical Field of the Invention

**[0001]** The present invention relates to processing of multidimensional, microscopic structures to provide electrical access to internal structures.

### Background of the Invention

**[0002]** As semiconductor fabrication processes pack more circuitry into smaller packages, integrated circuit (IC) designs are becoming more three-dimensional (3D). It is difficult to measure, analyze and locate faults in 3D microscopic (including nanoscopic) structures.

**[0003]** An engineer will typically identify a region-of-interest (ROI) that he wants to investigate, based upon, for example, aberrant electrical behavior of a circuit component. Most ROIs in conventional ICs are confined to a small volume of the device in a planar region. For example, a static random access memory (SRAM) or a conventional “not-and” (NAND) flash cell each occupies a distinct X and Y location, with a small volume of active area in the Z direction. An engineer typically identifies the ROI by starting with a logic bit or gate address, which can then be mapped to a physical X/Y location in an active region of the structure.

**[0004]** The ROI is often buried below layers of insulator and conductors. Once the ROI is identified, the circuit can be “deprocessed,” that is, overlying structures can be removed, to expose the ROI. Current deprocessing techniques typically provide access to the structure in a planar fashion – ion beam milling creates surfaces orthogonal to the device surface in order to allow imaging, probing, or other localization techniques. Likewise cleaving the wafer or parallel-lapping deprocessing provides access to a plane of the structure.

**[0005]** Techniques to analyze the ROI include, for example, micro-probing, in which conductive probes are contacted to the conductors on the IC to apply and/or measure voltages or currents. Another technique for analyzing a ROI is voltage contrast imaging, in which a charged particle beam image, which is sensitive to any voltage on the imaged surface, is obtained while a voltage is applied to a part of the circuit. Other analysis techniques include scanning probe microscopy, such as scanning-capacitance microscopy, in which a fine probe is scanned above the region of interest and the electrical or physical behavior of the probe is monitored. As used herein, analysis techniques include imaging techniques.

**[0006]** Current techniques map locations on an integrated circuit as if the device were a city in which buildings have only one floor – simply getting the street address is sufficient to

deliver the mail to the correct location. Emerging three dimensional (3D) IC fabrication technologies do not constrain the active area (i.e., transistor or memory cell) to one plane in the Z direction -- active areas occupy many levels of 3D devices. The city map is now populated by skyscrapers – the address information needs to reference to which floor the mail is to be delivered. Rather than identify a 2D region of interest, an engineer will require distinct isolation of a volume-of-interest (VOI) in three dimensions.

**[0007]** For 3D IC structures, prior art techniques that provide planar access are inherently limited to two dimensions of the structure, resulting in either more complicated or impossible final access to the VOI.

### **Summary of the Invention**

**[0008]** An embodiment of the present invention provides electrical access to internal components of a three-dimensional structure.

**[0009]** Multiple planes within the sample are exposed from a single perspective for imaging and/or probing. For example, the sample can be milled at a non-orthogonal angle to expose different layers as sloped surfaces. The non-orthogonal milling exposes edges of multiple, parallel conductor planes to provide access to multiple levels from above. Once exposed, the planes can be accessed, for example, for contacting with an electrical probe for applying or sensing a voltage. The level of an exposed layer to be contacted can be identified, for example, by counting down the exposed layers from the sample surface, since the non-orthogonal mill makes all layers visible from above. Alternatively, the sample can be milled orthogonally to the surface, and then tilted and/or rotated to provide access to multiple levels of the device. The milling is preferably performed away from the region of interest, to provide electrical access to the region while minimizing damage to the region.

**[0010]** Additional processing can be applied to the exposed layers, for example, using circuit edit-type techniques, such as passivating, depositing an insulator on part of the sample, cutting circuits, and depositing conductors to change behavior or creating probing points.

**[0011]** The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter. It should be appreciated by those skilled in the art that the conception and specific embodiments disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

### **Brief Description of the Drawings**

[0012] For a more thorough understanding of the present invention, and advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0013] FIG. 1 is shows a 3D storage device having a trench milled therein to expose a vertical face;

[0014] FIG. 2 is a top-down view of the 3D storage device of FIG. 1;

[0015] FIG. 3 shows a 3D storage device milled in accordance with an embodiment of the present invention;

[0016] FIG. 4 is a top-down view showing the storage device of FIG. 3;

[0017] FIG. 5 shows a portion of a tilted workpiece that provides access to buried conductive layers without requiring milling at an angle to the work piece surface;

[0018] FIG. 6 is a flowchart showing the steps of an embodiment of the invention; and

[0019] FIG. 7 shows schematically a dual beam system that can be used to implement the present invention.

### **Detailed Description of Preferred Embodiments**

[0020] In one conventional analysis of two-dimensional processing, a region of interest is exposed by ion beam milling and electrical probes are contacted to the region of interest, typically from above. The region of interest can be viewed from above using an electron beam with voltage applied for voltage contrast imaging. This works well for 2D structures, but for newer structures having transistors or memory cells on many layers, it is very difficult to access the correct layer in the stack when one is looking at the structure from the top. In accordance with an aspect of some embodiments of the invention, the sample is milled and/or tilted so that multiple planes within the sample are exposed from a single perspective, typically from above, for imaging or probing.

[0021] Also, most prior art cross-sectional techniques are preformed through the region of interest, such as the particular failing part in a failure analysis. Due to the increased complexity of new 3D structures it is advantageous to keep as much of the structure around the region of interest intact during analysis. In accordance with an aspect of some embodiments of the invention, the milling exposes the electrical connections to a ROI, and keeps much of the ROI intact while providing electrical access to the ROI. As used herein, the term ROI or region of interest is also used to refer to a volume of interest or VOI.

[0022] Off-angle mills, preferably from about 30° to about 45° from a normal to the

surface, spatially separate out the layers in a top-down view so that they may be viewed and accessed. The greater the deviation from orthogonality, the more surface is exposed to a vertical view from above the sample. A normal to the exposed area has a component in the vertical direction, so that the horizontal layer can be observed from above and contacted from above by an electrical probe. A tilted sample can provide the same effect, separating out layers for viewing and exposing them in a top down view.

**[0023]** By milling in an orientation that is not orthogonal to the work piece surface or tilting the structure after a vertical mill, users can see the electrical addressing connections to the ROI using an optical microscope or a SEM and can provide therefore electrical signals to the ROI without being able to actually see it. The tapered mills or tilted sample provide access to the sample in angled sidewalls to allow electrical localization of a defect or other ROI. Access to the angled side wall allows probing the plane at the z-depth of interest, while still providing access to the vertical conductor. Embodiments of the invention provide access to X, Y, and Z localization from a top-view of a sample, and allow electrical probing access to the VOI using current top-down probing techniques.

**[0024]** After the milling, angled or vertical, the sample is oriented so that both the milled face and top surface of the sample can be viewed and/or electrically probed. The viewing and probing are used, for example, for voltage contrast imaging, electrical characterization by probing different layers and observing the electrical response using diagnostic equipment, sensing atomic force microscope probe, or observation of photonic emission.

**[0025]** FIG. 1 shows a 3D storage device 100 having a trench milled therein to expose a vertical cross section. Such devices are typically encapsulated in glass (not shown). Vertical conductors 102 make electrical connections to vertically aligned elements in different horizontal layers. Patterned horizontal conductors 104 make connections in the x-y plane. Each of the three labeled conductors 104 contacts circuit elements in the same Y-Z plane (i.e., having the same x coordinate), but in different Z-planes. FIG. 1 shows a section milled out to expose a face 106. To make connections to face 106 requires a contact coming in from the side, rather than top down. It is difficult to see and manipulate a probe to provide the side access because the side of exposed vertical face is not visible from a top-down view and most probes are designed to contact a conductor from above. FIG. 2 is a top-down view of the 3D storage device. Note that while an X-Y location can be observed, no Z information is available from a top-down view of the milled face 106. In such a case, there is no reliable method of identifying if the defect is in the top layer or somewhere lower in the device stack.

**[0026]** FIG. 3 shows a storage device 300 having angled mills in accordance with an

embodiment of the invention that produces sloped sides 302 and 304, allowing for much easier electrical contact than the vertical face 106 of FIG. 1. FIG. 4 is a top-down view showing the angled milled surfaces 302 and 304 of device. The X-Y locations of contact points is easy to determine, as are the Z positions of the contact points in the stack. By making the various layers at different Z positions available for observation in the sloped faces, the conductor plane corresponding to the exact Z layer of interest may be identified and contacted to provide an electrical contact to the VOI. FIG. 4 shows electrical probes 402A and 402B that contact the exposed edge of internal conductors that are in electrical contact with the region of interest. Probe 402C contacts a vertical conductor 102 that is in electrical contact with the region of interest. The probes move horizontally under manual control or under control of an automated controller to a desired location, and then can move in the Z-direction, also either manually or under control of a controller, to be lowered to contact the selected conductive layer at a desired location. Electrical signals can be applied to one or more probes, while, for example, other electrical signals are sensed by one or more other probes, or a voltage contrast image is observed. The electrical probes are contacted onto the exposed conductor by lowering from above, while the process is being observed from above.

**[0027]** The angled mills expose contacts that allow a particular electrical component to be addressed even though that component itself is not exposed. Thus the component and neighboring components can remain intact. In some embodiments, each electrical structure represents a single bit, for example, in a 3D NAND or DRAM. The bit can be addressed using the exposed X and Y connections for the corresponding level, as well as the corresponding Z connection. The X and Y conductors for any level of Z can be easily observed from above when the conductors are exposed by the angled milling or tilted after a normal angle milling. The exposed conductors do not need to be adjacent to the structure of interest. A user can observe the number of steps in the angled mill to determine which Z level the x and y connectors are on by counting down layers.

**[0028]** Angled milling or tilting exposes the connection so that it can be contacted from above rather than from the side. Milling can be performed using the ion beam with or without an etch-enhancing glass, as described, for example, in U.S. Pat. App. No 13/921,466.

**[0029]** FIG. 5 shows a part of a 3D structure, analogous to the volume of FIG. 3 near the intersection of walls 302 and 304. In FIG. 5, however, the milled wall 502 and 504 are vertical. The work piece is then tilted so that a normal to each of the milled faces 502 and 504 has a component in the vertical direction. That is, the milled face 502 and 504 are visible from above and so the electrical probes 402A, 402B and 402C can be moved individually in

the horizontal plane to be positioned above selected conductors and then lowered from above to contact the appropriate layer to provide an electrical connection to the region of interest.

Multilayer device 504 is preferably tilted between about 30° to about 45°.

**[0030]** FIG. 6 is a flow chart showing the steps of a preferred embodiment of the invention. In step 602, a region of interest is identified. For example, the ROI may correspond to an element of a device that is found to perform poorly. The position of the ROI is determined from computer-aid-design information that maps a logic element to an electrical component and then to a physical location on the device. In step 604, the device is milled, preferably at an angle between about 30° to about 45°, to expose conductors near the region of interest. In step 606, the preferred position of probe contact is determined. For example, the layout of the chip is checked to determine which conductor on which conductive layer makes contact with the region of interest. The identified conductive layer can be identified by counting down from the top of the chip to the appropriate level, since the angled mill provides visibility of the multiple levels. In step 608, electrical probes are moved in the X-Y direction to position the probes appropriately as determined in step 606, and then in step 610, the probes are lowered in the Z direction to contact electrical conductors at or near the region of interest. It is understood that the probe motion may not be simple rectangular X-Y-Z motion, but the probe will move through space and downward to contact the electrical conductor. As used here, moving in the X-Y direction or Z direction does not require separate motions in the mentioned planes or direction, but includes rotations and simultaneous motions in different directions that accomplish the same result. In step 612, voltages or currents are applied to the sample through one or more of the probes. In step 614, the effect of the applied voltage or current is observed. Observing the effect can include, for example, sensing voltages or currents from one or more of the probes, observing the region of interest using voltage contrast imaging, micro-Raman analysis, or other imaging or analytical technique.

**[0031]** Additional processing can be applied to the exposed layers, for example, using circuit edit-type techniques, such as passivating, depositing an insulator on part of the sample, cutting circuits, and depositing conductors to change behavior or creating probing points. Circuit edit-type techniques are well known. For example, a conductor can be deposited by beam-induced deposition to connect two or more exposed layers. An insulator can be deposited by beam-induced deposition before the conductor deposition to electrically other exposed layers of the integrated circuit from the deposited conductor. Exposed conductors

can also be cut to with the ion beam to break an electrical contact.

**[0032]** FIG. 7 shows a typical dual beam system 710 suitable for practicing the present invention, with a vertically mounted SEM column and a FIB column mounted at an angle of approximately 52° from the vertical. Suitable dual beam systems are commercially available, for example, from FEI Company, Hillsboro, Oregon, the assignee of the present application. While an example of suitable hardware is provided below, the invention is not limited to being implemented in any particular type of hardware.

**[0033]** A scanning electron microscope 741, along with power supply and control unit 745, is provided with the dual beam system 710. An electron beam 743 is emitted from a cathode 752 by applying voltage between cathode 752 and an anode 754. Electron beam 743 is focused to a fine spot by means of a condensing lens 756 and an objective lens 758. Electron beam 743 is scanned two-dimensionally on the specimen by means of a deflection coil 760. Operation of condensing lens 756, objective lens 758, and deflection coil 760 is controlled by power supply and control unit 745.

**[0034]** Electron beam 743 can be focused onto substrate 722, which is on movable stage 725 within lower chamber 726. When the electrons in the electron beam strike substrate 722, secondary electrons are emitted. These secondary electrons are detected by a secondary electron detector 740 as discussed below.

**[0035]** Dual beam system 710 also includes focused ion beam (FIB) system 711 which comprises an evacuated chamber having an upper portion 712 within which are located an ion source 714 and a focusing column 716 including extractor electrodes and an electrostatic optical system. The axis of focusing column 716 is tilted 52 degrees from the axis of the electron column. The upper portion 712 includes an ion source 714, an extraction electrode 715, a focusing element 717, deflection elements 720, and a focused ion beam 718. Ion beam 718 passes from ion source 714 through focusing column 716 and between electrostatic deflectors 720 toward substrate 722, which comprises, for example, a semiconductor device positioned on movable stage 725 within lower chamber 726.

**[0036]** Stage 725 can preferably move in a horizontal plane (X and Y axes) and vertically (Z axis). Stage 725 can also tilt approximately 60° and rotate about the Z axis. A door 761 is opened for inserting substrate 722 onto X-Y stage 725 and also for servicing an internal gas supply reservoir, if one is used. The door is interlocked so that it cannot be opened if the system is under vacuum.

**[0037]** An ion pump (not shown) is employed for evacuating upper portion 712. The chamber 726 is evacuated with turbomolecular and mechanical pumping system 730 under

the control of vacuum controller 732. The vacuum system provides within chamber 726 a vacuum of between approximately  $1 \times 10^{-7}$  Torr and  $5 \times 10^{-4}$  Torr. If an etch-assisting gas, an etch-retarding gas, or a deposition precursor gas is used, the chamber background pressure may rise, typically to about  $1 \times 10^{-5}$  Torr.

**[0038]** The high voltage power supply provides an appropriate acceleration voltage to electrodes in ion beam focusing column focusing 716 for energizing and focusing ion beam 718. When it strikes substrate 722, material is sputtered, that is physically ejected, from the sample. Alternatively, ion beam 718 can decompose a precursor gas to deposit a material.

**[0039]** High voltage power supply 734 is connected to liquid metal ion source 714 as well as to appropriate electrodes in ion beam focusing column 716 for forming an approximately 1 keV to 60 keV ion beam 718 and directing the same toward a sample. Deflection controller and amplifier 736, operated in accordance with a prescribed pattern provided by pattern generator 738, is coupled to deflection plates 720 whereby ion beam 718 may be controlled manually or automatically to trace out a corresponding pattern on the upper surface of substrate 722. In some systems the deflection plates are placed before the final lens, as is well known in the art. Beam blanking electrodes (not shown) within ion beam focusing column 716 cause ion beam 718 to impact onto blanking aperture (not shown) instead of substrate 722 when a blanking controller (not shown) applies a blanking voltage to the blanking electrode.

**[0040]** The liquid metal ion source 714 typically provides a metal ion beam of gallium. The source typically is capable of being focused into a sub one-tenth micrometer wide beam at substrate 722 for either modifying the substrate 722 by ion milling, enhanced etch, material deposition, or for the purpose of imaging the substrate 722. Other ion sources, such as a plasma ion source, can also be used.

**[0041]** A probe assembly includes a probe motion mechanism 780 and probe tips 781. The probe tips can be moved individually to a desired position and lowered to contact the substrate 722. While three probe tips are shown, the number of probe tips can vary. Multiple probe motion mechanism can be used to control any number of probes. The probe tips can apply a voltage or current to the substrate 722 at a precise location and/or can sense a voltage or current. In some embodiments, the probes are mounted on a ring around the work piece.

**[0042]** A charged particle detector 740, such as an Everhart-Thornley detector or multi-channel plate, used for detecting secondary ion or electron emission is connected to a video circuit 742 that supplies drive signals to video monitor 744 and receives deflection signals from controller 719. The location of charged particle detector 740 within lower chamber 726

can vary in different embodiments. For example, a charged particle detector 740 can be coaxial with the ion beam and include a hole for allowing the ion beam to pass. In other embodiments, secondary particles can be collected through a final lens and then diverted off axis for collection.

**[0043]** An optical microscope 751 allows observation of the sample 722 and the probes 781. The optical microscope may be co-axial with one of the charged particle beams, as described, for example, in US Pat. No. 6,373,070 to Rasmussen, for "Method apparatus for a coaxial optical microscope with focused ion beam," is assigned to the applicant of the present application.

**[0044]** A gas delivery system 746 extends into lower chamber 726 for introducing and directing a gaseous vapor toward substrate 722. U.S. Pat. No. 5,851,413, to Casella et al. for "Gas Delivery Systems for Particle Beam Processing," assigned to the assignee of the present invention, describes a suitable gas delivery system 746. Another gas delivery system is described in U.S. Pat. No. 5,435,850, to Rasmussen for a "Gas Injection System," also assigned to the assignee of the present invention. For example, a metal organic compound can be delivered to the beam impact point to deposit a metal upon impact of the ion beam or the electron beam. A precursor gas, such as  $(CH_3)_3Pt(C_pCH_3)$  to deposit platinum or tungsten hexacarbonyl to deposit tungsten, can be delivered to be decomposed by the electron beam to provide the protective layer in step 108.

**[0045]** A system controller 719 controls the operations of the various parts of dual beam system 710. Through system controller 719, a user can cause ion beam 718 or electron beam 743 to be scanned in a desired manner through commands entered into a conventional user interface (not shown). Alternatively, system controller 719 may control dual beam system 710 in accordance with programmed instructions. A preferred controller is in communication with or includes a memory that stores instructions for automatically carrying out the steps of FIG. 6. System controller 719 can be used to control the probe motion assembly 780. In some embodiments, dual beam system 710 incorporates image recognition software, such as software commercially available from Cognex Corporation, Natick, Massachusetts, to automatically identify regions of interest, and then the system can manually or automatically expose cross sections for imaging in accordance with the invention. For example, the system could automatically locate similar features on semiconductor wafers including multiple devices, and expose and form images of features of interest on different (or the same) devices.

**[0046]** The invention has broad applicability and can provide many benefits as described

and shown in the examples above. The embodiments will vary greatly depending upon the specific application, and not every embodiment will provide all of the benefits and meet all of the objectives that are achievable by the invention. Particle beam systems suitable for carrying out the present invention are commercially available, for example, from FEI Company, the assignee of the present application.

**[0047]** Descriptions herein use the terms horizontal and vertical relative to a wafer or other work piece. It will be understood that “horizontal” typically is used to mean parallel to the work piece surface and the conductive planes deposited on to the work piece, and “vertical” is typically used to mean orthogonal to the work piece surface.

**[0048]** The invention has broad applicability and can provide many benefits as described and shown in the examples above. The embodiments will vary greatly depending upon the specific application, and not every embodiment will provide all of the benefits and meet all of the objectives that are achievable by the invention. Particle beam systems suitable for carrying out the present invention are commercially available, for example, from FEI Company, the assignee of the present application.

**[0049]** The present specification discloses both a method and an apparatus for performing the operations of the method. Such apparatus may be specially constructed for the required purposes, or may comprise a general purpose computer or other device selectively activated or reconfigured by a computer program stored in the computer. Various general purpose charged particle beam systems may be used with programs in accordance with the teachings herein. Alternatively, the construction of more specialized apparatus to perform the required method steps may be appropriate.

**[0050]** In addition, the present specification also implicitly discloses a computer program, in that it would be apparent to the person skilled in the art that the individual steps of the method described herein may be put into effect by computer code. The computer program is not intended to be limited to any particular programming language and implementation thereof. It will be appreciated that a variety of programming languages and coding thereof may be used to implement the teachings of the disclosure contained herein. Moreover, the computer program is not intended to be limited to any particular control flow. There are many other variants of the computer program, which can use different control flows without departing from the spirit or scope of the invention.

**[0051]** Such a computer program may be stored on any computer readable medium. The computer readable medium may include storage devices such as magnetic or optical disks, memory chips, or other storage devices suitable for interfacing with a general purpose

computer. The computer readable medium may also include a hard-wired medium such as exemplified in the Internet system, or wireless medium such as exemplified in the GSM mobile telephone system. The computer program when loaded and executed on such a general-purpose computer or controller for a charged particle beam and effectively results in an apparatus that implements the steps of the preferred method.

**[0052]** The invention may also be implemented as hardware modules. More particular, in the hardware sense, a module is a functional hardware unit designed for use with other components or modules. For example, a module may be implemented using discrete electronic components, or it can form a portion of an entire electronic circuit such as an Application Specific Integrated Circuit (ASIC). Numerous other possibilities exist. Those skilled in the art will appreciate that the system can also be implemented as a combination of hardware and software modules.

**[0053]** Although much of the previous description is directed at semiconductor wafers, the invention could be applied to any suitable substrate or surface. Further, whenever the terms "automatic," "automated," or similar terms are used herein, those terms will be understood to include manual initiation of the automatic or automated process or step. In the following discussion and in the claims, the terms "including" and "comprising" are used in an open-ended fashion, and thus should be interpreted to mean "including, but not limited to . . . ."

**[0054]** To the extent that any term is not specially defined in this specification, the intent is that the term is to be given its plain and ordinary meaning. The accompanying drawings are intended to aid in understanding the present invention and, unless otherwise indicated, are not drawn to scale.

**[0055]** The term "integrated circuit" refers to a set of electronic components and their interconnections (internal electrical circuit elements, collectively) that are patterned on the surface of a microchip. The term "semiconductor chip" refers generically to an integrated circuit (IC), which may be integral to a semiconductor wafer, separated from a wafer, or packaged for use on a circuit board. The term "FIB" or "focused ion beam" is used herein to refer to any collimated ion beam, including a beam focused by ion optics and shaped ion beams.

**[0056]** The embodiment above describes 3D NAND type structures, but the invention is not limited to such structures and is useful, for example, for DRAMS, and for characterizing trenches and other structures, as well as circular holes.

**[0057]** To the extent that any term is not specially defined in this specification, the intent is that the term is to be given its plain and ordinary meaning. The accompanying drawings are

intended to aid in understanding the present invention and, unless otherwise indicated, are not drawn to scale.

**[0058]** Some embodiments of the invention provide a method of analyzing a region of interest in a three dimensional integrated circuit structure having multiple layers of conductive materials, comprising directing a focused ion beam toward the three dimensional integrated circuit structure at a non-normal angle to the layers of conductive material to expose multiple horizontal conductive layers; determining which exposed horizontal conductor corresponds to the vertical position of a component of interest; moving one or more electrical probes to contact the exposed horizontal conductor from above; applying a voltage to the electrical probe; and observing the effect of the applied voltage to analyze the region of interest.

**[0059]** In some embodiments, directing a focused ion beam toward the three dimensional integrated circuit structure includes directing the focused ion beam to leave the region of interest intact while expose multiple horizontal conductive layers to provide electrical access to the region of interest.

**[0060]** In some embodiments, moving one or more electrical probes to contact the exposed horizontal conductor includes moving one or more of the electrical probes to position the probe over the exposed horizontal conductor and then moving the probe in a direction having a vertical component to contact the exposed horizontal conductor.

**[0061]** In some embodiments, the three dimensional structure comprises a data storage circuit.

**[0062]** In some embodiments, the three dimensional structure comprises a Logic circuit and/or a NAND, a SRAM, a DRAM, or a memory cell.

**[0063]** Some embodiment provide a method of analyzing a region of interest in a three dimensional integrated circuit structure, comprising directing a focused ion beam toward the three dimensional integrated circuit structure to mill a surface exposing multiple horizontal conductive layers; determining which exposed horizontal conductive layer corresponds to the vertical position of a region of interest; lowering an electrical probe to contact a conductor that is in the determined horizontal conductive layer and that corresponds to a region of interest; applying a voltage to the electrical probe; and observing the effect of the applied voltage to analyze the region of interest.

**[0064]** In some embodiments, directing a focused ion beam toward the three dimensional integrated circuit structure to mill a surface exposing multiple horizontal conductive layers includes directing the focused ion beam normal to the work piece surface and the

embodiment further comprises tilting the work piece so that a normal to the milled surface has a vertical component.

**[0065]** In some embodiments, tilting the work piece includes tilting the work piece at an angle of between about 30° to about 45°.

**[0066]** In some embodiments, directing a focused ion beam toward the three dimensional integrated circuit structure to mill a surface exposing multiple horizontal conductive layers includes directing the focused ion beam at a non-normal angle to the horizontal conductive layers.

**[0067]** In some embodiments, directing the focused ion beam at a non-normal angle to the horizontal conductive layers includes directing the focused ion beam at an angle of between about 30° to about 45° to the horizontal conductive layers.

**[0068]** In some embodiments, observing the effect of the applied voltage to analyze the region of interest includes using voltage contrast imaging, sensing an electrical signal, or using an atomic force microscope probe.

**[0069]** In some embodiments, sensing an electrical signal comprises sensing a voltage or current using an electrical probe or probes.

**[0070]** Some embodiments provide a system for analyzing a region of interest in a three-dimensional integrated circuit, comprising an ion optical column for providing a focused beam of ions; an electron optical column for providing a focused beam of electrons; a particle detector for detecting secondary particles emitted from the sample; an electrical probe movable in three dimensions for contacting the integrated circuit and providing electrical contact to the region of interest; a controller communicating to a computer memory, the computer memory storing instructions for directing a focused ion beam toward the three dimensional integrated circuit structure to mill a surface exposing multiple horizontal conductive layers; determining which exposed horizontal conductive layer corresponds to the vertical position of a region of interest; lowering an electrical probe to contact a conductor that is in the determined horizontal conductive layer and that corresponds to a region of interest; applying a voltage to the electrical probe; and observing the effect of the applied voltage to analyze the region of interest.

**[0071]** In some embodiments, the computer instructions for directing the focused ion beam toward the three dimensional integrated circuit structure includes computer instruction for directing the focused ion beam at a non-normal angle to the horizontal conductive layers.

**[0072]** In some embodiments, the computer instructions for directing the focused ion beam

toward the three dimensional integrated circuit structure includes directing the focused ion beam normal to the work piece surface and further comprise computer instructions for tilting the work piece so that a normal to the milled surface has a vertical component.

**[0073]** Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

**[0074]** We claim as follows:

## CLAIMS

1. A method of analyzing a region of interest in a three dimensional integrated circuit structure having multiple layers of conductive materials, comprising:
  - directing a focused ion beam toward the three dimensional integrated circuit structure at a non-normal angle to the layers of conductive material to expose multiple horizontal conductive layers;
  - determining which exposed horizontal conductor corresponds to the vertical position of a component of interest;
  - moving one or more electrical probes to contact the exposed horizontal conductor from above;
  - applying a voltage to the electrical probe; and
  - observing the effect of the applied voltage to analyze the region of interest.
2. The method of claim 1 in which directing a focused ion beam toward the three dimensional integrated circuit structure includes directing the focused ion beam to leave the region of interest intact while expose multiple horizontal conductive layers to provide electrical access to the region of interest.
3. The method of claim 1 or claim 2 in which moving one or more electrical probes to contact the exposed horizontal conductor includes moving one or more of the electrical probes to position the probed over the exposed horizontal conductor and then moving the probe in a direction having a vertical component to contact the exposed horizontal conductor.
4. The method of any of claims 1 - 3 in which directing a focused ion beam at a non-normal angle to the layers of conductive material surface includes directing the focused ion beam at an angle of between about 30° to about 45° from a normal to the surface.
5. The method of any of claims 1 – 4 in which observing the effect of the applied voltage includes analyzing the region of interest using voltage contrast imaging, sensing an electrical signal, or using an atomic force microscope probe.
6. The method of claim 5 in which sensing an electrical signal comprises sensing a voltage or current using an electrical probe or probes.
7. The method of any of claims 1 – 6 in which the three dimensional structure comprises a data storage circuit.
8. The method of any of claims 1 – 7 in which the three dimensional structure comprises a Logic circuit and/or a NAND, a SRAM, a DRAM, or a memory cell.

9. A method of analyzing a region of interest in a three dimensional integrated circuit structure, comprising:

directing a focused ion beam toward the three dimensional integrated circuit structure to mill a surface exposing multiple horizontal conductive layers;

determining which exposed horizontal conductive layer corresponds to the vertical position of a region of interest;

lowering an electrical probe to contact a conductor that is in the determined horizontal conductive layer and that corresponds to a region of interest;

applying a voltage to the electrical probe; and

observing the effect of the applied voltage to analyze the region of interest.

10. The method of claim 9 in which directing a focused ion beam toward the three dimensional integrated circuit structure to mill a surface exposing multiple horizontal conductive layers includes directing the focused ion beam normal to the work piece surface and further comprising tilting the work piece so that a normal to the milled surface has a vertical component.

11. The method of claim 10 in which tilting the work piece includes tilting the work piece at an angle of between about 30° to about 45°.

12. The method of claim 9 in which directing a focused ion beam toward the three dimensional integrated circuit structure to mill a surface exposing multiple horizontal conductive layers includes directing the focused ion beam at a non-normal angle to the horizontal conductive layers.

13. The method of claim 12 in which directing the focused ion beam at a non-normal angle to the horizontal conductive layers includes directing the focused ion beam at an angle of between about 30° to about 45° to the horizontal conductive layers.

14. The method of any of claims 9 – 13 in which observing the effect of the applied voltage to analyze the region of interest includes using voltage contrast imaging, sensing an electrical signal, or using an atomic force microscope probe.

15. The method of claim 14 in which sensing an electrical signal comprises sensing a voltage or current using an electrical probe or probes.

16. A system for analyzing a region of interest in a three-dimensional integrated circuit, comprising:

an ion optical column for providing a focused beam of ions;

an electron optical column for providing a focused beam of electrons;

a particle detector for detecting secondary particles emitted from the sample;  
an electrical probe movable in three dimensions for contacting the integrated circuit and providing electrical contact to the region of interest;  
a controller communicating to a computer memory, the computer memory storing instructions for:  
directing a focused ion beam toward the three dimensional integrated circuit structure to mill a surface exposing multiple horizontal conductive layers;  
determining which exposed horizontal conductive layer corresponds to the vertical position of a region of interest;  
lowering an electrical probe to contact a conductor that is in the determined horizontal conductive layer and that corresponds to a region of interest;  
applying a voltage to the electrical probe; and  
observing the effect of the applied voltage to analyze the region of interest.

17. The system of claim 16 in which the computer instructors for directing the focused ion beam toward the three dimensional integrated circuit structure includes computer instruction for directing the focused ion beam at a non-normal angle to the horizontal conductive layers.

18. The system of claim 16 or 17 in which the computer instructors for directing the focused ion beam toward the three dimensional integrated circuit structure includes directing the focused ion beam normal to the work piece surface and further comprising computer instructions for tilting the work piece so that a normal to the milled surface has a vertical component.

1 / 7

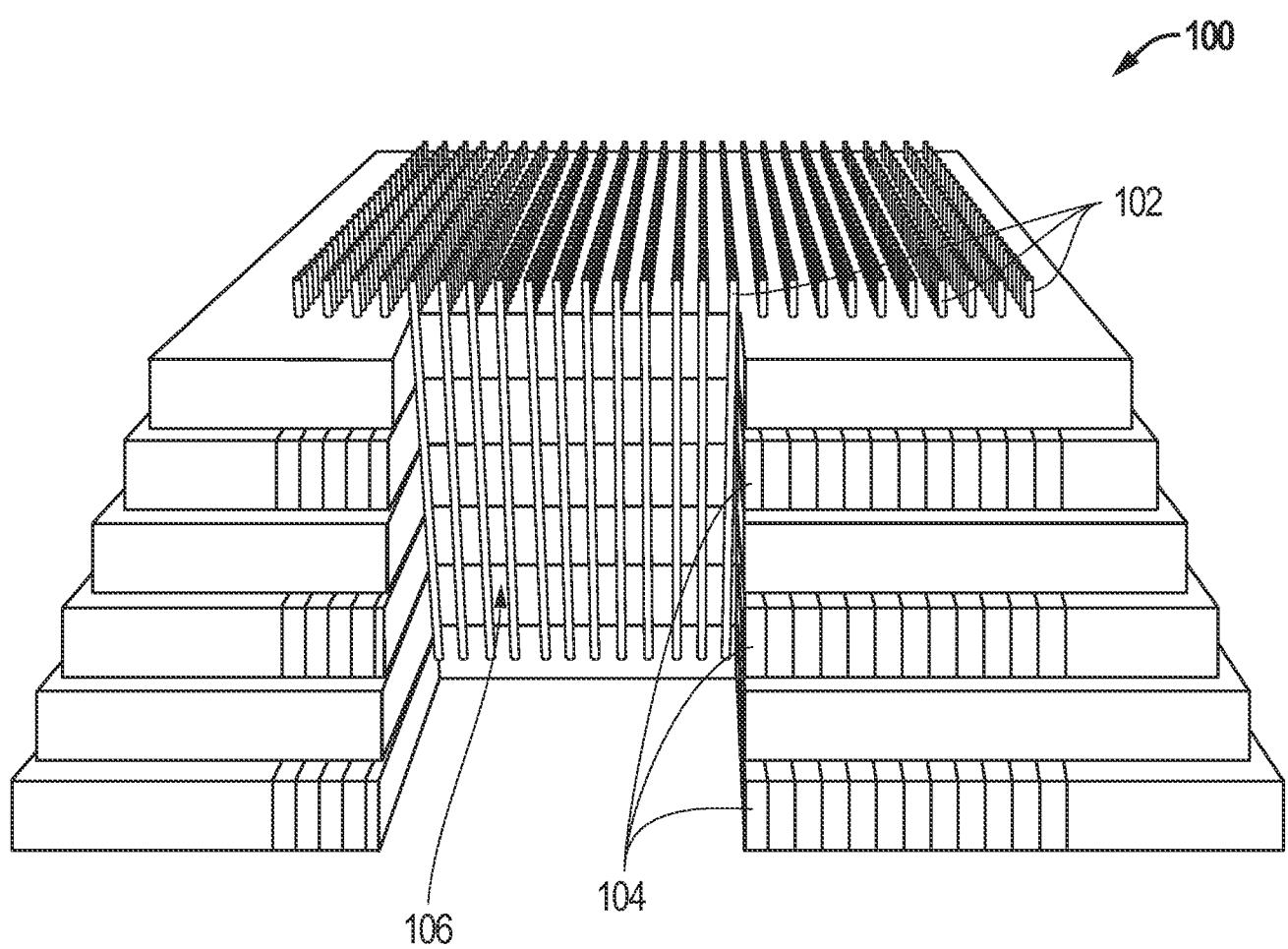


FIG. 1

2 / 7

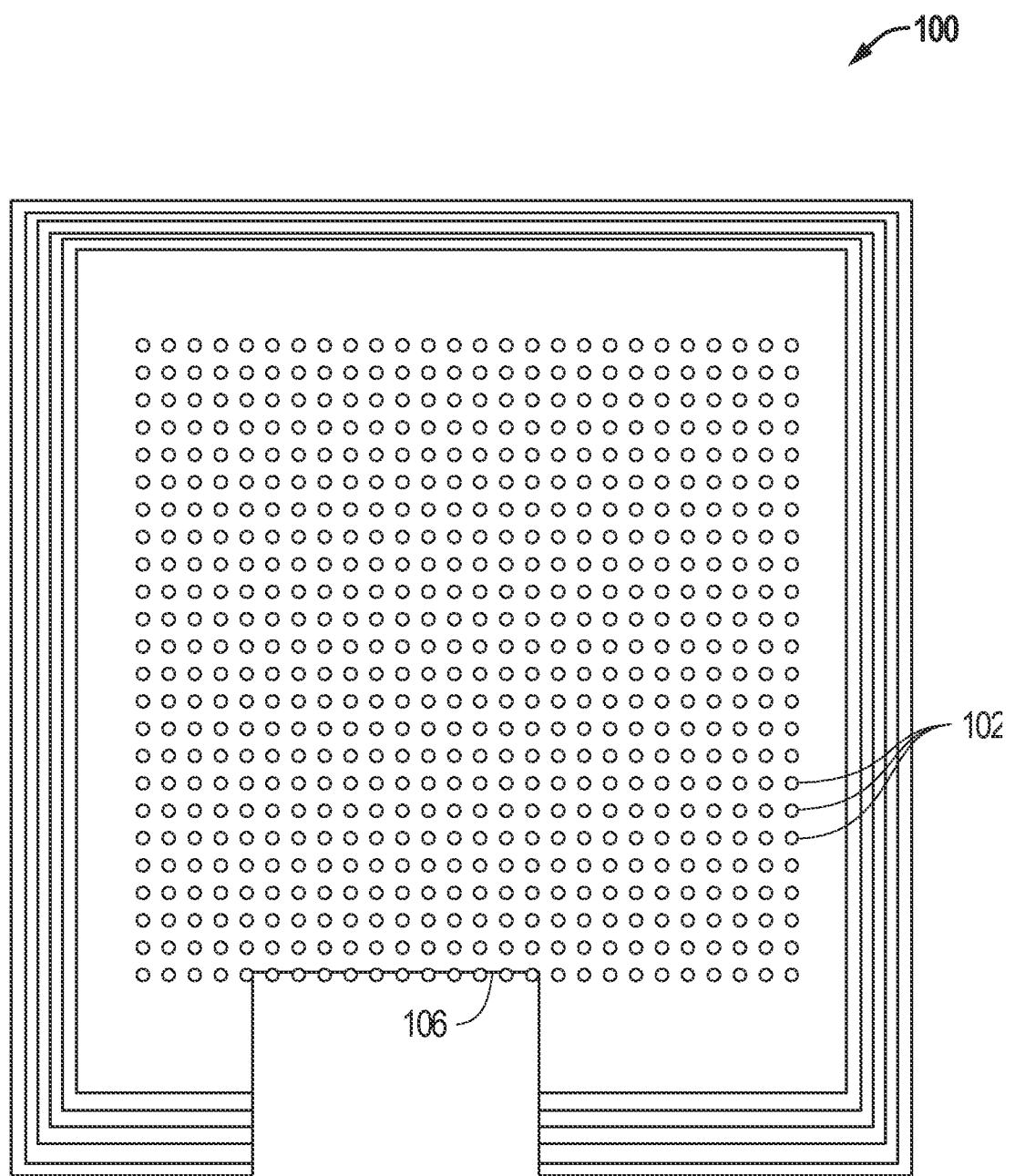


FIG. 2

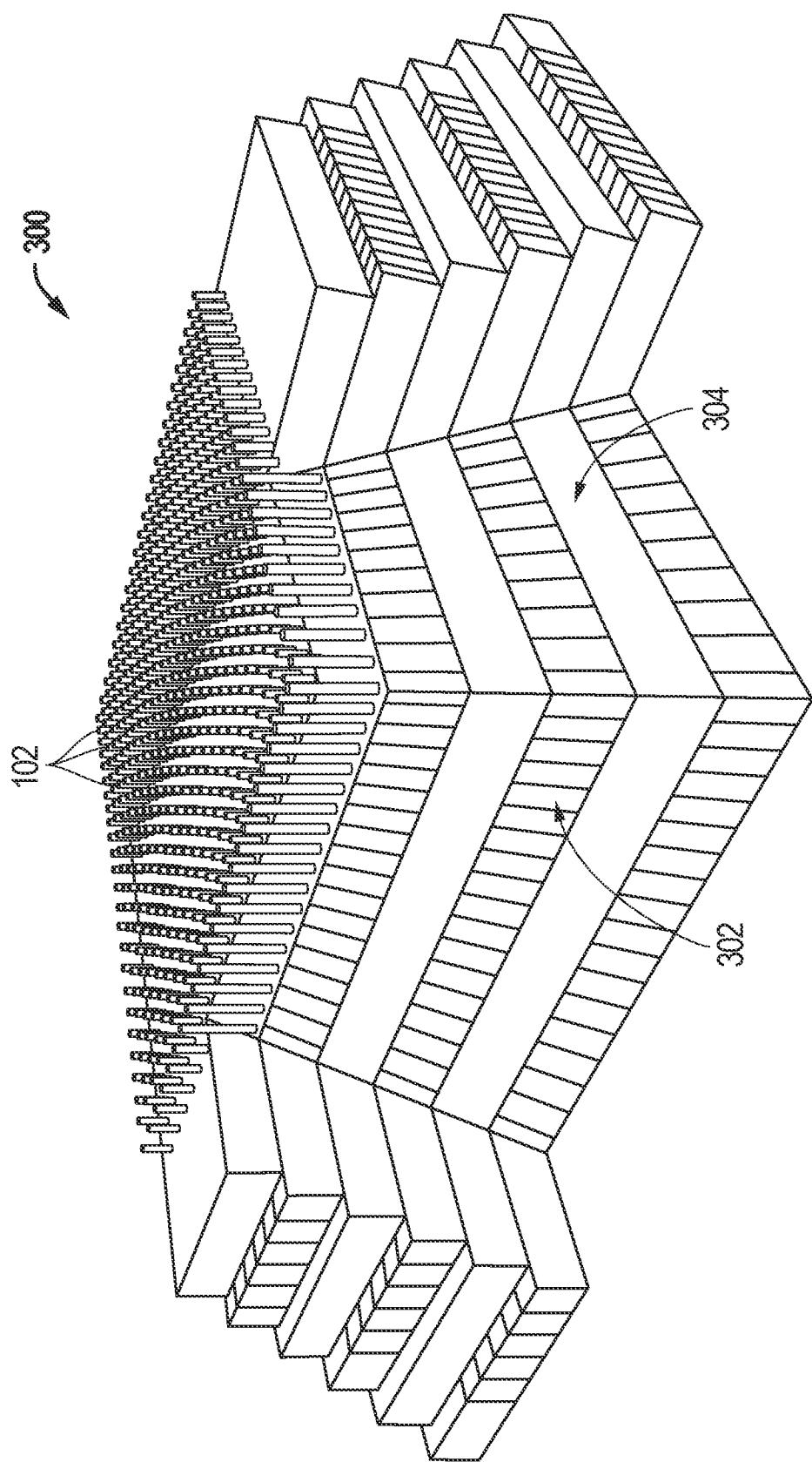


FIG. 3

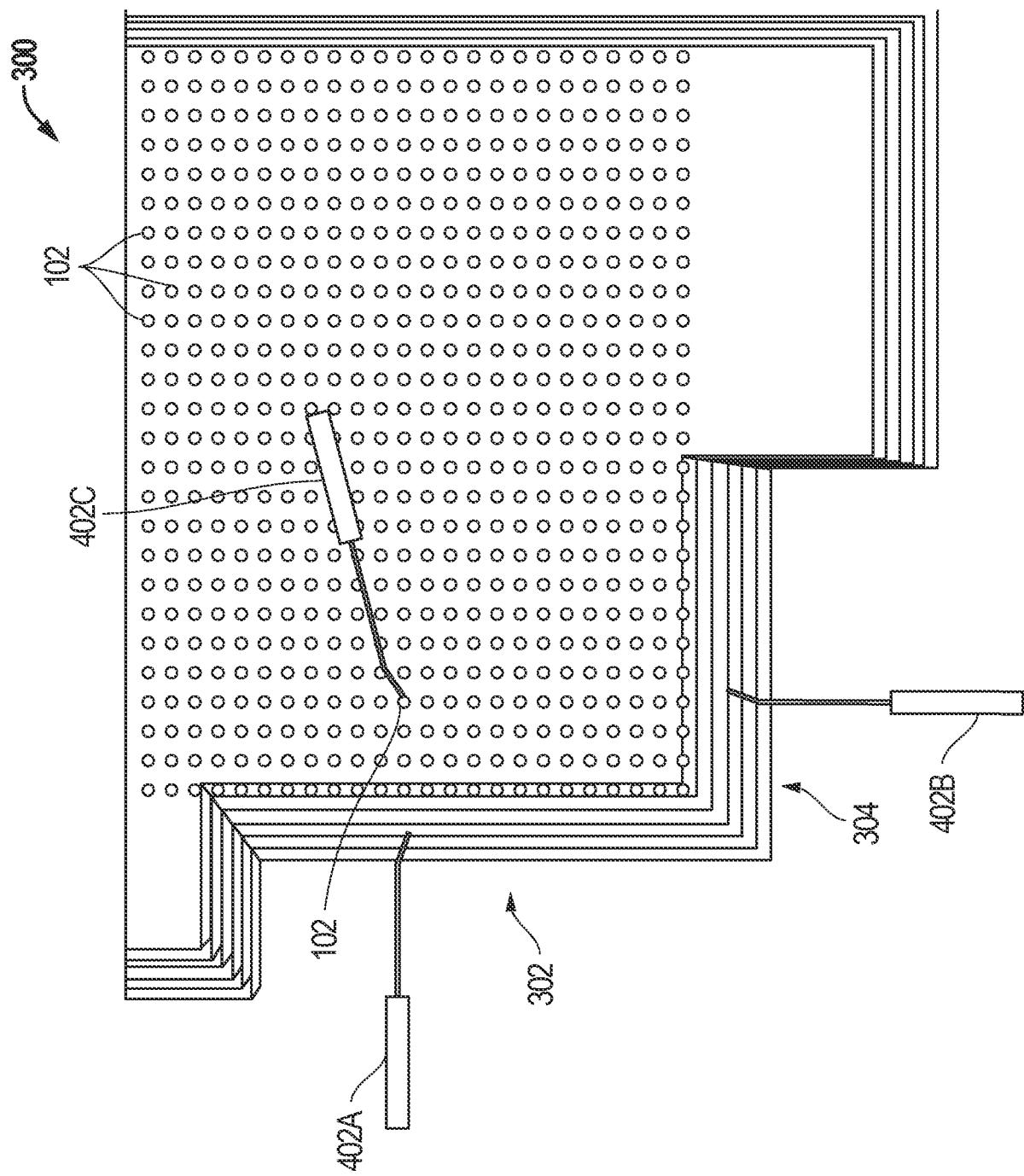


FIG. 4

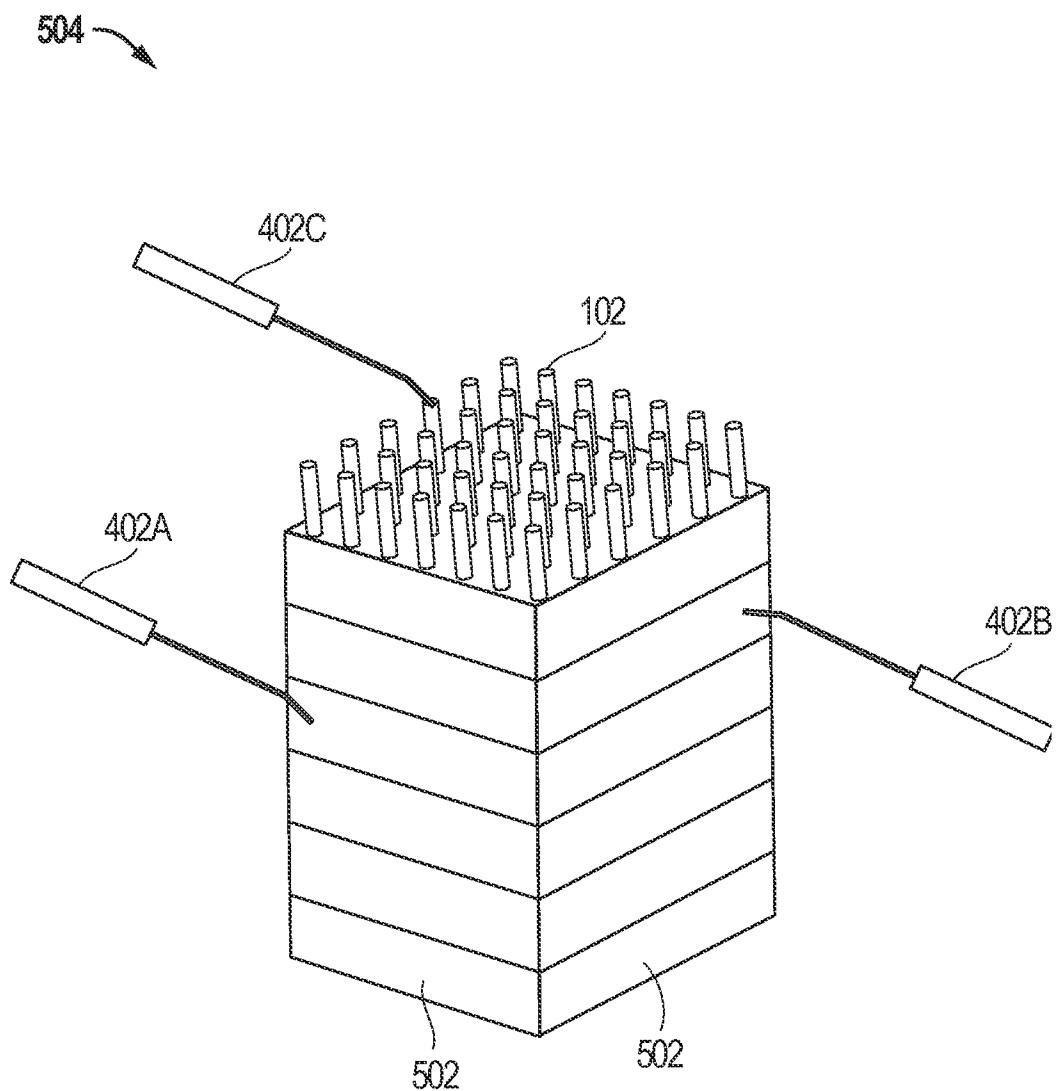


FIG. 5

6 / 7

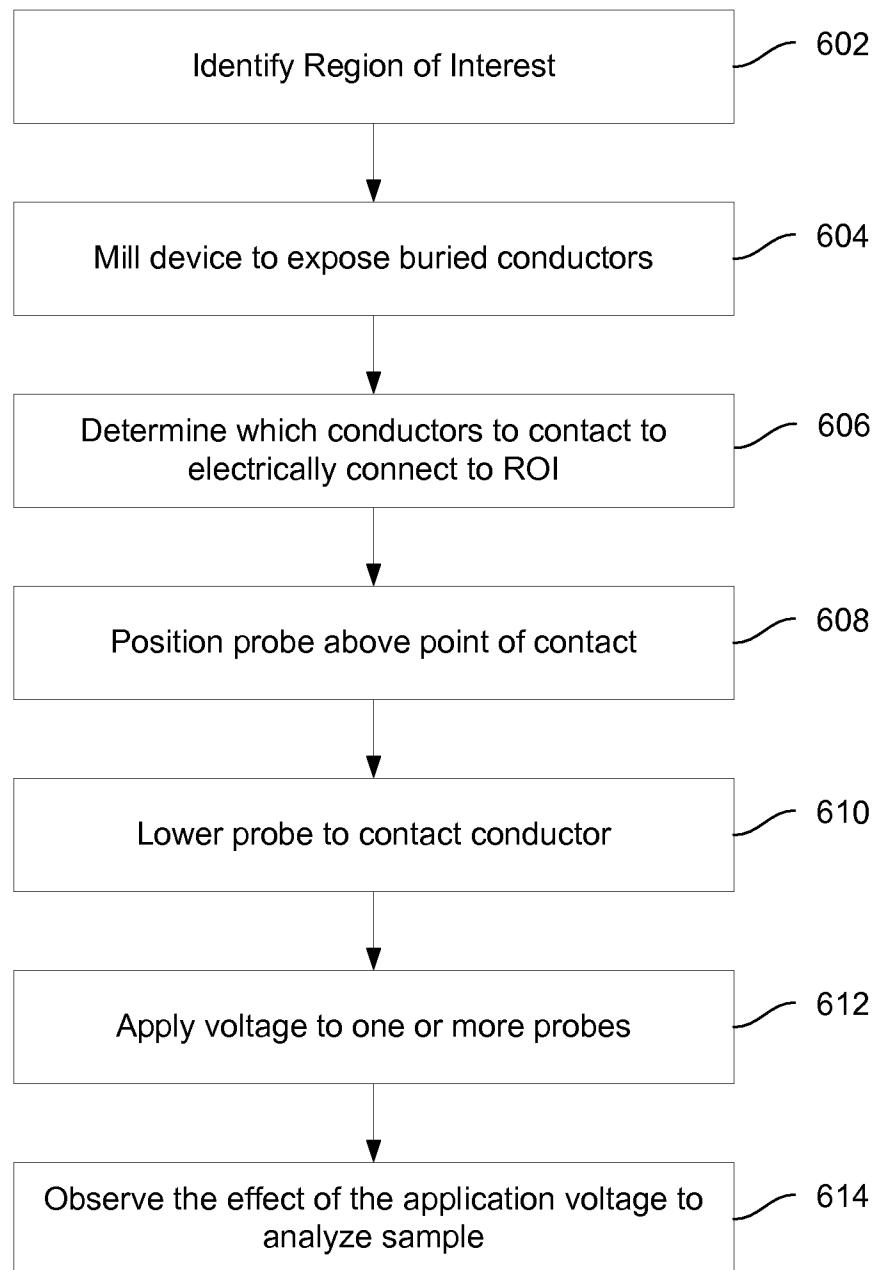


FIG. 6

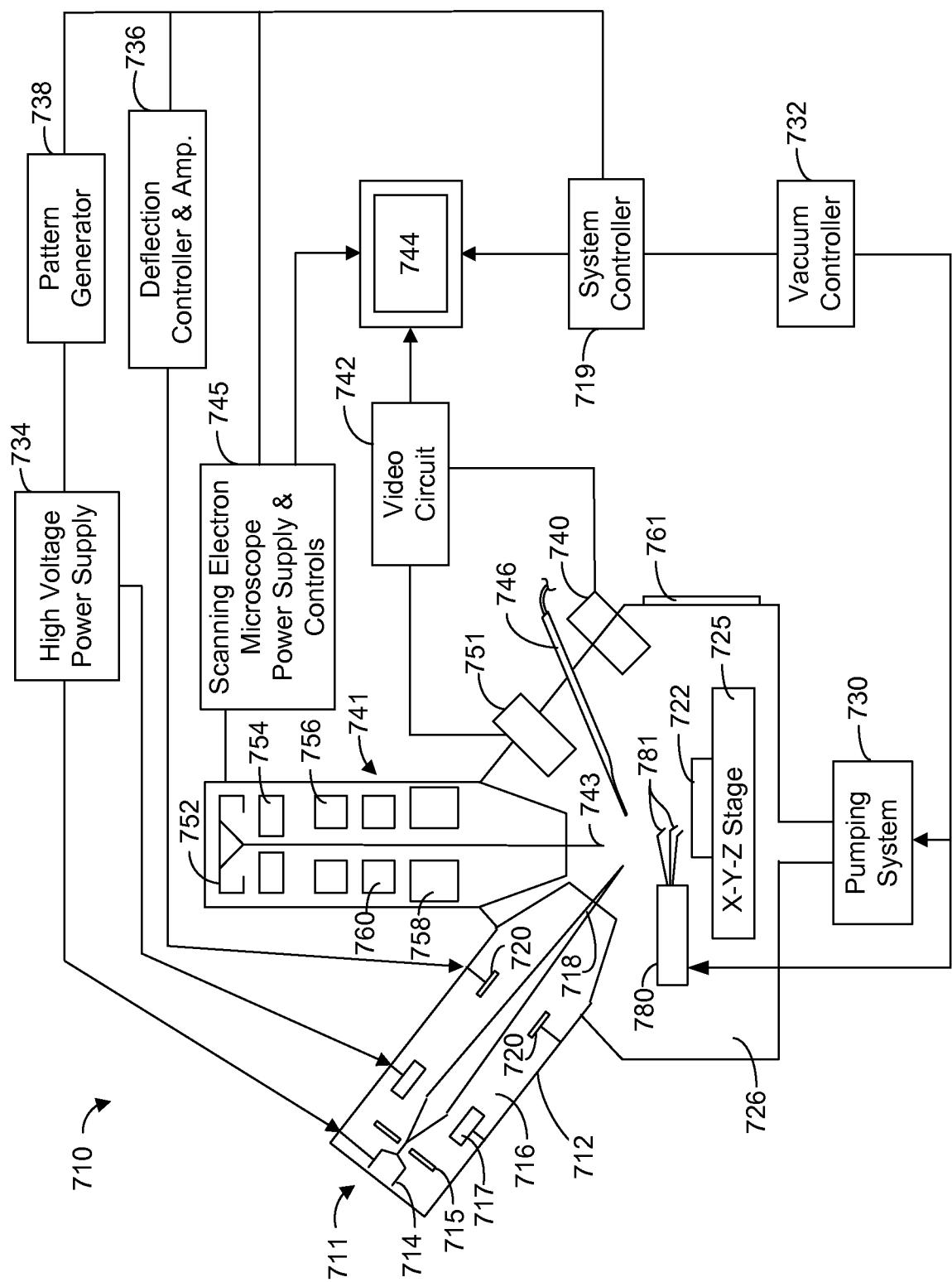


FIG. 7

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US2013/063556

## A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/66(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/66; G01R 31/26; G01R 31/28; H01J 37/305; G01N 23/00; H01J 37/20; G01B 11/28; H01L 21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
Korean utility models and applications for utility models  
Japanese utility models and applications for utility modelsElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
eKOMPASS(KIPO internal) & Keywords: ion beam, multiple layers, angle, probe, electric, milling and tilting

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2003-0086097 A1 (MOSHE FINAROV) 08 May 2003 See paragraphs [0004]-[0018], [0026]-[0055], claim 1 and figures 1, 3-4, 6B.	1-3, 9-18
Y	JP 2003-114252 A (HITACHI MAXELL LTD.) 18 April 2003 See paragraphs [0006]-[0051], claims 1-8 and figures 2-4.	1-3, 9-18
Y	US 2008-0245965 A1 (AKIYUKI SUGIYAMA et al.) 09 October 2008 See paragraphs [0029]-[0034], [0069]-[0072], claim 1 and figures 1-2, 9.	16-18
Y	JP 2012-113865 A (HITACHI HIGH-TECHNOLOGIES CORP.) 14 June 2012 See paragraphs [0019]-[0053], claims 1-6 and figures 1-3.	10-11, 18
A	US 2006-0292705 A1 (HARIHARAKESHAVE S. HEGDE et al.) 28 December 2006 See abstract, paragraphs [0023]-[0030] and figure 5.	1-3, 9-18

 Further documents are listed in the continuation of Box C. See patent family annex.

\* Special categories of cited documents:  
 "A" document defining the general state of the art which is not considered to be of particular relevance  
 "E" earlier application or patent but published on or after the international filing date  
 "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)  
 "O" document referring to an oral disclosure, use, exhibition or other means  
 "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention  
 "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone  
 "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art  
 "&" document member of the same patent family

Date of the actual completion of the international search  
17 February 2014 (17.02.2014)Date of mailing of the international search report  
**17 February 2014 (17.02.2014)**Name and mailing address of the ISA/KR  
Korean Intellectual Property Office  
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City,  
302-701, Republic of Korea  
Facsimile No. +82-42-472-7140Authorized officer  
CHOI, Sang Won  
Telephone No. +82-42-481-8291

**INTERNATIONAL SEARCH REPORT**International application No.  
**PCT/US2013/063556****Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.  Claims Nos.: because they relate to subject matter not required to be searched by this Authority, namely:
  
2.  Claims Nos.: 6 because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:  
Claim 6 is not clear, since it refers to multiple dependent claim 5 which does not comply with the third sentence of PCT Rule 6.4(a).
  
3.  Claims Nos.: 4-5, 7-8 because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

1.  As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
  
2.  As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
  
3.  As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
  
  
4.  No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2013/063556**

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003-0086097 A1	08/05/2003	IL 145699 A IL 145699 D0 US 2006-0176494 A1 US 7019850 B2 US 7289234 B2 WO 03-030250 A1	10/12/2006 30/06/2002 10/08/2006 28/03/2006 30/10/2007 10/04/2003
JP 2003-114252 A	18/04/2003	None	
US 2008-0245965 A1	09/10/2008	JP 2008-256541 A JP 4974737 B2 US 7772554 B2	23/10/2008 11/07/2012 10/08/2010
JP 2012-113865 A	14/06/2012	CN 103210467 A DE 112011103860 T5 KR 10-2013-0086046 A US 2013-0240353 A1 WO 2012-070517 A1	17/07/2013 14/08/2013 30/07/2013 19/09/2013 31/05/2012
US 2006-0292705 A1	28/12/2006	CN 101223584 A JP 2008-547150 A WO 2007-002011 A1	16/07/2008 25/12/2008 04/01/2007