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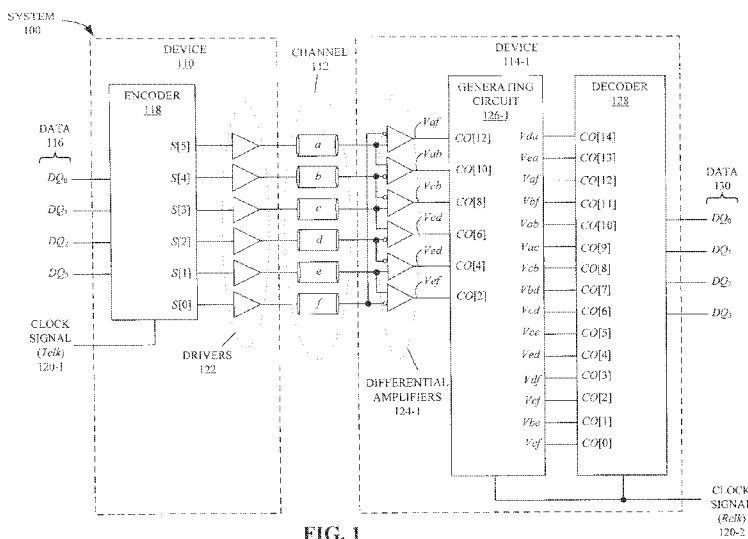


FIG. 1

(57) Abstract: Embodiments of a device that receives and decodes a series of parallel symbol sets over a series of time intervals is described. In this device, symbols in a respective parallel symbol set are received on nodes. Each node receives a respective symbol, which can have one of two possible logical values (e.g., a logic 0 or a logic 1). Differential amplifiers in the device provide primary comparison results, each of which compares symbols received on pairs of the links, and generation circuits in the device provide secondary comparison results from the primary comparison results. A decoder in the device decodes a respective parallel symbol set from the primary and secondary comparison results to recover encoded data.

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# RECEIVER FOR MULTI-WIRE COMMUNICATION WITH REDUCED INPUT CAPACITANCE

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## TECHNICAL FIELD

[001] Digital communication systems convey data over one or more conductors as varying voltages or currents that represent the data as series of symbols. Over a single wire, for  
10 example, relatively low and high voltages can be used to represent a logic '0' and a logic '1,' respectively. (This form of signaling is commonly referred to as 'single-ended signaling.' Also common, 'differential signaling' conveys logic '0' and '1' using complementary voltages on pairs of signal wires.) The bandwidth of a given communication channel is generally limited by the speed at which voltage or current expressing the '0' or '1' symbols  
15 can transition between logic levels (*e.g.*, between relatively high and low voltages or currents).

[002] Multi-wire communication (which is also referred to as 'vector signaling') has been proposed as a way to increase channel bandwidth. As used herein, 'vector signaling' refers to encoding methods in which successive sets of  $N$  symbols are each encoded into an  $M$ -  
20 symbol vector, where  $M$  is greater than  $N$ . Each of the  $N$  symbols is encoded such that decoding any given symbol requires consideration of more than two symbols in each codeword, or 'vector.' In contrast, decoding a single-ended signal requires consideration of just one level against a reference, and decoding differential signals requires consideration of just two complementary levels. Decoding vector signals thus requires relatively more  
25 complex receive circuitry as compared with single-ended or differential signals.

Furthermore, this added complexity grows rapidly as the number of wires increases. For example, many proposed multi-wire communication techniques include  $M(M-1)/2$  amplifiers at the receiver, where  $M$  is the number of symbols in each codeword and is the number of  
wires. Thus, for six wires there may be 15 amplifiers, for eight wires there may be 28  
30 amplifiers, and for ten wires there may be 45 amplifiers. This large number of amplifiers increases the complexity, power consumption and cost of the receiver. Moreover, parasitic capacitance on the wires increases as the number amplifiers is increased, which can, paradoxically, reduce the communication bandwidth.

**BRIEF DESCRIPTION OF THE FIGURES**

[003] FIG. 1 is a block diagram illustrating a system that encodes and decodes four-bit data  $DQ[3:0]$  in accordance with one embodiment.

5 [004] FIG. 2A is a time sequence illustrating how an embodiment of an encoder in the system of FIG. 1 implements the coding technique of Table 1 to encode a sequence of four-symbol data patterns  $DQ[3:0]$  into a series of parallel symbol sets  $S[5:0]$  to be conveyed on links  $a$  through  $f$ .

[005] FIG. 2B is a flowchart depicting the operation of an encoder of FIG. 1 in accordance  
10 with the coding technique of Table 1.

[006] FIG. 3A is a time sequence illustrating how an embodiment of a decoder in the system of FIG. 1 implements the coding technique of Table 1 to decode parallel symbol sets  $S[5:0]$  conveyed on links  $a$  through  $f$ .

[007] FIG. 3B is a flowchart depicting the operation of a generating circuit and a decoder of  
15 FIG. 1 in accordance with the coding technique of Table 1.

[008] FIG. 4A is a block diagram illustrating a device in the system of FIG. 1 that decodes four-bit data  $DQ[3:0]$  in accordance with one embodiment.

[009] FIG. 4B is a block diagram illustrating a device in the system of FIG. 1 that decodes four-bit data  $DQ[3:0]$  in accordance with one embodiment.

20 [010] FIG. 4C is a block diagram illustrating a device in the system of FIG. 1 that decodes four-bit data  $DQ[3:0]$  in accordance with one embodiment.

[011] FIG. 5 is a block diagram illustrating a circuit that compares symbols received on two links in the system of FIG. 1 in accordance with one embodiment.

[012] FIG. 6A is a block diagram illustrating a circuit that compares symbols received on a  
25 pair of links in the system of FIG. 1 in accordance with one embodiment.

[013] FIG. 6B is a block diagram illustrating a circuit that compares symbols received on a pair of links in the system of FIG. 1 in accordance with one embodiment.

[014] FIG. 7A is a block diagram illustrating an analog latch in the device of FIG. 4C in accordance with one embodiment.

30 [015] FIG. 7B is a block diagram illustrating an analog latch in the device of FIG. 4C in accordance with one embodiment.

[016] FIG. 8A is a block diagram illustrating a system that communicates data in accordance with one embodiment.

[017] FIG. 8B is a block diagram illustrating a system that communicates data in accordance with one embodiment.

[018] FIG. 9 is a graph of relative line power versus termination to a common node in accordance with one embodiment.

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### DETAILED DESCRIPTION

[019] FIG. 1 presents a block diagram illustrating a system 100 that includes a device 110 and a device 114-1 connected by a communication channel 112. A vector encoder 118 encodes four-bit data  $DQ[3:0]$  116 sampled on edges of an internal or external clock signal ( $Tclk$ ) 120-1 into a series of parallel codewords  $S[5:0]$ . The resulting codewords  $S[5:0]$  are transmitted as amplitude-modulated signals by single-ended drivers 122 over corresponding links  $a, b, c, d, e$  and  $f$  of the channel. Each codeword  $S[5:0]$  is expressed as two sets of equal-length symbols, one representing logic 0s on a first group of links (e.g.,  $S[4:2] = 000$  on links  $b, c$  and  $d$  of channel 112) and another representing logic 1s on the remaining links (e.g.,  $S[5] = 1$  on link  $a$  and  $S[1:0] = 11$  on links  $e$  and  $f$ ). Thus, each codeword is balanced. Differential amplifiers 124-1 in device 114-1 (and, more generally, comparison circuits) compare the parallel symbols received on six pairs of links  $a, b, c, d, e$  and  $f$ , and output these primary comparisons as analog voltages to even nodes  $CO[12:2]$  of generating circuit 126-1. Each different amplifier output is named for the links it compares. For example, differential amplifier output  $Vaf$  is: a positive analog voltage if the signal on link  $a$  is higher than the signal on link  $f$ , a negative analog voltage if the signal on link  $a$  is lower than the signal on link  $f$ , and is approximately zero if the signals on links  $a$  and  $f$  are the same.

[020] Generating circuit 126-1 derives nine analog secondary comparisons for additional pairs of received signals from the primary comparisons rather than directly from the received link pairs, and delivers the resultant fifteen primary and secondary comparisons to nodes  $CO[14:0]$  of decoder 128 (or an equivalent means for decoding). For example, differential amplifiers in generating circuit 126-1 may derive the analog secondary comparisons by taking differences of the analog primary comparisons. Deriving the secondary comparisons from the primary comparisons reduces the requisite number of differential amplifiers directly coupled to the links. Decoder 128 thresholds and samples the fifteen analog outputs from generating circuit 126-1 on edges of a clock signal ( $Rclk$ ) 120-2 to obtain digital values, such as logical 0s and 1s. Furthermore, decoder 128 decodes the resultant digital sample sets to recover data  $DQ[3:0]$  130. The total number of comparisons is fifteen in this example (and,

25  
30

more generally,  $M(M - 1)/2$ , where  $M$  is the number of links), but other embodiments can have more or fewer.

[021] In a typical example, devices 110 and 114-1 are respective integrated circuits (ICs), such as a memory IC that includes one or more arrays of dynamic, random-access memory (DRAM) and a memory controller IC, respectively. The following discussion refers to elements  $a$  through  $f$  alternatively as ‘links’ or ‘nodes.’ The former refers to the entire AC- or DC-coupled signal path between encoder 118 and differential amplifiers 124-1, whereas the latter refers to an input or output pin, wire, or terminal.

[022] The use of generating circuit 126-1 to generate the secondary comparisons from the primary comparisons reduces the number of differential amplifiers coupled to each of links  $a$  through  $f$  from five to two, which reduces the input capacitance of device 114-1. In addition, by reducing the number of differential amplifiers coupled to links  $a$  through  $f$ , the input nodes can be arranged to minimize the impact of routing in device 114-1. In a typical example, the capacitance for a memory IC is reduced from 1500 to 1000 fF, and the capacitance for a memory controller IC is reduced from 900 to 600 fF. In conjunction with vector (or “multi-wire”) signaling on links  $a$  through  $f$ , this reduced capacitance facilitates an increase in the communication bandwidth between devices 110 and 114-1.

[023] Table 1 illustrates a codespace with twenty balanced codewords, which have an equal number of 0s and 1s, and which may be communicated in parallel across six links or nodes. (For six links and binary symbols in each codeword, there are a total of 64 possible codewords, most of which are not balanced. The twenty balanced codewords are more than sufficient to communicate the sixteen possible combinations of four binary symbols.) For example, for codeword nine (CW#9), data  $DQ[3:0]$  116 is 1001 and is encoded as  $S[5:0]$  of 100011.

Codeword Number (CW#)	Data $DQ[3:0]$ 116	Codeword $S[5:0]$ for links $a b c d e f$	Differential Amplifiers 124-1 and Generating Circuit 126-1 Outputs $a-b a-c d-a e-a a-f c-b b-d b-e b-f c-d c-e c-f e-d d-f e-f$
0	0000	1 1 1 0 0 0	0   0   -1   -1   1   0   1   1   1   1   1   1   0   0   0
1	0001	1 1 0 1 0 0	0   1   0   -1   1   -1   0   1   1   -1   0   0   -1   1   0
2	0010	1 1 0 0 1 0	0   1   -1   0   1   -1   1   0   1   0   -1   0   0   0     1

3	0011	1 1 0 0 0 1	0   1   -1   -1   0   -1   1   1   0   0   0   -1   0   -1   -1
4	0100	1 0 1 1 0 0	1   0   0   -1   1   1   -1   0   0   0   1   1   -1   1     0
5	0101	1 0 1 0 1 0	1   0   -1   0   1   1   0   -1   0   1   0   1   1   0     1
6	0110	1 0 1 0 0 1	1   0   -1   -1   0   1   0   0   -1   1   1   0   0   -1   -1
7	0111	1 0 0 1 1 0	1   1   0   0   1   0   -1   -1   0   -1   -1   0   0   1   1
8	1000	1 0 0 1 0 1	1   1   0   -1   0   0   -1   0   -1   -1   0   -1   -1   0   -1
9	1001	1 0 0 0 1 1	1   1   -1   0   0   0   0   -1   -1   0   -1   -1   1   -1   0
10	1010	0 1 1 1 0 0	-1   -1   1   0   0   0   0   1   1   0   1   1   -1   1     0
11	1011	0 1 1 0 1 0	-1   -1   0   1   0   0   1   0   1   1   0   1   1   0     1

Table 1

Codeword Number (CW#)	Data DQ[3:0] 116	Codeword S[5:0] for links a b c d e f	Differential Amplifiers 124-1 and Generating Circuit 126-1 Outputs a-b a-c d-a e-a a-f c-b b-d b-e b-f c-d c-e c-f e-d d-f e-f
12	1100	0 1 1 0 0 1	-1   -1   0   0   -1   0   1   1   0   1   1   0   0   -1     -1
13	1101	0 1 0 1 1 0	-1   0   1   1   0   -1   0   0   1   -1   -1   0   0   1     1
14	1110	0 1 0 1 0 1	-1   0   1   0   -1   -1   0   1   0   -1   0   -1   -1   0   -1
15	1111	0 1 0 0 1 1	-1   0   0   1   -1   -1   1   0   0   0   -1   -1   1   -1   0
16	—	0 0 1 1 1 0	0   -1   1   1   0   1   -1   -1   0   0   0   1   0   1     1
17	—	0 0 1 1 0 1	0   -1   1   0   -1   1   -1   0   -1   0   1   0   -1   0

			-1
18	—	0 0 1 0 1 1	0   -1   0   1   -1   1   0   -1   -1   -1   0   0   1   -1   0
19	—	0 0 0 1 1 1	0   0   1   1   -1   0   -1   -1   -1   -1   -1   0   0   0

Table 1 (continued)

[024] In Table 1, the output voltages from the six differential amplifiers 124-1 are identified as node comparisons. For example, the output of amplifier  $V_{af}$  is proportional to the difference between the voltages on nodes  $a$  and  $f$ . The term ‘ $a-f$ ’ in Table 1 thus corresponds to an analog signal on the output node of amplifier  $V_{af}$  that represents a comparison of nodes  $a$  and  $f$ . The term ‘ $a-f$ ’ is one of six primary comparisons based upon considerations of nodes  $a$  through  $f$ . Generating circuit 126-1 includes additional differential amplifiers (not shown) that derive nine secondary comparisons based upon the six primary comparisons. For example, secondary comparison  $V_{ac}$  may be derived from primary comparisons  $V_{ab}$  and  $V_{cb}$ .

In particular,  $V_{ac}$  equals  $V_{ab} - V_{cb}$ . Thus, if  $V_{ab} = 1$  and  $V_{cb} = 0$ ,  $V_{ac} = 1$ . Similarly, if  $V_{ab} = 0$  and  $V_{cb} = -1$ ,  $V_{ac} = 1$ . In general, a respective secondary voltage can be derived from the sum or difference of two or more of the primary comparisons. The resulting fifteen comparisons are labeled  $V_{xx}$  in FIG. 1 and extend from generating circuit 126-1 to decoder 128.

[025] As shown in Table 1, each of the differential amplifiers in differential amplifiers 124-1 and generating circuit 126-1 can have one of three analog output values. Using the rightmost column, for example, differential-amplifier output voltage  $V_{ef}$ , which compares inputs  $e$  and  $f$ , is:

1. a negative analog voltage denoted by ‘-1’ (e.g., a negative voltage  $-V_p$ ) when symbols  $S[1]$  and  $S[0]$  on respective nodes  $e$  and  $f$  express logic values of 0 and 1, respectively;
2. a positive analog voltage denoted by ‘1’ (e.g., a positive voltage  $+V_p$ ) when nodes  $e$  and  $f$  express logic values of 1 and 0, respectively; and
3. an intermediate voltage denoted by ‘0’ (e.g., 0 V), when nodes  $e$  and  $f$  express like logic values (i.e., are both 1 or both 0).

[026] Of the fifteen primary and secondary comparisons  $V_{12}$  output by differential amplifiers 124-1 and generating circuit 126-1 for each codeword  $S[5:0]$ , six are intermediate voltages  $V_{int}$ . Each of the remaining nine voltages are positive or negative voltage  $\pm V_p$ .

Decoder 128 samples each of the fifteen values and decodes the resulting fifteen-bit digital value to recover the encoded four-bit data  $DQ[3:0]$  130. While in general  $M(M-1)/2$  comparisons are used by decoder 128, as detailed below, in one embodiment decoder 128 takes advantage of redundancy in the outputs from the differential amplifiers for different  
5 codewords to reduce the required number of differential amplifiers, which reduces the complexity and power consumption of device 114-1.

[027] FIG. 2A presents a time sequence 200 illustrating how an embodiment of encoder 118 of FIG. 1 implements the coding technique of Table 1 to encode a sequence of four-symbol data patterns  $DQ[3:0]$  116 into a series of parallel symbol sets  $S[5:0]$ . As noted previously,  
10 the bit positions of symbols  $S[5:0]$  correspond to respective links  $a, b, c, d, e$  and  $f$  (e.g.,  $S[5]$  is the logic value expressed on link  $a$ ). In the series of time intervals  $T_0$ - $T_9$  of FIG. 2A, data  $DQ[3:0]$  in each time interval is encoded into a corresponding codeword. Beginning at time  $T_0$ , the first data 1001 is expressed using codeword nine ( $CW\#9$ ), which has symbols  $S[5:0] = 100011$ . Then, at time  $T_1$ , data 1100 is expressed using codeword twelve ( $CW\#12$ ), which  
15 has symbols  $S[5:0] = 011001$ . Next, at time  $T_2$ , data 1111 is expressed using codeword fifteen ( $CW\#15$ ), which has symbols  $S[5:0] = 010011$ . This process is continued in subsequent time intervals.

[028] FIG. 2B presents a flowchart 250 depicting the operation of encoder 118 of FIG. 1 in accordance with the coding technique of Table 1. Beginning the encoding sequence at  
20 operation 260, encoder 118 receives data  $DQ[3:0]$  116. Then, at operation 265, encoder 118 encodes data  $DQ[3:0]$  116 as a corresponding codeword in accordance with Table 1, for example using a lookup table implemented in a *RAM*, *ROM* or by combinational logic, and outputs the symbols in the codeword  $S[5:0]$ . Next, at operation 270, encoder 118 awaits the next sequence of data  $DQ[3:0]$  116. The flow of operations 260 through 270 repeats for each  
25 successive codeword.

[029] FIG. 3A presents a time sequence 300 illustrating how an embodiment of decoder 128 of FIG. 1 reverses the coding technique of Table 1 to decode received parallel symbol sets  $CO[14:0]$  into data  $DQ[3:0]$  130. Decoder 128 receives outputs the primary and secondary comparisons output from generating circuit 126-1 as a series of fifteen-symbol sets  $CO[14:0]$ ,  
30 and determines the corresponding codeword (and thus, data  $DQ[3:0]$  130) in accordance with Table 1. FIG. 3A illustrates the symbol sets  $CO[14:0]$  after analog-to-digital conversion (e.g., after decoder 128 samples the primary and secondary comparisons). During this process, negative analog voltages are designated as logical 0s and positive analog voltages are designated as logical 1s. However, the analog voltages near zero volts (which are

compared to a threshold near zero volts) will be designated as either a logical 0 or a logical 1 value. Consequently, the digital samples corresponding to each of these analog voltages are indeterminate. These digital samples, which are denoted by 'x,' will be either a logical 0 or a logical 1.

5 **[030]** In the series of time intervals  $T_0$ - $T_9$  of FIG. 3A, parallel set of comparisons  $CO[14:0]$  in each time interval is decoded into corresponding data  $DQ[3:0]$  130, for example using a lookup table implemented in a *RAM*, *ROM* or by combinational logic. Beginning at time  $T_0$ , symbol set  $CO[14:0] = [0\ x\ x\ 0\ 1\ 1\ x\ x\ x\ 0\ 1\ 0\ x\ 0\ 0]$  specifies codeword nine ( $CW\#9$ ), which represents data  $DQ[3:0]$  130 of 1001. Then, at time  $T_1$ , symbol set  $CO[14:0] = [x\ x\ 0\ x\ 0\ 0\ x$   
 10  $1\ 1\ 1\ x\ 0\ 0\ 1\ x]$  specifies codeword twelve ( $CW\#12$ ), which represents data  $DQ[3:0]$  130 of 1100. Next, at time  $T_2$ , symbol set  $CO[14:0] = [x\ 1\ 0\ x\ 0\ x\ 0\ 1\ x\ 0\ 1\ 0\ x\ x\ 0]$  specifies codeword fifteen ( $CW\#15$ ), which represents data  $DQ[3:0]$  130 of 1111. This process is continued in subsequent time intervals.

**[031]** The non-x values in the symbol sets  $CO[14:0]$  provide sufficient information to  
 15 uniquely identify each codeword, and thus each  $CW\#$ . In Table 1, the zero values represent the intermediate values that produce 'x' values in the table of FIG. 3A. With reference to  $CW\#9$  in Table 1, each set of comparison outputs includes at least one determinate, non-zero value that distinguishes it from every other set. For example, contrasting two sets of  
 20 comparisons for codewords  $CW\#9$  with  $CW\#8$ , most of the corresponding comparisons are either representative of the same value (e.g., comparison  $a-b$  is '1' for both codewords) or include one indeterminate intermediate '0' value (e.g., comparison  $d-a$  is '0' in  $CW\#8$ ). However, the third to last comparison,  $e-d$ , plainly distinguishes codewords  $CW\#9$  with  
 25  $CW\#8$  without resort to an intermediate '0' value. This third to last value comparison is sufficient to distinguish  $CW\#9$  from  $CW\#8$ . Other comparisons similarly distinguish  
 30 codeword  $CW\#9$  from the remaining codewords. More generally, each codeword produces a set of comparisons that includes at least one assuredly different comparison for each of the other sets of comparisons. Decoder 128 can thus resolve each codeword, and consequently the encoded data, despite the indeterminate values of a subset of the comparisons.

**[032]** FIG. 3B presents a flowchart 350 depicting the operation of generating circuit 126-1  
 30 and decoder 128 of FIG. 1 in accordance with the coding technique of Table 1. Beginning the decoding sequence at operation 360, generating circuit 126-1 receives six primary comparisons from differential amplifiers 124-1. Then, at operation 365, generating circuit 126-1 derives the remaining nine secondary comparisons from the primary comparisons. For example, generating circuit 126-1 derives  $V_{ac}$  by taking the difference of  $V_{ab}$  and  $V_{cb}$ .

Next, at operation 370, decoder 128 samples the fifteen primary and secondary comparisons from generating circuit 126-1 for each codeword. Then, at operation 375, decoder 128 decodes them to produce the encoded data  $DQ[3:0]$  130. Next, at operation 380, decoder 128 awaits the next series of fifteen-symbol sets  $CO[14:0]$ . The flow of operations 360 through 5 380 repeats for each successive parallel symbol set.

**[033]** As shown in FIG. 4A, which presents device 114-2 in accordance with another embodiment of system 100 (FIG. 1) that decodes four-bit data  $DQ[3:0]$  130 (FIG. 1), primary comparisons of symbols received on pairs of nodes 410 that are output by differential amplifiers 124-1 may be sampled by analog latch 412-1 (*i.e.*, a sample-and-hold circuit).

10 Device 114-2 is similar to device 114-1 of FIG. 1, with like-identified elements being the same or similar. The secondary comparisons may be generated using one or more additional stages of differential amplifiers, such as differential amplifiers 124-2 (thus, generating circuit 126-1 may include one or more additional stages of differential amplifiers). These additional stages of differential amplifiers may be separated by optional analog latch 412-2. However, 15 if the delays associated with the differential amplifiers 124 in a given stage are matched, analog latches after a first stage of analog latches may not be needed because this first stage may synchronize the comparison signals. The matching of delays through different amplifiers or wires in a given stage or succession of stages without intermediate latches is determined by the requirement that the parallel output signals must be simultaneously present 20 for some minimum duration so that the eventual next latch or decoder 128 can consistently observe all of the signals. Furthermore, the delays associated with the differential amplifiers 124 in a given stage may be matched using optional buffers, such as optional buffer 414.

**[034]** While device 114-1 (FIG. 1) and 114-2 illustrate the use of differential amplifiers 124 that compare symbols on pairs of links, in some embodiments differential amplifiers that each 25 compare a respective symbol on a respective link to a common reference voltage may be used in one or more of the stages. This is shown in FIG. 4B, which presents a device 114-3 in accordance with another embodiment of system 100 (FIG. 1) that decodes four-bit data  $DQ[3:0]$  130 (FIG. 1). Device 114-3 is similar to device 114-1 of FIG. 1 and device 114-2 of FIG. 4A, with like-identified elements being the same or similar. In device 114-3, 30 differential amplifiers 416 each receive a signal from one of nodes 410 and each receive a reference voltage ( $V_{ref}$ ) 418, which can be generated on-chip (*i.e.*, on the *IC*) or off-chip. (Thus, differential amplifiers 416 each compare an input signal present on a single link to a common reference, as opposed to a complementary signal or another multi-wire signal.) As in device 114-2 (FIG. 4A), analog outputs from differential amplifiers 416 may be

compared in differential amplifiers 124-1. The use of differential amplifiers 416 reduces the number of amplifiers coupled to a given link to one, thereby reducing the on-chip routing and the capacitance of device 114-3.

[035] Receiving the parallel symbol set on links *a* through *f* can be complicated by differences or skew in the arrival times of two or more symbols on different links (for example, due to trace length differences from geometric constraints on *IC* package routing and printed circuit board routing). This problem is compounded in vector signaling because the arrival times of symbols on multiple links needs to be controlled. For example, over six links these routing constraints can result in a trace length mismatch of as much as 5 mm between links on the outside of channel 112 in FIG. 1, which can correspond to as much as 35 ps of skew between two of the symbols in a respective symbol set.

[036] Skew may be reduced or eliminated by adjusting the transmit phase, the receive phase or both. Receive phase adjustment is shown in FIG. 4C, which presents device 114-4 in accordance with another embodiment of system 100 (FIG. 1) that decodes four-bit data  $DQ[3:0]$  130 (FIG. 1). Device 114-4 is similar to device 114-1 of FIG. 1 and device 114-2 of FIG. 4A, with like-identified elements being the same or similar. In device 114-4, skew-compensation circuit 420 adjusts, relative to clock signal 120-2, the relative phases of the different timing signals that gate analog latches 422 (*i.e.*, sample-and-hold circuits) to compensate for skew between pairs of symbols received on nodes 410. While device 114-4 includes differential amplifiers 124-1, in other embodiments differential amplifiers 416 are used, as shown in device 114-3 (FIG. 4B).

[037] In some embodiments, a spatial order of nodes 410 in devices 114 may be selected in order to eliminate long interconnects or leads in the routing on devices. For example, an order of nodes 410 may be: 410-1, 410-6, 410-2, 410-5, 410-3, and 410-4 (*i.e.*, *a, f, b, e, c, d*). In these embodiments, if the worst case length mismatch between the links is 1 mm, then the worst case skew may be 14 ps.

[038] Devices 114 can operate at the bit or symbol rate of clock signal 120-2 in system 100 in FIG. 1 (*e.g.*, these devices may use dual data rate). However, in some embodiments there may be two or more instances of the receiver circuits in any of these devices. A respective receiver circuit may be gated by a half rate clock signal (*i.e.*, a clock signal that has twice the period of clock signal 120-2), such as a clock signal that includes even or odd edges. Consequently, two or more instances of the receiver circuits may provide a pipeline for opposite clock strobes or phases. If delays in differential amplifiers 124 are well defined,

waves of difference signals propagating through such a pipeline may be captured by a subsequent stage of differential amplifiers or decoder 128.

[039] Additional techniques can be used to reduce the effect of capacitance associated with receiver circuits in devices 114. For example, differential amplifiers 124-1 may be

5 disaggregated to provide a gain stage in close proximity to nodes 410 in a respective device.

FIG. 5 is a block diagram illustrating a circuit 500 that compares symbols received on links  $a$  and  $f$  in system 100 (FIG. 1), such as one of differential amplifiers 124-1 (FIG. 1) or a

differential amplifier in generating circuit 126-1 (FIG. 1), in accordance with other

embodiments. The amplifier in circuit 500 is divided or split into a transconductance

10 amplifier 512 and a transimpedance amplifier 514. This transconductance amplifier may be

proximate to nodes 410, while transimpedance amplifier 514 may be remotely located from

nodes 410, *i.e.*, interconnects 510-1 and 510-2 may be shorter than interconnects 510-3 and

510-4. Furthermore, routing (and the associated capacitance) to the tail node of the

differential pair in transconductance amplifier 512 may be reduced by replacing the current

15 source with two resistors or two transistors that are intentionally biased into the triode

regions, each of which is proximate to nodes 410-1 and 410-6. By reducing the length of

interconnects 510-1 and 510-2, the impedance of these interconnects is reduced, which

reduces the effect of input-node capacitance on the communication channel bandwidth.

[040] The impedance of nodes that include the routing capacitance may have a low

20 equivalent resistance (*e.g.*, the  $1/gm$  input impedance of the common-gate amplifier in a

cascode-type transimpedance amplifier), so that the communication bandwidth can be

maintained. For example, if the routing and amplifier capacitance is 300 fF, and the

equivalent resistance at a respective node is  $50\Omega$ , then the -3dB frequency may be 10.6GHz.

While transimpedance amplifier 514 can be implemented as a cascode stage (which is also

25 referred to as a common-gate amplifier) for transconductance amplifier 512, in other

embodiments a common-drain amplifier (such as a source follower) or a super-source

follower is used. Furthermore, circuit 500 can be implemented using *NMOS* transistors,

*PMOS* transistors or both.

[041] FIG. 6A depicts a circuit 600 and FIG. 6B depicts a circuit 650 that each compare

30 symbols received on a pair of links, such as one of differential amplifiers 124-1 (FIG. 1) or a

differential amplifier in generating circuit 126-1 (FIG. 1), in accordance with other

embodiments. Circuits 600 (FIG. 6A) and 650 can be implemented using *NMOS* transistors,

*PMOS* transistors or both.

[042] FIG. 7A depicts analog latch 700 and FIG. 7B depicts analog latch 750 in device 114-4 (FIG. 4C) in accordance with other embodiments. Analog latches 700 (FIG. 7A) and 750 can be implemented using *NMOS* transistors, *PMOS* transistors or both.

[043] Drivers 122 (FIG. 1) in device 110 (FIG. 1) can be designed single-ended drivers in which individual drivers sink the current independently. In other embodiments, all drivers in device 110 may share one current among them in order to minimize current peaks in power supply due to any driver mismatches such as driver strength, switching incidents, etc. In some embodiments, one or more of these drivers may have a different gain value or weighting  $W_i$  than the other drivers.

[044] In some embodiments, generating circuit 126-1 (FIG. 1) in system 100 (FIG. 1) is eliminated by using two threshold values in decoder 128 (FIG. 1) to quantize the analog voltages output by differential amplifiers 124-1 (FIG. 1). For example, a first threshold may be approximately midway between 0 and  $V_p$  and a second threshold may be approximately midway between 0 and  $-V_p$ . These thresholds may allow decoder 128 (FIG. 1) to recognize the three different analog voltages output by differential amplifiers 124-1 ( $-V_p$ , 0 and  $V_p$ ), which provides sufficient information to decode the codeword to recover data  $DQ[3:0]$  without deriving the secondary comparisons using generating circuit 126-1 (FIG. 1).

[045] In FIG. 4B, at least a portion of the receiver circuits in device 114-3 perform comparisons to a common reference voltage (as opposed to a complementary signal or another multi-wire signal). As noted previously, the use of differential amplifiers that perform such comparisons may reduce the number of differential amplifiers coupled to each of the links (relative to FIGs. 1 or 4A, from two differential amplifiers to one), and thus, the capacitance associated with the receiver circuits in device 114-1 (FIG. 1).

[046] In some embodiments, at least one stage in devices 114 (FIGs. 1 and 4A-4C) includes single-ended amplifiers, in each of which a comparison is made between a respective symbol received on a respective link and an internal reference voltage, such as a supply voltage or ground of the respective single-ended amplifier (as opposed to comparing the respective symbol to a reference voltage that is provided by device 110).

[047] As discussed previously, in some embodiments differential amplifiers compare each of the symbols in a respective parallel symbol set, which is received on links  $a$  through  $f$ , to a reference voltage that may be generated on-chip (*i.e.*, on the *IC*) or off-chip. If the reference voltage is generated on chip, the reference voltage may be better able to track noise signals that occur during communication between devices 110 and 114-1 (FIG. 1), which often limits the performance of systems that include differential amplifiers that perform

comparisons to a common reference voltage. On-chip generation of the reference voltage is shown in FIG. 8A, which presents a system 800 that communicates data in accordance with another embodiment. System 800 is similar to system 100 (FIG. 1), with like-identified elements being the same or similar.

5 [048] In system 800, a suitable reference voltage is obtained by partially terminating all of the links in channel 112 to common node 812 of differential amplifiers 810. Furthermore, by terminating half of the termination to this common node (*e.g.*, with  $R_1 = 100 \Omega$ ), a tracking bandwidth of the reference voltage greater than 1 GHz may be obtained. This termination technique reduces reflections due to improper modal termination, and reduces power  
10 consumption because part of the signaling current is returned back through common node 812 of the reference-voltage network.

[049] If a balanced code is used (or, for non-balanced codes, if the number of logic 0s and the number of logic 1s during a respective time interval is constant), noise due to simultaneous switching outputs (*SSOs*) can be reduced or eliminated. In addition, by  
15 partially terminating to common node 812, any noise generated at the transmit side of the channel 112 (for example, in drivers 122) is coupled to the receive side by the links in channel 112, and thus is coupled to the high-bandwidth reference-voltage network. Consequently, this noise is common to all of the links and common node 812, so it can be rejected by a pseudo-differential receiver circuit, such as differential amplifiers 810, each of  
20 which has one input coupled to the reference voltage and the other input driven by the symbol received on a respective one of the links.

[050] FIG. 8B presents a system 850 that communicates data in accordance with another embodiment, in which the termination is split between *Vdd*, ground and common node 812. System 850 is similar to system 100 (FIG. 1), with like-identified elements being the same or  
25 similar. This system extracts the reference voltage, tracks noise, and reduces power consumption associated with signaling and termination.

[051] If balanced coding is used in system 800 (FIG. 8A) and 850, and all of the symbols in a respective symbol set arrive at approximately the same time (for example, if there is no skew), common node 812 in these circuits is a virtual ground. In this case, the termination  
30 may match the impedance of the links and the impedance of drivers 122 (for example,  $R_1$  may be  $100 \Omega$  and  $R_2$  may be  $200 \Omega$ ).

[052] In order to adjust the reference voltage for a global offset in differential amplifiers 810, system 850 may include an optional adjustable voltage divider 862 in parallel with common node 812. Furthermore, if there are large length mismatches in the links, the

different arrival times of the symbols in a respective symbol set may result in voltage movement of the virtual ground in the reference-voltage network. One solution for this problem is to adjust the transmission times of drivers 122 to compensate for the resulting skew (as discussed previously). Another solution, which can be used separately or in  
5 combination with the skew compensation, is to include an optional low-pass filter 860 in parallel with common node 812.

[053] In the worst case, where the virtual ground provides no termination for the links, the equivalent impedance of the  $R_2$  resistors to  $V_{dd}$  and ground still provides 50% termination (if  $R_2 = 200 \Omega$ ). FIG. 9 depicts a graph 900 of the tradeoff between relative line power 910 and  
10 termination to a common node 912 (in %) in accordance with another embodiment.

[054] The foregoing embodiments employ the outputs from differential amplifiers to decode data, for example, using a look-up table or a state machine. Other embodiments decode data by considering additional amplifier outputs. For example, the decoder can sample all  
15 available differential-amplifier outputs over a number of time intervals and apply the resulting samples to a trellis to determine the most probable data sequence. Viterbi decoding is one well-known algorithm for finding a most probable trellis-encoded data sequence.

[055] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols are set forth to provide a thorough understanding of the present invention. In some instances, the terminology and symbols may imply specific details that  
20 are not required to practice the invention. For example, embodiments of the invention may be adapted for use with multi-pulse-amplitude-encoded (multi-PAM) signals.

[056] An output of a process for designing an integrated circuit, or a portion of an integrated circuit, comprising one or more of the circuits described herein may be a computer-readable medium such as, for example, a magnetic tape or an optical or magnetic disk. The computer-  
25 readable medium may be encoded with data structures or other information describing circuitry that may be physically instantiated as an integrated circuit or portion of an integrated circuit. Although various formats may be used for such encoding, these data structures are commonly written in Caltech Intermediate Format (CIF), Calma GDS II Stream Format (GDSII), or Electronic Design Interchange Format (EDIF). Those of skill in the art  
30 of integrated circuit design can develop such data structures from schematic diagrams of the type detailed above and the corresponding descriptions and encode the data structures on computer readable medium. Those of skill in the art of integrated circuit fabrication can use such encoded data to fabricate integrated circuits comprising one or more of the circuits described herein.

[057] While the present invention has been described in connection with specific embodiments, the claims are not limited to what is shown. For example, the foregoing embodiments depict four-to-six coding techniques. More generally, embodiments can support  $N$ -to- $M$  coding, where  $M$  is greater than  $N$  and is at least three (including odd values for  $N$  or  $M$ ). For example, encoder 118 (FIG. 1) may implement one or more of: 1-3 coding, 1.5-3 coding, 3-5 coding, 5-7 coding, 6-8 coding, 7-9 coding and 7-10 coding. As shown in Table 1, the  $N$ -symbol data can be represented using all or a subset of possible  $N$ -symbol values. Furthermore, the embodiments detailed above can be replicated or combined in series, in parallel, or both, to support different input data widths (*e.g.*, two four-to-six encoders can be logically combined to convey eight-bit data over twelve links). Moreover, some components are shown directly connected to one another while others are shown connected via intermediate components. In each instance the method of interconnection, or ‘coupling,’ establishes some desired electrical communication between two or more circuit nodes, or terminals. Such coupling may often be accomplished using a number of circuit configurations, as will be understood by those of skill in the art. For example, the foregoing codespaces provide balanced signaling, and support *AC*-coupled links. Other embodiments can be unbalanced, include *DC*-coupled links, or both. Therefore, the spirit and scope of the appended claims should not be limited to the foregoing description. Only those claims specifically reciting “means for” or “step for” should be construed in the manner required under the sixth paragraph of 35 U.S.C. §112.

**CLAIMS**

What is claimed is:

1. An integrated circuit comprising:  
input nodes to receive a series of parallel symbol sets over a series of time intervals;  
comparison circuits, each comparison circuit having at least a first input terminal, coupled to a respective input node, and a comparison-circuit output node to provide primary comparison results;  
generation circuits, each generation circuit having second and third input terminals, coupled to at least a respective pair of the comparison-circuit output nodes, and a generation-circuit output node to provide secondary comparison results; and  
a decoder having decoder input terminals coupled to the comparison-circuit output nodes and the generation-circuit output nodes, the decoder to decode the symbol sets from the primary comparison results and the secondary comparison results.
2. The integrated circuit of claim 1, wherein the comparison circuits include differential amplifiers and the primary comparison results are relative to a reference voltage.
3. The integrated circuit of claim 1, wherein the comparison circuits include single-ended amplifiers and each of the primary comparison results is relative to an internal reference voltage of a respective single-ended amplifier.
4. The integrated circuit of claim 1, wherein each comparison circuit has the first input terminal and a fourth input terminal, coupled to respective ones of a pair of the input nodes.
5. The integrated circuit of claim 4, wherein the comparison circuits include differential amplifiers.
6. The integrated circuit of claim 1, wherein the generation circuits include differential amplifiers.
7. The integrated circuit of claim 1, wherein the combination of the comparison circuits and the generation circuits provide comparisons for all pairs of symbols a respective symbol set received on the input nodes.
8. The integrated circuit of claim 1, wherein there are M symbols in each symbol set;  
and

wherein there are less than  $M(M-1)/2$  comparison circuits.

9. The integrated circuit of claim 1, wherein there are  $M$  symbols in each symbol set; and

wherein there are  $M(M-1)/2$  comparisons in the combination of the primary comparison results and the secondary comparison results.

10. The integrated circuit of claim 1, wherein the symbols in each symbol set include a first symbol type representative of a logic zero and a second symbol type representative of a logic one.

11. The integrated circuit of claim 10, wherein there are equal numbers of the first symbol type and the second symbol type in each symbol set.

12. The integrated circuit of claim 1, wherein the integrated circuit is to communicate information during inter-chip or intra-chip communication.

13. The integrated circuit of claim 1, wherein the integrated circuit includes a memory controller or a dynamic random access memory (*DRAM*).

14. The integrated circuit of claim 1, wherein the generating circuit includes a sample-and-hold circuit.

15. An integrated circuit comprising:

input nodes to receive a series of parallel symbol sets over a series of time intervals; comparison circuits, each comparison circuit having at least a first input terminal, coupled to a respective input node, and a comparison-circuit output node to provide primary comparison results;

generation circuits, each generation circuit having second and third input terminals, coupled to at least a respective pair of the comparison-circuit output nodes, and a generation-circuit output node to provide secondary comparison results; and

means for decoding the symbol sets from the primary comparison results and the secondary comparison results.

16. A system, comprising an integrated circuit that includes:

input nodes to receive a series of parallel symbol sets over a series of time intervals; comparison circuits, each comparison circuit having at least a first input terminal, coupled to a respective input node, and a comparison-circuit output node to provide primary

comparison results;

generation circuits, each generation circuit having second and third input terminals, coupled to at least a respective pair of the comparison-circuit output nodes, and a generation-circuit output node to provide secondary comparison results; and

a decoder having decoder input terminals coupled to the comparison-circuit output nodes and the generation-circuit output nodes, the decoder to decode the symbol sets from the primary comparison results and the secondary comparison results.

17. A method for communicating information, the method comprising:  
receiving a series of parallel symbol sets over a series of time intervals, the symbols in each symbol set received on respective nodes, and for each of the symbol sets:

comparing symbols on the nodes to determine primary comparison results; and  
generating secondary comparison results from the the primary comparison results;

and

decoding the respective symbol set from the primary comparison results and the secondary comparison results.

18. The method of claim 17, wherein the primary comparison results are relative to a reference voltage.

19. The method of claim 17, wherein each comparison result is for symbols received on a respective pair of the input nodes.

20. The method of claim 17, wherein the combination of the primary comparison results and the secondary comparison results provide comparisons for all pairs of symbols in the respective symbol set received on the input nodes.

21. The method of claim 17, wherein there are  $M$  symbols in each symbol set; and wherein there are less than  $M(M-1)/2$  primary comparison results.

22. The method of claim 17, wherein there are  $M$  symbols in each symbol set; and wherein there are  $M(M-1)/2$  comparisons in the combination of the primary comparison results and the secondary comparison results.

23. An integrated circuit comprising:  
input nodes to receive a series of parallel symbol sets over a series of time intervals;  
comparison circuits, each comparison circuit having at least a first input terminal,

coupled to a respective input node, and a comparison-circuit output node to provide comparison results, each comparison corresponding to a respective one of three analog values;

a decoder having decoder input terminals coupled to the comparison-circuit output nodes, the decoder to decode the symbol sets from the comparison results.

24. The integrated circuit of claim 23, wherein there are  $M$  symbols in each symbol set; and

wherein there are less than  $M(M-1)/2$  comparison results.

25. An integrated circuit comprising:

input nodes to receive a series of parallel symbol sets over a series of time intervals; comparison circuits, each comparison circuit having a first input terminal, coupled to a respective input node, a second input terminal, coupled to a common node, and a comparison-circuit output node to provide comparison results, wherein the common node is coupled to and partially terminates the input nodes; and

a decoder having decoder input terminals coupled to the comparison-circuit output nodes, the decoder to decode the symbol sets from the comparison results.

26. The integrated circuit of claim 25, wherein the common node is coupled to a reference voltage.

27. The integrated circuit of claim 26, wherein the reference voltage is adjustable.

28. The integrated circuit of claim 25, further comprising a low-pass filter coupled to the common node.

29. The integrated circuit of claim 25, wherein the common node includes a virtual ground.

30. A system, comprising an integrated circuit that includes:

input nodes to receive a series of parallel symbol sets over a series of time intervals; comparison circuits, each comparison circuit having a first input terminal, coupled to a respective input node, a second input terminal, coupled to a common node, and a comparison-circuit output node to provide comparison results, wherein the common node is coupled to and partially terminates the input nodes; and

a decoder having decoder input terminals coupled to the comparison-circuit output

nodes, the decoder to decode the symbol sets from the comparison results.

31. A method for communicating information, the method comprising:
  - coupling input nodes to a common node, which partially terminates the input nodes;
  - receiving a series of parallel symbol sets over a series of time intervals, the symbols in each symbol set received on respective input nodes, and for each of the symbol sets:
    - comparing symbols on the nodes to a reference voltage to determine comparison results; and
    - decoding a respective symbol set from the comparison results.

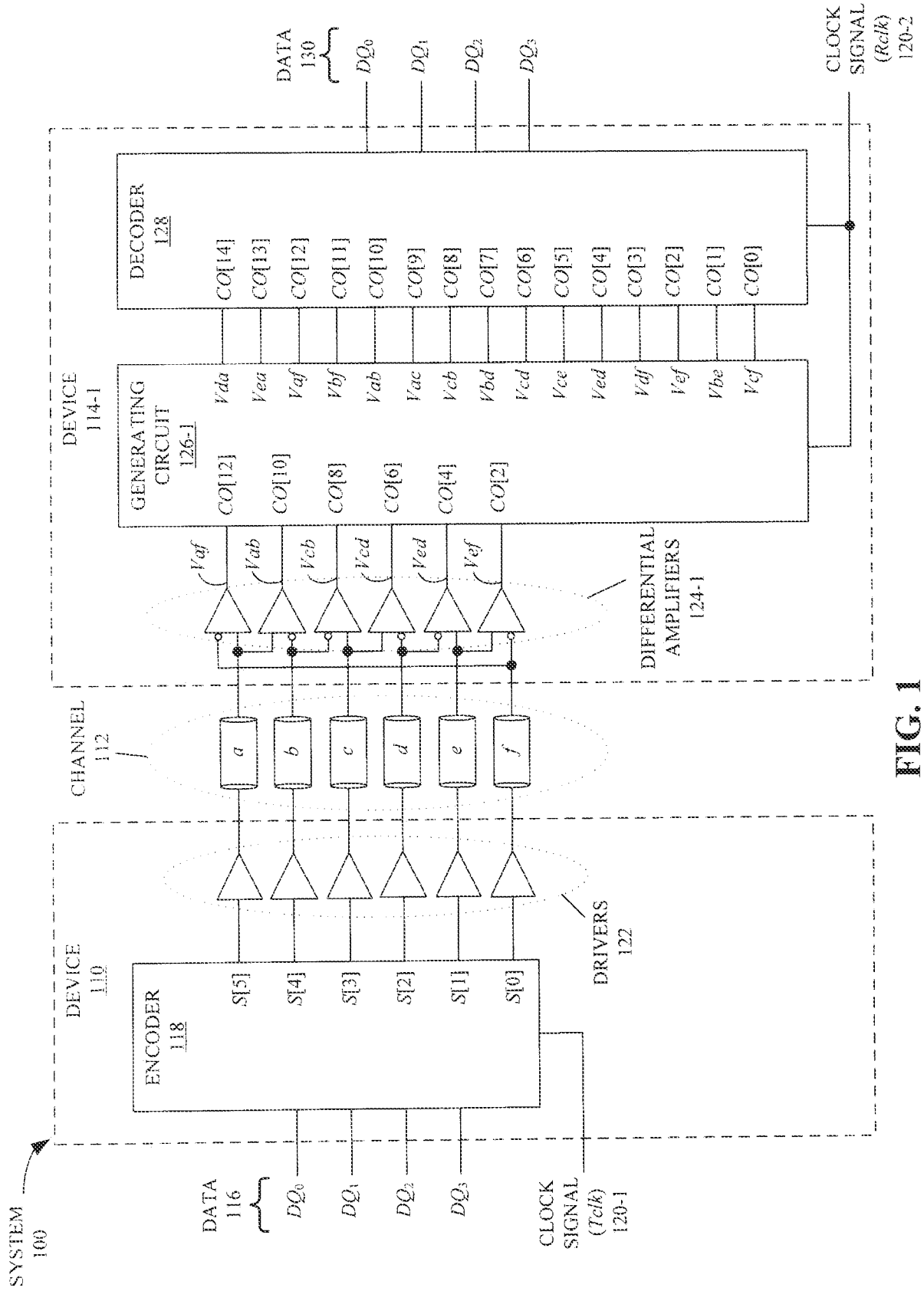


FIG. 1

200

DATA VALUE	9	12	15	8	11	14	7	5	4	1
<i>DQ</i> [3]	1	1	1	1	1	1	0	0	0	0
<i>DQ</i> [2]	0	1	1	0	1	1	1	1	1	0
<i>DQ</i> [1]	0	0	1	0	0	1	1	0	0	0
<i>DQ</i> [0]	1	0	1	0	1	0	1	1	0	1
<i>S</i> [5:0]	<i>a</i>	1	0	0	1	0	0	1	1	1
	<i>b</i>	0	1	1	0	1	1	0	0	1
	<i>c</i>	0	1	0	0	1	0	0	1	0
	<i>d</i>	0	0	0	1	0	1	1	0	1
	<i>e</i>	1	0	1	0	1	0	1	1	0
	<i>f</i>	1	1	1	1	0	1	0	0	0
<i>CW</i> #	9	12	15	8	11	14	7	5	4	1
	<i>T</i> <sub>0</sub>	<i>T</i> <sub>1</sub>	<i>T</i> <sub>2</sub>	<i>T</i> <sub>3</sub>	<i>T</i> <sub>4</sub>	<i>T</i> <sub>5</sub>	<i>T</i> <sub>6</sub>	<i>T</i> <sub>7</sub>	<i>T</i> <sub>8</sub>	<i>T</i> <sub>9</sub>

FIG. 2A

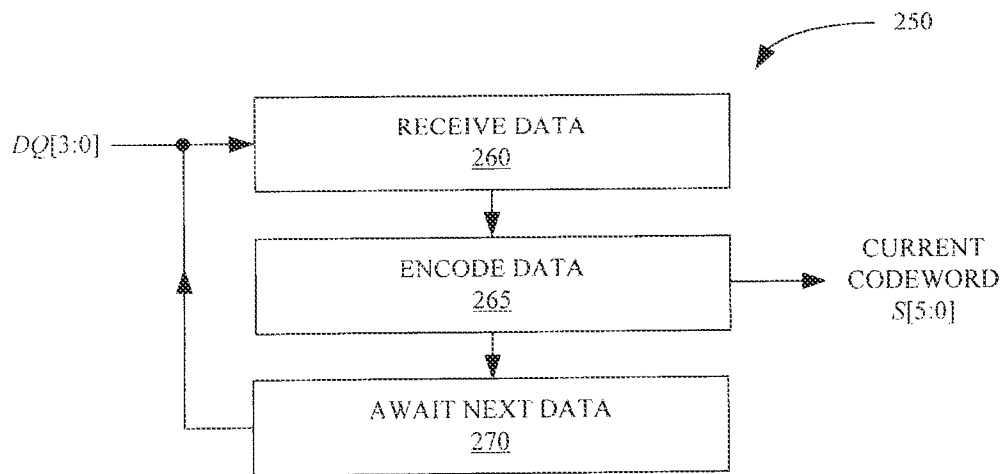


FIG. 2B



<i>DQ</i> [3:0]	1001	1100	1111	1000	1101	1110	0111	0101	0100	0001	
<i>CW</i> #	9	12	15	8	11	14	7	5	4	1	
<i>CO</i> [14]	0	<i>x</i>	<i>x</i>	<i>x</i>	<i>x</i>	1	<i>x</i>	0	<i>x</i>	<i>x</i>	
<i>CO</i> [13]	<i>x</i>	<i>x</i>	1	0	1	<i>x</i>	<i>x</i>	<i>x</i>	0	0	
<i>CO</i> [12]	<i>x</i>	0	0	<i>x</i>	<i>x</i>	0	1	1	1	1	
<i>CO</i> [11]	0	<i>x</i>	<i>x</i>	0	1	<i>x</i>	<i>x</i>	<i>x</i>	<i>x</i>	1	
<i>CO</i> [10]	1	0	0	1	0	0	1	1	1	<i>x</i>	
<i>CO</i> [9]	1	0	<i>x</i>	1	0	<i>x</i>	1	<i>x</i>	<i>x</i>	1	
<i>CO</i> [8]	<i>x</i>	<i>x</i>	0	<i>x</i>	<i>x</i>	0	<i>x</i>	1	1	0	
<i>CO</i> [7]	<i>x</i>	1	1	0	1	<i>x</i>	0	<i>x</i>	0	<i>x</i>	
<i>CO</i> [6]	<i>x</i>	1	<i>x</i>	0	1	0	0	1	<i>x</i>	0	
<i>CO</i> [5]	0	1	0	<i>x</i>	<i>x</i>	<i>x</i>	0	<i>x</i>	1	<i>x</i>	
<i>CO</i> [4]	1	<i>x</i>	1	0	1	0	<i>x</i>	1	0	0	
<i>CO</i> [3]	0	0	0	<i>x</i>	<i>x</i>	<i>x</i>	1	<i>x</i>	1	1	
<i>CO</i> [2]	<i>x</i>	0	<i>x</i>	0	1	0	1	1	<i>x</i>	<i>x</i>	
<i>CO</i> [1]	0	1	<i>x</i>	<i>x</i>	<i>x</i>	1	0	0	<i>x</i>	1	
<i>CO</i> [0]	0	<i>x</i>	0	0	1	0	<i>x</i>	1	1	<i>x</i>	
	<i>T0</i>	<i>T1</i>	<i>T2</i>	<i>T3</i>	<i>T4</i>	<i>T5</i>	<i>T6</i>	<i>T7</i>	<i>T8</i>	<i>T9</i>	

FIG. 3A

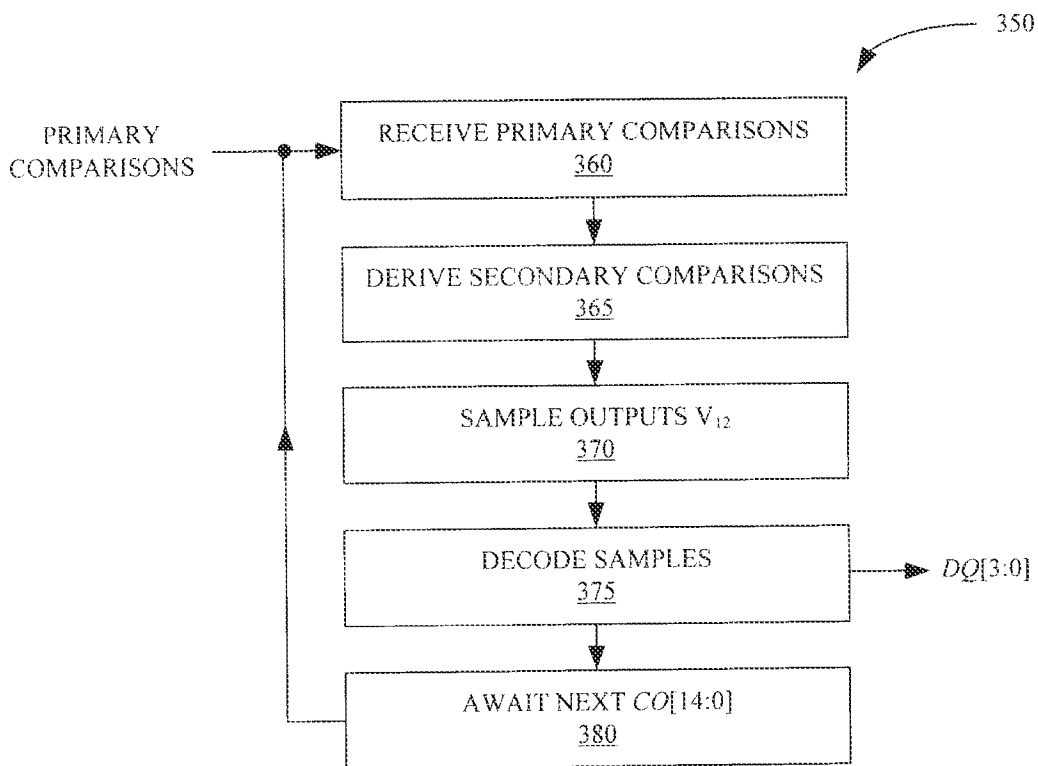


FIG. 3B

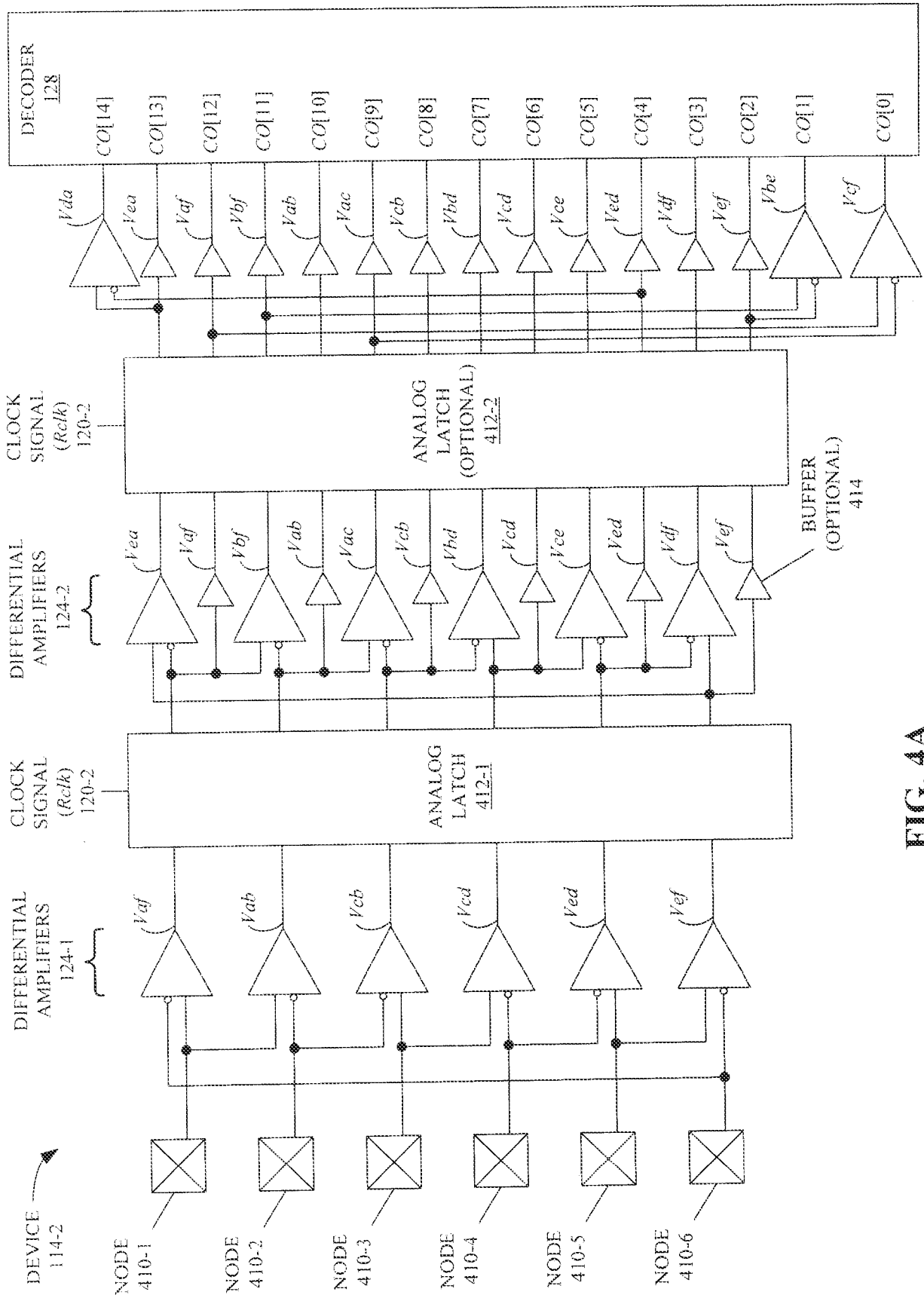


FIG. 4A

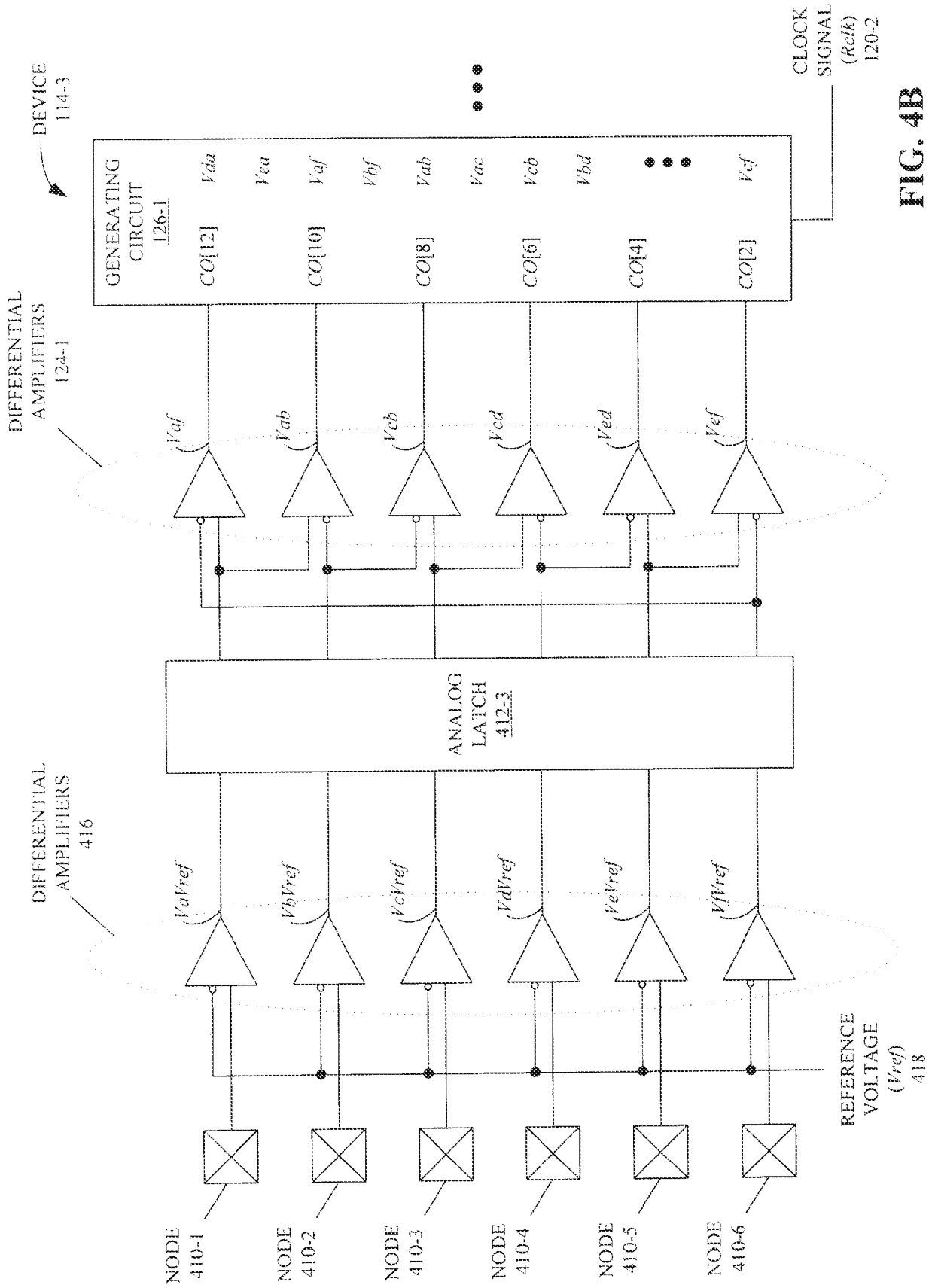


FIG. 4B

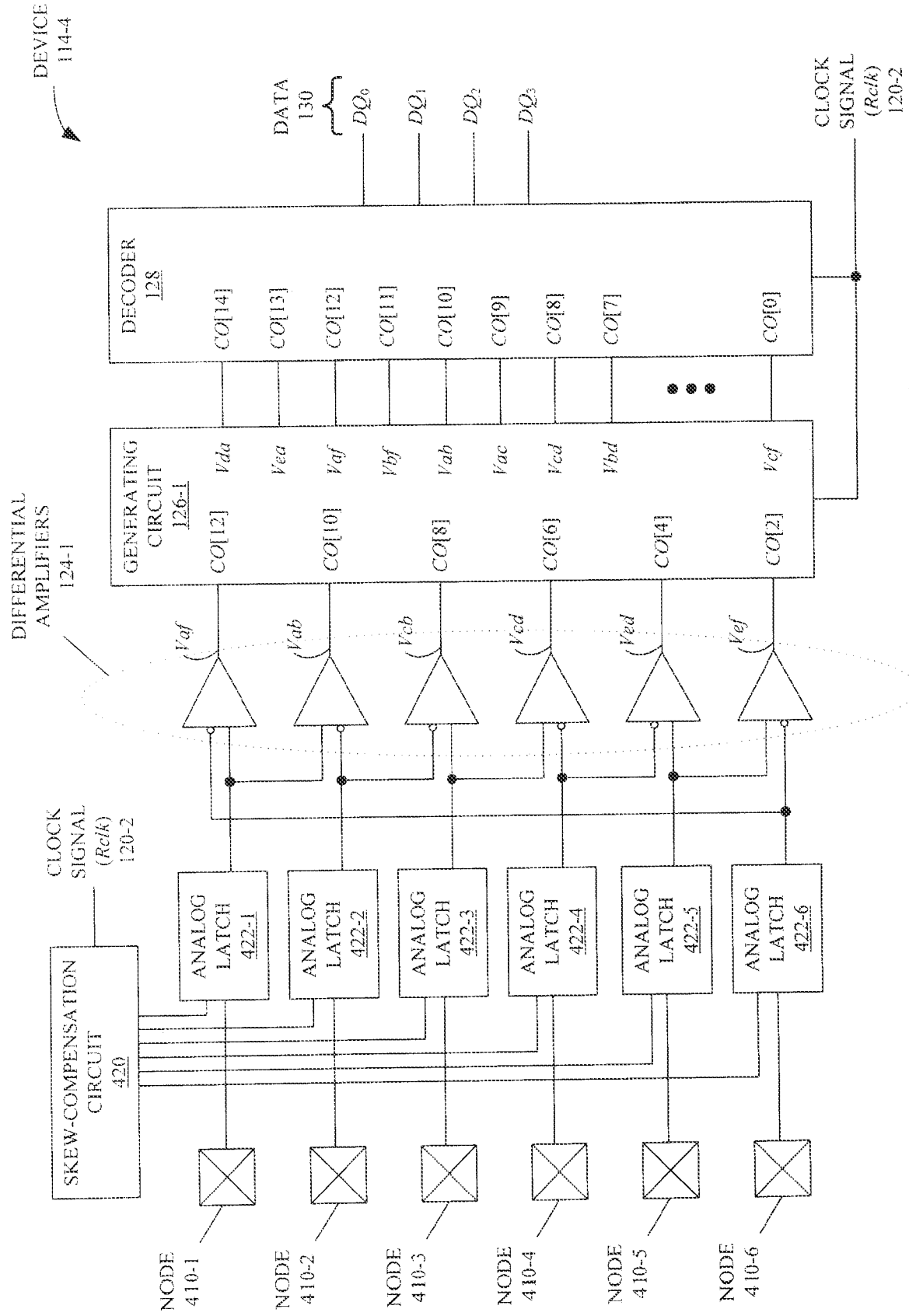


FIG. 4C

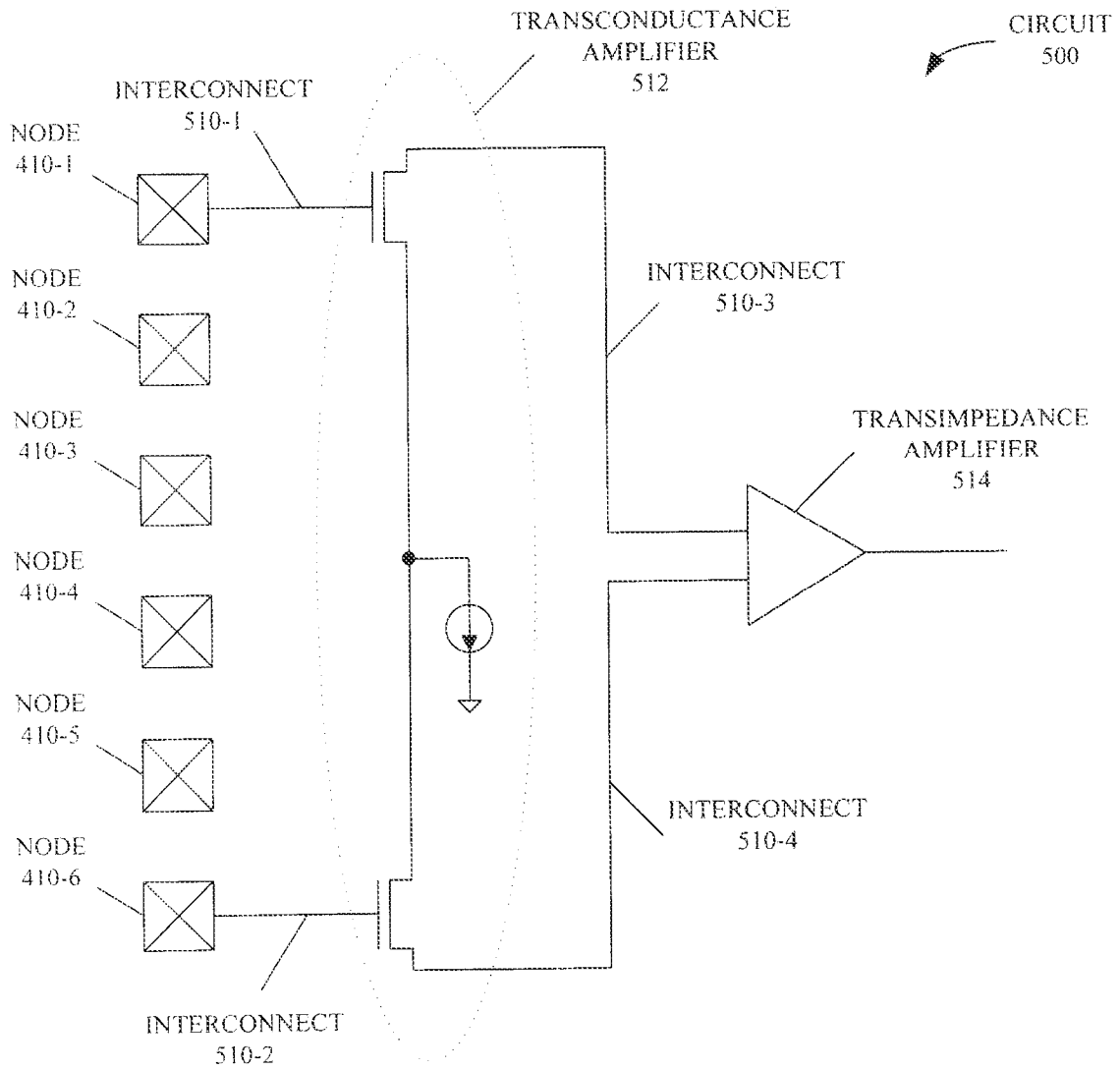


FIG. 5

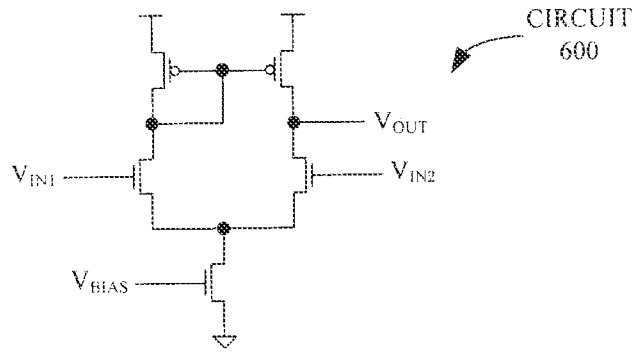


FIG. 6A

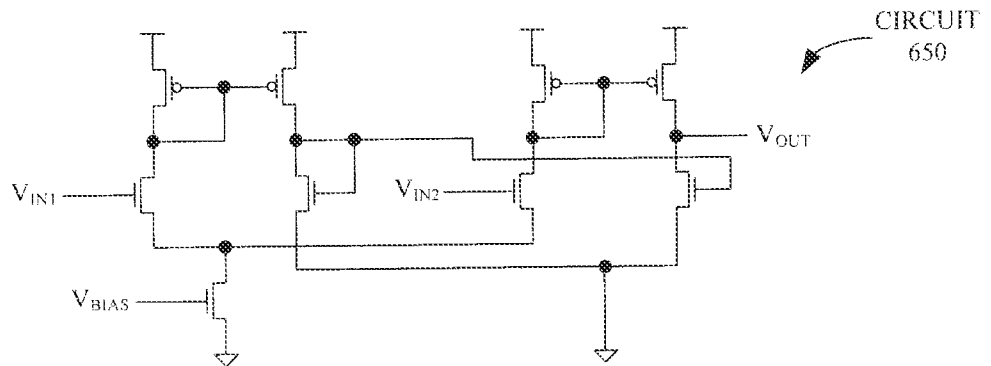


FIG. 6B

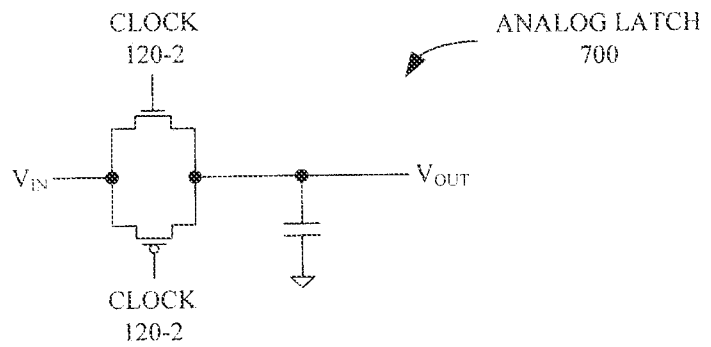


FIG. 7A

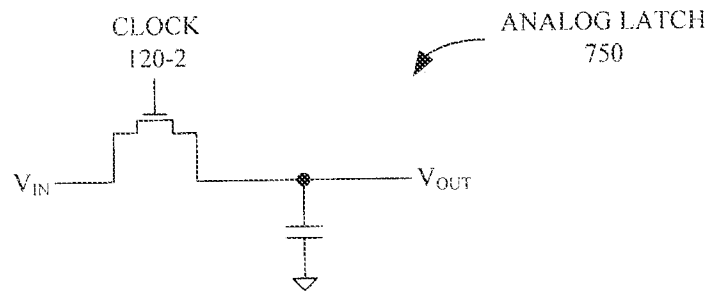


FIG. 7B

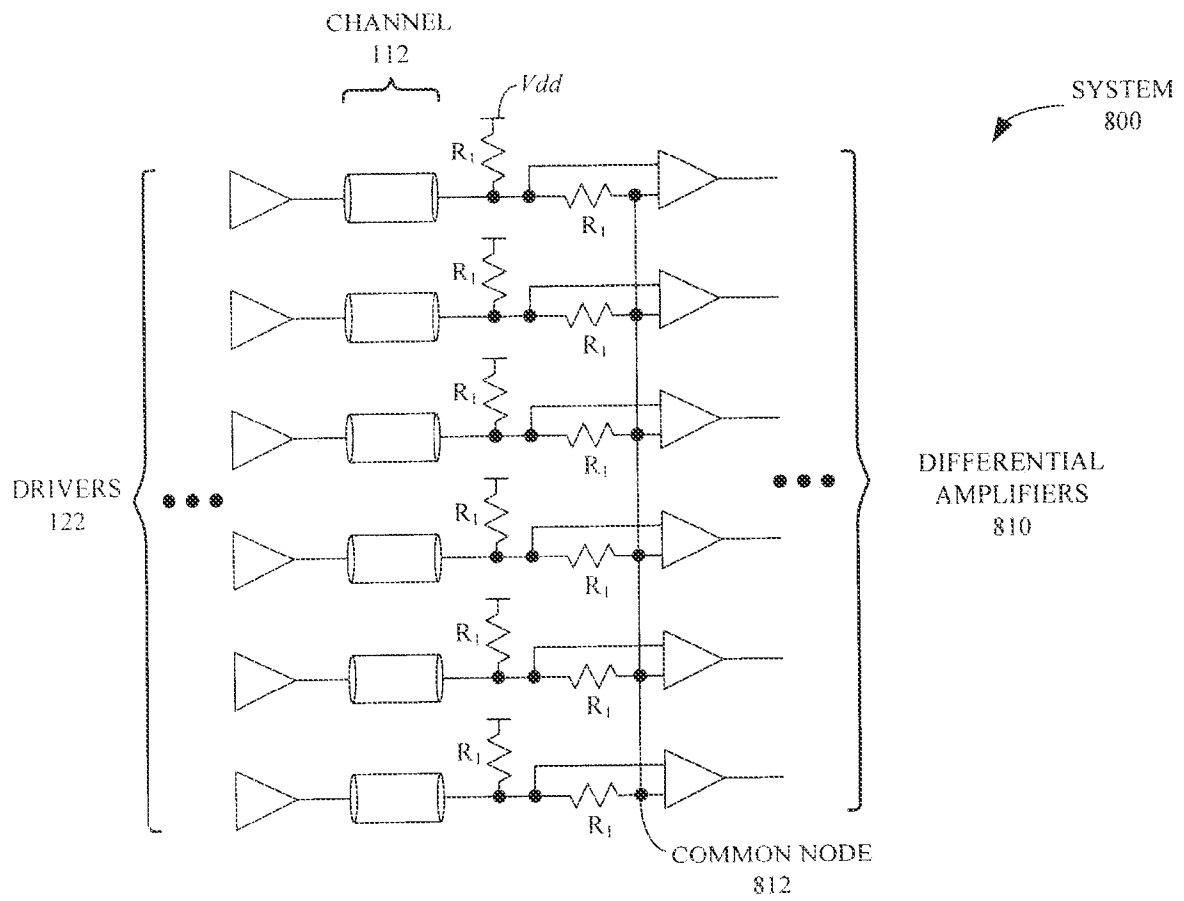


FIG. 8A

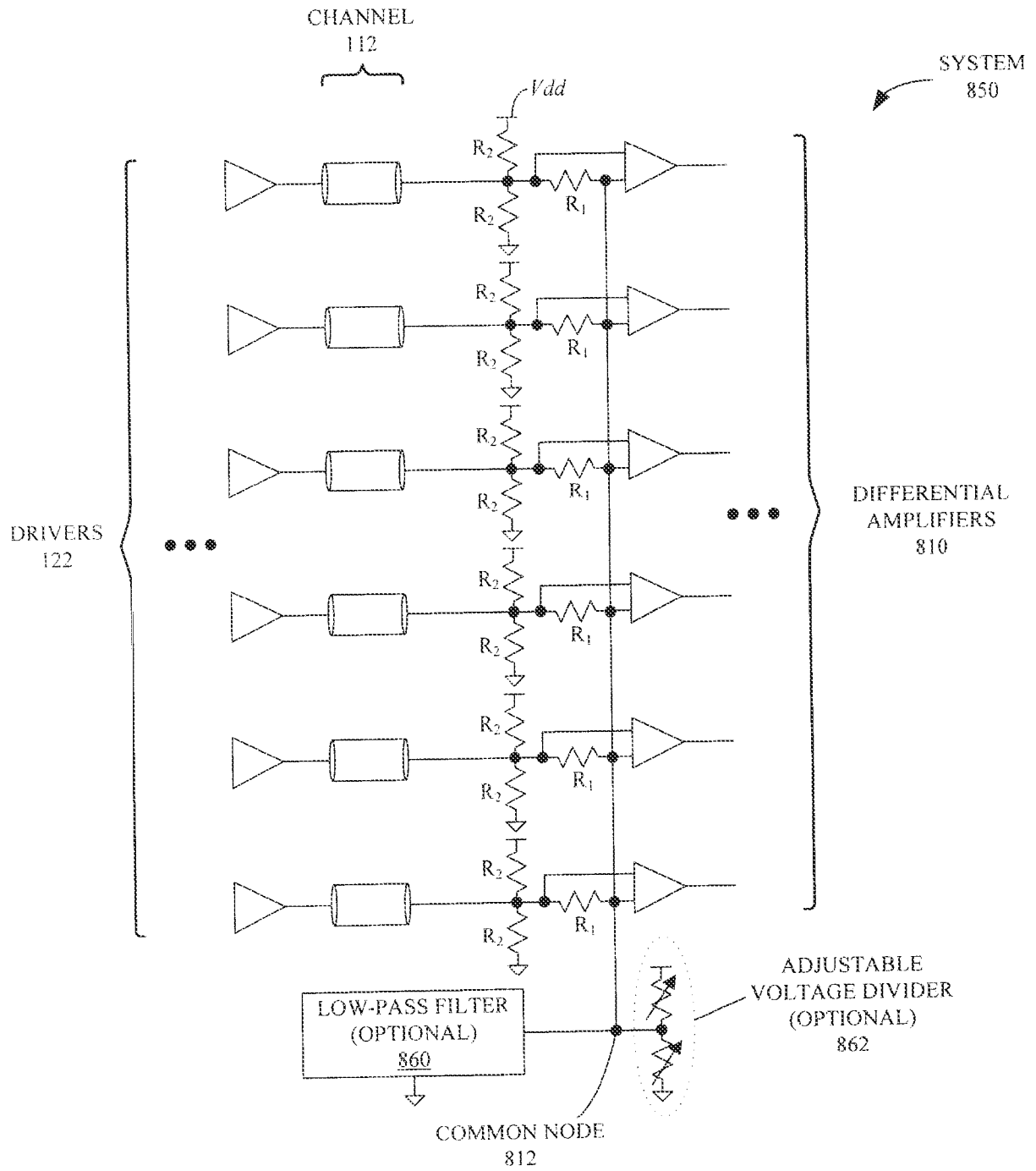


FIG. 8B

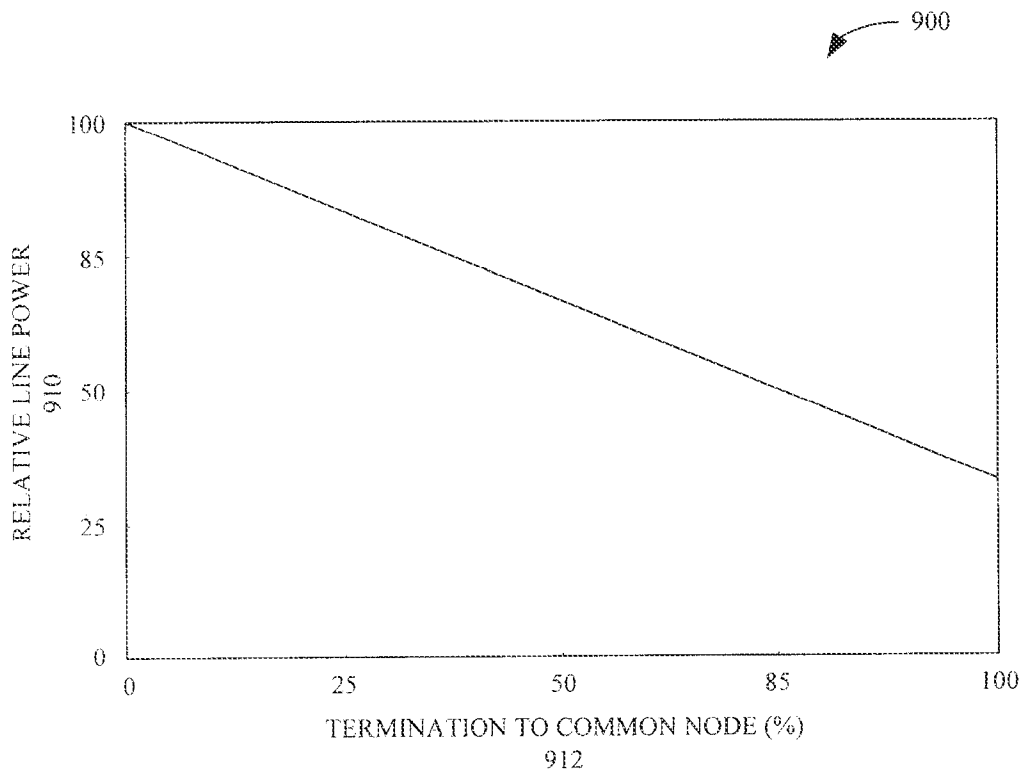


FIG. 9

**INTERNATIONAL SEARCH REPORT**

International application No

PCT/US2008/087639

**A. CLASSIFICATION OF SUBJECT MATTER**  
 INV. G06F13/42 H04L25/49

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
 G06F H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 278 740 B1 (NORDYKE KEITH D [US]) 21 August 2001 (2001-08-21) figures 5A,5B,5C	1-12, 14-31
Y	-----	13
Y	US 6 734 811 B1 (CORNELIUS WILLIAM [US]) 11 May 2004 (2004-05-11) the whole document	13
A	US 6 999 516 B1 (RAJAN SURESH [US]) 14 February 2006 (2006-02-14) abstract	1-31
A	US 2003/095606 A1 (HOROWITZ MARK A [US] ET AL) 22 May 2003 (2003-05-22) the whole document	1-31

Further documents are listed in the continuation of Box C.

See patent family annex.

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- \*8\* document member of the same patent family

Date of the actual completion of the international search

15 May 2009

Date of mailing of the international search report

12/06/2009

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# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2008/087639

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6278740	B1	21-08-2001	NONE
US 6734811	B1	11-05-2004	US 2004233074 A1 25-11-2004
US 6999516	B1	14-02-2006	US 2006115004 A1 01-06-2006
US 2003095606	A1	22-05-2003	NONE