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Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

[Continued on next page]

(54) **Title**: LARGE CAPACITY THIN FILM BATTERY AND METHOD FOR MAKING SAME

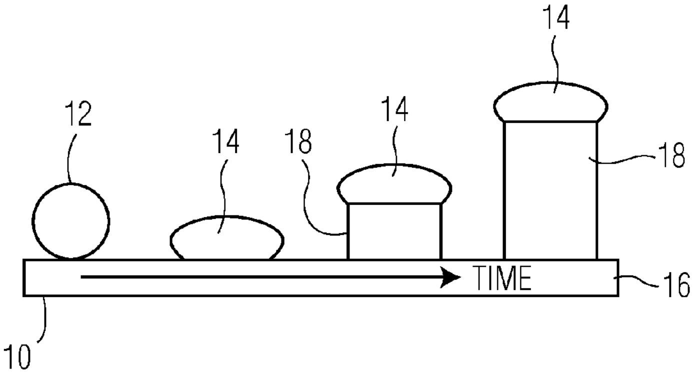

FIG. 1

(57) **Abstract**: A method for fabricating a battery includes growing (104) wires on a substrate to form a three-dimensional skeleton structure to increase a surface area. A battery stack is deposited (116) on the skeleton structure and may be thinner to increase stability and a lifetime of the battery.

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LARGE CAPACITY THIN FILM BATTERY AND METHOD FOR MAKING SAME

This disclosure relates to thin-film batteries, and more particularly to methods and batteries so formed using surface enlargement to provide high capacity functionality.

Micro power sources, such as all-solid-state thin film batteries (TFBs) are currently seen as the future power sources in many stand-alone and small-scale autonomous devices like sensor systems, RFID, medical implants and many more applications. State-of-the-art TFBs are of a planar nature (2D) and can thus only store a relatively small amount of energy per footprint area (~50 microAh/cm^2 per micron of cathode thickness).

It is known that Li can be intercalated into Si at a high concentration (4.4 Li atoms per Si atom), giving a theoretical energy capacity of about 4000 mAh/gr of Si. However, the expansion of the Si layer upon Li intercalation results in a degradation of the layer, and limits the number of cycles. Moreover, diffusion through thick Si layers is slow and limits the operation performance (power output and charging speed) of the battery.

The surface enlargement (and thus energy/power output enhancement), which can be realized by means of providing the substrate with a plurality of cavities, is generally done by dry etching processes such as Reactive Ion Etching and Ion Beam Etching, which are expensive and slow. Further, the etch rate drops dramatically when very high aspect ratio structures (e.g., very deep cavities) need to be processed. Moreover, the tool costs and investment are also very high.

In accordance with the present principles, an all-solid-state thin film energy source with very high energy storage properties per footprint area is provided. This can be realized through 3D surface enlargement of a bottom substrate. In accordance with one embodiment, a highly-controllable nanowire structure is grown for creating a 3D backbone or skeleton structure on a planar substrate. This backbone can be covered by a complete thin film battery stack. A battery comprising, e.g., LiMOx cathodes, solid-state electrolytes and Li-intercalation anodes (such as LiAl, LiSi, LiIn, LiZn, …) may be employed. These new 3D TFBs can theoretically deliver over 20 times the amount of energy per footprint area for the same cathode thickness, compared to their planar counterpart. The planar battery systems result from surface area enlargement generated by selectively etching 3D features in standard planar substrates by means of reactive ion etching (RIE) for example.

The present principles instead grow nanowires up from a substrate rather than etching structures into the substrate. Additionally, the surface coverage or wire density can be tuned accurately in a wide range (from 0.1% to over 50%). One advantage is that by using a skeleton structure, the battery stack does not suffer from degradation upon cycling, as the active intercalation/storage electrodes can remain very thin. This implies that employing surface area enlargement results in a battery device in which the same amount of energy can be stored per footprint (as compared to planar geometries), using thinner active electrodes. This is combined with a very high storage capacity, stability and fast diffusion through the thin active layers. Applications in which this power source can be utilized may include, for example, autonomous sensors for body area networks (BAN) and wireless sensor networks (WSN), lighting applications (presence detection), medical implants, etc.

A Vapor-Liquid-Solid (VLS) growth mechanism for semiconducting nanowires provides a mechanism for growing wires, e.g., from group IV, III-V and II-VI compound semiconductor materials. Other materials such as conductive materials and even insulating materials may also be employed for wires. The process controls impurity doping (p- and n-type), growth rate in the vertical and radial direction, and the fabrication of heterostructures. By using silicon nanowires, the expansion of the crystal is accommodated by the geometry and diffusion is fast across short distances. A storage capacity of, e.g., 3000 mAh/gr can be provided by such a system. However, the wires may show degradation after several charge/discharge cycles due to a collapse of the wire structures. Therefore, protection structures and formation methods are provided in accordance with the present principles to provide a robust skeleton structure to support a high performance and reliable thin film battery.

A method for fabricating a battery includes growing wires on a substrate to form a three-dimensional skeleton structure to increase a surface area. A battery stack is deposited on the skeleton structure and includes thinner active electrodes, which increases stability and a lifetime of the battery.

A method for fabricating a battery includes growing wires on a substrate to form a three-dimensional skeleton structure. The skeleton structure resists degradation due to intercalation cycling and an active intercalation material is deposited on the skeleton structure. A thin film battery (TFB) includes a substrate, and a plurality of vertical vapor-liquid-solid (VLS) grown nanowires attached to the substrate to form a three-dimensional skeleton structure. The skeleton structure resists degradation due to intercalation cycling. A shell layer is formed over the wires and preferably forms an active electrode of a battery stack. The battery stack is deposited on the skeleton structure. The battery stack includes an active intercalation material. The shell layer may be an anode or cathode of the battery. The anode may be defined as a negative electrode of the battery (e.g., the active electrode of the battery having the most negative potential). This is because in a rechargeable battery system the word anode or cathode actually depends on the whether the battery is being charged or discharged.

These and other objects, features and advantages of the present disclosure will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

This disclosure will present in detail the following description of preferred embodiments with reference to the following figures wherein:

FIG. 1 is a diagram showing a formation of a catalyst particle and the growth of a nanowire in accordance with the present principles;

FIG. 2 is a cross-sectional view of a nanowire having a shell layer and optional barrier layer formed thereon;

FIG. 3 is a cross-sectional view of a skeleton structure of grown nanowires in accordance with the present principles;

FIG. 4 is a cross-sectional view of the skeleton structure of FIG. 3 with a battery stack formed thereon in accordance with the present principles;

FIG. 5 is a diagram showing a formation of catalyst particles on sides of nanowires and grown to form branches in accordance with the present principles; and

FIG. 6 is a flow diagram showing steps for fabricating a battery in accordance with an illustrative embodiment.

The present disclosure describes an all-solid-state thin film energy source with very high energy storage properties per footprint area realized through 3D surface enlargement of the (bottom) substrate. Highly-controllable nanowire growth is employed for creating a 3D backbone or skeleton structure on a planar substrate. Additionally, the surface coverage or wire density can be tuned accurately in a wide range (from 0.1% to over 50%). Due to the inert nature of the skeleton material, the structure does not suffer from degradation upon cycling. This is combined with a very high storage capacity, stability and fast diffusion, which are achieved through the thin active layers. Based on experimental and theoretical evidence of planar solid-state thin film batteries, thinner active layers (active intercalation or storage electrodes) show substantially better performance with respect to lifetime (e.g., cycling). Therefore, enlargement of the surface area of the support (e.g., substrate) by a factor of X leads to the same storage capacity per footprint for a 1/X thickness of the active electrodes, compared to the planar situation. This reduction in active electrode thickness is a contributor to extended lifetime of the battery device.

It should be understood that the present invention will be described in terms of an illustrative battery structure and with illustrative materials; however, the teachings of the present invention are much broader and are applicable to any battery structures including any number of three dimensional shapes or components that can be mounted on, positioned on or otherwise placed on a substrate. Further other suitable materials may be employed in accordance with the present principles.

Referring now to the drawings in which like numerals represent the same or similar elements and initially to FIG. 1, a diagram depicts stages of nanowire growth on a substrate 10. Substrate 10 may include any suitable material that is compatible with the nanowires material selection. The substrate 10 may include an isolation material a conductive material or a semiconductive material, e.g., Si, Ge, GaAs, etc. Vertical nanowires are grown on the substrate 10 using, e.g.., a Vapor-Liquid-Solid (VLS) growth mechanism at a low temperature. In one embodiment, the temperature for growth may be, e.g., about 400 – 450 °C (preferably about 420°C). The VLS mechanism condenses a vapor to form catalyst particles 12 on substrate 10. The droplets or particles 12 settle to become elliptical in shape 14 to provide a position for growing nanowires 18. A deposition of the material for forming nanowires 18 causes the nanowires to grow below particles 14. As time 16 elapses, the nanowires 18 grow larger. These nanowires 18 have a small diameter (preferably about 20-50 nm) and grow to between about a hundred nm to several microns. To benefit from the area enlargement in a 3D TFB, a surface area enlargement of about 5 or greater, preferably 10 or greater, and more preferably 25 or greater, is achieved to provide better performance. The larger the surface area, the better the performance is.

A doping type and density of the nanowires 18 is controlled, such that in one embodiment we have at least about 10^{19} cm^{-3} free carriers to have a conductive system. Controlling the doping density and doping type is performed by adjusting in-situ processing parameters, such as the type of doping element and temperature of evaporation, etc. The material of a first layer which forms the nanowires 18 may be from group IV, III-V or II-VI. For example, group III-V materials may include, e.g., GaN or InP. A group II-VI compound may include, e.g., ZnO. Growth of the nanowire skeleton (e.g. wires 18) is terminated by decreasing the temperature and discontinuing a precursor flow.

Referring to FIG. 2, in a next step, a shell layer 22 is formed around the vertical nanowires 18. For example, the temperature may be greater than 420°C, but depends on the material selected for the shell layer 22. The thickness of layer 22 is controlled by the deposition time, and the layer 22 may include any semiconductor material, for example, Si, Ge, another group IV element, a II-VI material or III-V material may be employed. In one embodiment, a deposition of a Sb shell (e.g., about 10 nm in thickness) is formed around a Si core (nanowire 18). This yields an electrochemically stable structure, as long as one remains in the proper voltage limits (in this case the voltage needs to remain above 0.7V), in which the Si core is thermodynamically unable to store Li, whereas the shell (Sb), is able to reversibly insert/extract Li. For multiple materials this is shown in Table 1. The shell layer 22 preferably forms an active electrode of a TFB battery stack. In cases where the shell layer 22 is not an active battery electrode may include a situation where a non-doped skeleton structure is employed with a doped shell layer that can be utilized as a current collector, or the shell layer may be employed as a barrier layer.

Table 1: Lithium Insertion and Extraction Voltages are shown for selected materials.

Anode material	Lithium Insertion	Lithium Extraction
Si	0.25	0.45 V vs. Li/Li+
Ge	0.35	0.55 V vs. Li/Li+
Sn	0.5	0.6 V vs. Li/Li+
Pb	0.4	0.5 V vs. Li/Li+
Al	0.25	0.5 V vs. Li/Li+
Zn	0.3	0.6 V vs. Li/Li+
SnO	0.4	0.6 V vs. Li/Li+
SnNx	0.3	0.5 V vs. Li/Li+
InNx	0.8	0.8 V vs. Li/Li+
Bi	0.8	0.9 V vs. Li/Li+
Sb	0.9	1 V vs. Li/Li+
Ga	0.5	0.8 V vs. Li/Li+
GaP	0.5	0.7 V vs. Li/Li+
InP	0.5	0.7 V vs. Li/Li+
In2O3	0.8	1 V vs. Li/Li+
SiO	0.1	0.35 V vs. Li/Li+
SiNx	0.2	0.4 V vs. Li/Li+
ZnS	0.5	1 V vs. Li/Li+
Zn3P2	0.4	0.6 V vs. Li/Li+

Referring to Table 1, for example, if a Si core/skeleton structure is covered with a Sb shell, then operating this (anode) structure in a voltage range (vs. a Li/Li^+ reference couple) from 0.8V – 1.2V, one can reversibly store Li in the Sb shell, but not in the Si core (as this reversibly stores lithium in the 0.25 – 0.45V range). The core/shell structure material can be selected to provide a desired response for a battery in a desired voltage range. The shell layer 22 is used as an active electrode material that reversibly stores lithium, while the core material 18 is electronically conductive as it is used as a current collector. In one embodiment, any semiconductor material may be employed for the core material 18, and preferably a doped semiconductor material. In another embodiment, carbon nanotube/wires (which reversibly store Li between 0 – 0.3V) may be grown on a substrate using VLS growth. The carbon nanotubes/wires can be covered with a shell material that reversibly interacts with Li at potentials higher than that of carbon.

The shell layer 22 protects the wires 18 from degradation and collapse during charge/discharge cycles of intercalation cycling. Protection is provided by shell layer 22 to provide a robust skeleton structure to support a high performance and reliable thin film battery.

In one embodiment, an effective lithium barrier layer 24, such as Ta, Ti, TaN or TiN can be deposited on the core wires 18 (preferably before depositing the shell layer 22) to prevent Li diffusion into the wire structure (and the accompanying volume changes). This allows a much wider range of materials that can be used for both the shell layer 22 and/or core materials for wires 18. This TiN/Ta barrier layer 24 is impenetrable to, e.g., Li, but is an electronic conductor and therefore is a good current collector as well as a barrier layer. With use of the barrier layer 24 to chemically separate the core 18 and the shell 22 (or active electrode layers), a wide range of material combinations becomes possible, even those materials where the thermodynamics dictates that reversible Li storage of shell layer materials will occur at potentials more negative than those related to Li storage potentials of the core material.

Catalyst 14 may remain embedded in the structure. Optionally, the catalyst 14 can be removed, e.g., using a wet chemical etch based on, e.g., cyanide (CN^-) or iodide (I_3^-).

Referring to FIGS. 3 and 4, after deposition of the wires 18 has been completed, the surface-enhanced substrate 30 is ready for the next step. The surface-enhanced substrate 30 can subsequently be used to deposit a full battery stack 40 thereupon. The battery stack 40 comprises formation of battery stack components, such as back-to-back layer depositions of an anode, a solid electrolyte and a cathode (or vise versa). One of active electrodes (a cathode or an anode) of a battery stack may be formed as the shell layer 22.

To be able to step-conformally deposit the battery stack layers, a low pressure deposition technique may be employed. This technique may include, e.g., a Low Pressure Chemical Vapor Deposition (LPCVD), an Atomic Layer Deposition (ALD) or special types of Physical Vapor Deposition (PVD), such as, biased sputtering. The battery stack 40 may include, e.g., LiMOx cathodes, solid-state electrolytes and Li-intercalation anodes (such as LiAl, LiSi, LiIn, LiZn, …). In one illustrative embodiment, using LPCVD, step conformal anodes (silicon), solid electrolytes (Li_3PO_4) and cathodes ($LiCoO_2$) can be manufactured. Other materials and processes may also be employed.

The present principles employ highly-controllable nanowire growth for creating a 3D backbone or skeleton structure on a planar substrate, which can additionally be covered by a layer of active (Lithium intercalation) material, e.g., solid electrolytes (Li_3PO_4) and cathodes ($LiCoO_2$) of a battery stack. Additionally, the surface coverage or wire density can be tuned accurately in a wide range (from about 0.1% to over 50%). The tuning of the wire density may be controlled by chamber temperature and pressure during catalyst deposition/formation (12, 14). Further, the wire density may be controlled by creating conditions for forming a 3D skeleton. This may include depositing a second generation of catalyst particles on side walls of the nanowires and growing branches.

Catalysts used for either or both of the first and second generations may include Au, Ag, Cu, Ni, Fe, Co (transition metals), etc., preferably metals with a low melting temperature. However, catalyst materials may comprise the same element(s) as the nanowires 18 to be grown, such as, e.g., Ga, In, Zn, Al, etc.

Referring to FIG. 5, a sequence for growing branches 54 from nanowires 18 is illustratively depicted. A second generation of catalyst particles 52 is deposited on side walls of the nanowires 18. Using VLS, branches 54 are grown outward from the nanowire 18. This provides a greater topography and may increase the surface area of the skeleton employed for forming a thin-film battery. As with the nanowire 18, due to the inert nature of the skeleton material, the structure, which may be employed in batteries, does not suffer from degradation upon intercalation cycling, and provides a very high storage capacity, stability and fast diffusion through the thin active layers.

Referring to FIG. 6, a method for fabricating a battery in accordance with an illustrative embodiment is depicted. In block 102, a substrate is provided. In block 104, wires are grown on the substrate to form a three-dimensional skeleton structure. The skeleton structure resists degradation due to intercalation cycling through material selection. In block 106, in a preferred embodiment, a vapor-liquid-solid (VLS) mechanism is employed to grow the wires from the substrate. The VLS mechanism includes depositing catalyst particles on the substrate and growing the wires in a substantially vertical form at the sites of the catalyst particles. The wires are preferably nanowires and have a diameter of between about 20nm and 50 nm. In one embodiment, the wires include at least one of a group IV material, a II-IV material, a III-V material, and/or suitable combinations thereof. In particularly useful embodiments, the wires may include at least one of GaN, InP and ZnO. The wires on the substrate are formed at a first temperature, which is preferably less than or equal to 420 degrees Celsius. In block 108, a density of the wires is tunable in accordance with process parameters. The density can be adjusted from between about 0.1% to about 50%.

In block 110, a second deposition of catalyst particles may be formed on sides of the wires and the VLS mechanism is again applied to form branches from the sides of the wires. In block 112, doping type and density of the wires is controlled to ensure conductivity in the wires. In block 114, a barrier layer is optionally formed over the wires that ensures that no electrochemically active species (which may include Li(0) or Li+ in the case of lithium-ion batteries) can diffuse from active intercalation material which would be subsequently formed onto the underlying skeleton structure (e.g., a shell layer).

In block 116, a battery stack is formed over the wires of the skeleton structure. The battery stack layer includes a shell layer. The shell layer is formed in contact with the barrier layer or the wires of the skeleton structure. The shell layer may include at least one of Si, Ge, and a III-V material if the wires are formed from II-IV material or a III-V material. The shell layer includes an active intercalation material deposited on the barrier layer/skeleton structure. The active intercalation material may include a lithium compound, and is preferably part of a battery stack formed over the skeleton structure. The shell layer preferably forms a first active electrode, followed by an electrolyte and a second active electrode to form the battery stack.

In interpreting the appended claims, it should be understood that:

a) the word "comprising" does not exclude the presence of other elements or acts than those listed in a given claim;

b) the word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements;

c) any reference signs in the claims do not limit their scope;

d) several "means" may be represented by the same item or hardware or software implemented structure or function; and

e) no specific sequence of acts is intended to be required unless specifically indicated.

Having described preferred embodiments for a large capacity thin film battery and methods for making same (which are intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments of the disclosure disclosed which are within the scope and spirit of the embodiments disclosed herein as outlined by the appended claims. Having thus described the details and particularity required by the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.

CLAIMS:

1. A method for fabricating a battery, comprising:

growing (104) wires up from a substrate to form a three-dimensional skeleton structure to increase a surface area; and

depositing (116) a battery stack on the skeleton structure with increased surface area.

2. The method as recited in claim 1, wherein growing wires includes growing nanowires having a diameter of between about 20nm and 50 nm.

3. The method as recited in claim 1, wherein growing wires includes applying (106) a vapor-liquid-solid (VLS) mechanism to grow the wires from the substrate.

4. The method as recited in claim 3, wherein applying (106) the VLS mechanism includes depositing catalyst particles on the substrate and growing the wires in a vertical form at sites of the catalyst particles.

5. The method as recited in claim 4, further comprising depositing (110) second catalyst particles on sides of the wires and applying the VLS mechanism to form branches from the sides of the wires.

6. The method as recited in claim 1, further comprising controlling (112) doping type and density of the wires to provide conductivity in the wires.

7. The method as recited in claim 1, further comprising forming (116) a shell

layer over the skeleton structure wherein the shell layer includes an electrochemically stable structure which is thermodynamically unable to store or is able to reversibly insert and extract an active species material of the battery stack.

8. The method as recited in claim 1, further comprising forming (114) a barrier layer over the wires to reduce diffusion of an active species of the battery stack.

9. The method as recited in claim 1, wherein the battery stack includes a lithium compound.

10. The method as recited in claim 1, further comprising tuning (108) a density of the wires in accordance with process parameters.

11. The method as recited in claim 10, wherein the density is adjusted from between about 0.1% to about 50%.

12. A method for fabricating a battery, comprising:

growing (104) wires on a substrate to form a three-dimensional skeleton structure by applying a vapor-liquid-solid (VLS) mechanism to grow the wires from the substrate;

forming (116) a shell layer over the wires an a first active electrode which is thermodynamically unable to store or is able to reversibly insert and extract an active species of a battery stack; and

depositing (116) an electrolyte layer and a second active electrode to form the battery stack over the skeleton structure.

13. The method as recited in claim 12, wherein growing wires includes growing nanowires having a diameter of between about 20 and 50 nm.

14. The method as recited in claim 12, wherein applying (106) the VLS mechanism includes depositing catalyst particles on the substrate and growing the wires in a vertical form at sites of the catalyst particles, and depositing (108) second catalyst particles on sides of the wires and applying the VLS mechanism to form branches from the sides of the wires.

15. The method as recited in claim 12, further comprising controlling (112) doping type and density of the wires to provide conductivity in the wires.

16. The method as recited in claim 12, further comprising forming (114) a barrier layer over the wires to reduce diffusion of the active species of the battery stack.

17. The method as recited in claim 12, further comprising tuning (108) a density of the wires in accordance with process parameters, wherein the density is adjusted from between about 0.1% to about 50%.

18. A thin film battery (TFB), comprising:

a semiconductor substrate (10);

a plurality of vertical vapor-liquid-solid (VLS) grown nanowires (18) attached to the substrate to form a three-dimensional skeleton structure, the skeleton structure being formed to enhance surface area; and a battery stack (40) deposited on the skeleton structure, the battery stack having active electrodes with a thickness less than active electrode layers used with planar formed battery stacks of a same capacity resulting in increased lifetime and stability of the battery stack.

19. The battery as recited in claim 18, wherein the nanowires include a diameter of between about 20 and 50 nm.

20. The battery as recited in claim 18, further comprising branches (54) attached to sides of the nanowires.

21. The battery as recited in claim 18, further comprising a barrier layer (24) formed over the wires to reduce diffusion of an active species of the battery stack.

22. The battery as recited in claim 18, wherein the nanowires have a density between about 0.1% to about 50%.

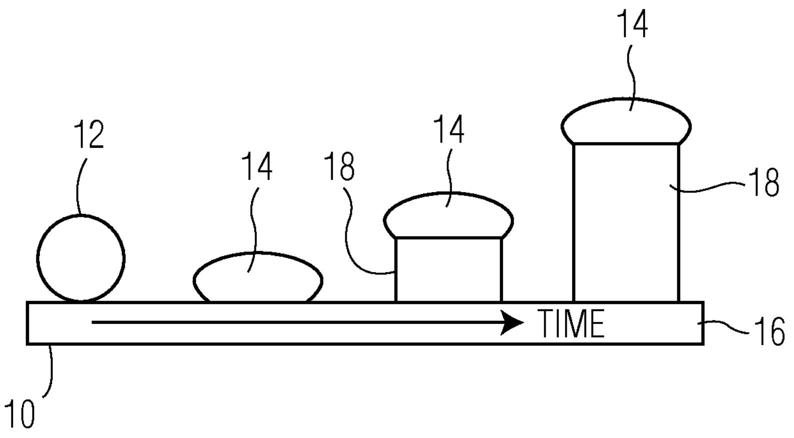

FIG. 1

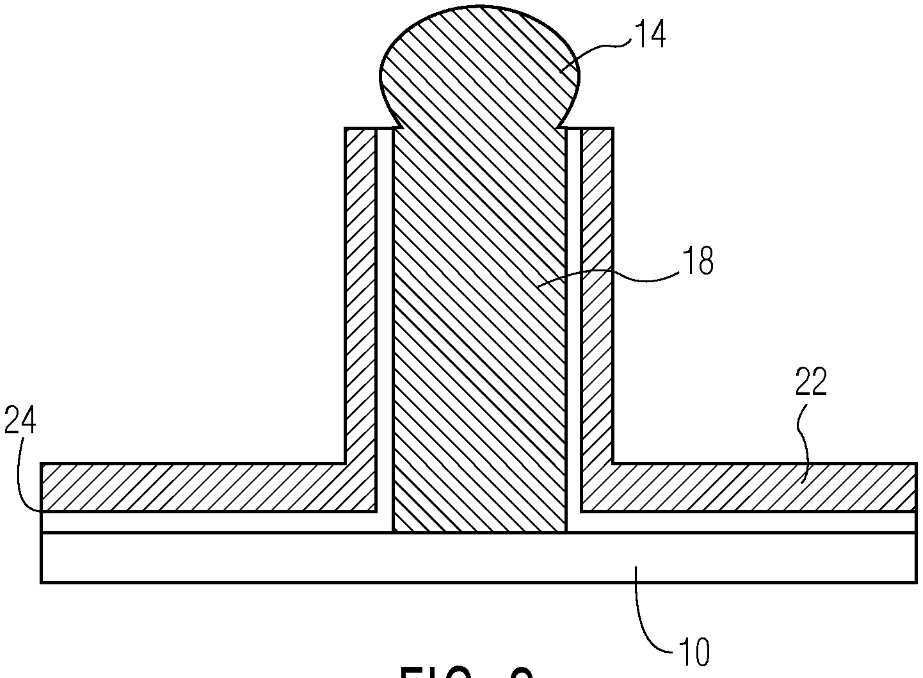

FIG. 2

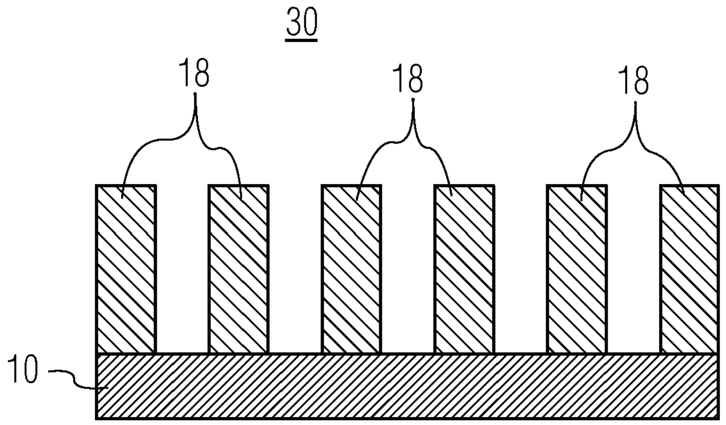

FIG. 3

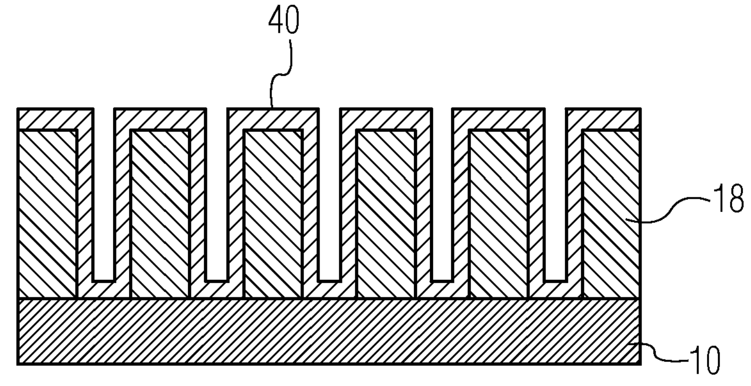

FIG. 4

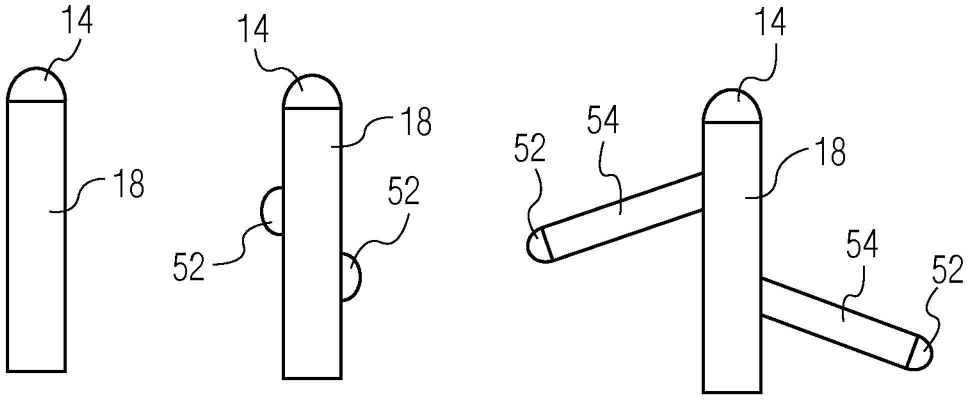

FIG. 5

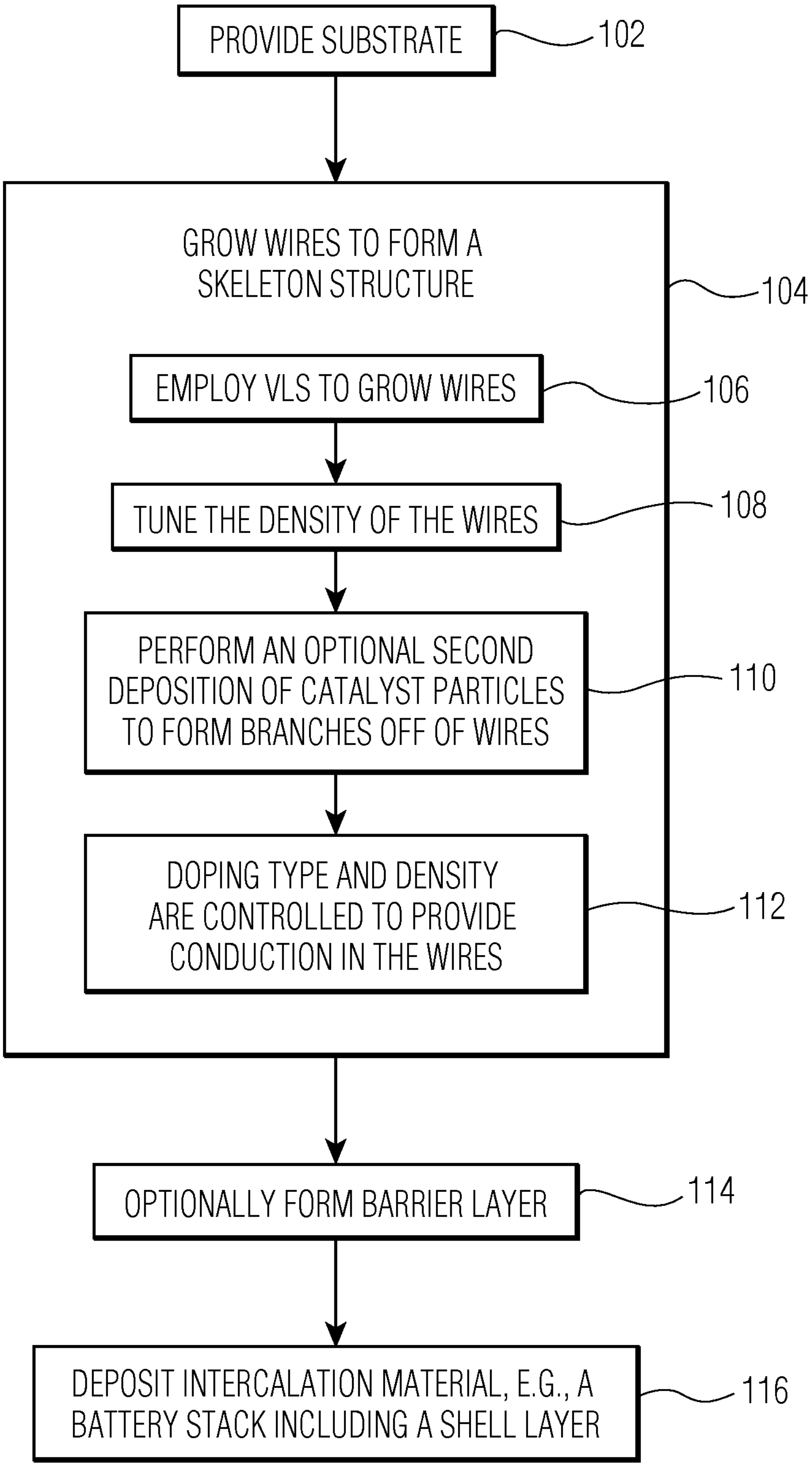
PROVIDE SUBSTRATE
102
GROW WIRES TO FORM A SKELETON STRUCTURE
104
EMPLOY VLS TO GROW WIRES
106
TUNE THE DENSITY OF THE WIRES
108
PERFORM AN OPTIONAL SECOND DEPOSITION OF CATALYST PARTICLES TO FORM BRANCHES OFF OF WIRES
110
DOPING TYPE AND DENSITY ARE CONTROLLED TO PROVIDE CONDUCTION IN THE WIRES
112
OPTIONALLY FORM BARRIER LAYER
114
DEPOSIT INTERCALATION MATERIAL, E.G., A BATTERY STACK INCLUDING A SHELL LAYER
116

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2010/050881

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01M4/1395 H01M4/134 H01M4/04 H01M10/0525 H01M4/70
H01M4/38 H01M6/40
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	LI-FENG CUI ET AL: "Crystalline-Amorphous Core-Shell Silicon Nanowires for High Capacity and High Current Battery Electrodes" NANO LETTERS, ACS, WASHINGTON, DC, US LNKD- DOI:10.1021/NL8036323, vol. 9, no. 1, 1 January 2009 (2009-01-01), pages 491-495, XP007913274 ISSN: 1530-6984 [retrieved on 2008-12-23]	1-4,6,7, 9,12,13, 18,19
Y	the whole document ----- -/--	5,8,10, 11, 14-17, 20-22

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search 8 June 2010	Date of mailing of the international search report 15/06/2010
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Maître, Jérôme

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2010/050881

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 2009/042102 A1 (CUI YI [US] ET AL) 12 February 2009 (2009-02-12) paragraphs [0029] - [0030], [0046] - [0050]; figures 1,2,4	1-4,6,9, 13,18
X	WO 01/96847 A1 (UNIV NORTH CAROLINA CHAPEL HIL [US]; ZHOU OTTO Z [US]; GAO BO [US]; SI) 20 December 2001 (2001-12-20) claims 1-16; figure 1	1,2,9,18
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