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(54) Title: STACKED DIE PACKAGE WITH THROUGH-MOLD THERMALLY CONDUCTIVE STRUCTURES BETWEEN A BOTTOM DIE AND A THERMALLY CONDUCTIVE MATERIAL

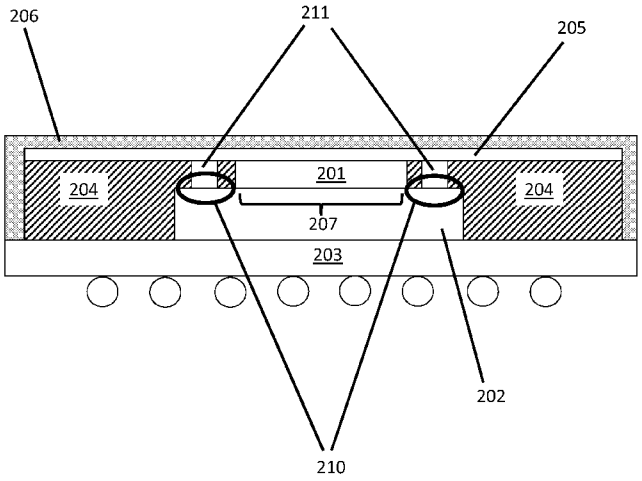


Fig. 2

(57) Abstract: An apparatus is described that includes a first semiconductor die. A second semiconductor die is stacked on the first semiconductor die. The first semiconductor die has a larger surface area than the second semiconductor die such that there exists a peripheral region of the first semiconductor die that is not covered by the second semiconductor die. The apparatus includes thermally conductive material above the second semiconductor die. The apparatus includes a compound mold between the thermally conductive materila and both the second semiconductor die and the peripheral region of the first semiconductor die. The apparatus includes a thermally conductive structure extending through the compound mold that thermally couples the peripheral region to the thermally conductive material.

STACKED DIE PACKAGE WITH THROUGH-MOLD THERMALLY CONDUCTIVE STRUCTURES BETWEEN A BOTTOM DIE AND A THERMALLY CONDUCTIVE MATERIAL

Field Of Invention

The field of invention pertains generally to the semiconductor arts, and, more specifically, to a stacked die package with through-mold thermally conductive structures between a bottom die and a thermally conductive material.

Background

The semiconductor arts has traditionally faced the challenge of attempting to integrate electronic functionality into as small a volume as possible. Chip stacking has recently emerged as a popular packaging technology for integrating multiple semiconductor die into a same semiconductor package. A problem, however, is the heat dissipation that multiple die can generate within the package.

Figures

A better understanding of the present invention can be obtained from the following detailed description in conjunction with the following drawings, in which:

Fig. 1 shows a prior art stacked die package;

Fig. 2 shows an improved prior art package;

Figs. 3a through 3i show a process flow for manufacturing the improved prior art package of Fig. 2;

Fig. 4 shows a methodology of the process flow of Figs. 3a through 3i;

Fig. 5 shows a computing system.

Detailed Description

Fig. 1 shows a standard stacked die structure that includes a top semiconductor die 101 stacked on top of a bottom semiconductor die 102. The top die 101 may be electrically and mechanically attached to the bottom die 102 through, e.g., a land grid array structure or micro-bumps. Likewise, the bottom die 102 is electrically and mechanically coupled to a substrate 103 with, e.g., a land grid array or micro-bumps. A ball grid array may exist on the bottom of the package substrate 103 which forms the I/Os of the package.

Surrounding the stacked die structure is a mold compound 104 that is covered by a thermally conductive interface material 105. The resulting structure is encapsulated with a lid 106 that may also act as a heat spreader. The thermally conductive interface material 105 is a layer of thermally conductive material (e.g., silicone polymer resin filled with a thermally conductive filler, a polymer based thermal grease, etc.) and is used to propagate heat generated from the stacked die 101, 102 to the lower surface area of the package lid 106.

The lid 106, by spreading the heat generated from the stacked die structure uniformly across its surface, can remove heat from the stacked die 101, 102 more efficiently.

As observed in Fig. 1, the thermally conductive interface material 105 is positioned in close proximity to the top surface of the upper die 101. Additionally, the thermal conductance between the top die 101 and the thermally conductive interface material 105 may be reduced, e.g., with a thermally conductive adhesive between the top die 101 and thermally conductive interface material 105 and/or thermally conductive lands/balls/studs formed on the upper surface of the top die 101 that are in contact with the thermally conductive interface material 105.

Higher thermal conductance may also exist between the portion 107 of the bottom die 102 that resides directly beneath the top die 101. As with the interface between the top die 101 and thermally conductive interface material 105, the interface between the top die 101 and portion 107 of the bottom die may be designed to exhibit high thermal conductivity with, e.g., a thermally conductive adhesive and/or lands/balls/studs that are mechanically coupled between the two die 101, 102.

A problem, however, concerns the regions 110 of the upper surface of the bottom die 102 that are not directly beneath the top die 101. The thermal conductance between these regions 110 and thermally conductive interface material 105 is determined primarily by the thermal conductance of the mold compound 104 that resides between these regions 110 and thermally conductive interface material 105.

Traditional mold compounds, such as silica filler molds, commonly have a thermal conductivity of less than 2.0 W/mK (e.g., approximately 1.0 W/mk) because the silica or other traditional mold compound filler is thermally insulating. Unfortunately, traditional compound molds having thermally insulating fillers do not possess a thermal conductivity that is high enough to properly remove heat from regions 110, particularly if the bottom die 102 exhibits a “hot spot” at regions 110. A hot spot is, e.g., a surface area of a semiconductor die that generates substantially more heat than other surface regions of the die (e.g., because the die includes high voltage, high current and/or high frequency transistors directly beneath the hot spot).

Non traditional mold compounds having higher thermal conductivities because they include fillers that are substantially thermally conductive exist (e.g., alumina filler molds, copper filler molds, etc., that exhibit thermal conductivities of approximately 4.0 W/mk of higher). However, these compounds unfortunately are more expensive than the traditional mold compounds and they exhibit a higher thermal coefficient of expansion. Besides the higher expense being undesirable, the higher thermal coefficient of expansion can cause reliability problems because stresses are induced within the package while the compound is conducting heat.

Fig. 2 shows an improved stacked die structure having thermally conductive structures 211 that are deliberately placed between the outer regions 210 of the upper surface of the bottom die 202 and the thermally conductive interface material 205. The thermally conductive structures 211 are designed to thermally couple regions 210 to the thermally conductive interface material 205 in order to dramatically reduce the thermal resistance that exists between corresponding regions 110 and the thermally conductive interface material 105 of Fig. 1.

In various embodiments, the thermally conductive structures 211 are strategically placed directly over a known hot spot of the bottom die 202. Here, designers of the bottom die 202 will be able to understand from their design which regions of the die surface will generate heat commensurate with a hot spot (e.g., by knowing which transistors operate with higher voltage, higher current and/or higher frequency).

With an understanding of where such hot spots will appear at outer regions 210, the designers of the package can strategically "drop-in" one or more thermally conductive structures 211 directly over each such hot spot. Alternatively or in combination, thermally conductive structures may be randomly and/or periodically located at various locations around the circumference of the upper surface bottom die 202 along regions 210 to more generally remove heat from the surface of the bottom die around regions 210.

Figs. 3a through 3i show a method for manufacturing the stacked package design of Fig. 2. As observed in Fig. 3a, in an embodiment a semiconductor wafer 322 containing multiple instances of the bottom die 302_1, 302_2, etc. is mounted to a carrier wafer 313 (e.g., with a removable adhesive). In an alternative process, rather than attached an entire wafer of bottom die to the carrier wafer 313, instead, singulated bottom die are individually placed and affixed to the carrier wafer. For simplicity, the remainder of the discussion will refer to a process in which an entire wafer of bottom die is attached to the carrier wafer 313.

As observed in Fig. 3b, a respective top die 301_1, 301_2, etc. is properly positioned and affixed to a corresponding respective one of the bottom die 302_1, 302_2. In an embodiment, micro-bumps are used to electrically and mechanically couple the top die 301_1, 301_2 to their respective bottom die 302_1, 302_2.

In the case of micro-bump coupling, micro-bumps of solder are affixed to the surfaces of one of the top and bottom die 301, 302. Receiving lands on the other die are aligned with the bumps. When the two die are mated, the solder bumps are coupled to their respective lands and reflowed to form multiple micro-bump joints. For simplicity Fig. 3b does not show any micro-bumps and instead suggests a land-grid array interface between the bottom and top die 301, 302. Either type of joint may be used to provide electrical and/or thermally conductive coupling between the top and bottom die 301, 302.

As observed in Fig. 3c, after the top die 301 are affixed to the bottom die 302 a conventional mold compound 304 as described above is formed over the stacked die array.

As observed in Fig. 3d, the mold 304 is etched, e.g., in strategic locations over expected hot spots of the lower die 302_1, 302_2 that extend beyond (i.e., are not respectively covered by) the surface area of the top die 301_1, 301_2. The etching may be performed with, e.g., laser ablation. With laser ablation, laser light is directed upon the mold 304 just above a hot spot region of the bottom die and mold compound material is steadily removed until the upper surface of the bottom die 302_1, 302_2 is reached.

As observed in Fig. 3e, a stencil 315 is then placed on the surface of the mold 304 and thermally conductive paste 316 (e.g., solder paste is one possible paste) is pressed through openings in the stencil 315 that are aligned with the openings that were just formed in the mold 304. After the applied solder paste 316 suitably fills the openings in the mold 304, the paste 316 is sintered (hardened) through application of an elevated temperature. Alternative thermally conductive materials and/or fill techniques may be used to fill the mold openings. For example, copper or other metal or metal alloy may be plated into the openings.

As observed in Fig. 3f, after the mold openings are filled with thermally conductive material 316, the resulting structure is thinned approximately to the top surface of the top die 301_1, 301_2. Here, various polishing or other planarization techniques may be used to form a substantially planar top surface 317 that extends approximately as high as the top surface of the top die 301_1, 301_2.

As observed in Fig. 3g, the carrier wafer 313 is removed and the bottom die wafer 322 is scribed and broken or sawed to singulate the array of stacked die structures that existed as of the end of the processing of Fig. 3f.

As observed in Fig. 3h, a singulated stacked die structure is mechanically and electrically attached to a package substrate 303. Here, the bottom surface of the bottom die 302 is electrically and mechanically coupled to the package substrate 303 through a land grid interface, micro-bump interface and/or via/stud interface. The electrical connections formed between the bottom of the bottom die 302 and the package substrate 303 correspond to the I/Os of the stacked structure. As such, electrical traces within the package substrate 303 run to, e.g., conductive balls 318 of a ball-grid array package interface.

As observed in Fig. 3i, the thermally conductive interface material 305 is affixed to the top surface of the top die 301 and a lid 306 is placed over the thermally conductive interface material 305 and mounted to the package substrate 303 to encapsulate the stacked die structure. In alternative embodiments, the thermally conductive interface material 305 may be placed on the structure of Fig. 3f prior to singulation. The thermal conductance between the top die 301 and the thermally conductive interface material 305 may be reduced, e.g., with a thermally conductive adhesive between the top die 301 and the thermally conductive interface material 305 and/or thermally conductive lands/studs formed on the top of the top die 301 that are in contact with the thermally conductive interface material 305.

Fig. 4 shows a method outlined by the process flow described just above. As observed in Fig. 4 the method includes stacking 401 a second semiconductor die onto a first semiconductor die to form a stacked semiconductor die structure, where, the first semiconductor die has a larger surface area than the second semiconductor die such that there exists a peripheral region of the first semiconductor die that is not covered by the second semiconductor die. The method also includes forming 402 a compound mold over the stacked semiconductor die structure. The method also includes creating 403 an opening in the compound mold over the peripheral region. The method includes inserting 404 first thermally conductive material into the opening. The method includes forming 405 a second thermally conductive material over the compound mold, the first thermally conductive material thermally coupling the second thermally conductive material and the peripheral region.

Fig. 5 shows a depiction of an exemplary computing system 500 such as a personal computing system (e.g., desktop or laptop) or a mobile or handheld computing system such as a tablet device or smartphone, or, a larger computing system such as a server computing system.

As observed in Fig. 5, the basic computing system may include a central processing unit 501 (which may include, e.g., a plurality of general purpose processing cores and a main memory controller disposed on an applications processor or multi-core processor), system memory 502, a display 503 (e.g., touchscreen, flat-panel), a local wired point-to-point link (e.g., USB) interface 04, various network I/O functions 505 (such as an Ethernet interface and/or cellular modem subsystem), a wireless local area network (e.g., WiFi) interface 506, a wireless point-to-point link (e.g., Bluetooth) interface 507 and a Global Positioning System interface 508, various sensors 509_1 through 509_N (e.g., one or more of a gyroscope, an accelerometer, a magnetometer, a temperature sensor, a pressure sensor, a humidity sensor, etc.), a camera 510, a battery 511, a power management control unit 512, a speaker and microphone 513 and an audio coder/decoder 514.

An applications processor or multi-core processor 550 may include one or more general purpose processing cores 515 within its CPU 501, one or more graphical processing units 516, a memory management function 517 (e.g., a memory controller) and an I/O control function 518. The general purpose processing cores 515 typically execute the operating system and application software of the computing system. The graphics processing units 516 typically execute graphics intensive functions to, e.g., generate graphics information that is presented on the display 503. The memory control function 517 interfaces with the system memory 502. The system memory 502 may be a multi-level system memory.

The computing system may contain a stacked die package as described above. For example, the upper die may be a system memory chip and the lower die may be a system-

on-chip that includes the processing cores (and, e.g., the memory controller and/or the I/O control unit).

Each of the touchscreen display 503, the communication interfaces 504 – 507, the GPS interface 508, the sensors 509, the camera 510, and the speaker/microphone codec 513, 514 all can be viewed as various forms of I/O (input and/or output) relative to the overall computing system including, where appropriate, an integrated peripheral device as well (e.g., the camera 510). Depending on implementation, various ones of these I/O components may be integrated on the applications processor/multi-core processor 550 or may be located off the die or outside the package of the applications processor/multi-core processor 550.

Embodiments of the invention may include various processes as set forth above. The processes may be embodied in machine-executable instructions. The instructions can be used to cause a general-purpose or special-purpose processor to perform certain processes. Alternatively, these processes may be performed by specific hardware components that contain hardwired logic for performing the processes, or by any combination of programmed computer components and custom hardware components.

Elements of the present invention may also be provided as a machine-readable medium for storing the machine-executable instructions. The machine-readable medium may include, but is not limited to, floppy diskettes, optical disks, CD-ROMs, and magneto-optical disks, FLASH memory, ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, propagation media or other type of media/machine-readable medium suitable for storing electronic instructions. For example, the present invention may be downloaded as a computer program which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals embodied in a carrier wave or other propagation medium via a communication link (e.g., a modem or network connection).

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

An apparatus has described that includes a first semiconductor die. A second semiconductor die is stacked on the first semiconductor die. The first semiconductor die has a larger surface area than the second semiconductor die such that there exists a peripheral region of the first semiconductor die that is not covered by the second semiconductor die. The apparatus includes thermally conductive material above the second semiconductor die. The apparatus includes a compound mold between the thermally conductive materila and both the second semiconductor die

and the peripheral region of the first semiconductor die. The apparatus includes a thermally conductive structure extending through the compound mold that thermally couples the peripheral region to the thermally conductive material.

In an embodiment, the compound mold comprises a thermally insulating filler. In yet another embodiment, the compound mold does not comprise a substantially thermally conductive filler. In yet another embodiment, the compound mold comprises a thermal conductivity of less than 2.0 W/mk. In yet another embodiment, the thermally conductive structure is formed from thermally conductive paste. In yet another embodiment, the thermally conductive structure is located over a hot spot of the first semiconductor die. In yet another embodiment, the apparatus includes a second thermally conductive structure over the hot spot, the thermally conductive structure extending through the compound mold that thermally couples the hot spot to the peripheral region. In yet another embodiment, the apparatus includes a second thermally conductive structure extending through the compound mold that thermally couples the peripheral region to the thermally conductive material.

A method has been described that includes stacking a second semiconductor die onto a first semiconductor die to form a stacked semiconductor die structure. The first semiconductor die has a larger surface area than the second semiconductor die such that there exists a peripheral region of the first semiconductor die that is not covered by the second semiconductor die. The method further includes forming a compound mold over the stacked semiconductor die structure. The further includes creating an opening in the compound mold over the peripheral region. The method further includes inserting first thermally conductive material into the opening. The method further includes forming second thermally conductive material over the compound mold, the first thermally conductive material thermally coupling the second thermally conductive material and the peripheral region.

In an embodiment, the compound mold comprises a silica filler. In another embodiment, the compound mold does not comprise an alumina or copper filler. In another embodiment the compound mold comprises a thermal conductivity of less than 2.0 W/mk. In another embodiment the first thermally conductive material comprises solder paste. In another embodiment the first thermally conductive material is located over a hot spot of the first semiconductor die.

A computer has also been described that includes a plurality of processing cores coupled to a memory controller. The memory controller is coupled to a system

memory and a peripheral control hub. The computer further includes a first semiconductor die and a second semiconductor die. The second semiconductor die is stacked on the first semiconductor die. The first semiconductor die has a larger surface area than the second semiconductor die such that there exists a peripheral region of the first semiconductor die that is not covered by the second semiconductor die. A thermally conductive material resides above the second semiconductor die. A compound mold exists between the thermally conductive material and both the second semiconductor die and the peripheral region of the first semiconductor die. A thermally conductive structure extends through the compound mold that thermally couples the peripheral region to the thermally conductive material.

In an embodiment the compound mold comprises a thermally insulating filler. In yet another embodiment the compound mold does not comprise a substantially thermally conductive filler. In yet another embodiment the compound mold comprises a thermal conductivity of less than 2.0 W/mk. In an embodiment the thermally conductive structure is formed from solder paste. In an embodiment the second semiconductor chip is a system memory chip and the first semiconductor chip is a semiconductor chip that comprises the plurality of processing cores.

Claims

An apparatus, comprising:

a first semiconductor die;

a second semiconductor die stacked on the first semiconductor die, the first semiconductor die having a larger surface area than the second semiconductor die such that there exists a peripheral region of the first semiconductor die that is not covered by the second semiconductor die;

thermally conductive material above the second semiconductor die;

a compound mold between the thermally conductive material and both the second semiconductor die and the peripheral region of the first semiconductor die; and,

a thermally conductive structure extending through the compound mold that thermally couples the peripheral region to the thermally conductive material.

2. The apparatus of claim 1 wherein the compound mold comprises a thermally insulating filler.

3. The apparatus of claim 1 wherein the compound mold does not comprise a substantially thermally conductive filler.

4. The apparatus of claim 1 wherein the compound mold comprises a thermal conductivity of less than 2.0 W/mk.

5. The apparatus of claim 1 wherein the thermally conductive structure is formed from thermally conductive paste.

6. The apparatus of claim 1 wherein the thermally conductive structure is located over a hot spot of the first semiconductor die.

7. The apparatus of claim 6 further comprising a second thermally conductive structure over the hot spot, the thermally conductive structure extending through the compound mold that thermally couples the hot spot to the peripheral region.

8. The apparatus of claim 1 further comprising a second thermally conductive structure extending through the compound mold that thermally couples the peripheral region to the thermally conductive material.

9. A method, comprising

stacking a second semiconductor die onto a first semiconductor die to form a stacked semiconductor die structure, the first semiconductor die having a larger surface area than the second semiconductor die such that there exists a peripheral region of the first semiconductor die that is not covered by the second semiconductor die;

forming a compound mold over the stacked semiconductor die structure;

creating an opening in the compound mold over the peripheral region;

inserting first thermally conductive material into the opening; and,

forming second thermally conductive material over the compound mold, the first thermally conductive material thermally coupling the second thermally conductive material and the peripheral region.

10. The method of claim 9 wherein the compound mold comprises a silica filler.

11. The method of claim 9 wherein the compound mold does not comprise an alumina or copper filler.

12. The method of claim 9 wherein the compound mold comprises a thermal conductivity of less than 2.0 W/mk.

13. The method of claim 9 wherein the first thermally conductive material comprises solder paste.

14. The method of claim 9 wherein the first thermally conductive material is located over a hot spot of the first semiconductor die.

15. A computer, comprising:

a plurality of processing cores coupled to a memory controller, the memory controller coupled to a system memory and a peripheral control hub, the computer further comprising:

a first semiconductor die;

a second semiconductor die stacked on the first semiconductor die, the first semiconductor die having a larger surface area than the second semiconductor die such that there exists a peripheral region of the first semiconductor die that is not covered by the second semiconductor die;

thermally conductive material above the second semiconductor die;

a compound mold between the thermally conductive material and both the second semiconductor die and the peripheral region of the first semiconductor die; and,

a thermally conductive structure extending through the compound mold that thermally couples the peripheral region to the thermally conductive material.

16. The computer of claim 15 wherein the compound mold comprises a ~~silica~~ thermally insulating filler.

17. The computer of claim 15 wherein the compound mold does not comprise a substantially thermally conductive filler.

18. The computer of claim 15 wherein the compound mold comprises a thermal conductivity of less than 2.0 W/mk.

19. The computer of claim 15 wherein the thermally conductive structure is formed from solder paste.

20. The computer of claim 15 wherein the second semiconductor chip is a system memory chip and the first semiconductor chip is a semiconductor chip that comprises the plurality of processing cores.

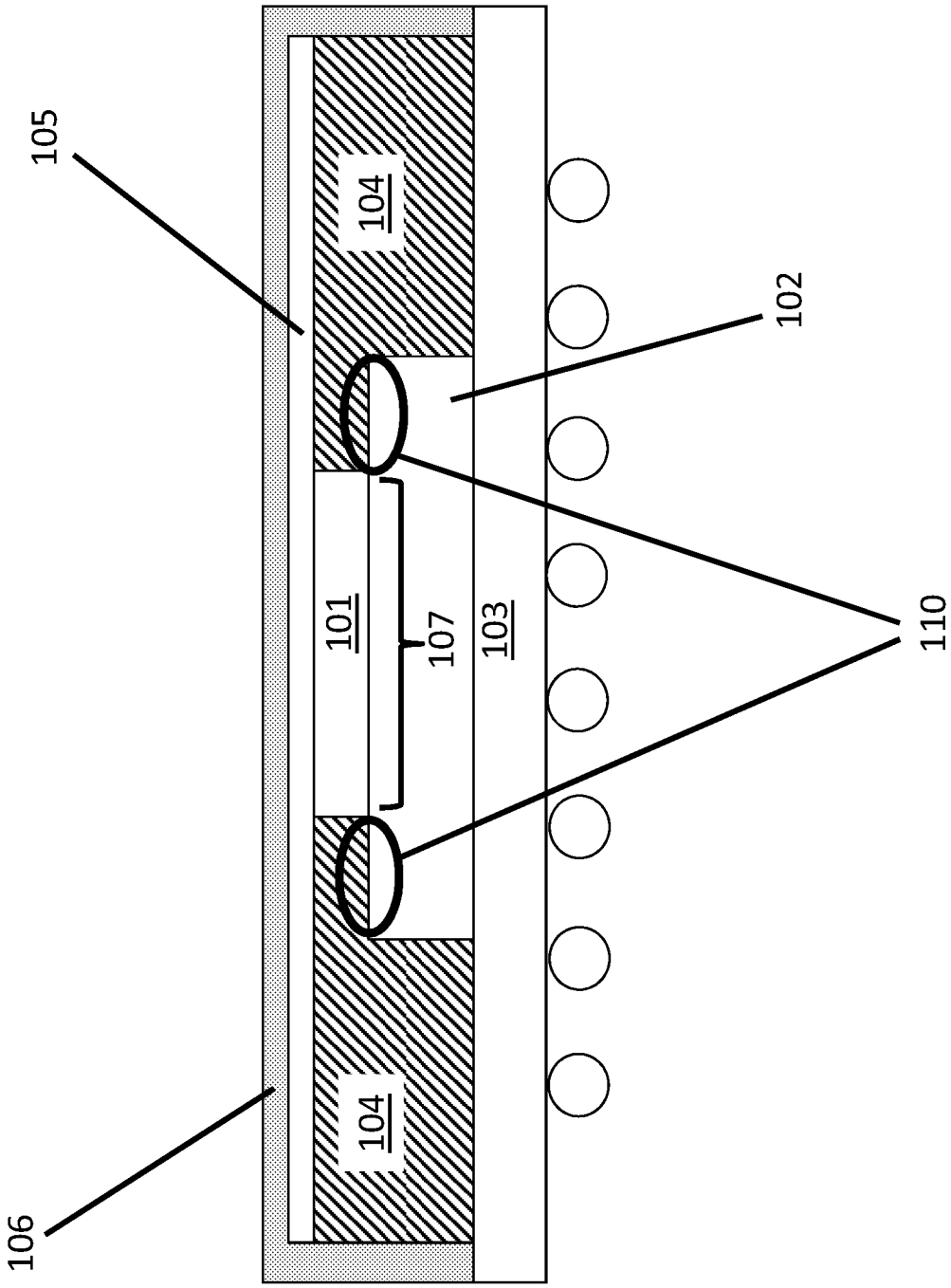


Fig. 1
(prior art)

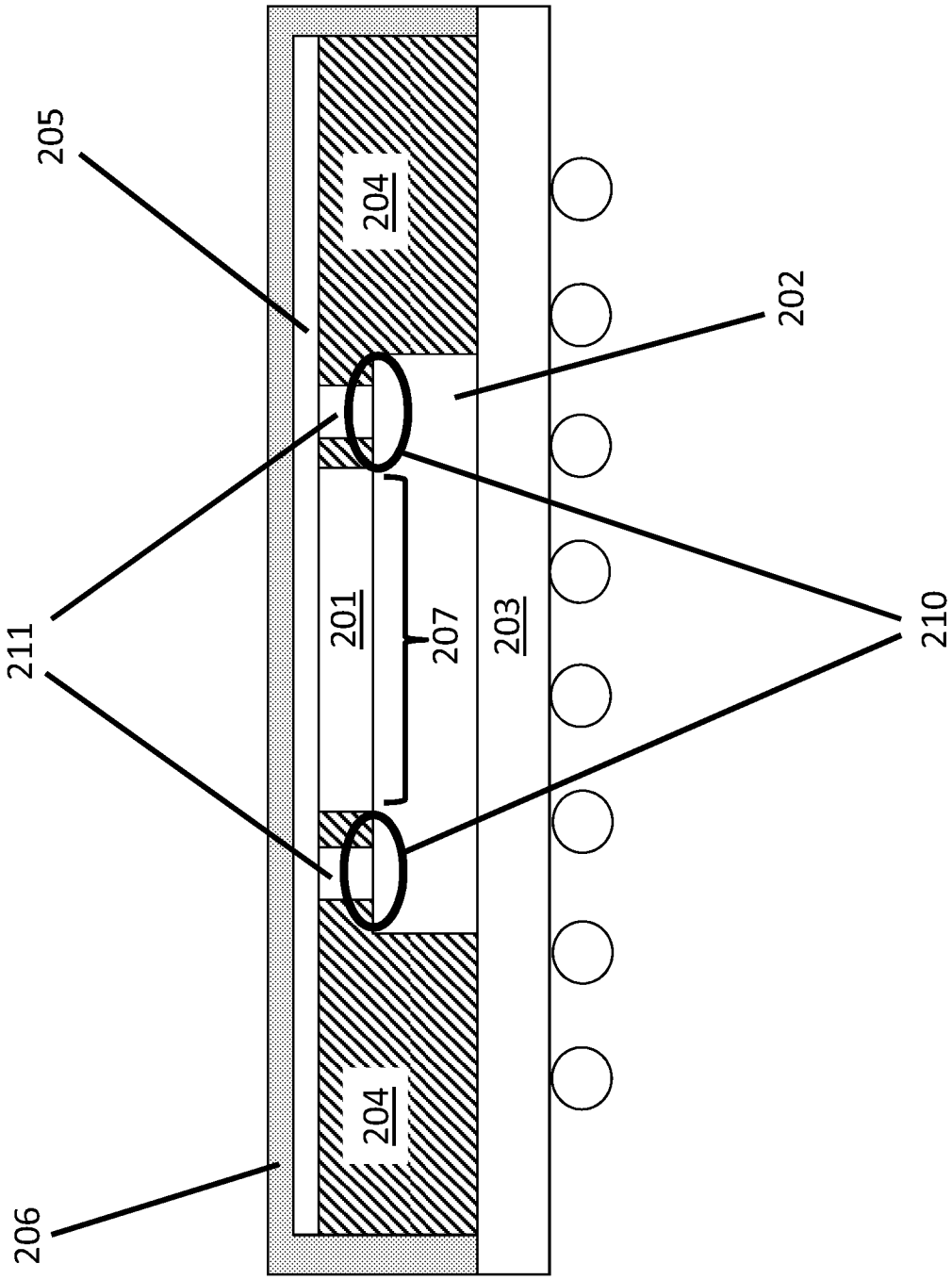


Fig. 2

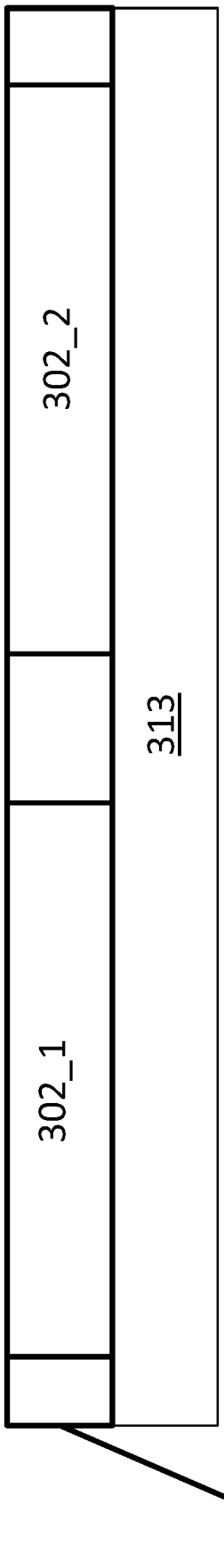


Fig. 3a

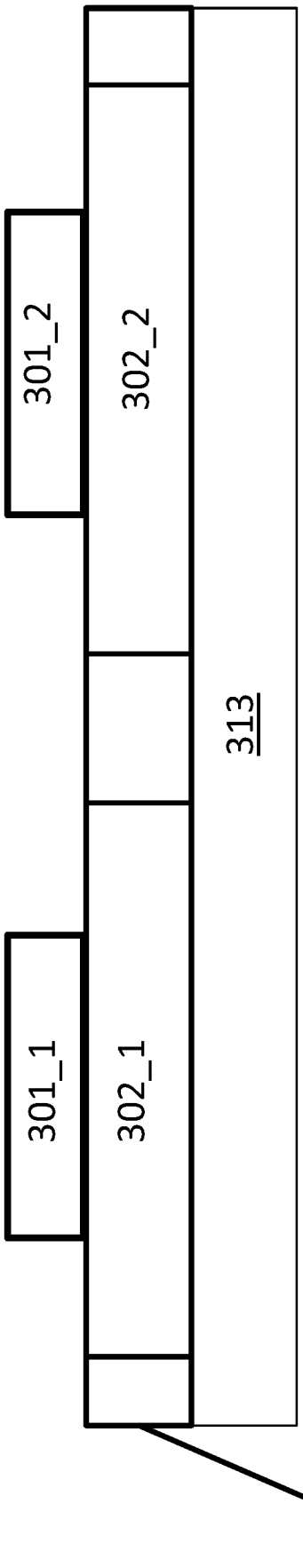


Fig. 3b

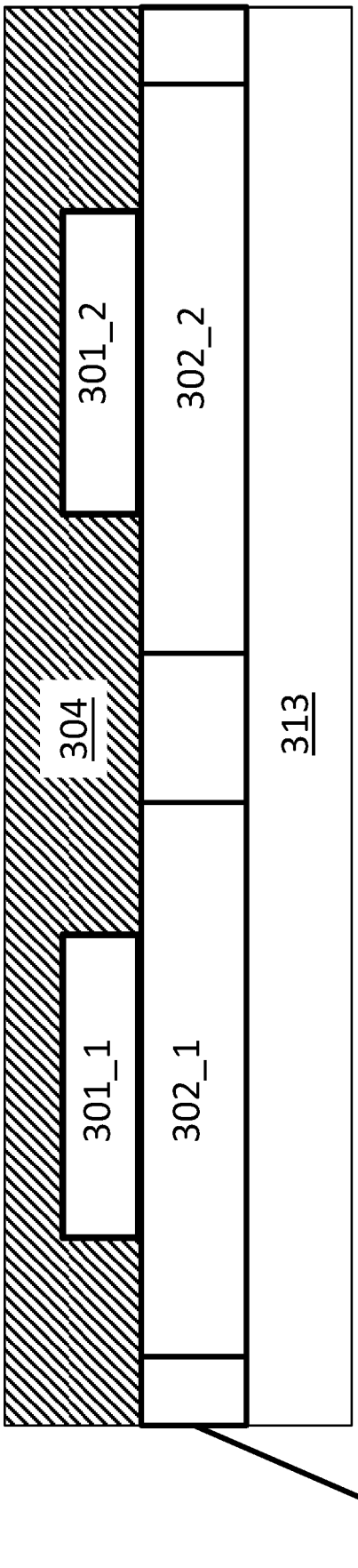


Fig. 3c

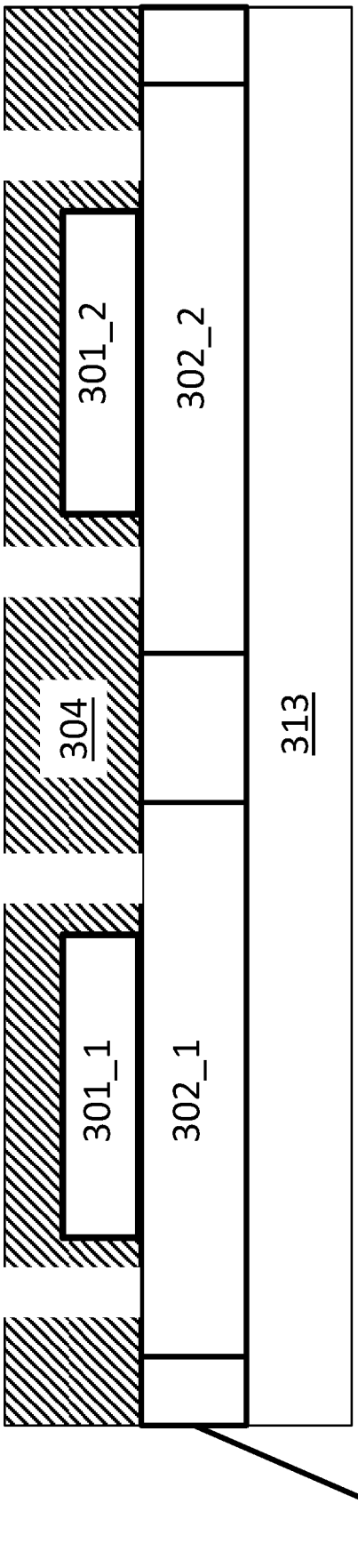


Fig. 3d

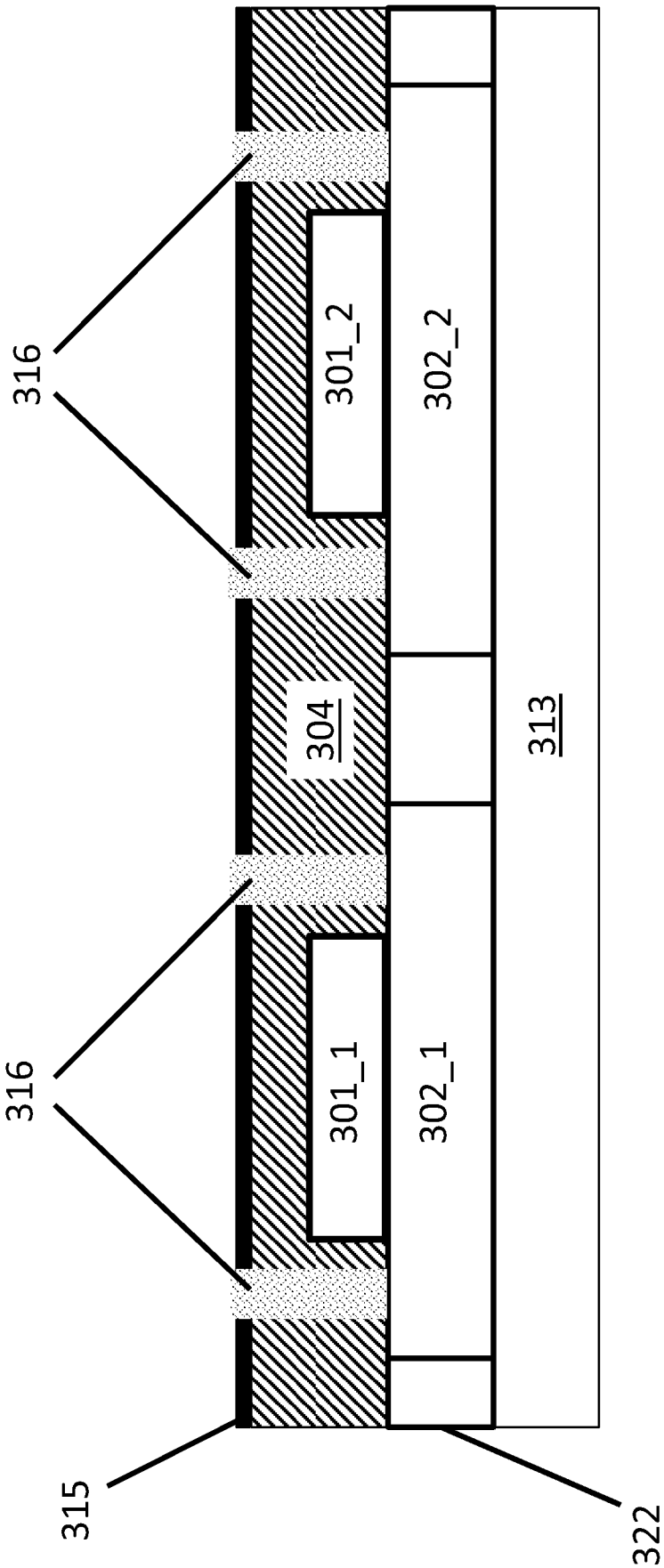


Fig. 3e

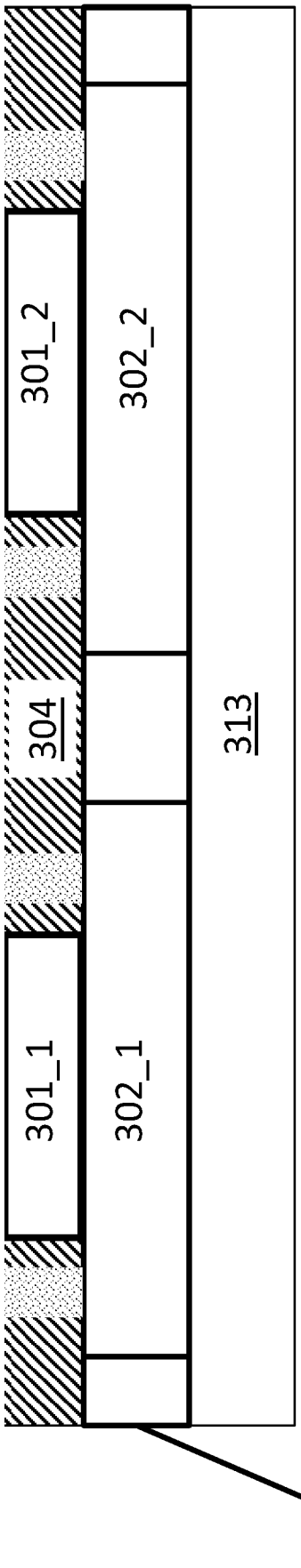


Fig. 3f

Fig. 3g

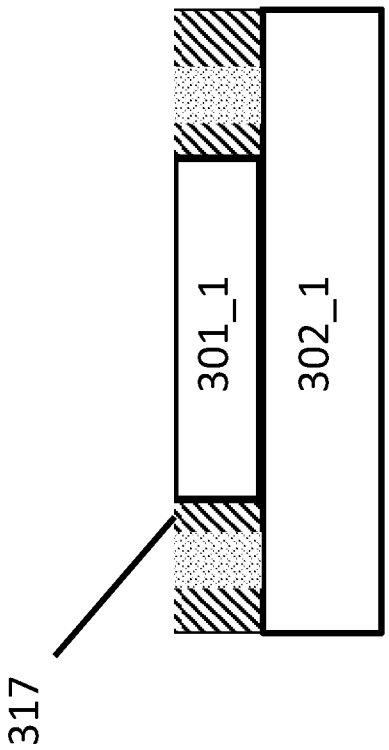
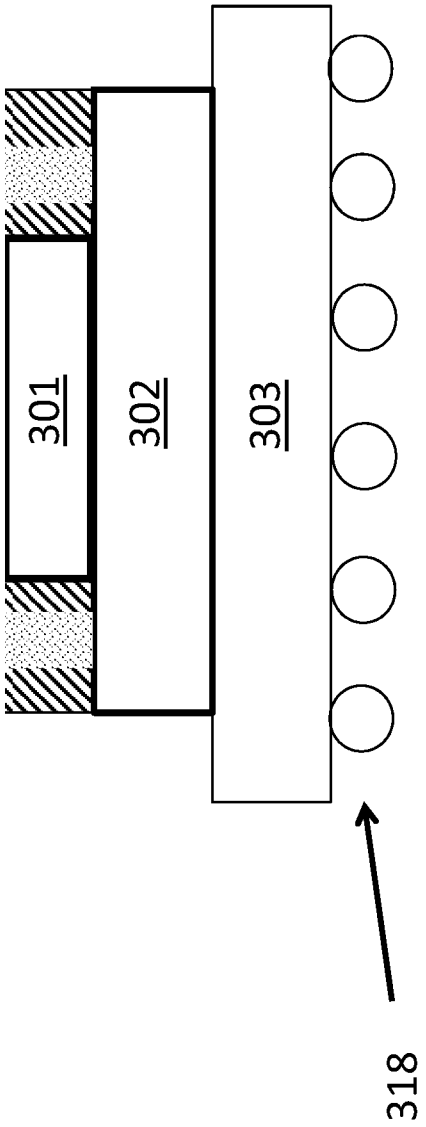


Fig. 3h



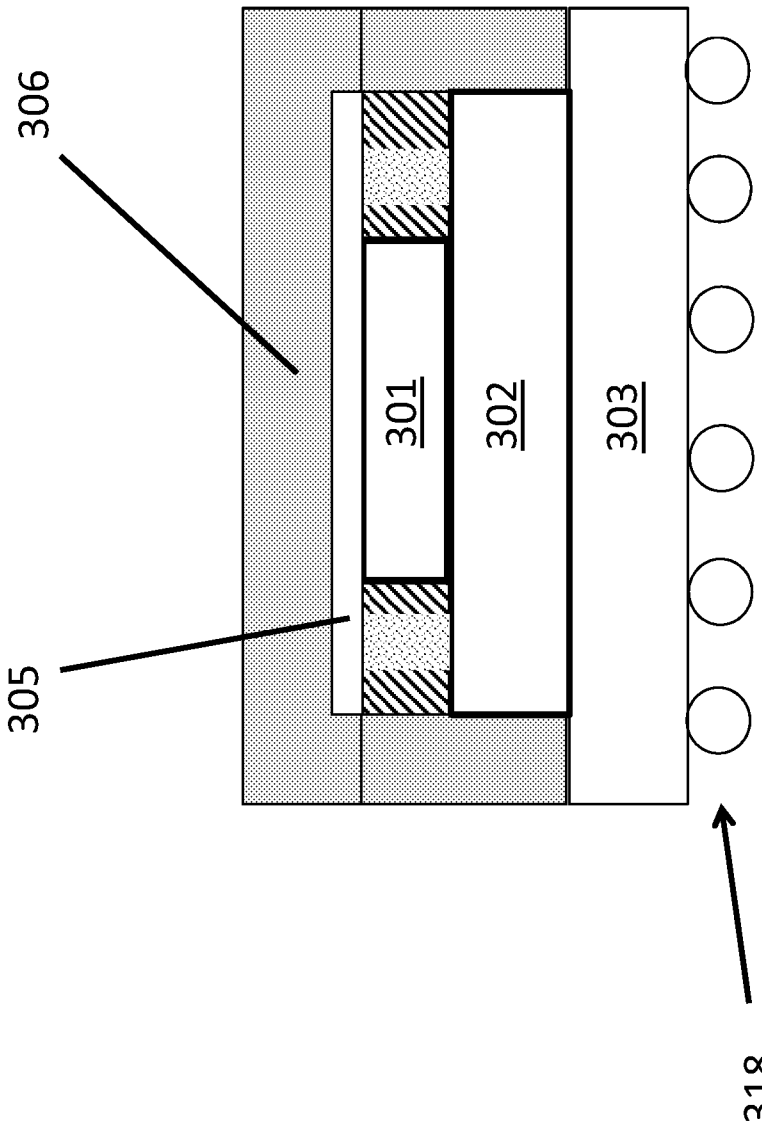


Fig. 3i

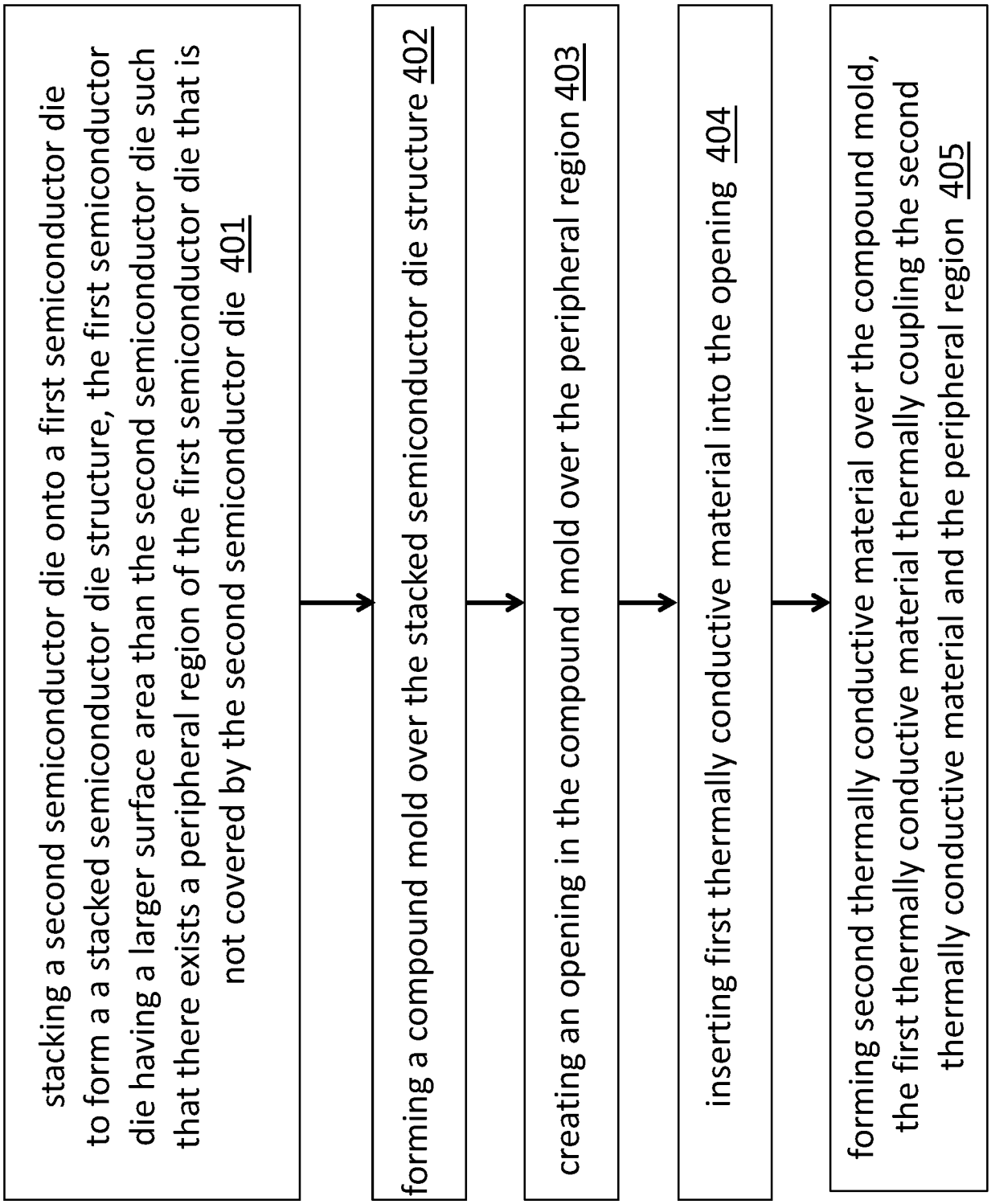

stacking a second semiconductor die onto a first semiconductor die to form a a stacked semiconductor die structure, the first semiconductor die having a larger surface area than the second semiconductor die such that there exists a peripheral region of the first semiconductor die that is not covered by the second semiconductor die 401
forming a compound mold over the stacked semiconductor die structure 402
creating an opening in the compound mold over the peripheral region 403
inserting first thermally conductive material into the opening 404
forming second thermally conductive material over the compound mold, the first thermally conductive material thermally coupling the second thermally conductive material and the peripheral region 405

Fig. 4

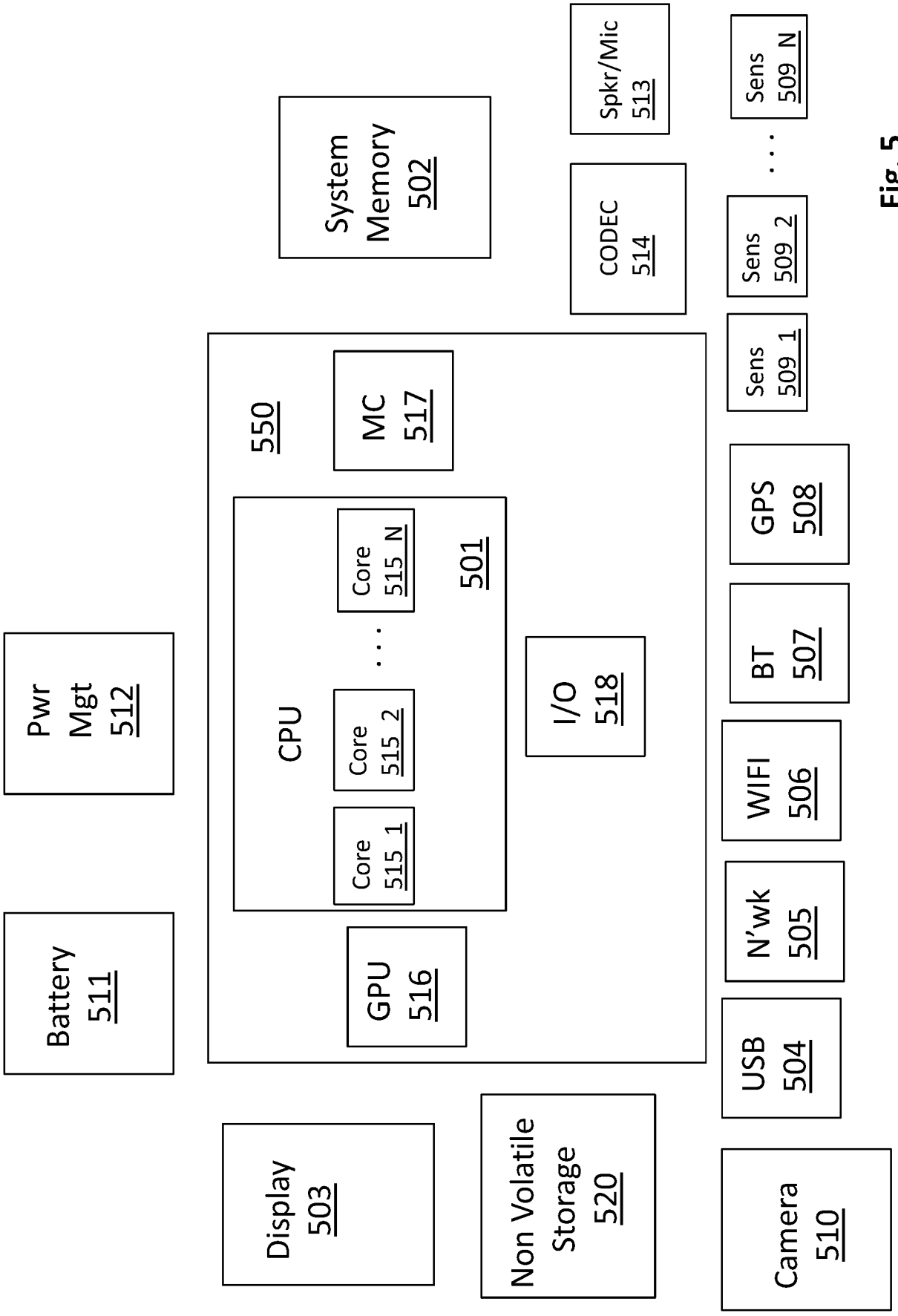

Pwr Mgt 512
Battery 511
Display 503
Non Volatile Storage 520
Camera 510
USB 504
N'wk 505
WIFI 506
BT 507
GPS 508
Sens 509_1
Sens 509_2
Sens 509_N
CODEC 514
Spkr/Mic 513
System Memory 502
550
MC 517
CPU
Core 515_1
Core 515_2
Core 515_N
501
GPU 516
I/O 518

Fig. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/063046

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/34(2006.01)i, H01L 23/12(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/34; H01L 21/56; H01L 21/50; H01L 23/36; H01L 23/48; H01L 23/29; H01L 25/10; H01L 23/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: die, thermal, heat, mold, package, via

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015-0069635 A1 (SAMSUNG ELECTRONICS CO., LTD.) 12 March 2015 See abstract, paragraphs [0042]-[0084] and figures 1-16.	1,3-9,11-15,17-20
Y		2,10,16
Y	US 2008-0061447 A1 (J. CHRISTOPHER MATAYABAS JR. et al.) 13 March 2008 See paragraphs [0012], [0013], and figures 2A-2B.	2,10,16
A	US 2009-0127700 A1 (MATTHEW ROMIG) 21 May 2009 See abstract, paragraphs [0015]-[0020] and figure 1.	1-20
A	US 2008-0277777 A1 (CHUN-MING LIAO et al.) 13 November 2008 See abstract, paragraphs [0028]-[0033] and figures 4A-4E.	1-20
A	US 2002-0140108 A1 (ERIC ARTHUR JOHNSON) 03 October 2002 See abstract, paragraphs [0028]-[0033] and figure 1. (** NOTE: Since claim number 1 is missing in this application, this International Search Report has been established on the assumption that the text above claim 2 on page 9 is regarded as claim 1.)	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 August 2016 (18.08.2016)	**18 August 2016 (18.08.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/063046

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2015-0069635 A1	12/03/2015	KR 10-2015-0030023 A	19/03/2015
		US 9177942 B2	03/11/2015
US 2008-0061447 A1	13/03/2008	US 2004-0262749 A1	30/12/2004
		US 2004-0266068 A1	30/12/2004
		US 7141454 B2	28/11/2006
		US 7332797 B2	19/02/2008
US 2009-0127700 A1	21/05/2009	None	
US 2008-0277777 A1	13/11/2008	TW 200845329 A	16/11/2008
		TW I338938 B	11/03/2011
		US 7608915 B2	27/10/2009
US 2002-0140108 A1	03/10/2002	US 6486554 B2	26/11/2002