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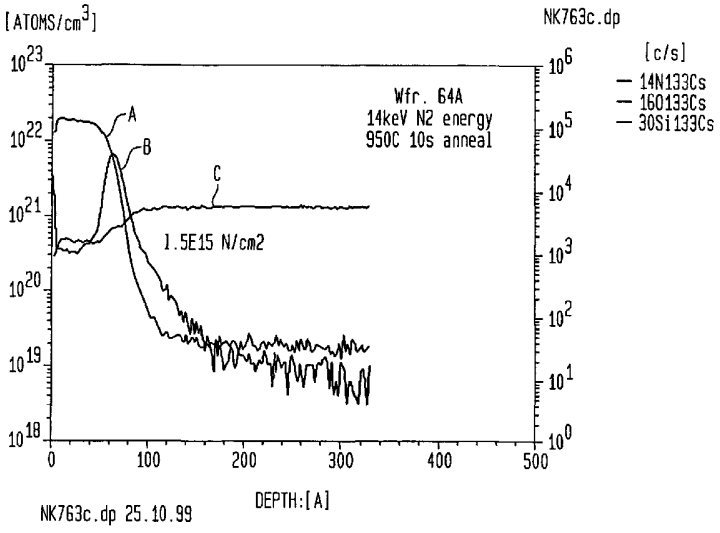
(54) Title: DUAL GATE OXIDE PROCESS FOR UNIFORM OXIDE THICKNESS



(57) Abstract: A process for forming dual gate oxides of improved oxide thickness uniformity for use in high performance DRAM systems or logic circuits, comprising:a) growing a sacrificial oxide layer on a substrate;b) implanting a dopant through the sacrificial oxide layer;c) implanting a first dosage of nitrogen ions in the absence of a photoresist to form a nitrided silicon layer; d) subjecting the substrate to a rapid thermal anneal for a sufficient time and at a sufficient temperature to allow nitrogen to diffuse to the silicon/oxide interface;e) masking the substrate with a photoresist to define the locations of the thin oxides of the dual gate oxide;f) implanting a second dosage of nitrogen ions through the photoresist;g) stripping the photoresist and the sacrificial oxide layers; and h) growing by oxidation gate oxide layers characterized by improved oxide thickness uniformity in the nitrogen ion implanted areas in the thin and thick oxides.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/8234

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 596 218 A (SOLEIMANI HAMID R ET AL) 21 January 1997 (1997-01-21) abstract; claims; figures column 3, line 27 -column 4, line 24	1-12
Y	US 5 330 920 A (SOLEIMANI HAMID R ET AL) 19 July 1994 (1994-07-19) abstract; claims; figures column 2, line 15 -column 3, line 20	1-12
A	US 6 048 769 A (CHAU ROBERT S) 11 April 2000 (2000-04-11) abstract; claims; figures 4A-4E column 5, line 38 -column 7, line 8	1-12

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2003	30/01/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Wirner, C

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	DOYLE B ET AL: "SIMULTANEOUS GROWTH OF DIFFERENT THICKNESS GATE OXIDES IN SILICON CMOS PROCESSING" IEEE ELECTRON DEVICE LETTERS, IEEE INC. NEW YORK, US, vol. 16, no. 7, 1 July 1995 (1995-07-01), pages 301-302, XP000514695 ISSN: 0741-3106 abstract page 301, right-hand column ---	1-12
A	GUPTA R ET AL: "Characterizing nitrogen implant effects on 0.17 mu m gate oxide thickness and charge-to-breakdown" 2000 INTERNATIONAL CONFERENCE ON ION IMPLANTATION TECHNOLOGY PROCEEDINGS. ION IMPLANTATION TECHNOLOGY - 2000 (CAT. NO.00EX432), 2000 INTERNATIONAL CONFERENCE ON ION IMPLANTATION TECHNOLOGY PROCEEDINGS. ION IMPLANTATION TECHNOLOGY - 2000, ALPBACH, AUS, pages 338-341, XP002227742 2000, Piscataway, NJ, USA, IEEE, USA ISBN: 0-7803-6462-7 abstract -----	1-12

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Information on patent family members

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