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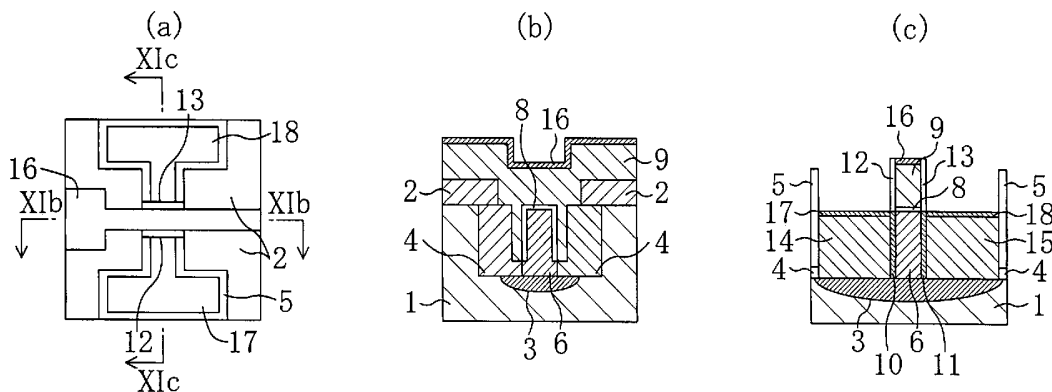
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(54) Title: FINFET-TYPE SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME



(57) Abstract: A semiconductor device includes: a semiconductor substrate in which a trench is formed; a source region and a drain region each of which is buried in the trench and contains an impurity of the same conductive type; a semiconductor FIN buried in the trench and provided between the source and drain regions; a gate insulating film provided on a side surface of the semiconductor FIN as well as the upper surface of the semiconductor FIN; and a gate electrode formed on the gate insulating film.

DESCRIPTION

FINFET-TYPE SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

5 TECHNICAL FIELD

The present invention relates to double-gate MOS field-effect transistors, and more particularly, the present invention relates to a FINFET having a gate electrode on a side or upper surface of a fin-shaped semiconductor layer.

10 BACKGROUND ART

In recent years, as one of means for improving the performance of semiconductor devices having a MOS structure, FINFETs, obtained by forming a convex semiconductor layer having a fin shape on a substrate and then forming a gate electrode on a side or upper surface of the semiconductor layer to form a channel region, have been proposed.

15 For example, a known FINFET is disclosed in J. Kedzierski et al., *IEDM Technical Digest* pp. 437-440 (2001) (which will be hereinafter referred to as Reference 1).

FIGS. **19(a)** and **19(b)** are perspective and cross-sectional views illustrating the known FINFET, respectively. As shown in FIGS. **19(a)** and **19(b)**, in the known FINFET, a thin silicon FIN **102** having a thickness of about 20 nm (in the x-axis direction) is formed
20 on a BOX (buried oxide film) **101**, i.e., an SOI substrate, so as to be elongate (in the y-axis direction), a gate electrode **103** made of polysilicon is formed so as to lay across the silicon FIN **102** with a gate oxide film **106** interposed between the silicon FIN **102** and the gate electrode **103**, and then a source pad **104** and a drain pad **105** are formed.

The FINFET has a double-gate structure in which a gate voltage can be applied
25 from both sides of the silicon FIN shown in FIG. **19(b)**. Accordingly, in the FINFET,

improvement of cutoff properties, suppression of the short channel effect and the like are achieved. Therefore, the FINFET is considered to be effective means for solving problems which arise when the gate length of a MOSFET is reduced.

Moreover, for example, in Reference 1, modified structures of the above-described
5 FINFET are proposed. For example, some structures in which by forming a FIN on a silicon substrate to allow application of a substrate bias, deterioration of the source-drain breakdown voltage due to influence of accumulated holes (in the case of an n-channel FET) which may possibly occur in a fully depleted transistor on an SOI substrate can be suppressed are disclosed in Reference 1.

10 The structures proposed therein include a structure which is characterized in that an insulating film having an opening portion is formed on a semiconductor substrate and a FIN and a gate electrode are formed in the opening portion and can be fabricated in a simple manner.

FIG. 20(a) is a plan view of an example of the known FINFET disclosed in
15 Reference 1 when the example is viewed from the top. FIG. 20(b) is a cross-sectional view taken along the line XXb-XXb shown in FIG. 20(a). FIG. 20(c) is a cross-sectional view taken along the line XXc-XXc shown in FIG. 20(a).

The known FINFET includes a p-type Si substrate **201** having an active region, source and drain regions **209** and **210** each of which is provided on the active region of the
20 p-type Si substrate **201** and made of a semiconductor containing an n-type impurity, and an LDD regions **208** which are provided so as to be in contact with the source and drain regions **209** and **210**, respectively, to face each other and to contain an n-type impurity at a lower concentration than that in the source and drain regions **209** and **210**, a convex Si FIN **203** provided on part of the active region of the p-type Si substrate **201** located between the
25 source and drain regions **209** and **210**, a gate oxide film **204** provided on side surfaces of

the Si FIN **203** as well as the upper surface of the Si FIN **203**, a first gate electrode **205** provided on the gate oxide film **204**, a second gate electrode **206** provided on the first gate electrode **205**, an insulating film **202** which surrounds the active region and is made of SiO₂, a gate side wall insulating film **207** provided on a side wall of the first gate electrode **205**, an interlevel insulating film **211** provided over the second gate electrode **206**, the source region **209** and the drain region **210**, and a contact plug **212** which passes through the interlevel insulating film **211** to reach the source region **209** or the drain region **210**.

As for methods for forming a FIN, a method in which a FIN is formed by removing the p-type Si substrate **201** by etching, a method in which a FIN is epitaxially grown in a region of the p-type Si substrate **201** corresponding to the opening portion of the insulating film **202**, and like method are disclosed.

Problems to be solved

However, a FINFET formed in any one of the above-described manners has a problem of poor surface evenness when the entire substrate is viewed.

FIG. **21** is a cross-sectional view illustrating a semiconductor device in which a known planar MOSFET and the known FINFET are mounted together. When the known FINFET and the known planar MOSFET are mounted together as shown in FIG. **21**, there may be cases where a gap between steps in a substrate is increased, thus resulting in an inconvenience in which process steps can not be uniformed. The left-hand side of FIG. **21** shows the FINFET shown in FIGS. **20(a)** through **20(c)** and the right-hand side of FIG. **21** shows a planar MOSFET including a source region **309**, a drain region **310**, an LDD region **308**, a first gate electrode **305**, a second gate electrode **306**, a source electrode **313**, a drain electrode **314**, a gate side wall insulating film **307** and a gate insulating film **315**.

As has been described, in order to fully utilize the performance of a FINFET in electronic equipment, it has been necessary to simplify integration of the FINFET and a

planar MOSFET.

It is therefore an object of the present invention to provide a FINFET which can be integrated with a planar MOSFET in a simple manner.

5 DISCLOSURE OF INVENTION

A first semiconductor device according to the present invention includes: a semiconductor substrate in which a trench is formed; a source region and a drain region each of which is buried in the trench and contains an impurity of the same conductive type; a semiconductor FIN buried in the trench and provided between the source region and the
10 drain region; a gate insulating film provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN; and a gate electrode provided on the gate insulating film.

In this structure, the semiconductor FIN, the source region and the drain region are provided in the trench. Thus, evenness of the upper surface of the substrate can be
15 improved, compared to that of a known semiconductor device. Accordingly, the inventive semiconductor device can be mounted with a planar MOSFET in a simple manner. Moreover, a protruding portion of the substrate is hardly damaged, resulting in an improved yield.

The semiconductor FIN is preferably made of one material selected from the group
20 consisting of Si, $\text{Si}_{1-x}\text{Ge}_x$ ($0 < x \leq 1$), and $\text{Si}_{1-y-z}\text{Ge}_y\text{C}_z$ ($0 < y < 1$, $0 < z < 1$, $0 < y + z < 1$). When Si is used, a highly reliable semiconductor device can be achieved at low costs. When SiGe or SiGeC is used, it is possible to increase mobility to a higher level than in the case where Si is used, so that the performance of the semiconductor device can be improved.

25 The gate electrode is provided on the gate insulating film so as to extend over the

semiconductor substrate, an isolation insulating film is further provided between part of the semiconductor substrate located in a side wall portion of the trench and part of the gate electrode located over the side wall of the semiconductor FIN; and an insulating film is further provided between part of the semiconductor substrate in which the trench is not
5 formed and the gate electrode.

With this structure, the gate insulating film, the isolation insulating film and the insulating film can be formed in different process steps, respectively. Thus, the thicknesses of the isolation insulating film and the insulating film can be appropriately changed so that the gate electrode and the semiconductor substrate can be reliably
10 insulated from each other.

The gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate, the gate insulating film is provided on the side and upper surfaces of the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and part of the gate insulating film located on the part of the
15 semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the gate electrode.

In this structure, the gate insulating film functions as an insulating film for insulating the gate electrode and the semiconductor substrate from each other. Therefore, each of the insulating films does not have to form in a separate process step, so that the
20 number of the process steps can be reduced.

The semiconductor FIN is preferably formed so as to have a convex shape when viewed from the bottom of the trench in view of suppressing the short channel effect.

A second semiconductor device according to the present invention includes: a first field-effect transistor including a semiconductor substrate in which a trench is formed, a
25 first source region and a first drain region each of which is buried in the trench and

contains an impurity of the same conductive type, a semiconductor FIN buried in the trench and provided between the first source region and the first drain region, a first gate insulating film provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN, and a first gate electrode formed on the first gate insulating film; and a second field-effect transistor including a second gate insulating film provided on the semiconductor substrate, a second gate electrode provided on the second gate insulating film, and second source and drain regions each of which contains an impurity and is provided in a region of the semiconductor substrate located on a side of and under the second gate electrode.

In this structure, the height of a substrate surface in part of the substrate in which the first gate electrode of the first field-effective transistor is provided and the height of a substrate surface in part of the substrate in which the second gate electrode of the second filed-effect transistor is provided can be made the same, and the heights of upper surfaces of the first source region and the first drain region and the heights of upper surfaces of the second source region and the second drain region can be made the same. This makes it possible to form members including these electrodes in the same process step.

The first gate electrode is provided on the first gate insulating film so as to extend over the semiconductor substrate, and the first field-effect transistor further includes an isolation insulating film formed between part of the semiconductor substrate located in a side wall portion of the trench and part of the first gate electrode provided over the side surface of the semiconductor FIN and an insulating film formed between the semiconductor substrate and the first gate electrode. Thus, by changing the thickness of the isolation insulating film according to a supply voltage and the like, the breakdown voltage can be ensured in a simple manner in the first filed-effect transistor.

The first gate electrode is provided on the first gate insulating film so as to extend

over the semiconductor substrate, the first gate insulating film is provided on the side and upper surfaces of the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the first gate electrode. Thus, the gate insulating film, the isolation insulating film and the insulating film can be formed as one unit. Therefore, the number of the fabrication process steps can be reduced.

A method for fabricating a semiconductor device according to the present invention is a method for fabricating a semiconductor device including a semiconductor substrate in which a trench is formed, a source region and a drain region each of which is buried in the trench and contains an impurity of the same conductive type, a semiconductor FIN buried in the trench and provided between the source and drain regions, a gate insulating film provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN, and a gate electrode formed on the gate insulating film, and includes steps of: (a) forming a semiconductor layer in the trench formed in the semiconductor substrate; (b) forming a gate insulating film on an upper surface of part of the semiconductor layer which is to be the semiconductor FIN as well as a side surface of the part of the semiconductor layer; (c) forming a gate electrode on the gate insulating film; and (d) introducing an impurity into the semiconductor layer, using the gate electrode as a mask, to form a source region and a drain region in regions of the semiconductor layer located on sides of and under the gate electrode, respectively, and then forming a semiconductor FIN in a region of the semiconductor layer interposed between the source region and the drain region and located directly under the gate electrode.

With this method, a semiconductor device which includes source and drain regions and a semiconductor FIN buried in a trench and of which substrate surface is more even

than that of a known device can be fabricated.

In the process step (c), the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate, and the method further includes the step (e) of forming an isolation insulating film in a side wall portion of the trench and the step (f) of forming an insulating film on the semiconductor substrate. Thus, the thickness of the gate voltage can be changed according to a gate voltage in the steps (e) and (f). Therefore, the breakdown voltage can be ensured in a simple manner.

The gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate, the gate insulating film formed in the step (b) is provided on side and upper surfaces of part of the semiconductor layer which is to be the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and in the step (c), the gate electrode is provided so that the gate insulating film is interposed between the part of the gate electrode and the semiconductor substrate. Thus, the number of the fabrication process steps can be reduced, resulting in reduction in fabrication costs.

15

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a perspective view of a FINFET according to a first embodiment of the present invention.

FIG. 2(a) is a plan view illustrating respective steps for fabricating the FINFET of the first embodiment; and FIGS. 2(b) and 2(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 3(a) is a plan view illustrating respective steps for fabricating the FINFET of the first embodiment; and FIGS. 3(b) and 3(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 4(a) is a plan view illustrating respective steps for fabricating the FINFET of

25

the first embodiment; and FIGS. 4(b) and 4(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 5(a) is a plan view illustrating respective steps for fabricating the FINFET of the first embodiment; and FIGS. 5(b) and 5(c) are cross-sectional views illustrating
5 respective steps for fabricating the FINFET.

FIG. 6(a) is a plan view illustrating respective steps for fabricating the FINFET of the first embodiment; and FIGS. 6(b) and 6(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 7(a) is a plan view illustrating respective steps for fabricating the FINFET of
10 the first embodiment; and FIGS. 7(b) and 7(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 8(a) is a plan view illustrating respective steps for fabricating the FINFET of the first embodiment; and FIGS. 8(b) and 8(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 9(a) is a plan view illustrating respective steps for fabricating the FINFET of
15 the first embodiment; and FIGS. 9(b) and 9(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 10(a) is a plan view illustrating respective steps for fabricating the FINFET of the first embodiment; and FIGS. 10(b) and 10(c) are cross-sectional views illustrating
20 respective steps for fabricating the FINFET.

FIG. 11(a) is a plan view illustrating respective steps for fabricating the FINFET of the first embodiment; and FIGS. 11(b) and 11(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 12 is a cross-sectional view illustrating a semiconductor device in which the
25 FINFET of the first embodiment of the present invention and a planar MOSFET are

integrated on the same substrate.

FIG. 13(a) is a plan view illustrating respective steps for fabricating the FINFET of a second embodiment of the present invention; and FIGS. 13(b) and 13(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

5 FIG. 14(a) is a plan view illustrating respective steps for fabricating the FINFET of the second embodiment; and FIGS. 14(b) and 14(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 15(a) is a plan view illustrating respective steps for fabricating the FINFET of the second embodiment; and FIGS. 15(b) and 15(c) are cross-sectional views illustrating
10 respective steps for fabricating the FINFET.

FIG. 16(a) is a plan view illustrating respective steps for fabricating the FINFET of the second embodiment; and FIGS. 16(b) and 16(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 17(a) is a plan view illustrating respective steps for fabricating the FINFET of
15 the second embodiment; and FIGS. 17(b) and 17(c) are cross-sectional views illustrating respective steps for fabricating the FINFET.

FIG. 18 is a perspective view illustrating the FINFET of the second embodiment of the present invention.

FIGS. 19(a) and 19(b) are perspective and cross-sectional views illustrating a
20 known FINFET, respectively.

FIG. 20(a) is a plan view of an example of the known FINFET when the FINFET is viewed from the top; FIG. 20(b) is a cross-sectional view taken along the line **XXb-XXb** shown in FIG. 20(a); and FIG. 20(c) is a cross-sectional view taken along the line **XXc-XXc** shown in FIG. 20(a).

25 FIG. 21 is a cross-sectional view illustrating a semiconductor device in which an

FINFET according to the known example and a planar MOSFET are integrated on the same substrate.

BEST MODE FOR CARRYING OUT THE INVENTION

5 - First Embodiment-

Hereinafter, a first embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. 1 is a perspective view of a FINFET according to the first embodiment. FIG. 11(a) is a plan view of the FINFET of the first embodiment. FIG. 11(b) is a cross-sectional view of the FINFET taken along the line **XIb-XIb** shown in FIG. 11(a). FIG. 11(c) is a cross-sectional view of the FINFET taken along the line **XIc-XIc** shown in FIG. 11(a).

As shown in FIGS. 11(a) through 11(c), the FINFET of this embodiment includes: a p-type well **1** which is provided in a semiconductor substrate made of Si or the like and in which a trench is formed; source and drain regions **14** and **15** each of which is buried in the trench of the p-type well **1** and contains an n-type impurity; a source-LDD region **10** which is provided so as to be in contact with the source region **14** and contains an n-type impurity at a lower concentration than that in the source region **14**; a drain-LDD region **11** which is provided so as to be in contact with the drain region **15** and contains an n-type impurity at a lower concentration than that in the drain region **15**; a convex semiconductor FIN **6** buried in the trench of the p-type well **1** and provided between the source region **14** and the drain region **15** (i.e., between the source-LDD region **10** and the drain-LDD region **11**); a gate insulating film **8** provided on side surfaces of the semiconductor FIN **6** as well as the upper surface of the semiconductor FIN **6** and made of SiO₂ or the like; a first gate electrode **9** provided on the gate insulating film **8** so as to extend over a portion of the p-

type well **1** in which the trench is not formed and made of, for example, polysilicon; a second gate electrode **16** provided on the first gate electrode **9** and made of, for example, titanium silicide; an isolation insulating film **4** which is provided in the trench of the p-type well **1** and surrounds the semiconductor FIN **6** and the first gate electrode **9**; a first
5 insulating film **5** provided on side surfaces of the source region **14** and the drain region **15** and made of SiO₂ or the like; a second insulating film **2** provided at least in a region of the substrate in which the trench is not formed and which is located between the p-type well **1** and the first gate electrode **9**; gate side wall insulating films **12** (source side) and **13** (drain side) provided on both sides of the first gate electrode **9**, respectively; a source electrode **17**
10 provided on the source region **14** and made of, for example, titanium silicide; and a drain electrode **18** provided on the drain region **15** and made of, for example, titanium silicide. Moreover, a heavily doped impurity region **3** to serve as a channel stopper layer containing a p-type impurity at a concentration of about $5 \times 10^{17} \text{ cm}^{-3}$ is provided in part of the p-type well **1** located at a bottom portion of the trench, i.e., part of the p-type well **1** located under
15 the source region **14**, the drain region **15** and the semiconductor FIN **6**.

The semiconductor FIN **6** may be made of, for example, silicon epitaxially grown, Si_{1-x}Ge_x ($0 < x \leq 1$), or Si_{1-y-z}Ge_yC_z ($0 < y < 0$, $0 < z < 1$, $0 < y + z < 1$).

Moreover, the concentration of the impurity contained in the p-type well **1** is, for example, about $5 \times 10^{15} \text{ cm}^{-3}$. The concentration of the impurity contained in the source
20 region **14** and the drain region **15** is, for example, about $4 \times 10^{20} \text{ cm}^{-3}$. Moreover, the concentration of the impurity contained in the semiconductor FIN **6** is, for example, about $5 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$.

In an exemplary design in which the semiconductor FIN **6** is made of Si, the semiconductor FIN **6** has a thickness of about 20 nm in the x direction (i.e., the gate width
25 direction) shown in FIG. 1 and a height of about 200 nm in the z direction (i.e., the height

direction) shown in FIG. 1. Moreover, the thickness of the gate insulating film 8 is about 2 nm, the thickness of part of the first gate electrode 9 located on a side of the semiconductor FIN 6 is about 75 nm, the thickness of the isolation insulating film 4 for isolating the part of the first gate electrode 9 located on a side of the semiconductor FIN 6 and the p-type well 1 from each other is 150 nm.

A feature of the FINFET of this embodiment is that the semiconductor FIN 6 is buried in the trench of the p-type well 1 together with the source region 14 and the drain region 15. Accordingly, surface unevenness of a substrate is smaller in the FINFET of this embodiment than that of the known FINFET shown in FIGS. 19(a) and 19(b) and FIG. 21. Therefore, as will be described later, the FINFET of this embodiment can be mounted together with a planar semiconductor device in a simple manner.

FIG. 12 is a cross-sectional view illustrating a semiconductor device in which the FINFET of this embodiment and a planar MOSFET are integrated on the same substrate. In FIG. 12, a FINFET shown in the left-hand side is the same FINFET shown in FIGS. 11(a) through 11(c) and each member also shown in FIGS. 11(a) through 11(c) is identified by the same reference numeral. In this case, a planar MOSFET shown in the right-hand side of FIG. 12 includes: a gate insulating film 78 provided on a p-type well (or a semiconductor substrate) 1; a first gate electrode 79 provided on the gate insulating film 78; a second gate electrode 86 provided on the first electrode 79; source and drain regions 84 and 85 each of which provided in a region of the p-type well 1 located on a side of and under the first gate electrode 79; a source electrode 87 provided on the source region 84; a drain electrode 88 provided on the drain region 85; a isolation insulating film 19 buried in the p-type well 1.

As can be seen from comparison between the FIGS. 12 and 21, in the semiconductor device of this embodiment, the height of the substrate surface in a region of

the substrate in which the FINFET is formed and the height of the substrate surface in a region of the substrate in which the planar MOSFET is formed can be made the same. More specifically, in this embodiment, the source region **14**, the drain region **15** and the semiconductor FIN **6** are buried in the p-type well **1**. Accordingly, the height of a substrate surface in regions of the substrate in which the source electrode **17** and drain electrode **18** of the FINFET are provided and the height of a substrate surface in regions of the substrate in which the source **17** and drain electrode **18** of the MOSFET are provided can be made the same. Thus, in the FINFET of this embodiment, the heights of regions of the substrate in which members such as the source electrode and the drain electrode can be made substantially the same. Accordingly, the process steps, such as the process step of forming a source/drain electrode and a gate electrode, used in fabricating a FINFET can be also used in fabricating a planar MOSFET. Therefore, a semiconductor device in which a FINFET and a planar MOSFET are integrated can be fabricated in a more simple manner than in the case of the known FINFET. Moreover, the known FINFET has many portions protruding from a substrate surface, and in many cases, a device is damaged in fabrication process steps. However, the FINFET of this embodiment has improved surface evenness, resulting in an improved yield. Furthermore, a more even substrate surface than that of known device can be obtained, so that the process step of forming an interconnect can be performed in a simple manner.

Next, an exemplary method for fabricating a FINFET according to the first embodiment will be described with reference to the accompanying drawings.

FIGS. **2** through **11** are cross-sectional views illustrating respective steps for fabricating the FINFET of this embodiment. In each of FIGS. **2** through **11**, **(a)** is a plan view of the FINFET viewed from the top; **(b)** is a cross-sectional view of the FINFET in the lateral direction (i.e., the x direction) shown in **(a)**; and **(c)** is a cross-sectional view of

the FINFET in the longitudinal direction (i.e., the y direction) shown in (a). Note that the x, y and z directions in this case are the same as those shown in FIG. 1.

First, in the process steps shown in FIGS. 2(a) through 2(c), a semiconductor substrate which is made of, for example, Si and in which a p-type well 1 is formed is prepared. Subsequently, a second insulating film 2, for example, which has a thickness of 300 nm and is made of SiO₂ is formed on the substrate and, using this as a mask, a region of the p-type well 1 in which a transistor is to be formed is removed by etching. Thus, a trench 100 is formed. In this case, the thickness of part of the trench (opening) 100 located in the p-type well 1 is about 200 nm. Next, for example, boron ions are implanted into the substrate and then annealing is performed thereto to form a p-type heavily doped impurity region 3 to serve as a channel stopper in part of the p-type well 1 located around a bottom portion of the trench 100.

Next, in the process steps shown in FIGS. 3(a) through 3(c), an inner wall portion of the trench 100 of the p-type well 1 is thermally oxidized, thereby forming an isolation insulating film 4. Furthermore, for example, SiO₂ or SiN is deposited over the substrate as well as a region of the substrate in which the trench 100 is formed. Thus, a first insulating film 5 is deposited so that the trench 100 is not completely filled.

In this case, in an exemplary design for part of the substrate in which a semiconductor FIN 6 is formed, the dimensions for part of the trench 100 in which a FIN is to be formed are as follows. The width in the x direction is 320 nm, the height in the z direction is 200 nm, the thickness of a side wall of the first insulating film 5 is 75 nm, and the thickness of a side wall of the isolation insulating film 4 is 150 nm. Moreover, the thickness of part of the first insulating film 5 located on the second insulating film 2 is about 100 nm. However, in the case of a size-reduced FINFET, the thickness of an isolation insulating film 4 is preferably 20 nm or more. With the thickness of 10 nm or

more, breakdown voltage properties can be ensured.

Next, in the process steps shown in FIGS. 4(a) through 4(c), the first insulating film 5 and the isolation insulating film 4 are removed, by etching or the like, with side wall portions of the first insulating film 5 and the isolation insulating film 4 left, so that the heavily doped impurity region 3 is exposed.

Subsequently, in the process steps shown in FIGS. 5(a) through 5(c), for example, Si is epitaxially grown on the heavily doped impurity region 3 which has been made exposed in the previous process steps, thereby forming a semiconductor layer 6a in the trench 100. The semiconductor layer 6a is formed so as to have an H shape when viewed from the top and has regions to serve as source/drain pads and a portion corresponding part of the H shape having a small width. A portion of the semiconductor layer 6a having a small width is to be a semiconductor FIN 6 in a later process step.

Next, in the process steps shown in FIGS. 6(a) through 6(c), using as a mask a resist 7 having an opening in a region in which a first gate electrode 9 is to be formed, the first insulating film 5 is removed, so that parts of side and upper surfaces of part of the semiconductor layer 6a which is to be a semiconductor 6 are exposed.

Subsequently, in the process steps shown in FIGS. 7(a) through 7(c), exposed parts of the semiconductor layer 6a are oxidized to form a gate insulating film 8 which extends on side surfaces of the part to be the semiconductor FIN 6 as well as the upper surface of the part to be the semiconductor FIN 6 and is made of an SiO₂ film. In this case, the thickness of the gate insulating film 8 is, for example, about 2 nm.

Next, in the process steps shown in FIGS. 8(a) through 8(c), using the resist 7 as a mask, for example, polysilicon is deposited so as to be located over the part of the semiconductor layer 6a to be the semiconductor FIN 6 with the gate insulating film 8 interposed between the resist 7 and the part of the semiconductor layer 6a. Thus, the first

gate electrode 9 is formed.

Subsequently, in the process steps shown in FIGS. 9(a) through 9(c), after the resist 7 has been removed, using the first gate electrode 9 as a mask, for example, phosphorus ions are implanted into the semiconductor layer 6a, thereby forming a source-LDD region 10 and a drain-LDD region 11 in parts of the substrate located on sides of and under the first gate electrode 9, respectively. In this case, each of the source-LDD region 10 and the drain-LDD region 11 are formed so as to partially overlap with an end portion of the first gate electrode 9 when viewed from the top. The concentration of phosphorus contained in the source-LDD region 10 and the drain-LDD region 11 is about $5 \times 10^{19} \text{ cm}^{-3}$.

Next, in the process steps shown in FIGS. 10(a) through 10(c), gate side wall insulating films 12 and 13 are formed on side surfaces of the first gate electrode 9, respectively. Thereafter, using the first gate electrode 9 and the gate side wall insulating films 12 and 13 as a mask, for example, phosphorus ions are implanted into the semiconductor layer 6a. Thus, a source region 14 and a drain region 15 are formed so that the first gate electrode 9 is interposed between the source region 14 and the drain region 15. The concentration of phosphorus contained in the source region 14 and the drain region 15 is about $4 \times 10^{20} \text{ cm}^{-3}$. Note that through these process steps and the process steps of forming LDD regions shown in FIGS. 9(a) through 9(c), part of the semiconductor layer 6a overlapping with the first gate electrode 9 (except for LDD regions) becomes a convex semiconductor 6.

Next, in the process steps shown in FIGS. 11(a) through 11(c), upper surface portions of the source region 14, the drain region 15 and the first gate electrode 9 are made into, for example, titanium silicide, to form a second gate electrode 16, a source electrode 17 and a drain electrode 18 on the first gate electrode 9, the source region 14 and the drain region 15, respectively. In this manner, the FINFET of FIG. 12 is formed.

According to the fabrication method of this embodiment, a FINFET which has an even substrate surface and in which the semiconductor FIN 6 is not protruding from the surface of the p-type well 1 (i.e., a silicon surface) can be formed. Accordingly, the FINFET can be integrated with a planar MOSFET in a simple manner. For example, a salicide process step shown in FIGS. 11(a) through 11(c), the process step of forming an interconnect, the process step of forming an interlevel insulating film and like step can be also used in a FINFET forming region and a planar MOSFET forming region.

Moreover, after the trench has been formed in the p-type well 1 and then the side wall has been formed, the semiconductor FIN 6 is epitaxially grown. Accordingly, the semiconductor FIN 6 having an even smaller width than an exposure limit can be formed in a simple manner. Moreover, in the FINFET of this embodiment, the semiconductor FIN 6 in an operation state is fully depleted, so that the short channel effect hardly occurs. Furthermore, the FINFET of this embodiment has advantageously a smaller substrate capacitance than that of a regular MOSFET.

Moreover, by forming a deep trench in the substrate, the semiconductor FIN 6 having a great height can be formed. Accordingly, a wide channel area can be obtained in a small area. Furthermore, even if the semiconductor FIN 6 is as tall as, for example, about 300-600 nm, each member is not damaged in fabrication process steps because the semiconductor FIN 6 is buried. Therefore, the FINFET can stably keep a constant shape. Furthermore, the p-type well 1 and the semiconductor FIN 6 are in contact with each other. Thus, a bias can be applied to the semiconductor FIN 6 via a stopper layer or a substrate, and also reduction in breakdown voltage due to accumulated holes which tends to occur in a fully depleted SOI device is not caused. Therefore, for the FINFET of this embodiment, an SOI substrate is preferably used as a Si substrate.

Note that in the FINFET of this embodiment, the gate insulating film 8, the

isolation insulating film 4 and the second insulating film 2 are formed in different process steps, respectively. Therefore, it is possible to arbitrarily set the thickness of each of the isolation insulating film 4 and the second insulating film 2 to ensure required breakdown voltage properties.

5 Moreover, in the FINFET of this embodiment, the thickness of the gate insulating film 8 is substantially uniform in parts of the gate insulating film 8 provided in the side and upper surfaces of the semiconductor FIN 6. However, even if the part of the gate insulating film 8 provided on the upper surface of the semiconductor FIN 6 is made to have a larger thickness than that of the part of the gate insulating film 8 provided on the side
10 surfaces of the semiconductor FIN 6, the FINFET of this embodiment can be operated as a double-gate FINFET.

Note that although only the structure of an n-channel FINFET has been described above, a p-channel FINFET can be formed in a similar manner.

15 (Second Embodiment)

Hereinafter, a FINFET according to a second embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. 17(a) is a plan view of the FINFET of this embodiment viewed from the top. FIG. 17(b) is a cross-sectional view of the FINFET of this embodiment taken along the
20 line XVIIb-XVIIb shown in FIG. 17(a). FIG. 17(c) is a cross-sectional view of the FINFET of this embodiment taken along the line XVIIc-XVIIc shown in FIG. 17(a). FIG. 18 is a perspective view illustrating the FINFET of this embodiment.

As shown in FIGS. 17(a) through 17(c), the FINFET of the second embodiment includes: a p-type well 51 which is provided in a semiconductor substrate made of Si or the
25 like and in which a trench is formed; source and drain regions 62 and 63 each of which is

provided in the trench of the p-type well **51** and contains an n-type impurity; a source-LDD region **58** which is provided so as to be in contact with the source region **62** and contains an n-type impurity at a lower concentration than that in the source region **62**; a drain-LDD region **59** which is provided so as to be in contact with the drain region **63** and contains an n-type impurity at a lower concentration than that in the drain region **63**; a convex semiconductor FIN **54** provided in part of the p-type well **51** located in the trench and between the source region **62** and the drain region **63** (i.e., between the source-LDD region **58** and the drain-LDD region **59**); a gate insulating film **55** provided at least on a side surface of the semiconductor FIN **54** as well as the upper surface of the semiconductor FIN **54** and made of SiO₂ or the like; a first gate electrode **57** provided on the gate insulating film **55** so as to extend over a portion of the p-type well **51** in which the trench is not formed and made of, for example, polysilicon; a second gate electrode **64** provided on the first gate electrode **57** and made of, for example, titanium silicide; a first insulating film **53** provided on side surfaces of the source region **62** and the drain region **63** and made of SiO₂ or the like; gate side wall insulating films **60** (source side) and **61** (drain side) provided on both sides of the first gate electrode **57**, respectively; a source electrode **65** provided on the source region **62** and made of, for example, titanium silicide; and a drain electrode **66** provided on the drain region **63** and made of, for example, titanium silicide. Then, in the FINFET of this embodiment, the gate insulating film **55** is located not only on the side and upper surfaces of the semiconductor FIN **54** but also bottom face and side walls of the trench and part of the p-type well **51** located outside of the trench. In other words, the gate insulating film **55** has a portion interposed between the first gate electrode **57** and the semiconductor FIN **54** and a portion interposed between the first gate electrode **57** and the p-type well **51**. Note that the thickness of the gate insulating film **55** is about 2 nm.

Moreover, a heavily doped impurity region **52** to serve as a channel stopper layer

containing a p-type impurity at a concentration of about $5 \times 10^{17} \text{ cm}^{-3}$ is provided in part of the p-type well **51** located at a bottom portion of the trench, i.e., part of the p-type well **51** located under the source region **62**, the drain region **63** and the semiconductor FIN **54**.

The FINFET of this embodiment is different from the FINFET of the first embodiment in that the gate insulating film, the second insulating film and the isolation insulating film are provided as one unit. Specifically, in the FINFET of this embodiment, the gate insulating film **55** extends to reach the outside of the trench and also takes a role corresponding to those of the second insulating film **2** (see FIG. **11**) and isolation insulating film **4** of the first embodiment.

With this structure, an insulating film for insulating the first gate electrode **57** and the p-type well **51** from each other can be formed simultaneously with the gate insulating film **55**. Accordingly, the number of fabrication process steps can be reduced, so that fabrication costs can be reduced. Moreover, the evenness of gate electrode portions is better than that of the FINFET of the first embodiment.

Next, an exemplary method for fabricating the FINFET of the second embodiment will be described with reference to the accompanying drawings.

FIGS. **13** through **17** are cross-sectional views illustrating respective steps for fabricating the FINFET of this embodiment. In each of FIGS. **13** through **17**, (a) is a plan view of the FINFET viewed from the top; (b) is a cross-sectional view of the FINFET in the lateral direction (i.e., the x direction) shown in (a); and (c) is a cross-sectional view of the FINFET in the longitudinal direction (i.e., the y direction) shown in (a). Note that the x, y and z directions in this case are the same as those shown in FIG. **1**.

First, in the process steps shown in FIGS. **13(a)** through **13(c)**, an insulating film **49** made of, for example, SiO_2 is formed in the p-type well **51** formed on the semiconductor substrate and then, for example, using a resist **50** as a mask, the insulating film **49** and part

of the p-type well **51** desired to be removed are removed to form a desired trench (which is almost the same as that of FIG. 2 and therefore not shown). This trench has the same dimensions and shape as those in the first embodiment. Thereafter, boron ions are implanted into the p-type well **51** and then annealing is performed thereto to form a p-type heavily doped impurity region **52** to serve as a channel stopper (punch-through stopper) in part of the p-type well **51** located around a bottom portion of the trench.

Next, a first insulating film **53** made of, for example, a SiO₂ film is formed on side surfaces of the trench. Thereafter, for example, Si is epitaxially grown on the heavily doped impurity region **52** of the p-type well **51**, thereby forming a semiconductor layer **54a** in the trench. The semiconductor layer **54a** is formed so as to have an H shape when viewed from the top and has regions to serve as source/drain pads and a portion corresponding part of the H shape having a small width. The portion of the semiconductor layer **54a** having the small width is to be a semiconductor FIN **54** in a later process step.

Next, in the process steps shown in FIGS. **14(a)** through **14(c)**, for example, using as a mask a resist **56** having an opening in a region in which a first gate electrode **57** is to be formed, parts of the first insulating film **53** and the insulating film **49** provided in part of the semiconductor layer to be the semiconductor FIN **54** are removed, so that part of the semiconductor layer **54a** which is to be the semiconductor FIN **54** is exposed. Subsequently, exposed part of the semiconductor layer **54a** which is later to be the semiconductor FIN **54** and exposed part of the p-type well **51** are oxidized to form a gate insulating film **55**. The gate insulating film **55** formed in this embodiment is provided so as to be located not only on side and upper surfaces of the part to be the semiconductor FIN but also on a bottom portion and side walls of the trench and part of the p-type well **51** located outside of the trench.

Next, in the process steps shown in FIGS. **15(a)** through **15(c)**, using the resist **56**

as a mask, polysilicon is deposited so as to fill an empty space and also to be located over the part of the semiconductor layer **54a** which is to be the semiconductor FIN **54** with the gate insulating film **55** interposed between the resist and the part of the semiconductor layer **54a**. Thus, a first gate electrode **57** is formed. Subsequently, after the resist **56** has
5 been removed, using the first gate electrode **57** as a mask, for example, phosphorus ions are implanted into the semiconductor layer **54a** to form a source-LDD region **58** and a drain-LDD region **59** in regions of the semiconductor layer **54a** located on both sides of and under the first gate electrode **57**, respectively.

Next, in the process steps shown in FIGS. **16(a)** through **16(c)**, after gate side wall
10 insulating films **60** and **61** have been formed by a known method, using as a mask the first gate electrode **57** and the gate side wall insulating films **60** and **61**, for example, phosphorus ions are implanted to form a source region **62** and a drain region **63** in parts of the semiconductor layer **54a** located on both sides of and under the first gate electrode **57**, respectively. Note that through these process steps and the process steps of forming LDD regions shown in FIGS. **15(a)** through **15(c)**, part of the semiconductor layer **54a** (except
15 for LDD regions) overlapping with the first gate electrode **57** when viewed from the top becomes a convex semiconductor FIN **54**.

Next, in the process steps shown in FIGS. **17(a)** through **17(c)**, upper surface portions of the first gate electrode **57**, the source region **62** and the drain region **63** are
20 made into, for example, titanium silicide to form a second gate electrode **64**, a source electrode **65** and a drain electrode **63** on the first gate electrode **57**, the source region **62** and the drain region **63**, respectively. In this manner, the FINFET of this embodiment of FIG. **18** is formed.

According to this embodiment, the height of a substrate surface in regions of the
25 substrate of the FINFET in which the source electrode **65** and the drain electrode **66** are

formed and the height of a substrate surface in regions of the substrate of a planar MOSFET in which a source electrode and a drain electrode are formed can be also made substantially the same.

According to the FINFET of this embodiment, the gate insulating film **55** formed in
5 the process steps shown in FIGS. **14(a)** through **14(c)** also has the function as an isolation insulating film between the first gate electrode **57** and the p-type well **51**. Accordingly, in the method for fabricating a FINFET according to this embodiment, the process step of forming an isolation insulating film is not needed, so that a semiconductor device can be formed in a more simple manner than in the method for fabricating a semiconductor device
10 according to the first embodiment. Moreover, in the FINFET of this embodiment, the thickness of the gate insulating film **55** is substantially uniform in a thickness of 2 nm. The first gate electrode **57** has also excellent evenness.

Note that the gate insulating film **55** functions as an isolation insulating film between the first gate electrode **57** and the p-type well **51**, so that the breakdown voltage of
15 the FINFET of this embodiment is limited. However, even if the thickness of the gate insulating film functioning as an isolation insulating film is about 2 nm, the first gate electrode **57** and the p-type well **51** can be electrically isolated because as the size of the semiconductor integrated circuits is reduced, the supply voltage is reduced. Therefore, the FINFET of this embodiment is preferably used in a circuit for low voltage application.

20 Note that in the semiconductor device of each of the first and second embodiment, as a material for the semiconductor FIN, besides epitaxially grown silicon, silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$ ($0 < x \leq 1$)), silicon germanium carbon ($\text{Si}_{1-y-z}\text{Ge}_y\text{C}_z$ ($0 < y < 1$, $0 < z < 1$, $0 < y + z < 1$)) or the like may be used.

Moreover, in this embodiment, the FIN is a silicon semiconductor and a side wall
25 for forming the FIN is an insulating film (the first insulating film **53**). However, a FIN and

a side wall may be formed of a silicon germanium semiconductor and a silicon semiconductor in this combination with which selective etching can be performed.

Moreover, the gate insulating film **55** is not limited to the SiO₂ film but may be formed of a SiN film or a high-k material. A material for the first gate electrode **57** is not
5 limited to polysilicon, as long as the material is a conductive material. Specifically, a metal material such as W (tungsten) may be used.

INDUSTRIAL APPLICABILITY

A semiconductor device according to the present invention is used for electronic
10 equipment required to have a reduced-size and improved-performance, and more particularly, the semiconductor device is used for electronic equipment in which a semiconductor device such as a planar MOSFET and a FINFET are mounted together.

CLAIMS

1. A semiconductor device comprising:
- a semiconductor substrate in which a trench is formed;
- a source region and a drain region, each of which is buried in the trench and
- 5 contains an impurity of the same conductive type;
- a semiconductor FIN buried in the trench and provided between the source region and the drain region;
- a gate insulating film provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN; and
- 10 a gate electrode provided on the gate insulating film.
2. The semiconductor device of claim 1, wherein the semiconductor FIN is made of one material selected from the group consisting of Si, $\text{Si}_{1-x}\text{Ge}_x$ ($0 < x \leq 1$), and $\text{Si}_{1-y-z}\text{Ge}_y\text{C}_z$ ($0 < y < 1$, $0 < z < 1$, $0 < y + z < 1$).
- 15
3. The semiconductor device of claim 1, wherein the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate,
- wherein an isolation insulating film is further provided between part of the semiconductor substrate located in a side wall portion of the trench and part of the gate
- 20 electrode located over the side wall of the semiconductor FIN; and
- wherein an insulating film is further provided between part of the semiconductor substrate in which the trench is not formed and the gate electrode.
4. The semiconductor device of claim 1, wherein the gate electrode is provided on
- 25 the gate insulating film so as to extend over the semiconductor substrate,

wherein the gate insulating film is provided on the side and upper surfaces of the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and

wherein part of the gate insulating film located on the part of the semiconductor
5 substrate in which the trench is not formed is interposed between the semiconductor substrate and the gate electrode.

5. The semiconductor device of any one of claims 1 through 4, wherein the semiconductor FIN is formed so as to have a convex shape when viewed from the bottom
10 of the trench.

6. A semiconductor device comprising:

a first field-effect transistor including a semiconductor substrate in which a trench is formed, a first source region and a first drain region each of which is buried in the trench
15 and contains an impurity of the same conductive type, a semiconductor FIN buried in the trench and provided between the first source region and the first drain region, a first gate insulating film provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN, and a first gate electrode formed on the first gate insulating film; and

20 a second field-effect transistor including a second gate insulating film provided on the semiconductor substrate, a second gate electrode provided on the second gate insulating film, and second source and drain regions each of which contains an impurity and is provided in a region of the semiconductor substrate located on a side of and under the second gate electrode.

7. The semiconductor device of claim 6, wherein the first gate electrode is provided on the first gate insulating film so as to extend over the semiconductor substrate, and

wherein the first field-effect transistor further includes an isolation insulating film
5 formed between part of the semiconductor substrate located in a side wall portion of the trench and part of the first gate electrode provided over the side surface of the semiconductor FIN and a second insulating film formed between the semiconductor substrate and the first gate electrode.

10 8. The semiconductor device of claim 6, wherein the first gate electrode is provided on the first gate insulating film so as to extend over the semiconductor substrate,

wherein the first gate insulating film is provided on the side and upper surfaces of the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and

15 wherein part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the first gate electrode.

9. A method for fabricating a semiconductor device, the device including a
20 semiconductor substrate in which a trench is formed, a source region and a drain region each of which is buried in the trench and contains an impurity of the same conductive type, a semiconductor FIN buried in the trench and provided between the source and drain regions, a gate insulating film provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN, and a gate electrode formed on the gate
25 insulating film, the method comprising steps of:

(a) forming a semiconductor layer in the trench formed in the semiconductor substrate;

(b) forming a gate insulating film on an upper surface of part of the semiconductor layer which is to be the semiconductor FIN as well as a side surface of the part of the
5 semiconductor layer;

(c) forming a gate electrode on the gate insulating film; and

(d) introducing an impurity into the semiconductor layer, using the gate electrode as a mask, to form a source region and a drain region in regions of the semiconductor layer located on sides of and under the gate electrode, respectively, and then forming a
10 semiconductor FIN in a region of the semiconductor layer interposed between the source region and the drain region and located directly under the gate electrode.

10. The method for fabricating a semiconductor device of claim 9, wherein in the process step (c), the gate electrode is provided on the gate insulating film so as to extend
15 over the semiconductor substrate, and

wherein the method further includes the step (e) of forming an isolation insulating film in a side wall portion of the trench and the step (f) of forming an insulating film on the semiconductor substrate.

20 11. The method for fabricating a semiconductor device of claim 9, wherein the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate,

wherein the gate insulating film formed in the step (b) is provided on side and upper surfaces of part of the semiconductor layer which is to be the semiconductor FIN as
25 well as part of the semiconductor substrate in which the trench is not formed, and

wherein in the step (c), the gate electrode is provided so that the gate insulating film is interposed between the part of the gate electrode and the semiconductor substrate.

AMENDED CLAIMS

[received by the International Bureau on 06th August, 2004 (06.08.04)
original claims 1, 6, 9, 10 and 11 amended; other claims remaining unchanged (5 pages)]

1. (Amended) A semiconductor device comprising:

a semiconductor substrate in which a trench is formed;

a source region and a drain region, each of which is buried in the trench and
5 contains an impurity of the same conductive type;

a semiconductor FIN buried in the trench and provided between the source region
and the drain region;

a gate insulating film provided on a side surface of the semiconductor FIN as well
as an upper surface of the semiconductor FIN; and

10 a gate electrode having two end portions each of which protrudes downward in the
trench so as to extend along the gate insulating film on the semiconductor FIN and formed
on the gate insulating film.

2. The semiconductor device of claim 1, wherein the semiconductor FIN is made
15 of one material selected from the group consisting of Si, $\text{Si}_{1-x}\text{Ge}_x$ ($0 < x \leq 1$), and $\text{Si}_{1-y-z}\text{Ge}_y\text{C}_z$ ($0 < y < 1$, $0 < z < 1$, $0 < y + z < 1$).

3. The semiconductor device of claim 1, wherein the gate electrode is provided on
the gate insulating film so as to extend over the semiconductor substrate,

20 wherein an isolation insulating film is further provided between part of the
semiconductor substrate located in a side wall portion of the trench and part of the gate
electrode located over the side wall of the semiconductor FIN; and

wherein an insulating film is further provided between part of the semiconductor
substrate in which the trench is not formed and the gate electrode.

25

4. The semiconductor device of claim 1, wherein the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate,

wherein the gate insulating film is provided on the side and upper surfaces of the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and

wherein part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the gate electrode.

5. The semiconductor device of any one of claims 1 through 4, wherein the semiconductor FIN is formed so as to have a convex shape when viewed from the bottom of the trench.

6. (Amended) A semiconductor device comprising:

a first field-effect transistor including a semiconductor substrate in which a trench is formed, a first source region and a first drain region each of which is buried in the trench and contains an impurity of the same conductive type, a semiconductor FIN buried in the trench and provided between the first source region and the first drain region, a first gate insulating film provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN, and a first gate electrode having two end portions each of which protrudes downward in the trench so as to extend along the gate insulating film on the semiconductor FIN and formed on the gate insulating film; and

a second field-effect transistor including a second gate insulating film provided on the semiconductor substrate, a second gate electrode provided on the second gate insulating film, and second source and drain regions each of which contains an impurity

and is provided in a region of the semiconductor substrate located on a side of and under the second gate electrode.

7. The semiconductor device of claim 6, wherein the first gate electrode is
5 provided on the first gate insulating film so as to extend over the semiconductor substrate, and

wherein the first field-effect transistor further includes an isolation insulating film formed between part of the semiconductor substrate located in a side wall portion of the trench and part of the first gate electrode provided over the side surface of the
10 semiconductor FIN and a second insulating film formed between the semiconductor substrate and the first gate electrode.

8. The semiconductor device of claim 6, wherein the first gate electrode is provided on the first gate insulating film so as to extend over the semiconductor substrate,
15 wherein the first gate insulating film is provided on the side and upper surfaces of the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and

wherein part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor
20 substrate and the first gate electrode.

9. (Amended) A method for fabricating a semiconductor device, the device including a semiconductor substrate in which a trench is formed, a source region and a drain region each of which is buried in the trench and contains an impurity of the same
25 conductive type, a semiconductor FIN buried in the trench and provided between the

source and drain regions, a gate insulating film provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN, and a gate electrode formed on the gate insulating film, the method comprising steps of:

- (a) forming the trench in the semiconductor substrate;
- 5 (b) forming an insulating film on a side wall of the trench;
- (c) forming a semiconductor layer including the semiconductor FIN in the trench using the insulating film as a mask;
- (d) removing the insulating film;
- (e) forming a gate insulating film on an upper surface of part of the semiconductor
- 10 layer which is to be the semiconductor FIN as well as a side surface of the part of the semiconductor layer;
- (f) forming a gate electrode on the gate insulating film; and
- (g) introducing an impurity into the semiconductor layer, using the gate electrode as a mask, to form a source region and a drain region in regions of the semiconductor layer
- 15 located on sides of and under the gate electrode, respectively, and then forming a semiconductor FIN in a region of the semiconductor layer interposed between the source region and the drain region and located directly under the gate electrode.

10. (Amended) The method for fabricating a semiconductor device of claim 9, wherein in the process step (f), the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate, and

wherein the method further includes the step (h) of forming an isolation insulating film in a side wall portion of the trench and the step (i) of forming an insulating film on the semiconductor substrate.

11. (Amended) The method for fabricating a semiconductor device of claim 9, wherein the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate,

wherein the gate insulating film formed in the step (e) is provided on side and
5 upper surfaces of part of the semiconductor layer which is to be the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and

wherein in the step (f), the gate electrode is provided so that the gate insulating film is interposed between the part of the gate electrode and the semiconductor substrate.

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FIG. 1

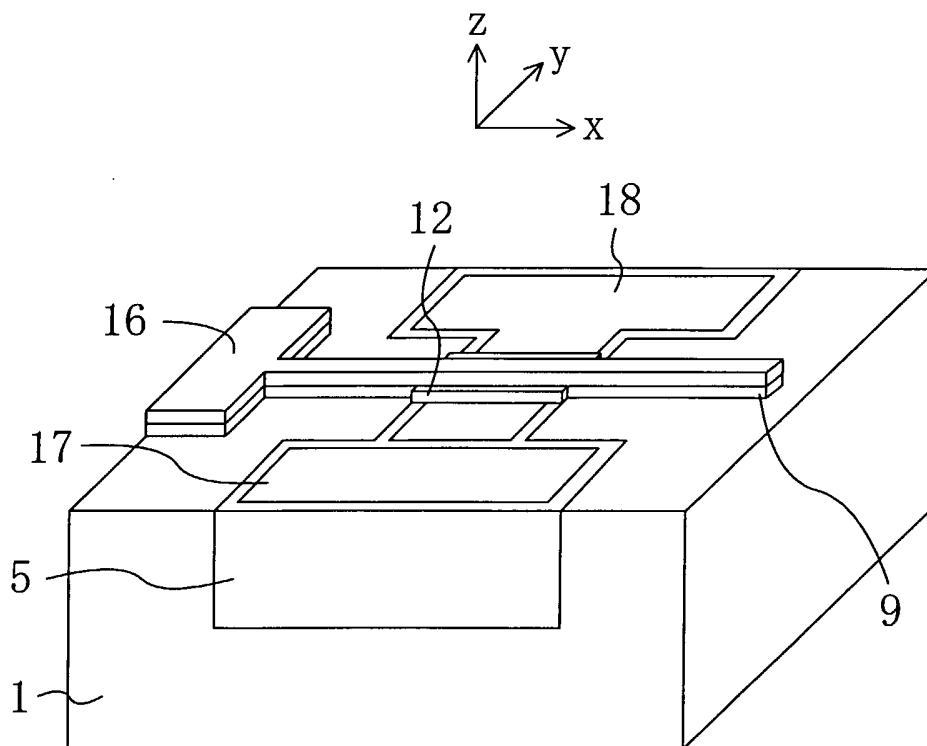


FIG. 2

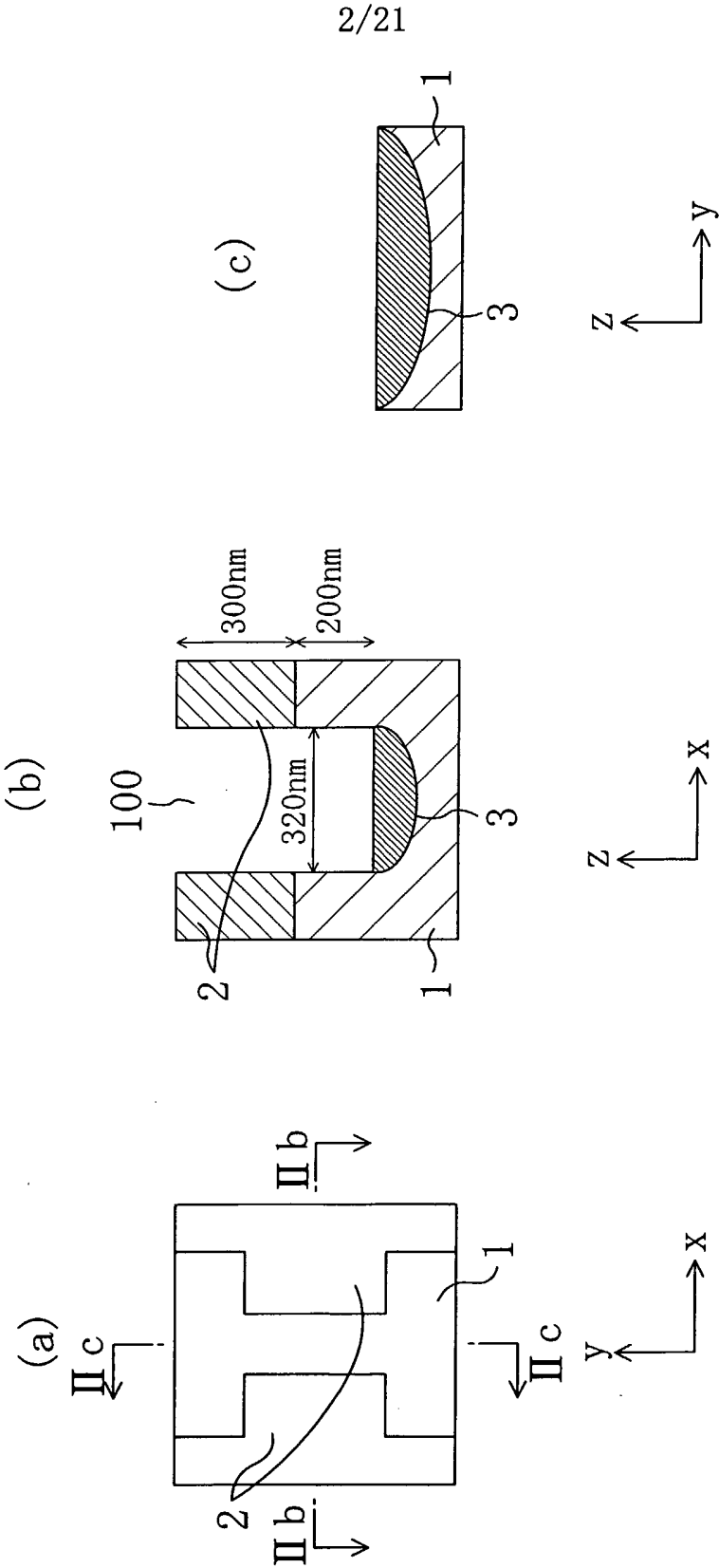


FIG. 3

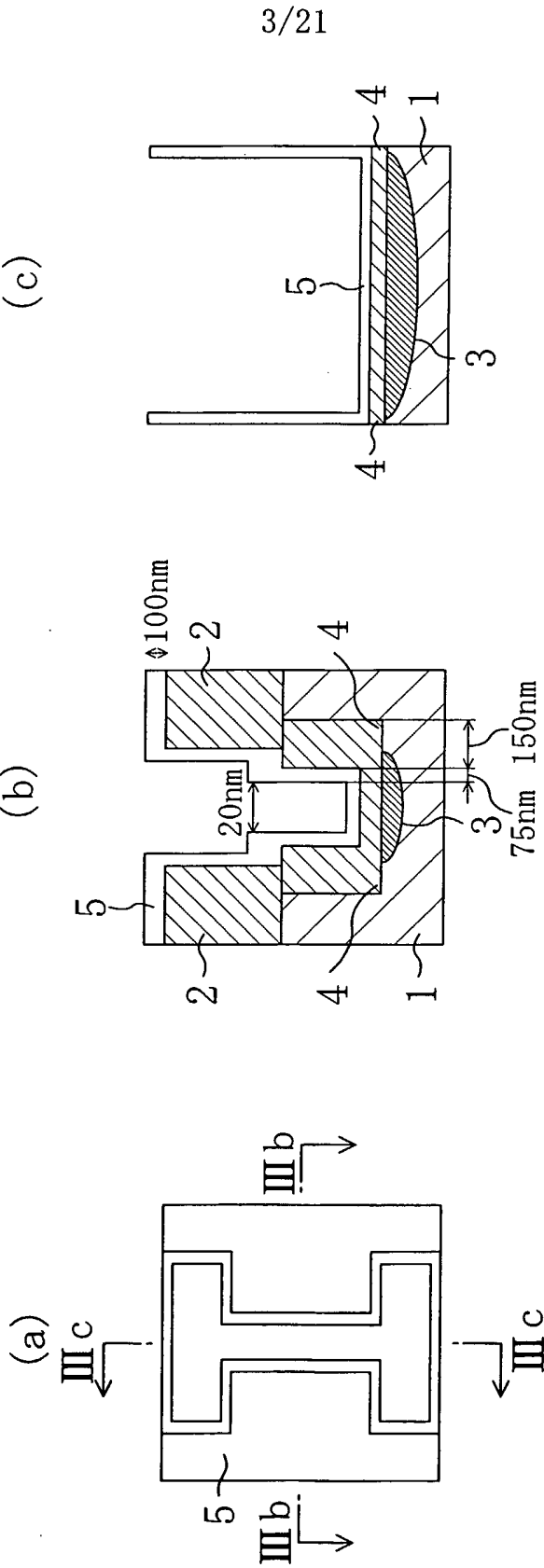


FIG. 4

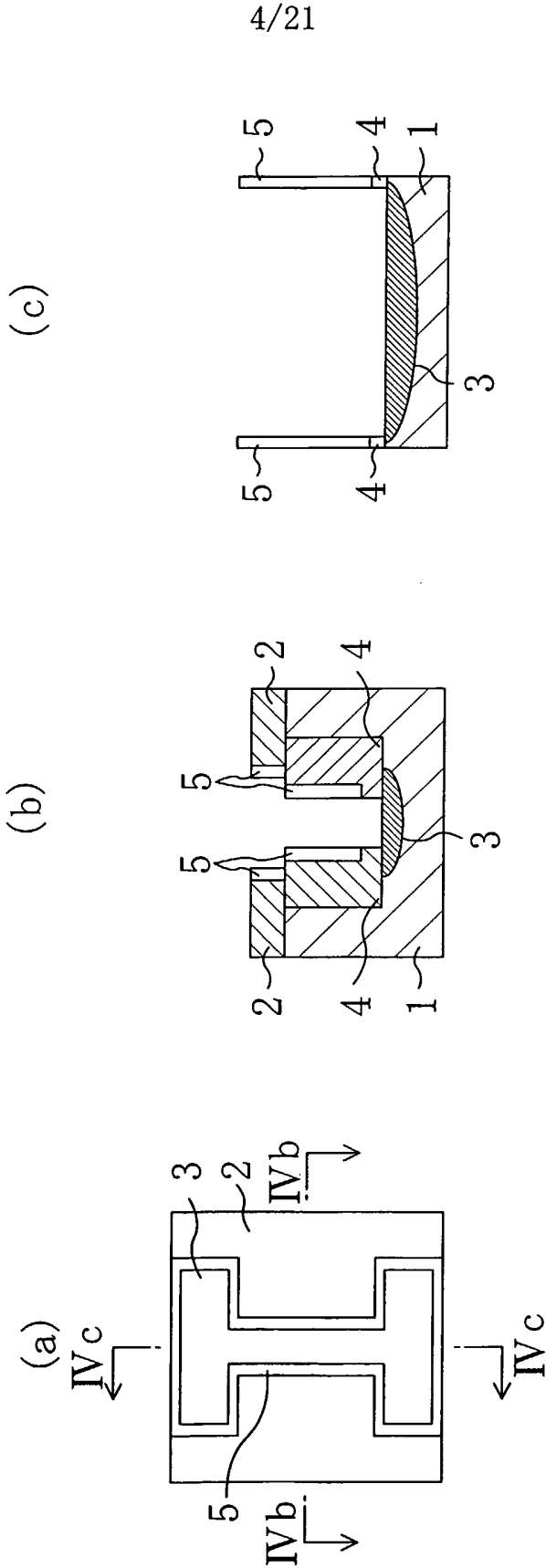


FIG. 5

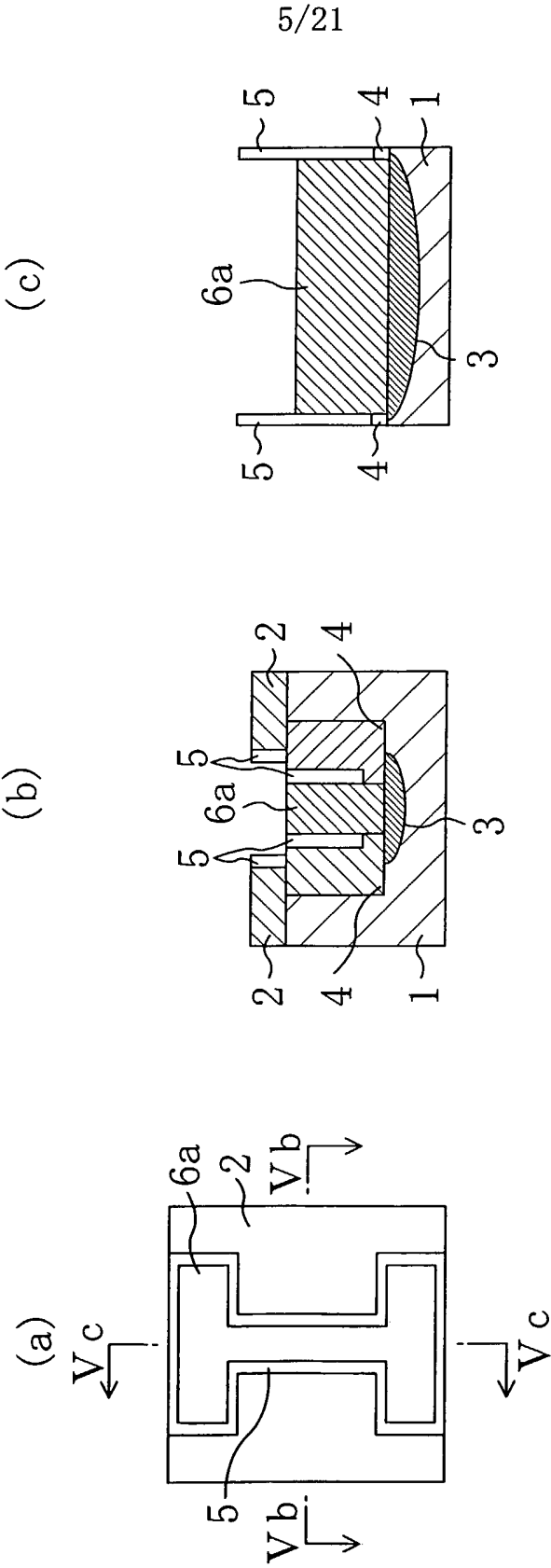


FIG. 6

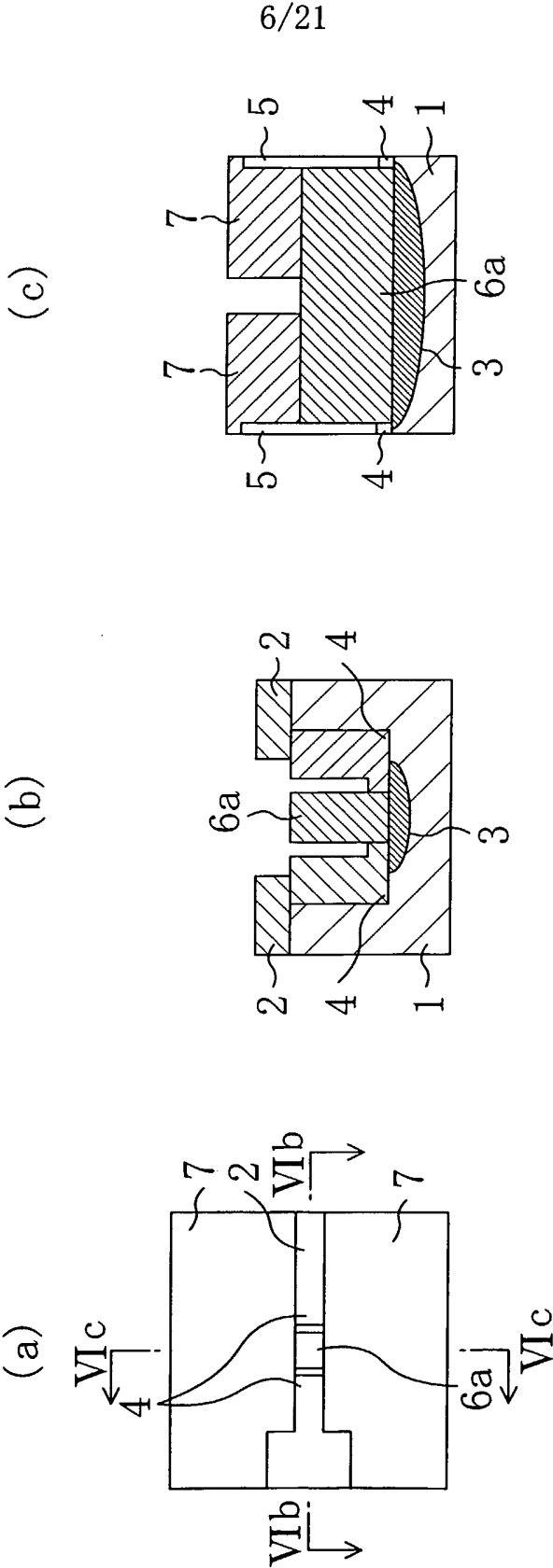


FIG. 7

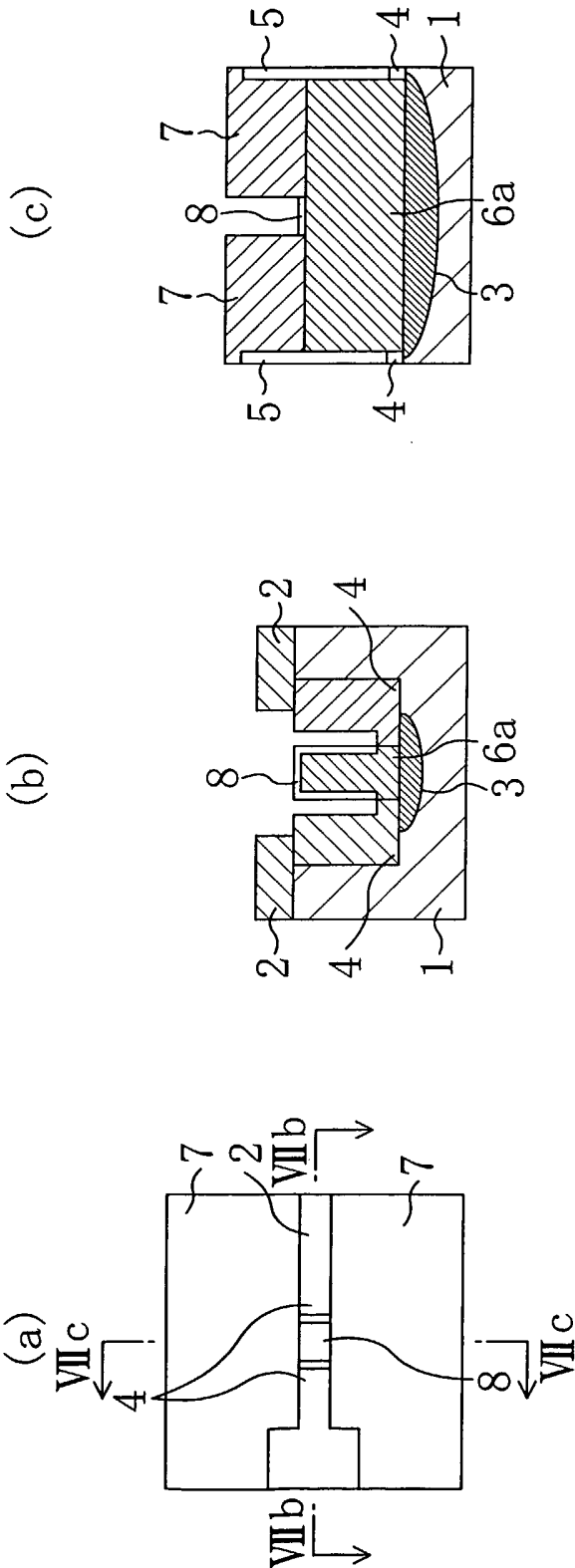


FIG. 8

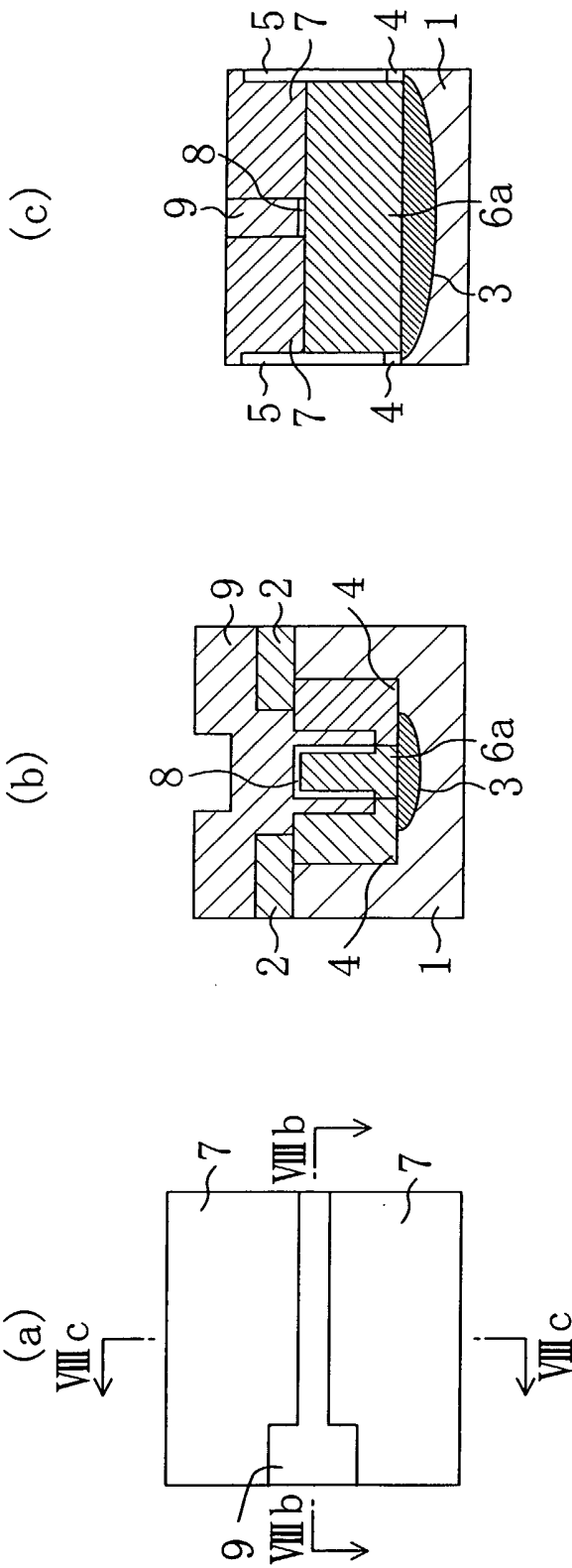


FIG. 9

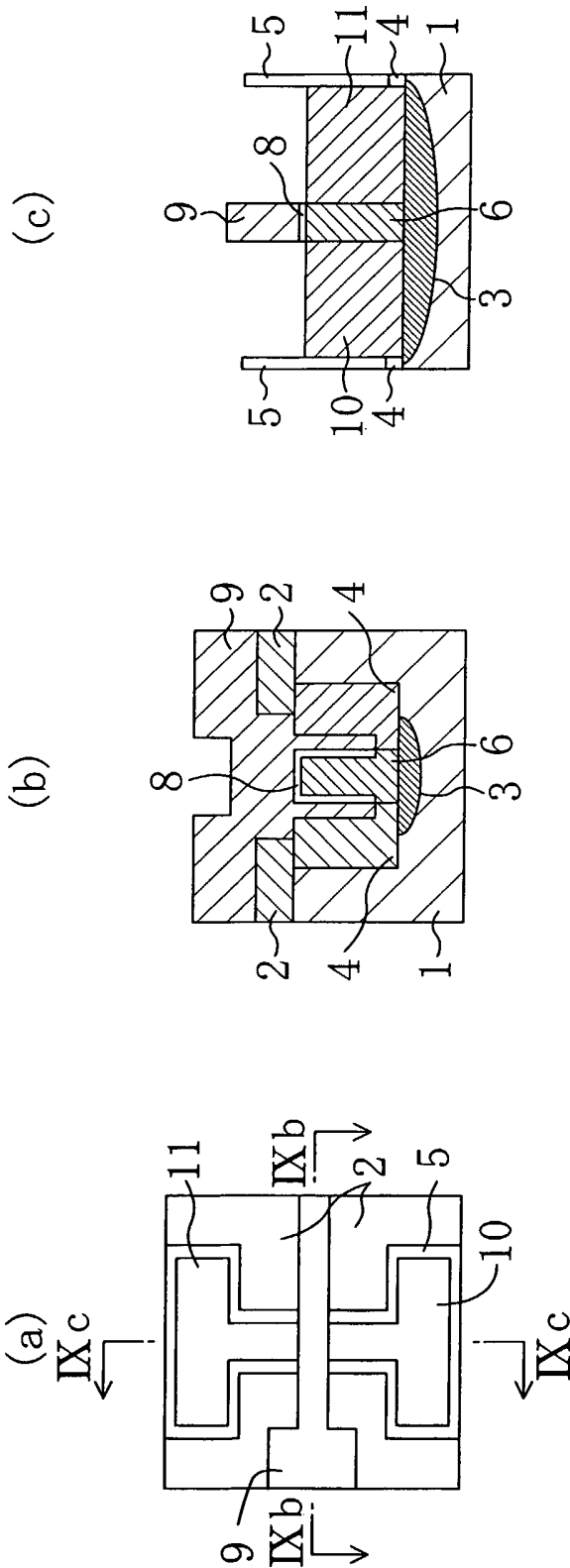


FIG. 10

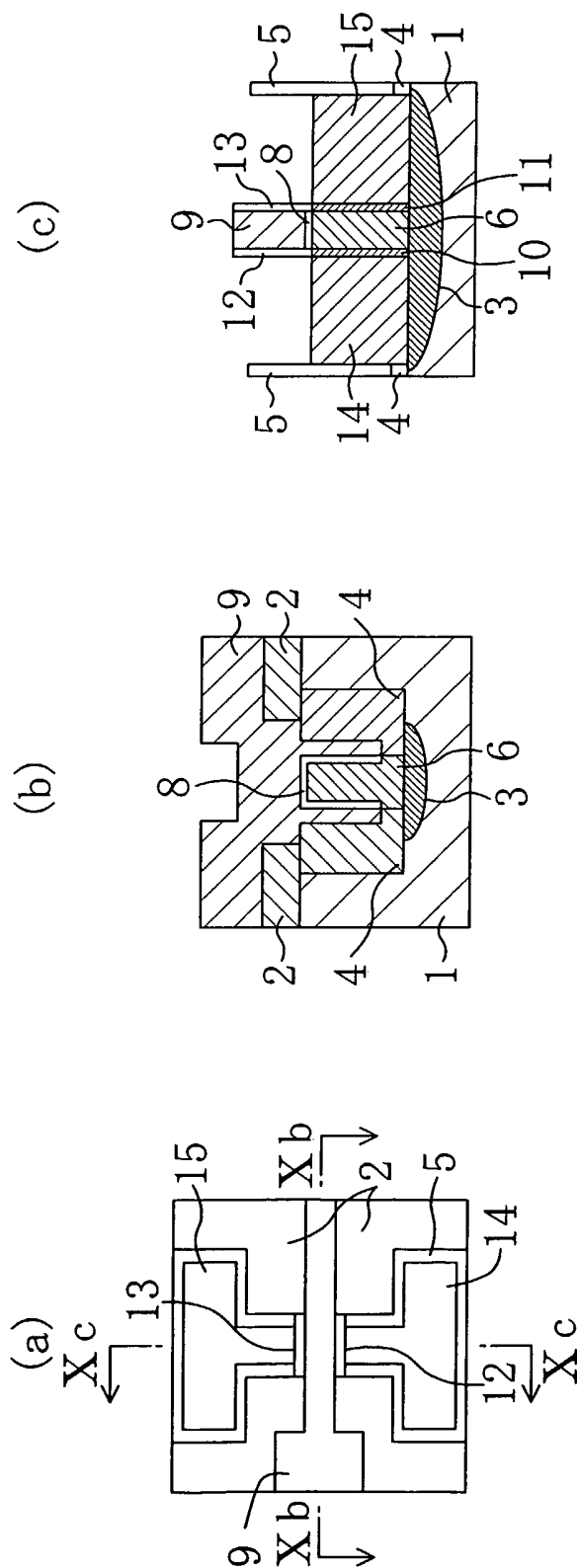


FIG. 11

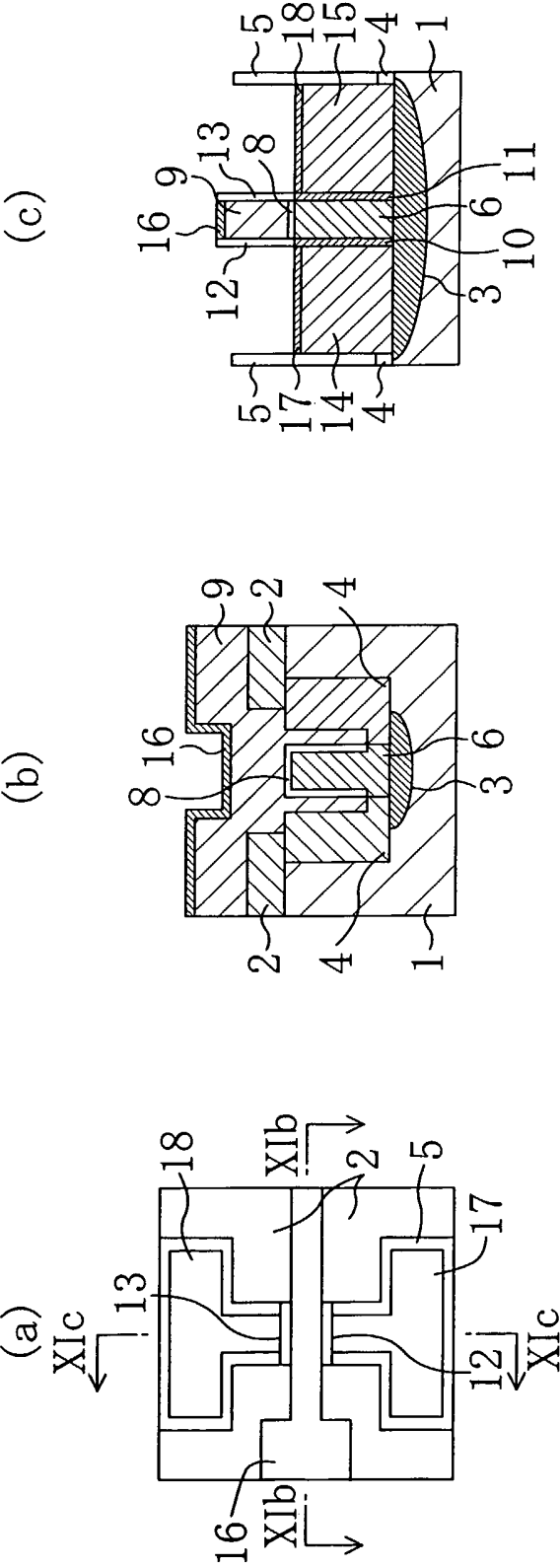
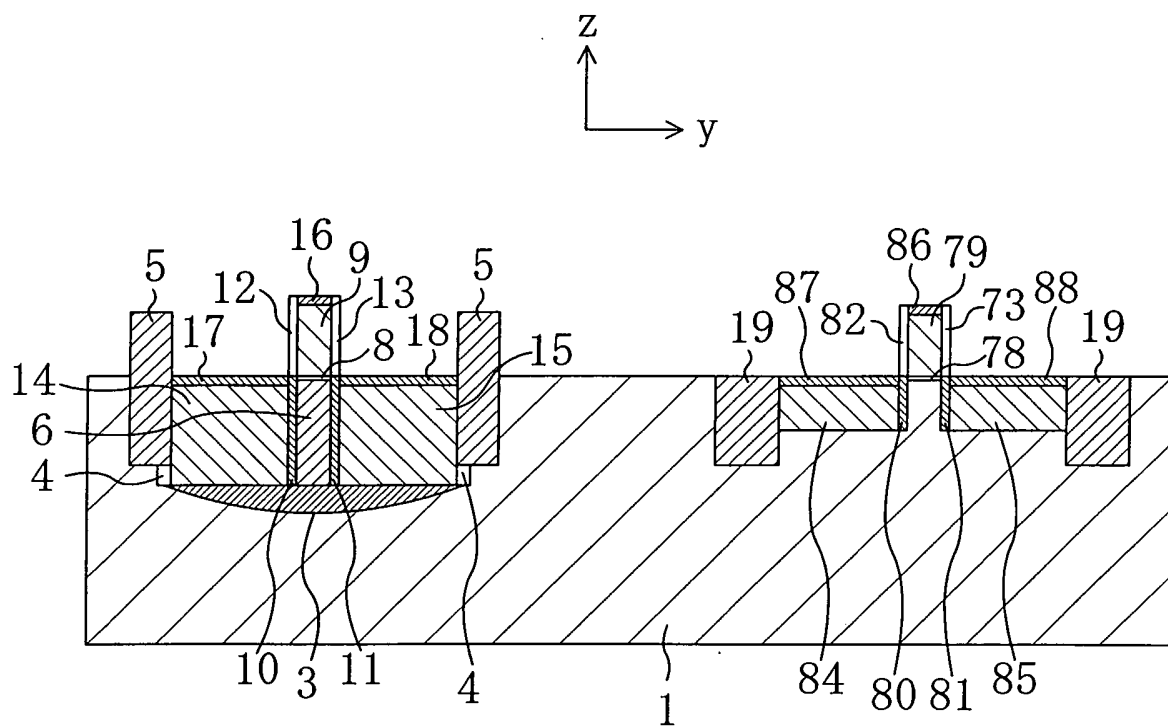


FIG. 12



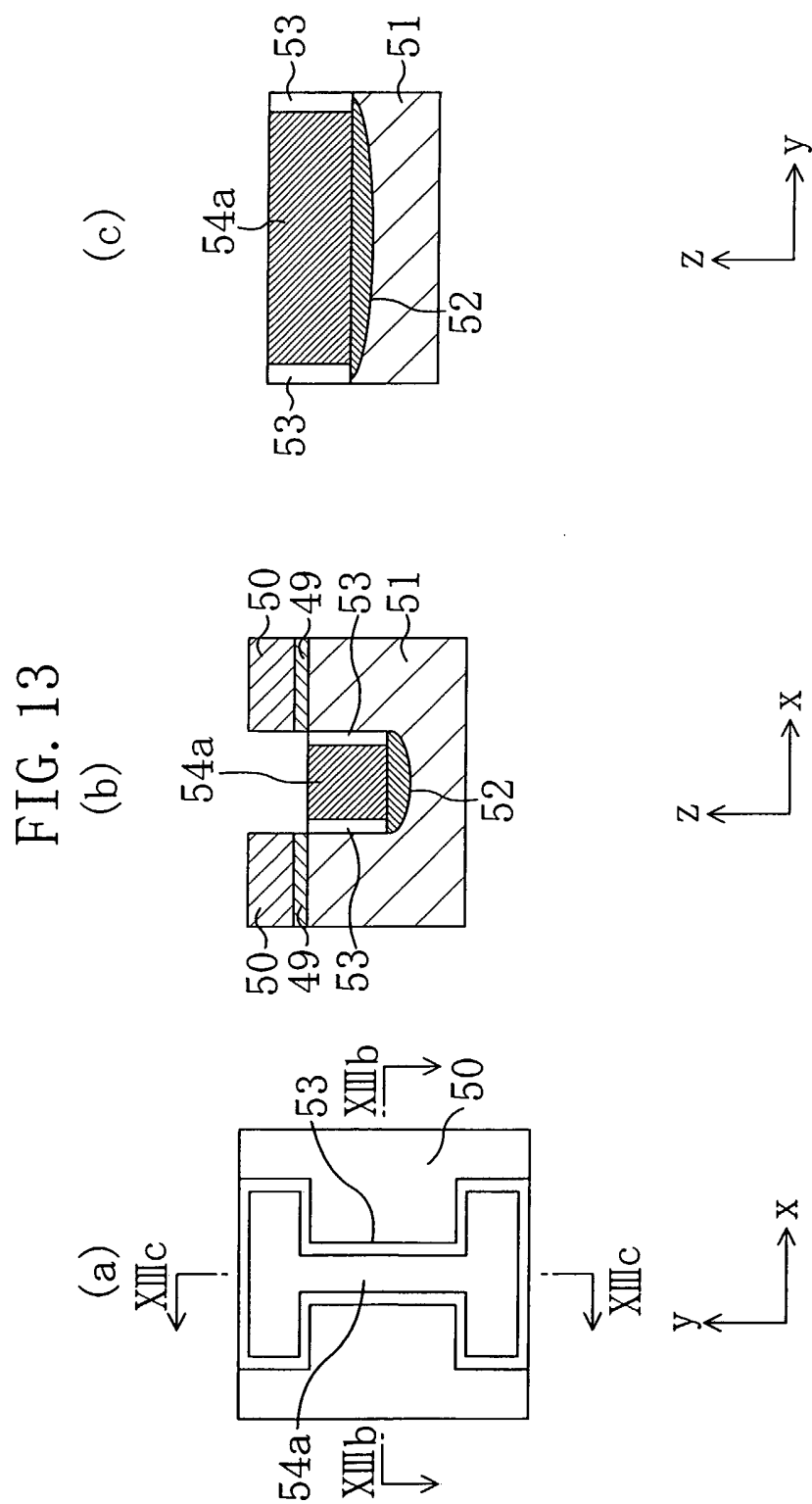


FIG. 14

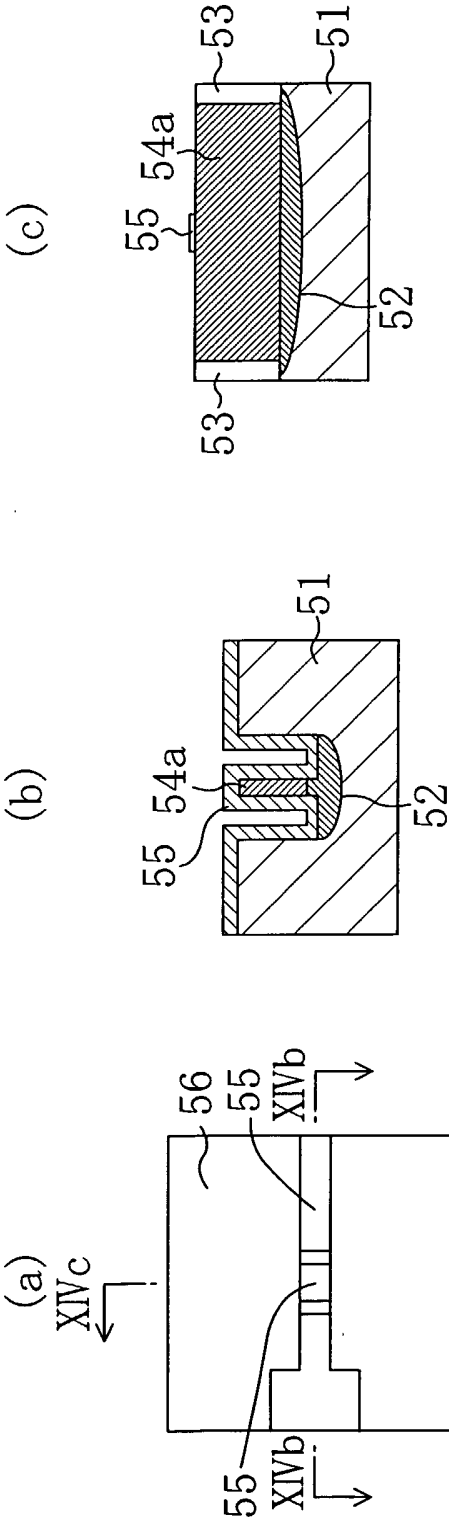


FIG. 15

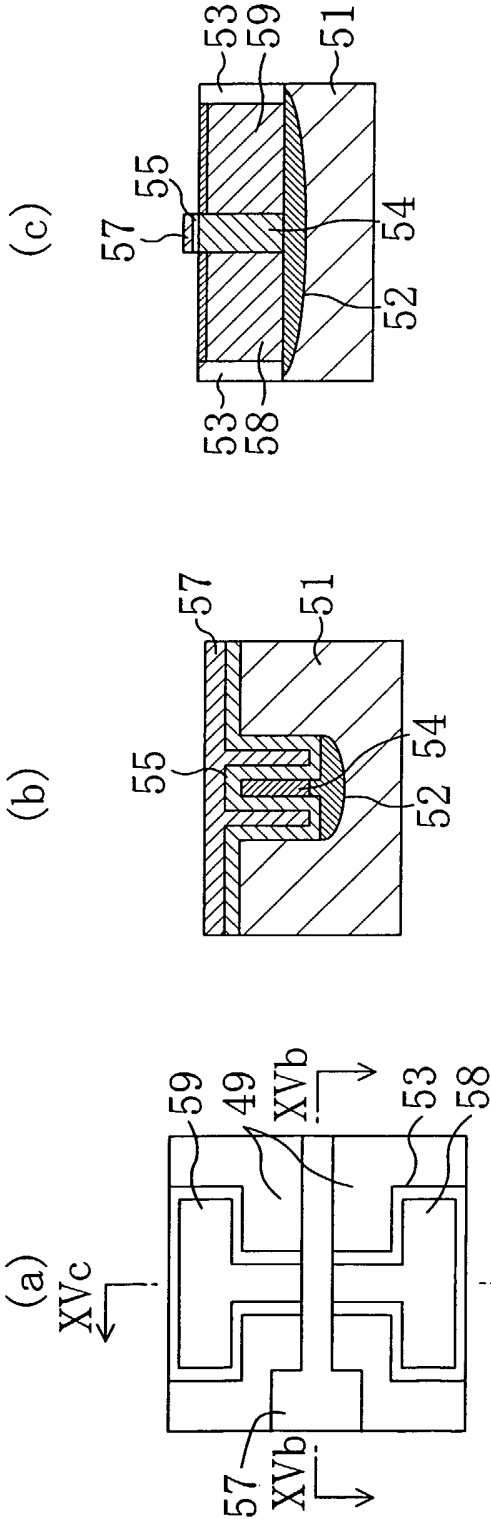


FIG. 16

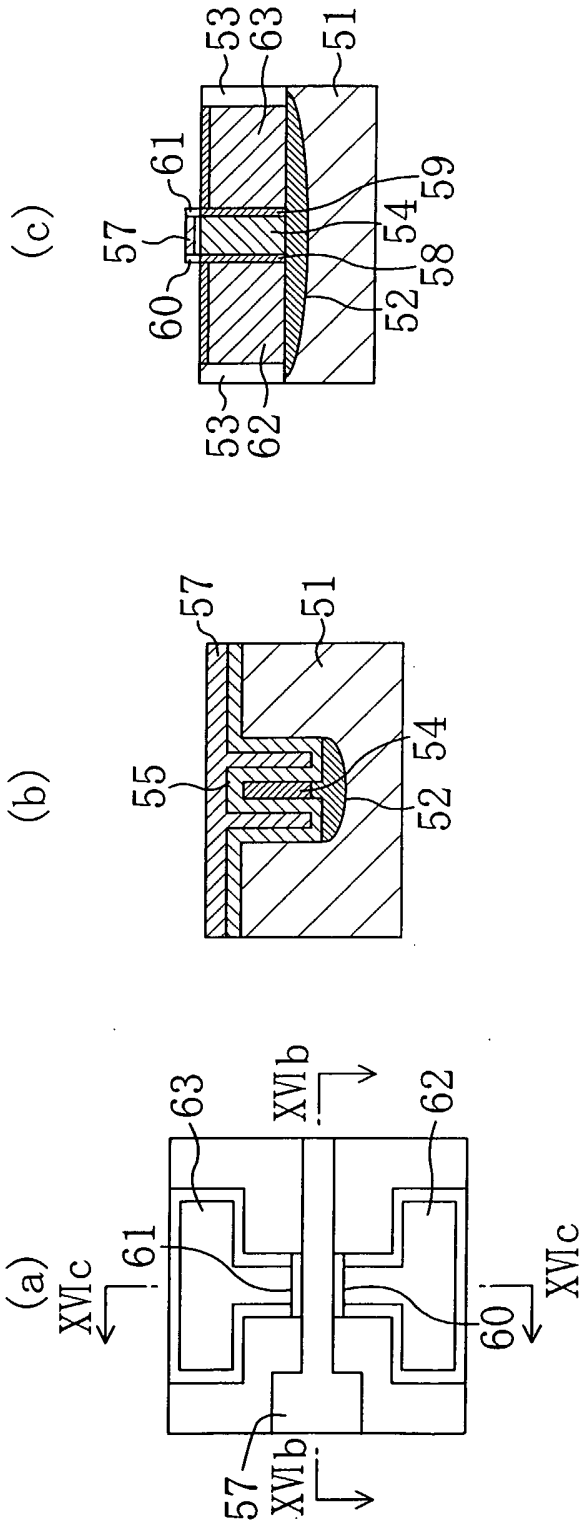
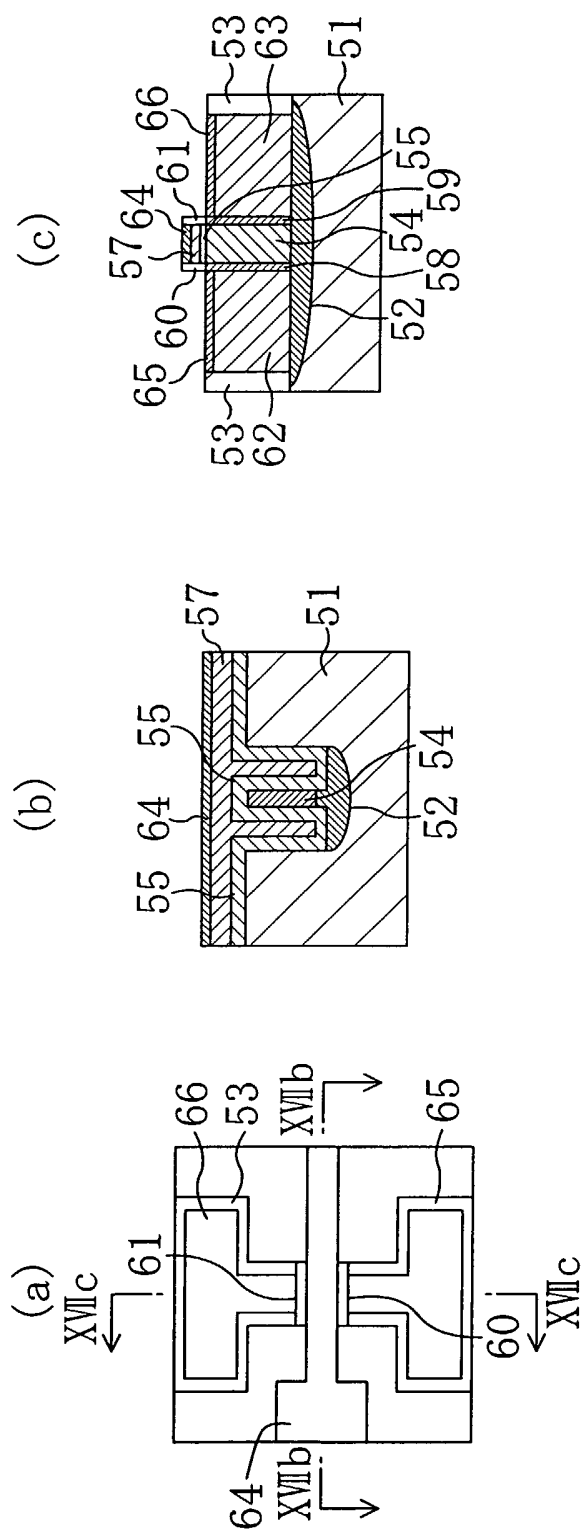
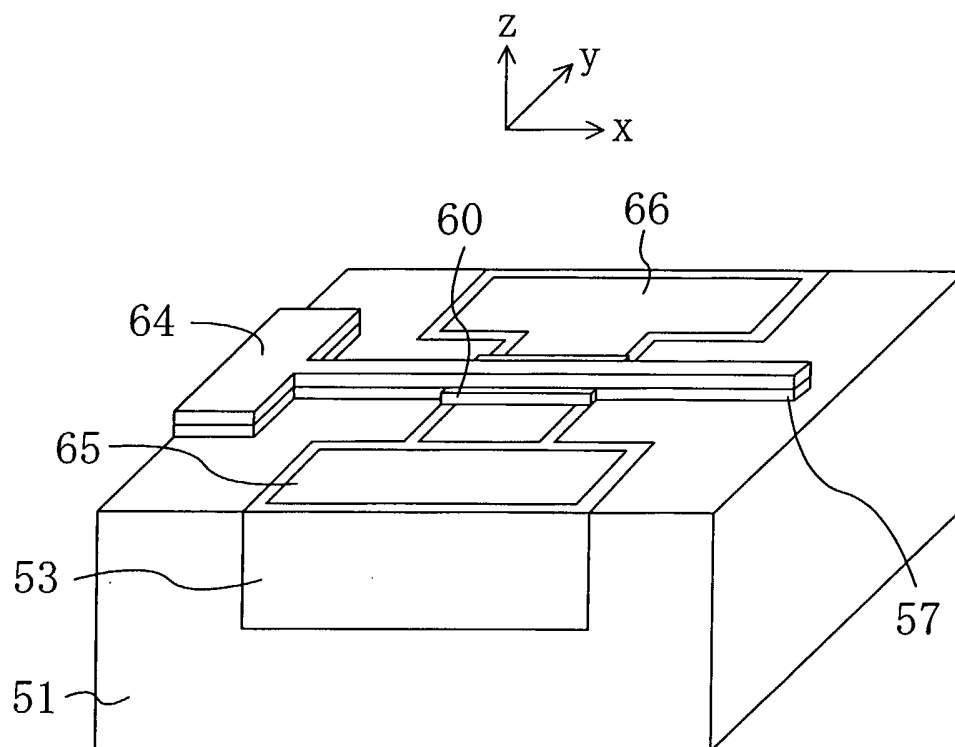


FIG. 17
(b)

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FIG. 18



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FIG. 19

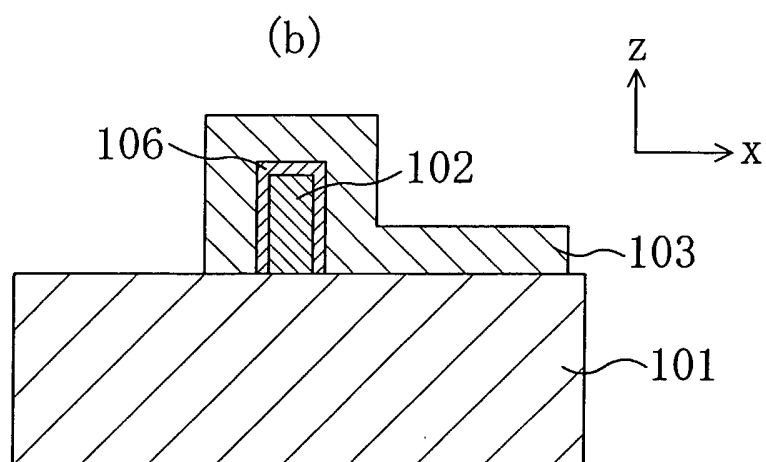
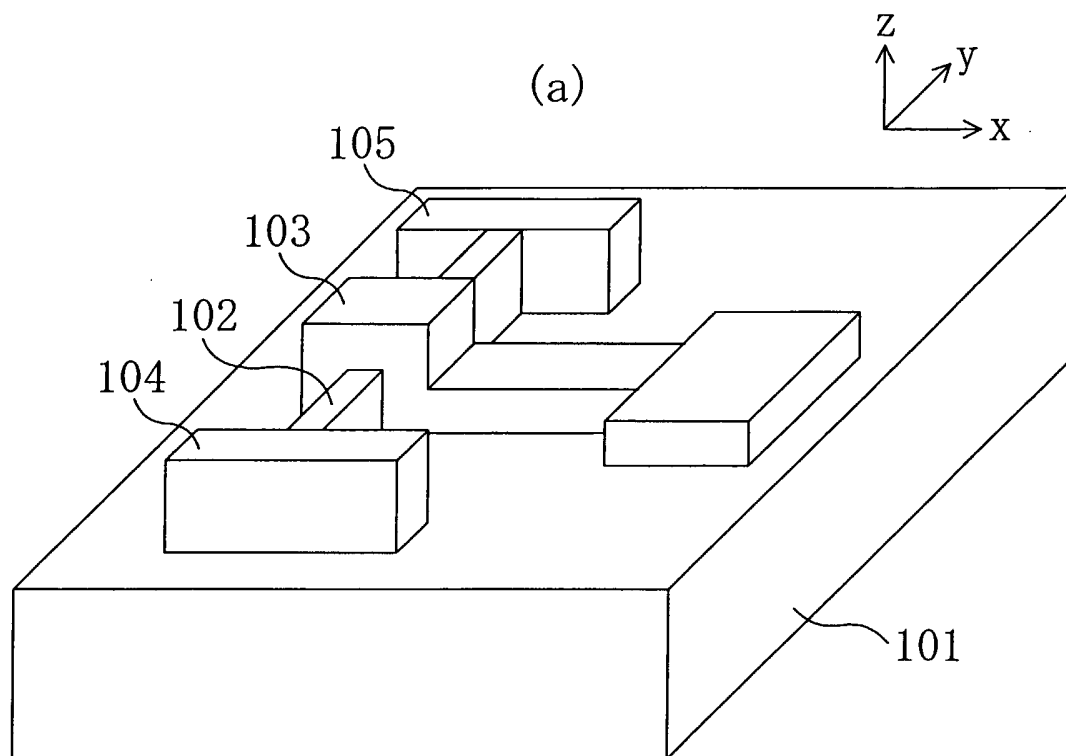


FIG. 20

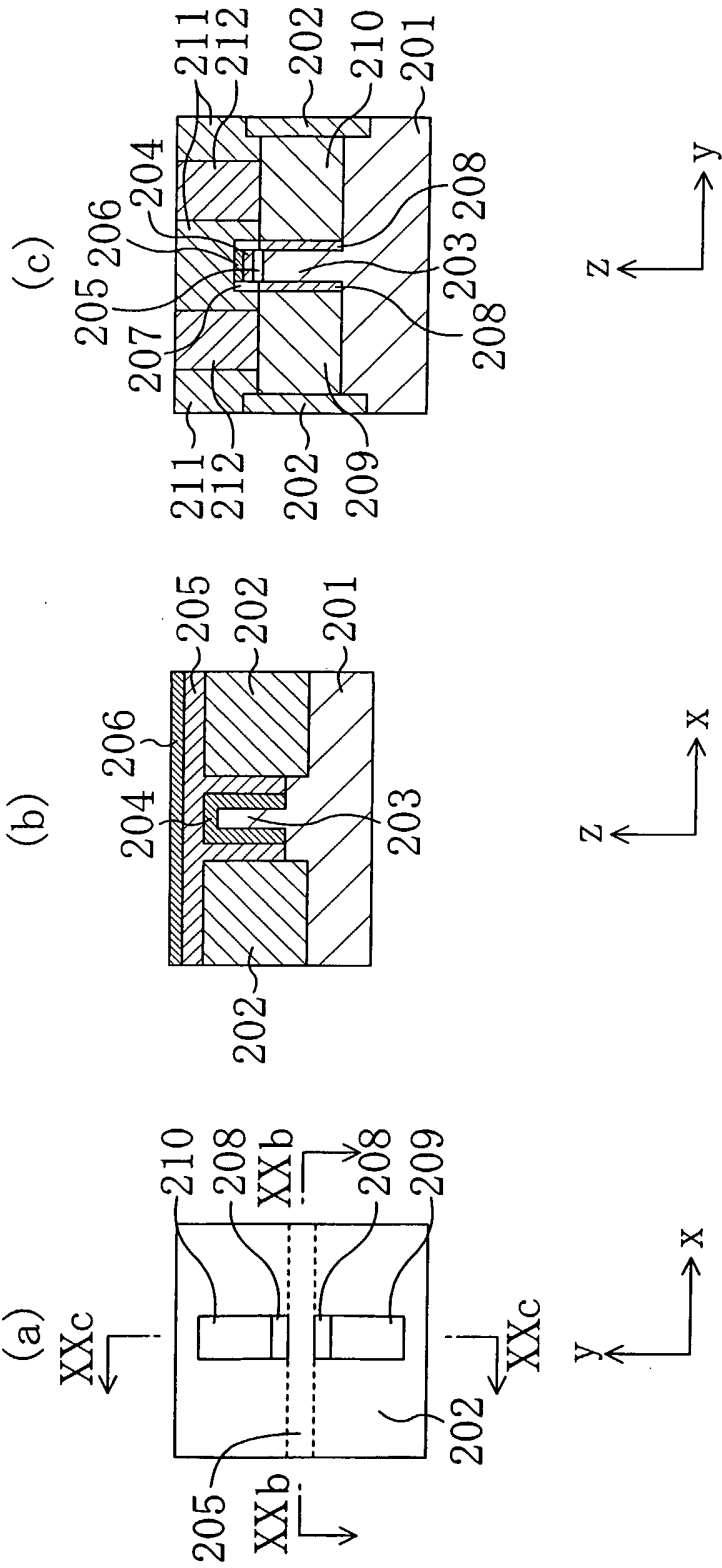
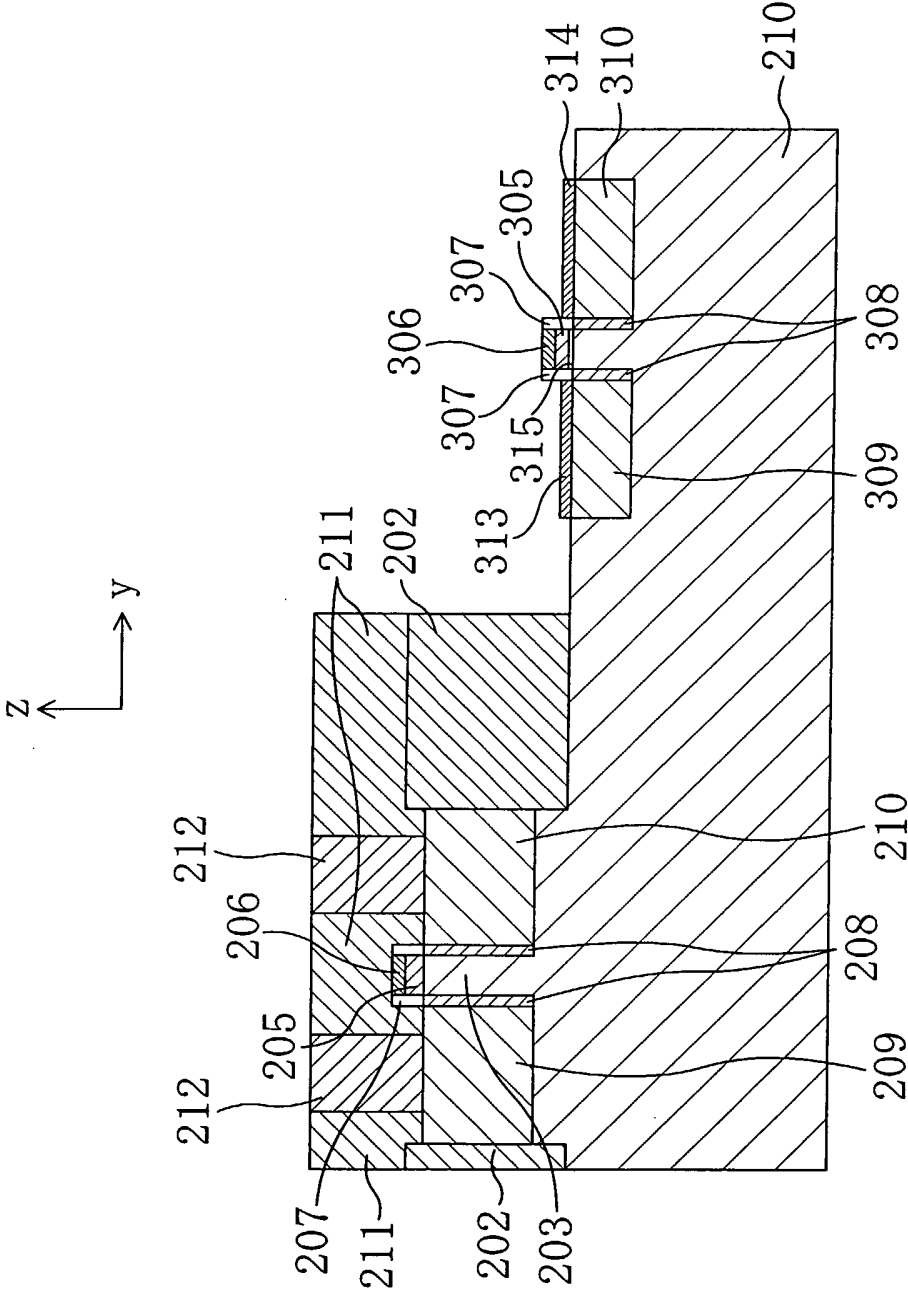


FIG. 21



INTERNATIONAL SEARCH REPORT

International Application No

PCT/JP 20/04003808

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L21/336 H01L29/423 H01L29/786 H01L21/84 H01L27/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, COMPENDEX, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 996 574 A (SHIRASAKI MASAHIRO) 26 February 1991 (1991-02-26) column 7, line 34 -column 8, line 15; claims 11-13; figures 10,11 ---	1-11
X	EP 0 623 963 A (SIEMENS AG) 9 November 1994 (1994-11-09) the whole document ---	1-11
X	US 2002/003256 A1 (MAEGAWA SHIGETO) 10 January 2002 (2002-01-10) page 6, paragraph 89 - paragraph 94 page 7, paragraph 100 -page 9, paragraph 123; claims; figures 1-23 --- -/--	1-11

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

14 June 2004

Date of mailing of the international search report

22/06/2004

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/JP 20/0400380

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
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A	KEDZIERSKI J ET AL: "High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices" INTERNATIONAL ELECTRON DEVICES MEETING 2001. IEDM. TECHNICAL DIGEST. WASHINGTON, DC, DEC. 2 - 5, 2001, NEW YORK, NY: IEEE, US, 2 December 2001 (2001-12-02), pages 1951-1954, XP010575161 ISBN: 0-7803-7050-3 cited in the application the whole document -----	1-11

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