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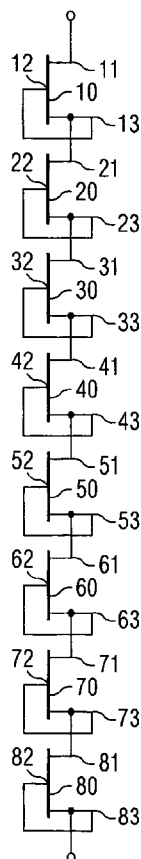
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(54) Title: RESISTANCE COMPONENT

(57) Abstract: A resistance component comprises a multitude of pHEMTs (10, 20, 30, 40, 50, 60, 70, 80) which are connected in series.

FIG 1





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Description

Resistance component

The invention concerns a resistance component which may be formed on a substrate or a semiconductor material. The resistance component may be part of an integrated circuit.

High-ohmic resistances having linear current-voltage-relation and low current consumption may be useful in integrated circuits, for example in an integrated circuit for processing digital signals. In GaAs technology typically only low-ohmic resistors are provided. Examples are a thin film resistor or TFR, which may have 50 Ohm/sq, a base resistor, which may have 200 Ohm/sq, and a wide recess resistor, which may have 500 Ohm/sq. These resistors may not occupy much chip area.

Resistors in GaAs technology are reported in the following papers: Fabian Radulescu, Jinhong Yang, Paul Miller, Ron Herring, Chi-Fung Lo, and Wolfgang Liebl: "High Value Thin Film Resistor for GaAs IC Manufacturing", CS MANTECH Conference, 2006, Vancouver; Hong Shen, Jose Arreaga, Ravi Ramanathan, Heather Knoedler, John Sawyer, and Shibani Tikku: "Fabrication and characterization of thin film resistors for GaAs-based power amplifiers", 2003 International Conference on Compound Semiconductor Mfg.; Yong Cheong and James Morris: "N-Minus Resistance Control for 6 inch GaAs MESFET Manufacturing", US patent 7199016, and US patent application 2004/0080396.

Merged or stacked FET-HBT integration schemes, often called BiFET or BiHEMT and containing both HBT and FET or pHEMT device on a single GaAs substrate, are reported in the following papers from the CS MANTECH Conference 2007: William Peatman, Mohsen Shokrani, Boris Gedzberg, Wojciech

Krystek, and Michael Trippe: "InGaP-Plus_{TM}: Advanced GaAs BiFET Technology and Applications"; T. Henderson, J. Middleton, J. Mahoney, S. Varma, T. Rivers, C. Jordan, and B. Avrit: "High-Performance BiHEMT HBT / E-D pHEMT Integration"; Todd D. Basso and Richard B. Brown: "A Complementary GaAs Microprocessor for Space Applications"; Ravi Ramanathan, Mike Sun, Peter J. Zampardi, Andre G. Metzger, Vincent Ho, Cejun Wei, Peter Tran, Hongxiao Shao, Nick Cheng, Cristian Cismaru, Jiang Li, Shiaw Chang, Phil Thompson, Mark Kuhlman, Kenneth Weller: "Commercial Viability of a Merged HBT-FET (BiFET) Technology for GaAs Power Amplifiers"; C. K. Lin, T. C. Tsai, S. L. Yu, C. C. Chang, Y. T. Cho, J. C. Yuan, C. P. Ho, T. Y. Chou, J. H. Huang, M. C. Tu, and Y. C. Wang: "Monolithic Integration of E/D-mode pHEMT and InGaP HBT Technology on 150-mm GaAs Wafers".

High-ohmic resistors are needed to save occupied chip area and/or current consumption. A conventional high-ohmic resistor requires a thin layer, the thinner the layer the higher the sheet resistance. However, resistance layers with more than 50 Ohm/sq are usually not available in GaAs processes, because of limitations to the linearity and temperature coefficient of the resistance and limitations related to manufacturability and reliability. Moderate ohmic resistors would occupy less space at the expense of higher current consumption.

There is a need for a high-ohmic resistor requiring less chip area. It may be further desired to have a very small temperature coefficient.

For this aim a resistance component is provided, the resistance component comprising a multitude of pHEMTs which are connected in series.

The pHEMT or pseudomorphic high electron mobility transistor is a type of a FET or field effect transistor. One embodiment of the pHEMT is available in a GaAs technology. The pHEMT may be manufactured in BiFET technology which is suitable for provision of GaAs HBT designs in combination with pHEMT.

The multitude of pHEMTs may be formed on a substrate or a semiconductor material. In one embodiment the multitude of pHEMTs serves as a resistance component of an integrated circuit.

The multitude of pHEMTs serves as a high-ohmic resistor, which operates at a low current and may occupy less chip area in comparison with a conventional resistor. The resistance component has a linear current-voltage-characteristic over a wide range and has low current consumption. The resistance component which comprises a multitude of pHEMTs enables the reduction of power consumption, chip area and cost. This component may be formed in GaAs pHEMT/BiFET technology.

Preferably, the pHEMTs are depletion mode transistors. A D-mode pHEMT is conducting when the gate source voltage (V_{gs}) is more positive than a negative threshold voltage (V_t).

Each of the pHEMTs has a gate electrode, a source and a drain, the gate electrode and the source being bypassed, which means that they are electrically connected, so that a voltage V_{gs} between the gate electrode and the source is $V_{gs}=0$.

Preferably, the pHEMTs are designed as long-gate pHEMTs. In one embodiment, at least one long-gate pHEMT of the multitude of the pHEMTs comprises a channel having a length L , which is equal or larger than $0.5\mu\text{m}$ (micrometer).

Preferably, at least one long-gate pHEMT of the multitude of the pHEMTs comprises a channel having a length L and a width W , wherein $L \gg W$, which means that the length L is significantly larger than the width W . In one embodiment the ratio L/W is larger than 10, for example $L=40\mu\text{m}$ and $W=3\mu\text{m}$. The channel is an area located beneath the gate electrode. The current flows through the channel between source and drain.

A FET or a pHEMT having a channel dimensioned as described above is a long-gate FET or pHEMT, which may serve as current source having a relative low current value in comparison with a conventional FET.

In one embodiment, the multitude of pHEMTs comprises a first pHEMT and a second pHEMT, wherein the gate electrode and the source of the first pHEMT are electrically connected with the drain of the second pHEMT, so that the first and second pHEMTs are connected in series, wherein the voltage V_{gs} between gate and source is $V_{gs}=0$. This arrangement may be cascaded so that the drain of a third pHEMT is electrically connected with the source and gate electrode of the second pHEMT. The drain of a fourth pHEMT may be electrically connected with the source and gate electrode of the third pHEMT, and so on. Metal connections may be provided for electrically connecting the source and the drain.

In one embodiment, the multitude of pHEMTs comprises a first pHEMT and a second pHEMT, wherein the source of the first pHEMT and the drain of the second pHEMT are formed by an interconnection layer which may be a structured layer. The drain and source may be merged. The interconnection layer may be designed to be rather compact, for example as a rectangular structure serving as source and drain, the structure being located between two gate electrodes.

In one embodiment the multitude of pHEMTs comprises a first pHEMT, a second pHEMT and a third pHEMT. The gate electrode of the first pHEMT is located adjacent to the gate electrode of the second pHEMT. The gate electrode of the second pHEMT is located adjacent to the gate electrode of the third pHEMT. The drain of the first pHEMT is located adjacent to the source of the second pHEMT. The source of the first pHEMT is located adjacent to and electrically connected with the drain of the second pHEMT. The drain of the second pHEMT is located adjacent to the source of the third pHEMT. The source of the second pHEMT is located adjacent to and electrically connected with the drain of the third pHEMT. Metal connections may be provided for electrically connecting the source and the drain. The sources and gate electrodes of each pHEMT are connected so that $V_{gs}=0V$, for example by a metal connection. This arrangement may be cascaded. The meandering layout described above is space saving.

Another embodiment comprises a first pHEMT, a second pHEMT and a third pHEMT. The gate electrode of the first pHEMT is located adjacent to the gate electrode of the second pHEMT. The gate electrode of the second pHEMT is located adjacent to the gate electrode of the third pHEMT, which means that the first, second, and third pHEMTs may be arranged in a row. The drain of the first pHEMT is located adjacent to the source of the second pHEMT. The source of the first pHEMT and the drain of the second pHEMT are formed by a first interconnection layer, which may be formed as a structured layer. The drain of the second pHEMT is located adjacent to the source of the third pHEMT. The source of the second pHEMT and the drain of the third pHEMT are formed by a second interconnection layer, which may be formed as a structured layer. The interconnection layer may be u-shaped so that the interconnection layer runs between two gate electrodes arranged in a row. The source and gate electrode of each pHEMT are connected so that $V_{gs}=0V$. The

arrangement may be cascaded. The meandering layout described above is space saving.

In one embodiment the resistance component is formed in GaAs technology. The resistance component is a high ohmic resistor requiring little chip area. The resistance component may be formed in GaAs pHEMT/BiFET technology. The resistance component may be a useful component for circuit design of GaAs integrated circuits, for example MMIC, RFIC.

Further features and refinements become apparent from the following description of the exemplary embodiments in connection with the accompanying figures.

Figure 1 shows a schematic diagram of an embodiment of a high resistance component which comprises a multitude of pHEMTs.

Figure 2A shows the characteristics of a single long-gate pHEMT and a resistance component which comprises a multitude of long-gate pHEMTs.

Figure 2B shows the small-signal resistance of the single pHEMT and the resistance component.

Figures 3 to 5 show exemplary layouts of a resistance component.

Figure 1 shows an embodiment of a high resistance component which comprises a multitude of pHEMTs 10, 20, 30, 40, 50, 60, 70, 80 of depletion mode type. In this exemplary embodiment a first pHEMTs 10, a second pHEMT 20, a third pHEMT 30, a fourth pHEMT 40, a fifth pHEMT 50, a sixth pHEMT 60, a seventh pHEMT 70, and an eight pHEMT 80 are provided.

A pHEMT or pseudomorphic high electron mobility transistor is a FET or field effect transistor incorporating a junction between two materials with different bandgaps. One material combination may be GaAs and AlGaAs.

Each pHEMT 10, 20, 30, 40, 50, 60, 70, 80 comprises a drain 11, 21, 31, 41, 51, 61, 71, 81, a source 13, 23, 33, 43, 53, 63, 73, 83 and a gate electrode 12, 22, 32, 42, 52, 62, 72, 82. The source 13, 23, 33, 43, 53, 63, 73, 83 and the gate electrode 12, 22, 32, 42, 52, 62, 72, 82 of each pHEMT 10, 20, 30, 40, 50, 60, 70, 80 are bypassed, which means that the voltage V_{gs} between its gate electrode 12, 22, 32, 42, 52, 62, 72, 82 and its source 13, 23, 33, 43, 53, 63, 73, 83 is equal or nearly equal to zero, i.e. $V_{gs}=0$.

The pHEMTs 10, 20, 30, 40, 50, 60, 70, 80 are connected in series, which means that the gate electrode 12 and the source 13 of the first pHEMT 10 are electrically connected with the drain 21 of the second pHEMT 20. The gate electrode 22 and the source 23 of the second pHEMT 20 are electrically connected with the drain 31 of the third pHEMT 30. Further pHEMTs 40, 50, 60, 70, 80 are cascaded in the same way. A supply voltage can be applied between the drain 11 of the first pHEMT 10 and the gate electrode 82 and source 83 of the last pHEMT 80 of the series connection of the pHEMTs 10, 20, 30, 40, 50, 60, 70, 80.

Preferably the pHEMTs 10, 20, 30, 40, 50, 60, 70, 80 are long-gate pHEMTs. This means that a length L of a channel of the pHEMTs is equal or larger than $0.5\mu\text{m}$ or micrometer. One embodiment has a channel length of several hundred micrometers. A conventional FET may have a channel length L being approximately $0.5\mu\text{m}$.

Figure 4 shows the length L and a width W of a channel 17 of one of the pHEMTs 10. The channel 17 is formed beneath the gate electrode 12. The current between the drain 11 and source 13 flows through the channel 17.

The current of a FET scales with W/L . Reducing the width W and/or increasing the length L causes reduction of the current. A FET having a small width W and a long length L is called a long-gate FET. Preferably the length L is much larger than the width, i.e. $L \gg W$.

Referring to Figure 2A, the characteristics of a single long-gate pHEMT and a high resistance component which comprises a multitude of N long-gate pHEMTs are shown. N is the number of pHEMTs comprised by the resistance component. In this embodiment the resistance component comprises $N=5$ pHEMTs. The pHEMTs may have a width $W=3\mu\text{m}$ and a length $L=640\mu\text{m}$. The current I_{ds} (in μA) versus the voltage V_{ds} (in Volt) applied to the single long-gate pHEMT and the multitude of long-gate pHEMTs, respectively, are shown. The voltage V_{ds} is applied between the drain and source of the single pHEMT. The voltage V_{ds} is applied between the drain of the first pHEMT and source of the last pHEMT of the resistance component. Graph n1 indicates the characteristic of the single long-gate pHEMT. Graph n2 indicates the characteristic of the resistance component which comprises the multitude of pHEMTs.

Each graph n1, n2 comprises a linear region in which the I_d - V_{ds} -characteristics are nearly linear, and a saturation region in which the current I_d is nearly constant. In the linear region of the graphs for n1 and n2, the resistance is nearly constant, and the single pHEMT and the multitude of the pHEMTs may be used as resistors. The linear region is from 0 to 0.3V for the single pHEMT and from 0 to 1.5V for the multitude of pHEMTs. In the saturation of the graphs for n1 and n2, the

current is nearly constant, and the single pHEMT and the multitude of the pHEMTs may be used as current sources.

Figure 2B shows the small-signal resistance dV_{ds}/dI_{ds} versus V_{ds} of the single pHEMT, indicated by graph m1, and of the multitude of pHEMTs, indicated by graph m2.

The plots in Figures 2A and 2B show that at low V_{ds} the multitude of pHEMTs has a larger equivalent resistance, which is also more constant over a wider V_{ds} range.

The series connection of the multitude of pHEMTs causes this effect. The maximum current of the multitude of pHEMTs at high V_{ds} is unchanged in comparison with a single pHEMT, but the linear I_{ds} - V_{ds} slope at the origin is N times smaller, N being the number of pHEMTs, which corresponds to an N times higher resistance. Also the output resistance at high V_{ds} is N times higher.

When a given voltage V_{ds} , which is in the linear region, is applied to the single pHEMT a respective current I_{ds} flows. When the same voltage V_{ds} is applied to the multitude of N pHEMTs only a fraction of the voltage V_{ds} , which is about V_{ds}/N , is applied to one of the multitude of pHEMTs. Thus, the current I_{ds} through the pHEMTs is reduced. The current I_{ds} which flows through the single pHEMT is N times larger than the current I_{ds} flowing through the multitude of N pHEMTs. Therefore the I_{ds} - V_{ds} plot n2 of the multitude of pHEMTs looks like a horizontally stretched I_{ds} - V_{ds} plot n1 of the single pHEMT.

Figure 3 shows an exemplary layout of a resistance component. The resistor comprises eight long-gate pHEMTs 10, 20, 30, 40, 50, 60, 70, 80.

Each pHEMT 10, 20, 30, 40, 50, 60, 70, 80 comprises a drain 11, 21, 31, 41, 51, 61, 71, 81, a source 13, 23, 33, 43, 53, 63, 73, 83 and a gate electrode 12, 22, 32, 42, 52, 62, 72, 82, which has a gate terminal 14, 24, 34, 44, 54, 64, 74, 84 to which a potential can be applied.

The pHEMTs 10, 20, 30, 40, 50, 60, 70, 80 in this embodiment are arranged in an array having two columns of four pHEMTs each. The pHEMTs 10, 20, 30, 40 in the right column are orientated so that their sources 13, 23, 33, 43 are directed to a first direction, which is the top of figure 3, and so that their drains 11, 21, 31, 41 are directed to a second direction, which is the bottom of figure 3, the second direction being opposite to the first direction. The pHEMTs 50, 60, 70, 80 in the other column are orientated contrariwise. Their drains 51, 61, 71, 81 are directed to the first direction. Their sources 53, 63, 73, 83 are directed to the second direction.

In the right column, the source 13 of the first pHEMT 10 and the drain 21 of the second pHEMT 20 are merged by a layer, for example by a structured layer which may be etched or implanted. The source 23 of the second pHEMT 20 and the drain 31 of the third pHEMT 31 are also merged. The source 33 of the third pHEMT 30 and the drain 41 of the fourth pHEMT 40 are merged, too.

In the other column, the source 53 of the fifth pHEMT 50 and the drain 61 of the sixth pHEMT 60 are merged, for example by a structured layer which may be etched or implanted. The source 63 of the sixth pHEMT 60 and the drain 71 of the seventh pHEMT 70 are merged as well as the source 73 of the seventh pHEMT 70 and the drain 81 of the eighth pHEMT 80.

The channels 17, 27, 37, 47, 57, 67, 77, 87 between the sources 13, 23, 33, 43, 53, 63, 73, 83 and the drains 11, 21, 31, 41, 51, 61, 71, 81 run beneath the gate electrodes 12, 22, 32, 42, 52, 62, 72, 82.

The sources 13, 23, 33, 43, 53, 63, 73, 83 and the gate terminals 12, 22, 32, 42, 52, 62, 72, 82 of each pHEMT 10, 20, 30, 40, 50, 60, 70, 80 are connected so that $V_{gs}=0V$ by metal connections 15, 25, 35, 45, 55, 65, 75, 85, so that the gate-source voltage V_{gs} of each pHEMT is $V_{gs}=0$.

The left and right columns are connected by a metal connection 45, which connects the gate terminal 44 and the source 43 of the fourth pHEMT 40 with the drain 51 of the fifth pHEMT 50.

The gate electrodes 12, 22, 32, 42, 52, 62, 72, 82, the gate terminals 14, 24, 34, 44, 54, 64, 74, 84 and the metal connections 15, 25, 35, 45, 55, 65, 75, 85 are made of metal, for example gold. They are arranged over layers in which the sources 13, 23, 33, 43, 53, 63, 73, 83, the drains 11, 21, 31, 41, 51, 61, 71, 81 and the channels 17, 27, 37, 47, 57, 67, 77, 87 are formed. An isolation layer (not shown in figure 3) is sandwiched between the semiconductor material and the metal connections. Vias 18, 28, 38, 48, 58, 68, 78, 88 in the isolation layer are provided for connecting the metal interconnects 15, 25, 35, 45, 55, 65, 75, 85 to the drains 11, 21, 31, 41, 51, 61, 71, 81 and sources 13, 23, 33, 43, 53, 63, 73, 83 located beneath.

The eight long-gate pHEMTs 10, 20, 30, 40, 50, 60, 70, 80 serve as resistance component. A supply voltage for the resistance component is applied between the drain 11 of the first pHEMT 10 and the source 83 of the eighth pHEMT 80, which is connected with the gate terminal 84 of the eighth pHEMT 80.

In one embodiment, the source 83 of the eighth pHEMT 80 is connected with a ground potential.

In one embodiment each long-gate pHEMT 10, 20, 30, 40, 50, 60, 70, 80 has the channel width $W=3\mu\text{m}$ and the channel length $L=40\mu\text{m}$.

Figure 4 shows another embodiment of an exemplary layout of a resistor. The resistance component comprises eight long-gate pHEMTs 10, 20, 30, 40, 50, 60, 70, 80.

Each pHEMT 10, 20, 30, 40, 50, 60, 70, 80 comprises a drain 11, 21, 31, 41, 51, 61, 71, 81, a source 13, 23, 33, 43, 53, 63, 73, 83 and a gate electrode 12, 22, 32, 42, 52, 62, 72, 82, which is connected with the source 13, 23, 33, 43, 53, 63, 73, 83 of the respective pHEMT by connections 16, 26, 36, 46, 56, 66, 76, 86. Figure 4 schematically shows the channel 17, 27, 37, 47, 57, 67, 77, 87 of each pHEMT 10, 20, 30, 40, 50, 60, 70, 80.

In this embodiment the gate electrodes 12, 22, 32, 42, 52, 62, 72, 82 are arranged in a row, so that the sources 13, 33, 53, 73 of the odd-numbered pHEMTs, which are the first, the third, the fifth and the seventh pHEMT, 10, 30, 50, 70 are orientated to the first direction, which is the top of figure 4. The drains 11, 31, 51, 71 of the odd-numbered pHEMTs 10, 30, 50, 70 are orientated to the second direction, which is the bottom of figure 4. The even-numbered pHEMTs 20, 40, 60, 80 are orientated contrariwise. The sources 23, 43, 63, 83 are orientated to the second direction. The drains 21, 41, 61, 81 are orientated to the first direction. In other words, one of the pHEMTs is positioned in the reverse orientation with respect to the pHEMTs which is located adjacent. The sources 13, 33, 53, 73 and drains 21, 41, 61, 81 which are orientated to the first direction are arranged in a row and may be

aligned along a line. The sources 23, 43, 63, 83 and drains 11, 31, 51, 71 which are directed to the first direction are also arranged in a row.

Metal connections 15, 25, 35, 45, 55, 65, 75, 85 are provided for connecting the drains and sources of adjacent pHEMTs. The source 13 of the first pHEMT 10 is connected by a metal connection 15 with the drain 21 of the second pHEMT 20. The source 23 of the second pHEMT 20 is connected by a metal connection 25 with the drain 31 of the third pHEMT 30, and so on.

The supply voltage for the resisting component is applied between the drain 11 of the first pHEMT 10 and the source 83 of the eighth pHEMT 80. In one embodiment, the source 83 of the eighth pHEMT 80 is connected with the ground potential.

Figure 5 shows another embodiment of an exemplary layout of a resistance component which comprises eight long-gate pHEMTs 10, 20, 30, 40, 50, 60, 70, 80.

In this embodiment the gate electrodes 12, 22, 32, 42, 52, 62, 72, 82 are arranged in a row, so that the sources 13, 33, 53, 73 of the odd-numbered pHEMTs 10, 30, 50, 70 are orientated to the first direction. The drains 11, 31, 51, 71 are orientated to the second direction. The even-numbered pHEMTs 20, 40, 60, 80 are orientated contrariwise.

This embodiment differs from the embodiment shown in figure 4 in the following way. Metal contacts for serial connection of the pHEMTs 10, 20, 30, 40, 50, 60, 70, 80 are not provided. The source 13 of the first pHEMT 10 and the drain 21 of the second pHEMT 20 are formed as an interconnection layer which is structured so that it connects the first and second channel 17, 27. The other sources and drains of the cascaded structure

are connected in the same way. The connection between source and drain is an internal, semiconductor or metal contact, connection instead of a metal connection as mentioned above.

The meandering layouts shown in figure 4 and 5 may be more space saving in comparison to the layout shown in figure 3. The pHEMTs 10, 20, 30, 40, 50, 60, 70, 80 are arranged so that a sequence of channels 17, 27, 37, 47, 57, 67, 77, 88 and the connections between these channels 17, 27, 37, 47, 57, 67, 77, 88 runs in a meandering manner. Alternatively they may be arranged in a different shape, for example a winding shape, which may be formed like a spiral. The area reduction by meandering or another form may be restrained by the spacing which is provided between the gates of the pHEMTs of the resistance component. More area may be saved by merging the gate-source contacts.

Other implementations are within the scope of the claims. Elements of different embodiments may be combined to form implementations not specifically described herein.

Reference numerals

10, 20, 30, 40, 50, 60, 70, 80	pHEMT
11, 21, 31, 41, 51, 61, 71, 81	drain
12, 22, 32, 42, 52, 62, 72, 82	gate electrode
13, 23, 33, 43, 53, 63, 73, 83	source
14, 24, 34, 44, 54, 64, 74, 84	gate terminal
15, 25, 35, 45, 55, 65, 75, 85	metal connection
16, 26, 36, 46, 56, 66, 76, 86	connection
17, 27, 37, 47, 57, 67, 77, 87	channel
18, 28, 38, 48, 58, 68, 78, 88	via
n1, n2, m1, m2	graph

Claims

1. A resistance component comprising a multitude of pHEMTs (10, 20, 30, 40, 50, 60, 70, 80) which are connected in series.
2. The resistance component according to claim 1, wherein the pHEMTs (10, 20, 30, 40, 50, 60, 70, 80) are of depletion mode type.
3. The resistance component according to claim 1 or 2, wherein each of the pHEMTs (10, 20, 30, 40, 50, 60, 70, 80) has a gate electrode (12, 22, 32, 42, 52, 62, 72, 82), a source (13, 23, 33, 43, 53, 63, 73, 83) and a drain (11, 21, 31, 41, 51, 61, 71, 81), the gate electrode (12, 22, 32, 42, 52, 62, 72, 82) and the source (13, 23, 33, 43, 53, 63, 73, 83) being connected so that voltage between the gate electrode and source is equal or nearly equal to zero.
4. The resistance component according to any of the claims 1 to 3, wherein at least one of the multitude of the pHEMTs (10, 20, 30, 40, 50, 60, 70, 80) comprises a channel (17, 27, 37, 47, 57, 67, 77, 87) having a length L, which is equal or larger than 0.5 μ m.
5. The resistance component according to any of the claims 1 to 4, wherein at least one of the multitude of the pHEMTs (10, 20, 30, 40, 50, 60, 70, 80) comprises a channel (17, 27, 37, 47, 57, 67, 77, 87) having a length L and a width W, wherein $L \gg W$.
6. The resistance component according to any of the claims 3 to 5, wherein the multitude of pHEMTs comprises a first pHEMT (10) and a second pHEMT (20), wherein the gate electrode (12) and the source (13) of the first pHEMT (10)

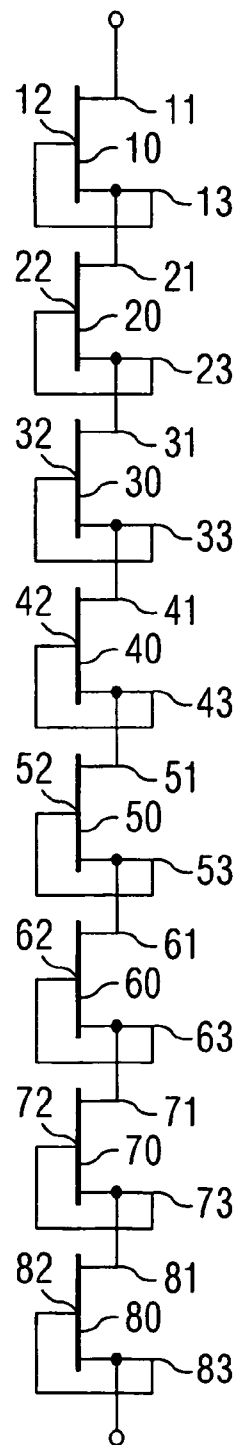
are electrically connected with the drain (21) of the second pHEMT (20).

7. The resistance component according to claim 6, wherein a metal connection (15) is provided for connecting the source (13) of the first pHEMT (10) with the drain (21) of the second pHEMT (20).
8. The resistance component according to any of the claims 3 to 5, wherein the multitude of pHEMTs comprises a first pHEMT (10) and a second pHEMT (20), wherein the source (13) of the first pHEMT (10) and the drain (21) of the second pHEMT (20) are connected using the source and the drain as an interconnection layer.
9. The resistance component according to any of the claims 3 to 5, wherein the multitude of pHEMTs comprises a first pHEMT (10), a second pHEMT (20) and a third pHEMT (30), the gate electrode (12) of the first pHEMT (10) being located adjacent to the gate electrode (22) of the second pHEMT (20), the gate electrode (12) of the second pHEMT (20) being located adjacent to the gate electrode (32) of the third pHEMT (30), the drain (11) of the first pHEMT (10) being located adjacent to the source (23) of the second pHEMT (20), the source (13) of the first pHEMT (10) being located adjacent to and electrically connected with the drain (21) of the second pHEMT (20), the drain (21) of the second pHEMT (20) being located adjacent to the source (33) of the third pHEMT (30), the source (23) of the second pHEMT (20) being located adjacent to and electrically connected with the drain (31) of the third pHEMT (30).

10. The resistance component according to any of the claims 3 to 5, wherein the multitude of pHEMTs comprises a first pHEMT (10), a second pHEMT (20) and a third pHEMT (30), the gate electrode (12) of the first pHEMT (10) being located adjacent to the gate electrode (22) of the second pHEMT (20), the gate electrode (22) of the second pHEMT (20) being located adjacent to the gate electrode (32) of the third pHEMT (30), the drain (11) of the first pHEMT (10) being located adjacent to the source (23) of the second pHEMT (20), the source (13) of the first pHEMT (10) and the drain (21) of the second pHEMT (20) are connected using the source and the drain as a first interconnection layer, the drain (21) of the second pHEMT (20) being located adjacent to source (33) of the third pHEMT (30), the source (23) of the second pHEMT (20) and the drain (31) of the third pHEMT (30) are connected using the source and the drain as a second interconnection layer.
11. The resistance component according to claim 3 to 10, wherein a metal connection (15, 25, 35, 45, 55, 65, 75) is provided for connecting the source (13, 23, 33, 43, 53, 63, 73, 83) with the gate electrode (12, 22, 32, 42, 52, 62, 72, 82).
12. The resistance component according to any of the claims 1 to 11, being formed in GaAs technology.

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FIG 1



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FIG 2A

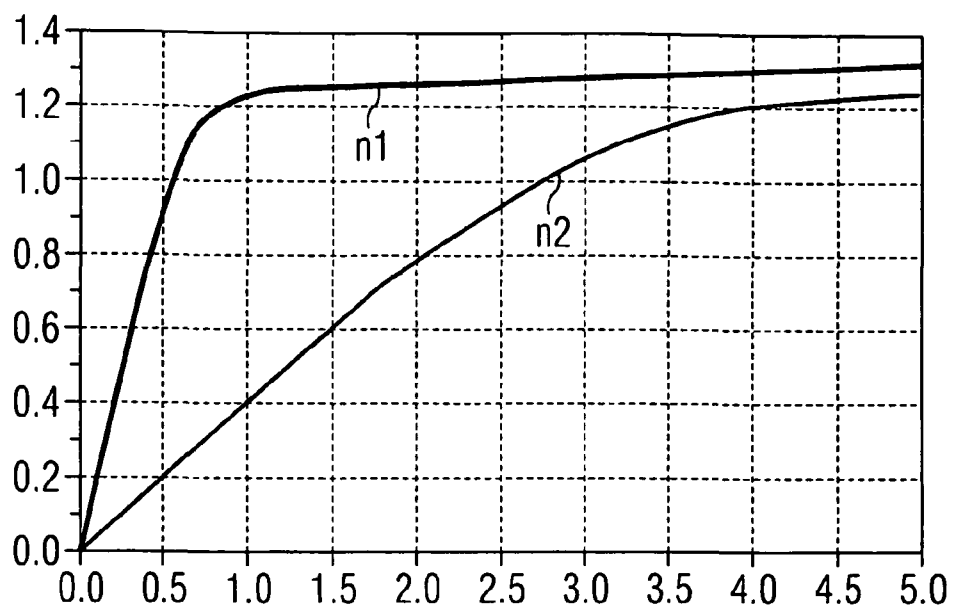
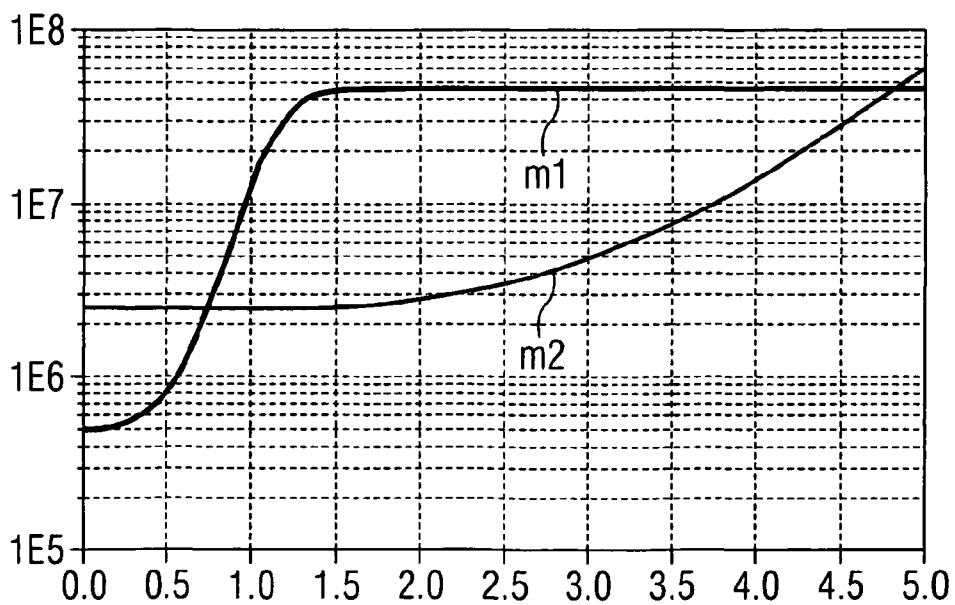
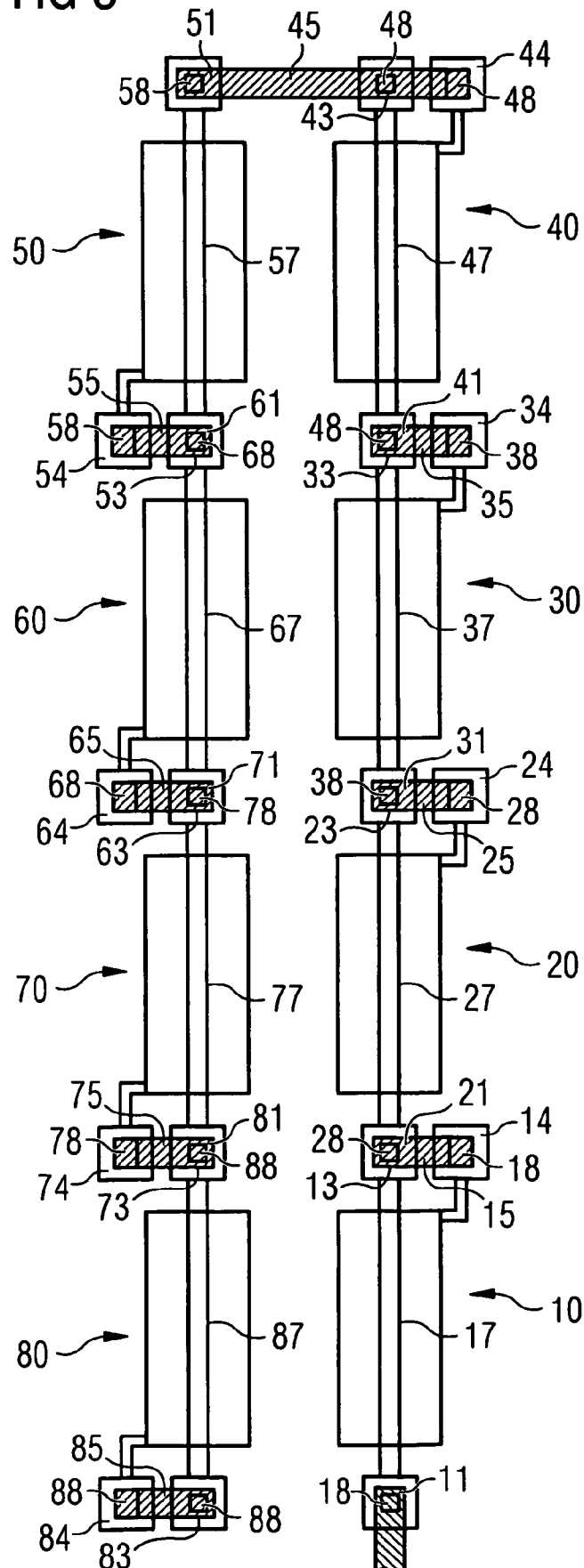


FIG 2B



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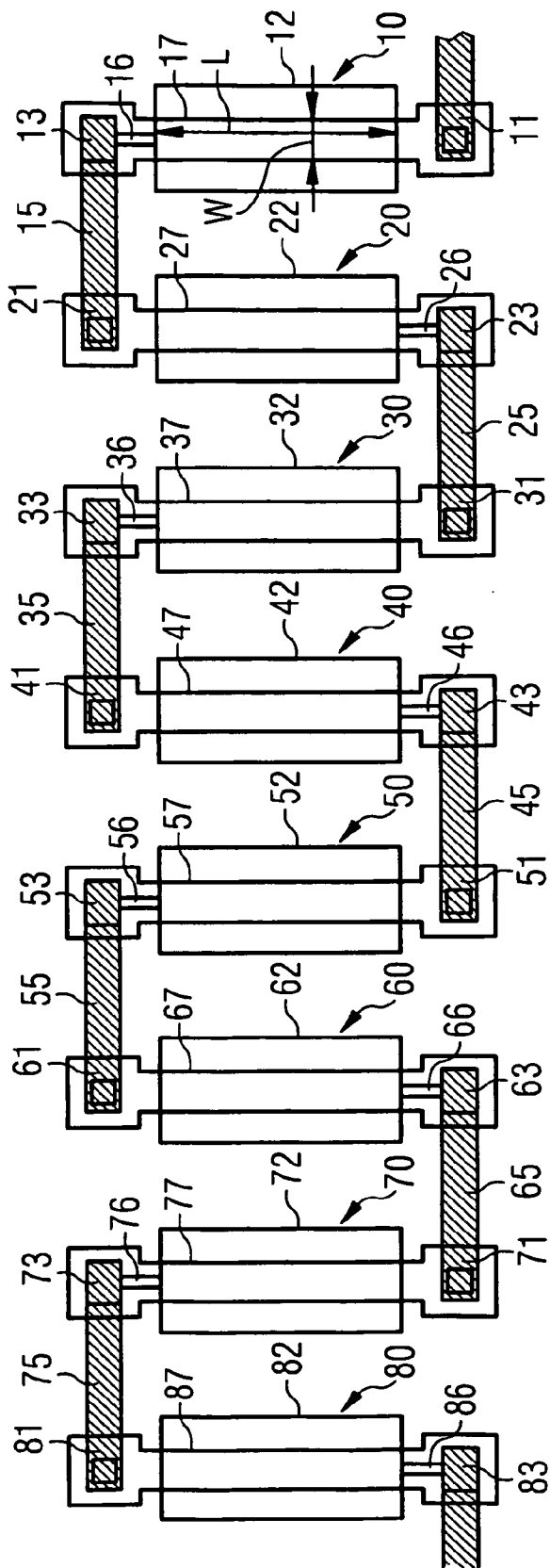
FIG 3



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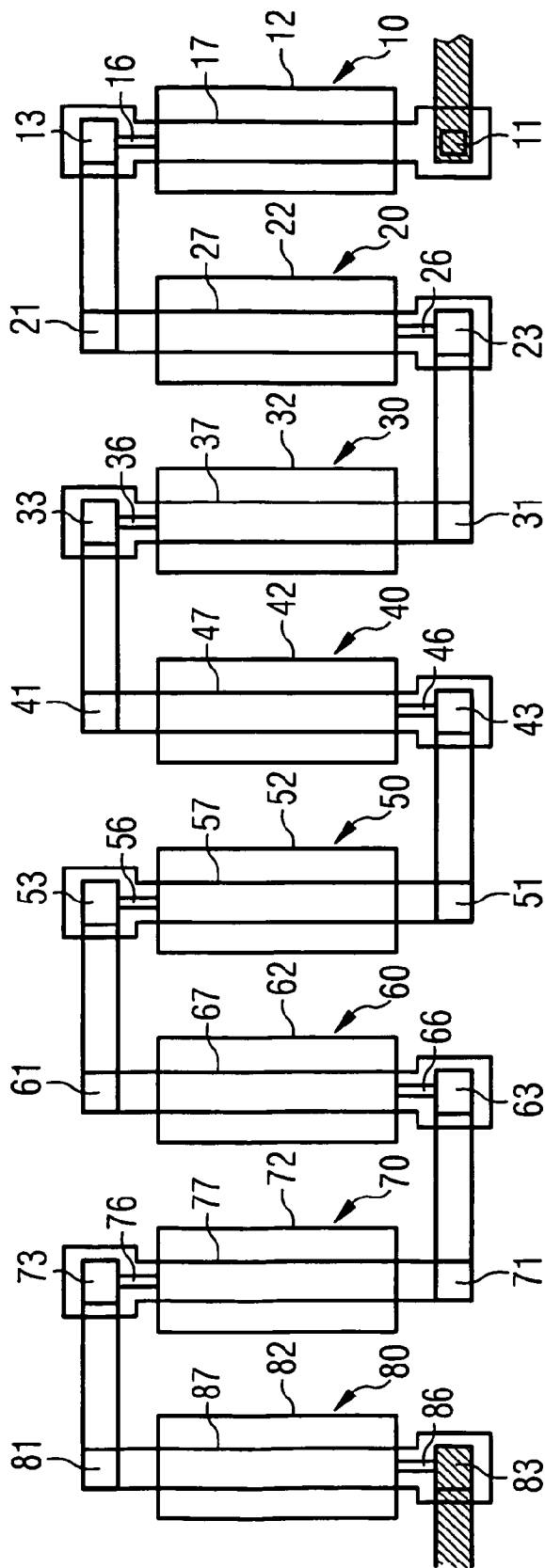
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FIG 4



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FIG 5



INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2010/052857

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L27/085 G05F1/56
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L G05F H03H H03G H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPQ-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/239440 A1 (NYBERG PETRI [FI]) 2 December 2004 (2004-12-02) paragraphs [0013], [0023]; figure 4	1,12
X	US 4 810 907 A (TOHYAMA KAY [JP]) 7 March 1989 (1989-03-07) column 7, line 34 - line 38; figures 5,10 column 7, line 50 - line 54 column 1, line 47 - line 50 column 2, line 32 - line 35 column 3, line 21 - line 23	1-4,6, 8-12
X	US 4 001 612 A (AOKI TAKAAKI ET AL) 4 January 1977 (1977-01-04) column 1, line 62 - line 64; figure 2 column 2, line 31 - line 33	1-12
	-/--	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

7 October 2010

Date of mailing of the international search report

25/10/2010

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Seck, Martin

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/052857

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SCHWIERZ F: "Microwave transistors - the last 20 years" DEVICES, CIRCUITS AND SYSTEMS, 2000. PROCEEDINGS OF THE 2000 THIRD IEEE INTERNATIONAL CARACAS CONFERENCE ON MARCH 15-17, 2000, PISCATAWAY, NJ, USA, IEEE, 15 March 2000 (2000-03-15), pages 157-163, XP010512050 ISBN: 978-0-7803-5766-2 Sections III and IV; figures 4,5,7,9 -----	1,12
A	KWOK K NG: "A Survey of Semiconductor Devices" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 43, no. 10, 1 October 1996 (1996-10-01), XP011015940 ISSN: 0018-9383 page 1762; table I -----	1
A	US 2006/238234 A1 (BENELBAR REBOUH [US] ET AL) 26 October 2006 (2006-10-26) paragraphs [0027], [0051]; figures 4,5 -----	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2010/052857

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004239440 A1	02-12-2004	WO 03021777 A1 FI 20011634 A	13-03-2003 14-02-2003
US 4810907 A	07-03-1989	DE 3673605 D1 EP 0222467 A1 JP 61272964 A	27-09-1990 20-05-1987 03-12-1986
US 4001612 A	04-01-1977	DE 2653484 A1 FR 2335958 A1 GB 1558486 A JP 1041252 C JP 52074289 A JP 55031625 B	30-06-1977 15-07-1977 03-01-1980 23-04-1981 22-06-1977 19-08-1980
US 2006238234 A1	26-10-2006	NONE	