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(54) SEMICONDUCTOR DEVICE STRUCTURES INCLUDING METAL SILICIDE INTERCONNECTS AND DIELECTRIC LAYERS AT SUBSTANTIALLY THE SAME FABRICATION LEVEL

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Publication Classification

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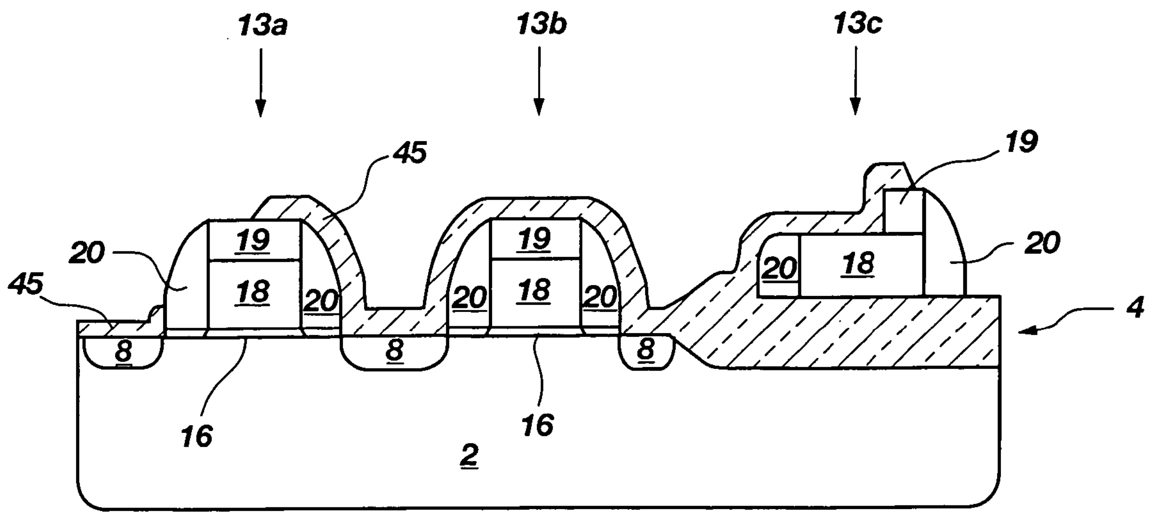
(57) **ABSTRACT**

A semiconductor device includes a metal silicide interconnect structure and a dielectric layer that are located at substantially the same fabrication level. The metal silicide interconnect and dielectric layer may be fabricated by forming an amorphous or polycrystalline silicon layer on a substrate including at least one gate structure, forming a layer of silicon nitride over the silicon layer, removing a portion of the silicon nitride layer, oxidizing the exposed portion of the silicon layer, removing the remaining portion of the silicon nitride layer, optionally removing the oxidized silicon layer, forming a metal layer over the resulting structure, annealing the metal layer in an atmosphere comprising nitrogen, and removing any metal nitride regions. The local metal silicide interconnect structure may overlie the at least one gate structure.



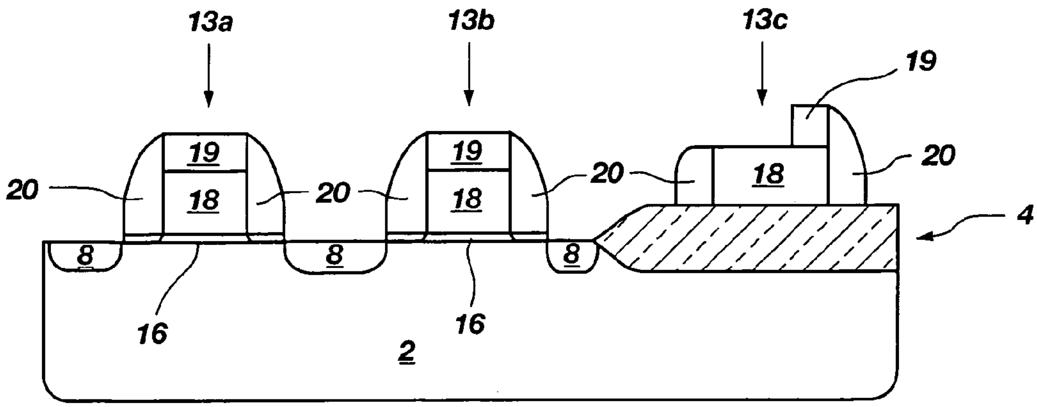

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Fig. 1

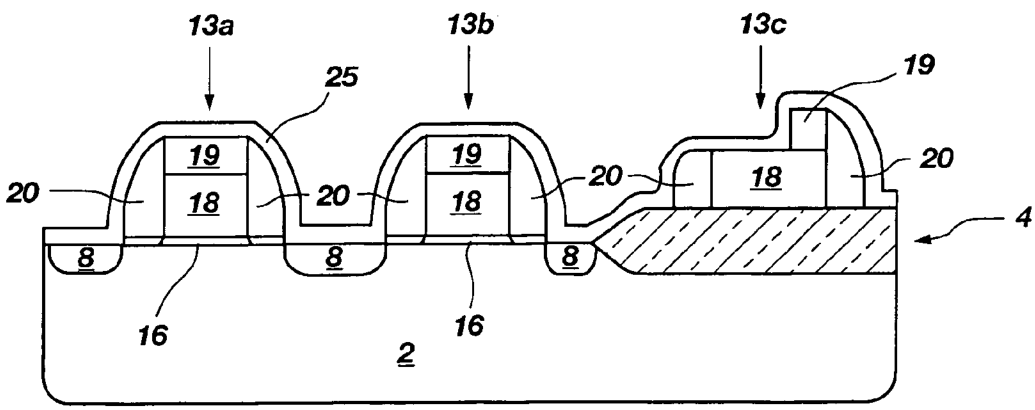
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Fig. 2

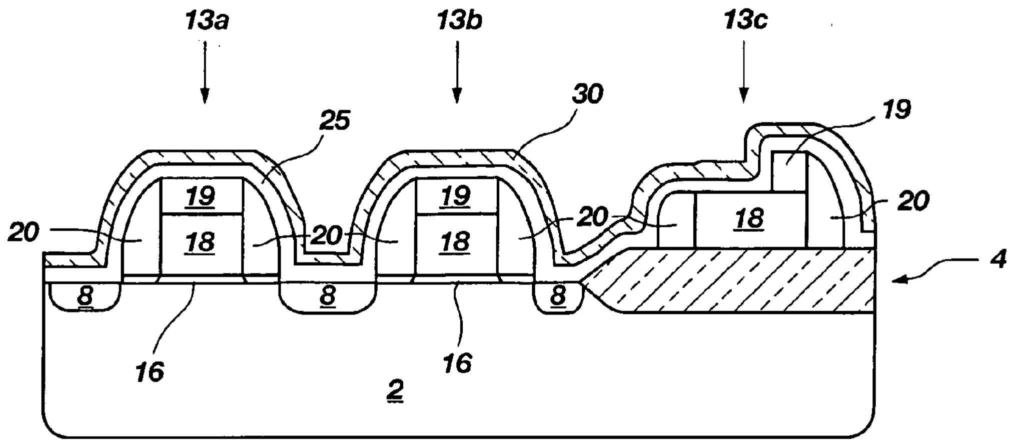
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Fig. 3

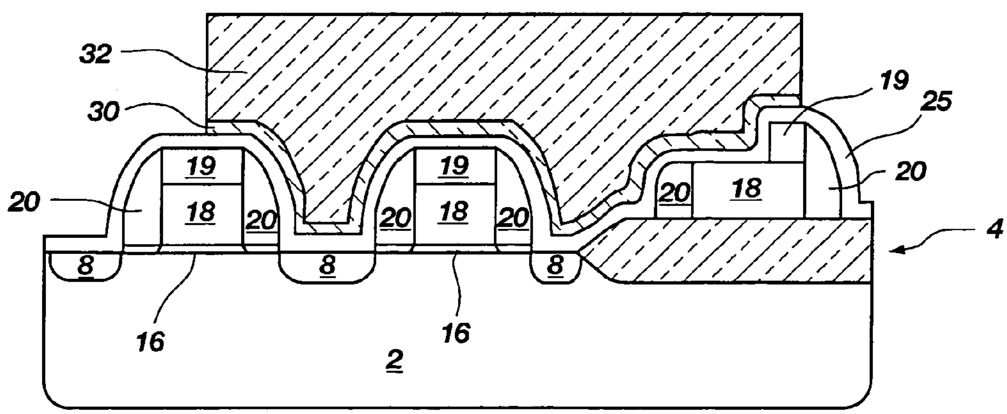
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Fig. 4

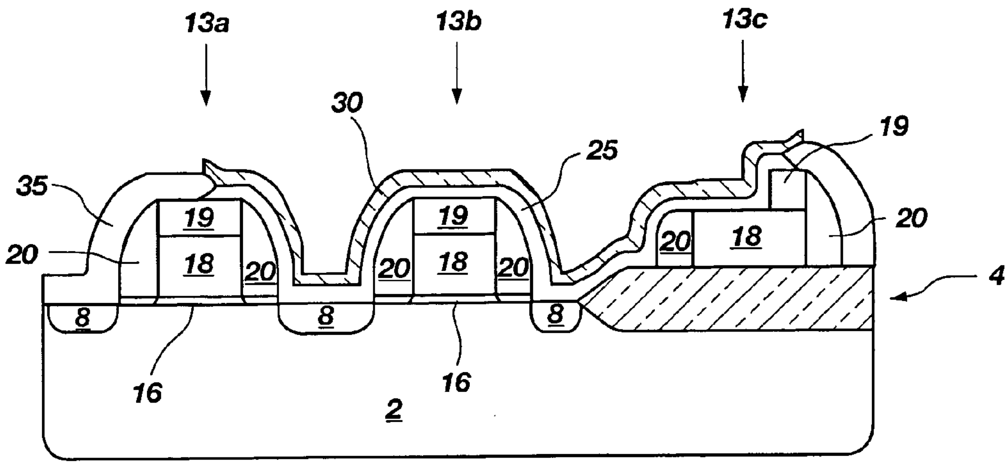
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Fig. 5

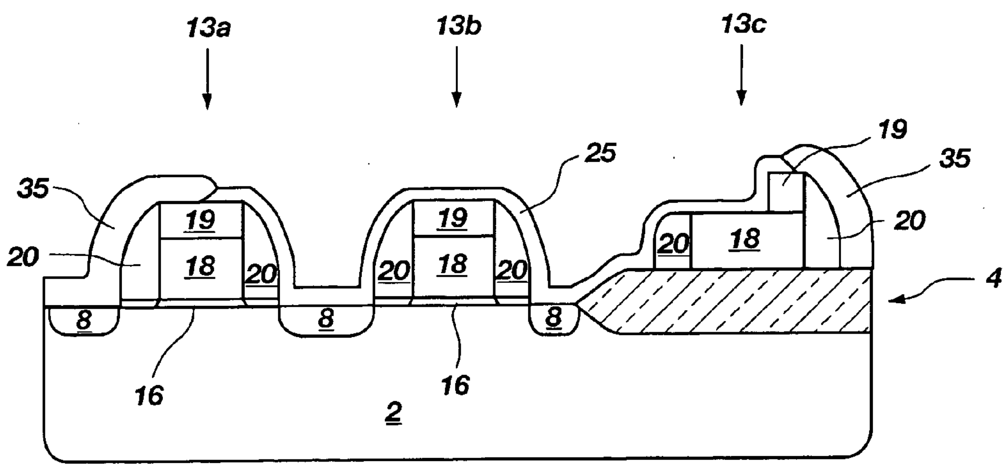
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Fig. 6

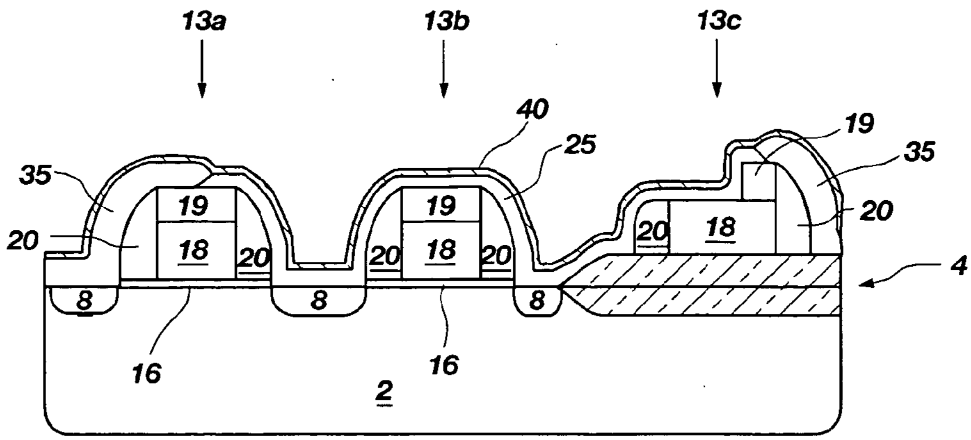
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Fig. 7a

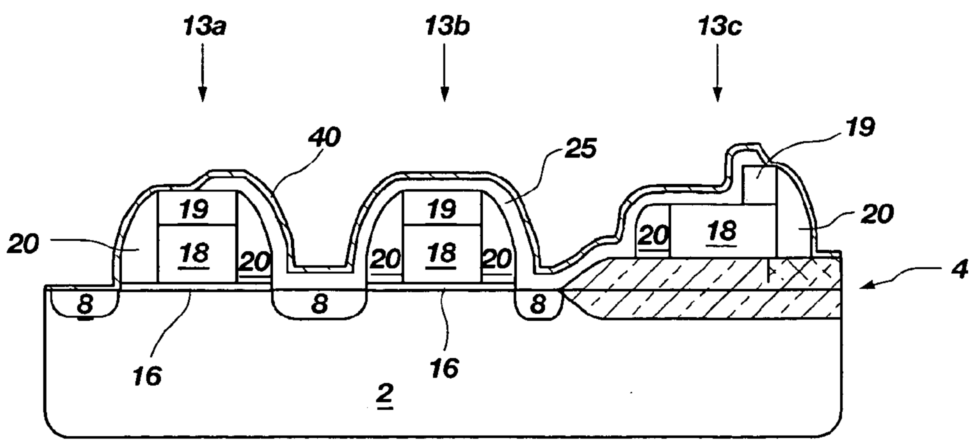
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Fig. 7b

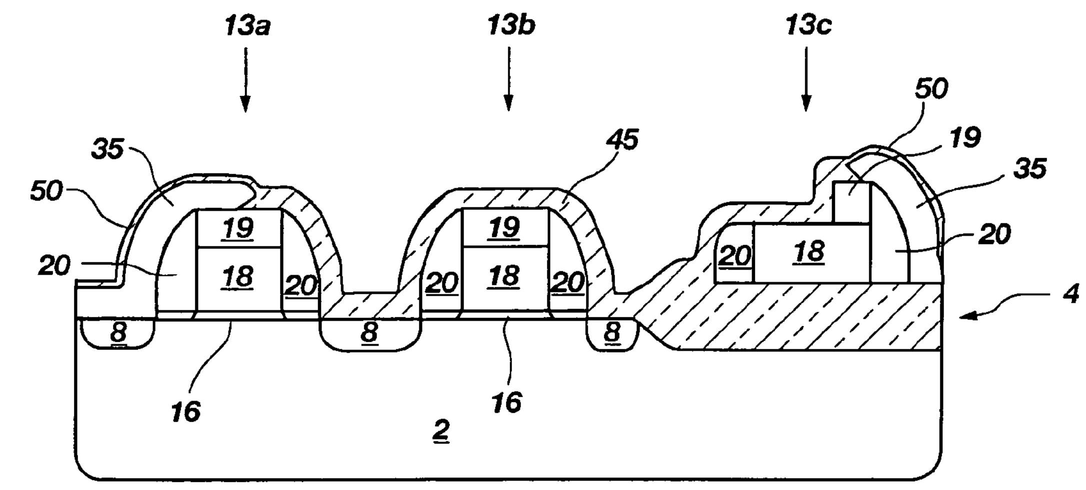
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Fig. 8a

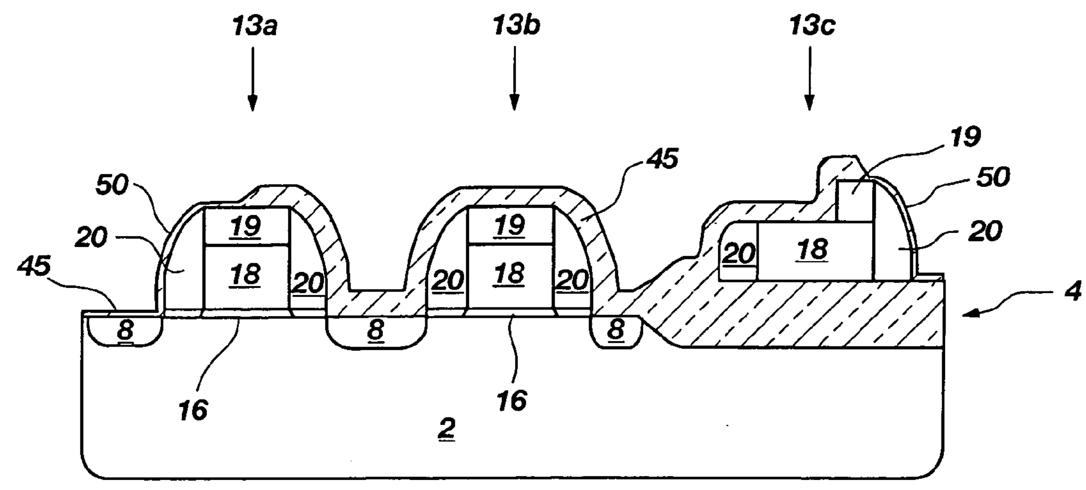
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Fig. 8b

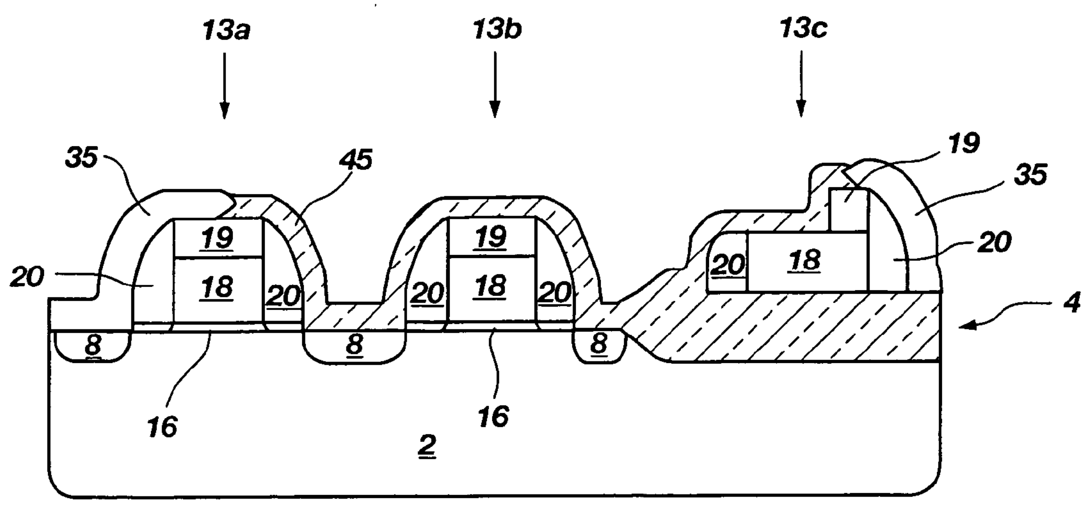

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Fig. 9a

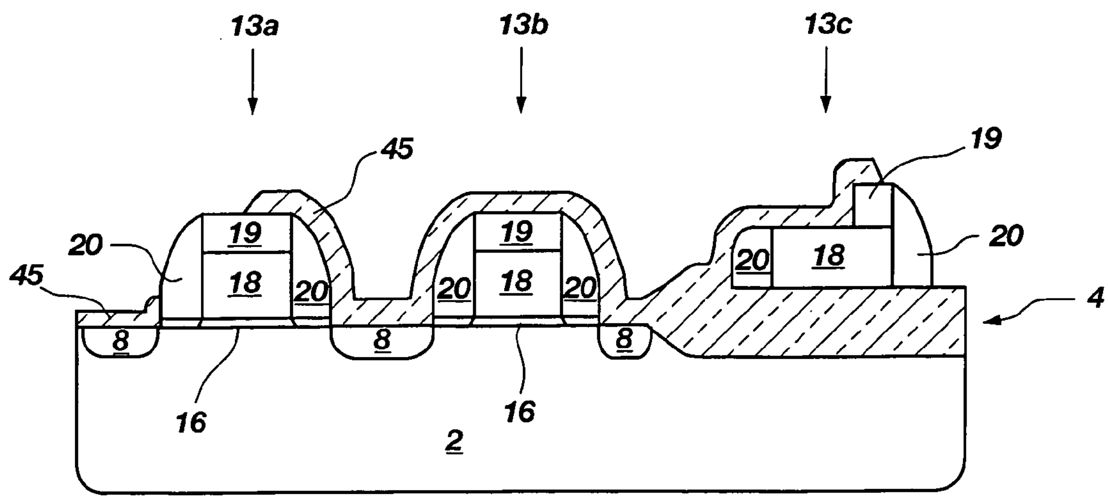

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Fig. 9b

SEMICONDUCTOR DEVICE STRUCTURES INCLUDING METAL SILICIDE INTERCONNECTS AND DIELECTRIC LAYERS AT SUBSTANTIALLY THE SAME FABRICATION LEVEL

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of application Ser. No. 09/795,746, filed Feb. 28, 2001, pending, which is a divisional of application Ser. No. 09/291,762, filed Apr. 14, 1999, now U.S. Pat. No. 6,429,124, issued Aug. 6, 2002.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates generally to the field of integrated circuit design and fabrication. Specifically, the invention relates to methods for making local interconnect structures for integrated circuits and the structures formed thereby.

[0004] 2. Background of Related Art

[0005] Integrated circuits (ICs) contain individual active and passive devices which are interconnected during fabrication by an intricate network of conductive material. The quality of these inter-device interconnections often affects the performance and reliability of the overall IC device.

[0006] Local interconnects, unlike other interconnects such as multi-level interconnects, electrically connect the individual devices of the overall IC device at a level or levels below customary metallization levels. For example, local interconnects connect gates and emitters to diffusion areas and N+ and P+ regions across field oxide regions. See T. Tang et al., *Titanium Nitride Local Interconnect Technology for VLSI*, IEEE Trans. Electron Devices, Vol. ED-34, 3 (1987) p. 682, the disclosure of which is incorporated herein by reference.

[0007] Several materials have been employed in local interconnects, such as titanium nitride, refractory metals, and titanium silicide ($TiSi_x$). $TiSi_x$ has been used frequently as a local interconnect material because of its low resistance and high conductivity. Methods for fabricating local interconnects, such as $TiSi_x$ local interconnects, include those described in U.S. Pat. Nos. 4,975,756, 5,589,415, 5,605,853, and 5,612,243, the disclosures of which are incorporated herein by reference.

[0008] U.S. Pat. No. 5,483,104, the disclosure of which is incorporated herein by reference, discloses a method for fabricating $TiSi_x$ local interconnects. Silicided regions, which protect source and drain regions from an overlying local interconnect, are formed by depositing titanium (Ti) on a silicon (Si) substrate and annealing the titanium to the silicon in a nitrogen atmosphere. The local interconnect structure is then formed on the silicide regions by depositing a doped polysilicon layer, sputtering titanium on the polysilicon, and annealing in a nitrogen atmosphere. Such a technique, however, often results in poor contact between the silicided active area and the silicided local interconnect if the polysilicon deposition is not very well controlled.

[0009] Another method for manufacturing $TiSi_x$ local interconnects is disclosed in U.S. Pat. No. 5,496,750 ("the '750 patent"), the disclosure of which is incorporated herein by reference. The '750 patent describes a method for fabricating elevated source/drain junction metal-on-silicon field effect transistors (MOSFETs) extending from gate sidewalls to isolation structures surrounding the FET gate area. Unfortunately, the method described in the '750 patent is limited because the method disclosed therein does not include the fabrication of a flexible local interconnect structure.

[0010] Using titanium silicide as a local interconnect can result in several problems, as explained in U.S. Pat. No. 5,341,016, the disclosure of which is incorporated herein by reference. One problem is that titanium silicide severely agglomerates when exposed to temperatures greater than 850° C. Agglomeration can increase both silicided source/drain and polycide sheet resistance and lead to excessive leakage and/or gate oxide degradation. Another problem with titanium silicide is unwanted dopant segregation, which can reduce the minority carrier lifetime during device operation and cause contact resistance problems.

[0011] A particular problem with $TiSi_x$ local interconnects has been poor step coverage. Conventionally, in forming the local interconnect, Ti has been deposited first, followed by physical vapor deposition (PVD) of silicon. PVD silicon, however, suffers from poor step coverage. This poor step coverage often detracts from the quality of the semiconductor device.

SUMMARY OF THE INVENTION

[0012] The present invention relates to a method for selectively fabricating a flexible metal silicide local interconnect over gates or other structures of a semiconductor device. The method of the present invention includes forming at least one gate structure on a substrate, disposing an amorphous or polycrystalline silicon layer on the substrate, disposing a layer of silicon nitride (SiN) over the silicon layer, removing a portion of the silicon nitride layer, oxidizing the exposed portion of the silicon layer, removing the remaining portion of the silicon nitride layer, optionally removing the oxidized silicon layer, forming a metal layer over the resulting structure, annealing the metal layer in an atmosphere comprising nitrogen, and removing any metal nitride regions. Preferably, the silicon layer is formed on the substrate and the at least one gate structure. In removing the portion of the silicon nitride layer, a remaining portion is preferably left overlying the at least one gate structure. More preferably, the method leaves a local interconnect layer overlying the at least one gate structure.

[0013] The present invention provides at least one advantage when compared to conventional local interconnect fabrication methods, in that the present invention forms $TiSi_x$ local interconnects with good step coverage because the silicon forming the interconnects is deposited via chemical vapor deposition (CVD).

[0014] Other features and advantages of the present invention will become apparent to those of skill in the art through consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0015] Certain aspects of the present invention are illustrated by the accompanying drawings in which:

[0016] **FIGS. 1-9** illustrate cross-sectional views of a process of forming local interconnects, and the resulting structure, according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] This invention provides a flexible metal silicide local interconnect for integrated circuit and semiconductor devices. In particular, the present invention provides a process for forming a flexible local interconnect structure. As used in the context of the present invention, the term "flexible" means that the method of the present invention can be employed to make a local interconnect structure that contacts any desired active device region, or active region, of the semiconductor device and that traverses over gates or other structures of the semiconductor device.

[0018] The local interconnects of the present invention can be used in CMOS logic devices and are especially suitable for SRAM devices. The local interconnects and methods of fabrication described below exemplify the inventive process and structure in a CMOS logic device. However, the inventive process and structure as disclosed may be modified to be included in any desired device.

[0019] The following description provides specific details, such as material thicknesses and types, in order to provide a thorough understanding of the present invention. The skilled artisan, however, will understand that the present invention may be practiced without employing these specific details. Indeed, the present invention can be practiced in conjunction with fabrication techniques conventionally used in the industry.

[0020] The process steps and structures described below do not form a complete process flow for manufacturing IC devices, the remainder of which is known to those of ordinary skill in the art. Accordingly, only the process steps and structures necessary to understand the present invention are described.

[0021] As shown in **FIG. 1**, device isolation regions **4** are first formed in substrate **2**. Substrate **2** may be any surface suitable for device formation, such as a semiconductor wafer, and may be doped and/or include an epitaxial layer. Preferably, substrate **2** is a silicon wafer or a bulk silicon region, such as a silicon-on-insulator or silicon-on-sapphire structure. Impurities comprising atoms of one conductivity type (e.g., P-type) may optionally be incorporated into the substrate. Device isolation regions **4** are illustrated in **FIG. 1** as field oxide regions, but the present invention can be practiced using other isolation technologies, such as trench-and-refill isolation regions.

[0022] A thin dielectric layer is then formed over substrate **2**. This dielectric layer comprises any dielectric material used in semiconductor device fabrication. Examples of such dielectric materials include silicon oxide, silicon nitride, silicon oxynitride, silicon oxide containing dopants such as B or P, organic dielectrics, or a layered dielectric film of these materials. Preferably, this dielectric layer is silicon oxide. This dielectric layer may be formed by any suitable manufacturing method, such as a thermal reaction or vapor deposition process.

[0023] Next, a conductive layer is deposited. Since this conductive layer will form the gate electrode, any suitable gate electrode material may be employed. Preferably, the conductive layer is a doped polysilicon layer. Optionally, a second dielectric layer is formed over this conductive layer. This second dielectric layer may comprise any dielectric material used in IC device fabrication, such as those listed above. This second dielectric layer preferably comprises silicon oxide or silicon nitride. More preferably, this second dielectric layer is silicon oxide.

[0024] The conductive layer, dielectric layer, and second dielectric layer (if present) are then patterned and etched, as illustrated in **FIG. 1**, to form gate structures **13***a*, **13***b*, and **13***c*. The gate structures contain gate dielectric **16**, gate electrode **18**, and, if desired, second gate dielectric **19**. Gate structures **13***a*, **13***b*, and **13***c* can be formed by any suitable pattern and etch process, preferably using substrate **2** as an etch stop.

[0025] Sidewall dielectric spacers **20** on the gate structures are then formed. Spacers **20** may be formed by depositing a dielectric layer overall and etching the dielectric layer to leave substantially vertical sidewall dielectric spacers **20**. Preferably, this dielectric layer comprises silicon oxide or silicon nitride. More preferably, this dielectric layer is silicon oxide.

[0026] Diffusion regions **8**, such as source/drain regions, are then formed in substrate **2**. Diffusion regions **8** can be formed by implanting a suitable dopant, such as B, As, or P, at an energy and dose sufficient, optionally through a dielectric layer, to form the desired dopant concentration. Diffusion regions **8** may be created by ion implanting a high concentration of dopant atoms into substrate **2** to form doped regions which are aligned to the edge of the dielectric spacers **20**. Dielectric spacers **20** can optionally be removed and a second implant performed to form doped regions which are aligned with the gate structures. An optional diffusion step may be employed to drive in the dopants.

[0027] Gate contacts, if desired, are then formed. Gate contacts are formed by removing a portion of second gate dielectric **19**, if present, to expose the gate electrode **18**. This removal can be performed by patterning and etching the second gate dielectric. For example, the pattern and etch may proceed by coating substrate **2** with a first photoresist to planarize the wafer and then baking the first photoresist. The first photoresist is then blanket etched until second gate dielectric **19** is exposed. An isolation mask is then used to isolate second gate dielectric **19**. An etch is then conducted to remove the desired portion of the second gate dielectric **19** and expose gate electrode **18**, as shown with respect to gate structure **13***c*.

[0028] As shown in **FIG. 2**, a layer **25** of amorphous or polycrystalline silicon is deposited or otherwise formed on substrate **2** and gate structures **13***a*, **13***b* and **13***c*. Preferably, silicon layer **25** is polycrystalline silicon (poly-silicon). The thickness of silicon layer **25** may range from about 300 to about 600 Å, and should be selected considering the device characteristics and processing requirements. For example, the silicon layer **25** thickness should be selected so that the

$TiSi_x$ or $CoSi_2$ or any other silicide interconnect forms through the original interface between the deposited silicon and the underlying active areas. Preferably, the thickness of the layer of silicon facilitates the fabrication of a substantially confluent metal silicide layer. Silicon layer **25** may be deposited by any IC device fabrication process yielding the desired chemical and physical characteristics, such as a highly conformal or a partially conformal deposition process. Exemplary processes include a PVD process, such as evaporation or sputtering, or a CVD process. Preferably, silicon layer **25** is deposited by any CVD process yielding good step coverage.

[**0029**] Silicon layer **25**, especially when it is poly-silicon, may be optionally doped. The dopant may be ion implanted at a dose and energy sufficient to obtain the desired concentration. Any dopant can be employed, such as As, P, or B.

[**0030**] As illustrated in **FIG. 3**, silicon nitride layer **30** is then deposited or otherwise formed over silicon layer **25**. Silicon nitride layer **30** can be deposited by any fabrication method yielding the desired physical and chemical characteristics, such as a CVD or PVD process. Preferably, silicon nitride is deposited using a CVD low-pressure chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition (PECVD). The thickness of the silicon nitride layer may range from about 100 Å to about 400 Å, and should be selected considering the device characteristics and processing requirements.

[**0031**] As depicted in **FIG. 4**, a portion of silicon nitride layer **30** is then removed, the portion of silicon nitride layer **30** remaining on silicon layer **25** overlying those portions of the device on which the silicide local interconnect will be formed. Removal of portions of silicon nitride layer **30** is preferably performed by a photolithographic patterning and etch process using photoresist layer **32**, followed by a dry etch of the silicon nitride.

[**0032**] As illustrated in **FIG. 4**, removing portions of silicon nitride layer **30** will expose underlying regions of silicon layer **25**. These exposed regions are then oxidized to form silicon oxide layer **35**, as shown in **FIG. 5**, which is located at the same fabrication elevation, or level, as adjacent, remaining portions of silicon layer **25**. Any oxidation process can be employed to oxidize the exposed portions of silicon layer **25**, provided it yields a silicon oxide layer **35** with the desired physical and chemical characteristics. Preferably, the oxidation process is thermal oxidation in an atmosphere containing oxygen or steam at a temperature of from approximately 700° C. to 1000° C. for approximately 1 to 30 minutes. Silicon nitride layer **30** serves as an oxidation mask and prevents undesired oxide growth on the portions of silicon layer **25** covered thereby.

[**0033**] As shown in **FIG. 6**, the remaining portion of silicon nitride layer **30** is then removed. Any removal process can be employed, provided it neither removes silicon oxide layer **35** nor degrades silicon layer **25**. This removal process can be accomplished using a plasma etch or wet strip chemistry using silicon layer **25** as an etch stop. Preferably, the remaining portions of silicon nitride layer **30** are removed using a wet etch solution comprising hot phosphoric acid.

[**0034**] Silicon oxide layer **35** can then be removed, if desired. Whether silicon oxide layer **35** is removed depends on whether the silicon regions underlying the silicon oxide layer **35** will be silicided. For example, as explained below, if silicided diffusion regions **8** are not desired, silicon oxide layer **35** is not removed. Conversely, if silicided diffusion regions **8** are desired, silicon oxide layer **35** is removed. Any suitable fabrication process can be employed to remove the silicon oxide, provided it does not degrade either silicon layer **25** or silicon regions underlying silicon oxide layer **35**. For example, this removal process can be accomplished using a plasma etch or wet strip chemistry. Preferably, the silicon oxide layer is removed using a wet etch solution comprising hydrofluoric acid (HF).

[**0035**] As shown in **FIG. 7*a*** (in an embodiment where silicon oxide layer **35** remains) and **FIG. 7*b*** (in an embodiment where silicon oxide layer **35** has been removed), metal layer **40** is deposited over the surface of the semiconductor device. Metal layer **40** may be formed by any fabrication process imparting the necessary characteristics to the layer, such as a PVD or CVD process. Preferably, metal layer **40** is formed by a sputtering process, such as sputter deposition in an Ar atmosphere.

[**0036**] The metal layer may comprise any metal or material which forms a silicide when alloyed with silicon, such as a refractory metal. Preferably, the metal is Co, Ta, or Ti. More preferably, the refractory metal layer is Ti. The thickness of the metal layer should be proportional to the thickness of the silicon layer. The thickness of the layer of metal should be sufficient to substantially completely consume the silicon as the metal and silicon are annealed. For example, if Ti is employed as the metal, the thickness of the layer of Ti should be about half of the thickness of the layer of silicon to substantially completely consume the silicon layer. The thickness of the metal layer should also be sufficient to facilitate the fabrication of a substantially confluent metal silicide layer during the annealing of the metal to the silicon. Preferably, the thickness should range from about 200 to about 400 Å.

[**0037**] As depicted in **FIG. 8*a*** (in an embodiment where silicon oxide layer **35** remains) and **FIG. 8*b*** (in an embodiment where silicon oxide layer **35** has been removed), metal layer **40** is then converted to silicide interconnect **45** and metal nitride layer **50**. Preferably, this conversion is performed by annealing in a nitrogen-containing atmosphere. The annealing initiates a chemical reaction between the metal layer and the underlying silicon and between the metal and the nitrogen ambient. A metal silicide layer forms in the regions where the metal contacts silicon, thereby yielding silicide interconnect **45**. Metal nitride layer **50** forms in the regions where the metal contacts an insulating or dielectric material.

[**0038**] The annealing process is performed in a nitrogen-containing atmosphere for a time and a temperature sufficient to react metal layer **40** and silicon layer **25** and form a silicide; thus, silicide interconnect **45** is located at substantially the same fabrication elevation, or level, as that at which silicon layer **25** was previously located and, in **FIG. 8*a***, where silicon oxide layer **35** remains, at substantially the same fabrication elevation, or level, as silicon oxide layer **35**. Preferably, the temperature ranges from about 600 to about 750° C. and the time ranges from about 20 seconds to about 10 minutes.

[**0039**] The nitrogen-containing atmosphere may comprise a gas or a mixture of gases providing nitrogen for the annealing atmosphere, yet not adversely influencing conversion of the metal layer. Examples of such gases include nitrogen, ammonia, or a mixture thereof. Preferably, the nitrogen-containing atmosphere contains substantially pure nitrogen. The annealing atmosphere may also contain other gases, such as argon or hydrogen.

[**0040**] This conversion process should proceed until a metal silicide forms through the original interface between silicon layer **25** and underlying substrate **2**. The time and temperature of the annealing process, as well as the thickness of silicon layer **25**, must therefore be selected carefully.

[**0041**] Metal nitride layer **50** is then removed to obtain the structures shown in **FIG. 9***a* (in an embodiment where silicon oxide layer **35** remains) and **FIG. 9***b* (in an embodiment where silicon oxide layer **35** has been removed). Any process for removing the metal nitride layer **50** without removing or adversely affecting silicide interconnect **45** may be employed. A wet etch solution containing H_2O, H_2O_2, and NH_4OH can be used to remove the metal nitride layer **50** without etching away the silicide interconnect **45**.

[**0042**] After removing the metal nitride layer **50**, subsequent processing may be undertaken to form the desired semiconductor device. For example, a high temperature anneal may be performed to reduce the silicide interconnect sheet resistivity. Additionally, a dielectric layer could be deposited, contact holes formed in the dielectric layer, and a patterned metal layer formed to achieve a desired pattern of electrical interconnections.

[**0043**] While the preferred embodiments of the present invention have been described above, the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

What is claimed is:

1. A semiconductor device structure, comprising:

at least one active device region;

at least one transistor gate structure positioned laterally adjacent to the at least one active device region; and

an interconnect comprising a layer including metal silicide and positioned to directly contact the at least one active device region; and

a film comprising dielectric material at substantially the same fabrication level of the semiconductor device structure as the interconnect.

2. The semiconductor device structure of claim 1, wherein the interconnect is positioned to extend at least partially over the at least one transistor gate structure.

3. The semiconductor device structure of claim 2, wherein the interconnect is also positioned to extend substantially over another transistor gate structure of the semiconductor device structure.

4. The semiconductor device structure of claim 1, wherein the metal silicide comprises titanium silicide, tantalum silicide, or cobalt silicide.

5. The semiconductor device structure of claim 1, wherein the metal silicide comprises titanium silicide.

6. The semiconductor device structure of claim 1, wherein the at least one active device region comprises an n-well.

7. The semiconductor device structure of claim 1, wherein the film comprising dielectric material comprises a silicon oxide.

8. The semiconductor device structure of claim 1, further comprising:

a film comprising a metal nitride over at least portions of the film comprising dielectric material.

9. A semiconductor device structure, comprising:

a substrate comprising semiconductor material;

at least one structure positioned adjacent to an active surface of the substrate;

an interconnect comprising a layer including metal silicide located over the active surface and adjacent to the at least one structure; and

a film comprising dielectric material at substantially the same fabrication level of the semiconductor device structure as the interconnect.

10. The semiconductor device structure of claim 9, further comprising:

at least one active device region within the semiconductor material.

11. The semiconductor device structure of claim 10, wherein the interconnect contacts the at least one active device region.

12. The semiconductor device structure of claim 10, wherein the at least one active device region comprises an n-well.

13. The semiconductor device structure of claim 9, wherein the at least one structure comprises a transistor gate structure.

14. The semiconductor device structure of claim 13, wherein the dielectric material comprises at least a side wall of the transistor gate structure.

15. The semiconductor device structure of claim 9, wherein the dielectric material comprises at least one of a silicon oxide and a silicon nitride.

16. The semiconductor device structure of claim 9, wherein the metal silicide comprises a refractory metal silicide.

17. The semiconductor device structure of claim 16, wherein the refractory metal silicide comprises titanium silicide, tantalum silicide, or cobalt silicide.

18. The semiconductor device structure of claim 9, wherein the metal silicide comprises titanium silicide.

19. The semiconductor device structure of claim 9, wherein at least a portion of the interconnect is located adjacent to the dielectric material of the at least one structure.

20. The semiconductor device structure of claim 19, wherein the dielectric material of the at least one structure comprises at least one of a silicon oxide and a silicon nitride.

* * * * *