

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization

International Bureau



(10) International Publication Number

WO 2013/024404 A2

(43) International Publication Date
21 February 2013 (21.02.2013)

(51) International Patent Classification:
H04B 5/00 (2006.01) *H02J 17/00* (2006.01)

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(21) International Application Number:
PCT/IB2012/054057

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(22) International Filing Date:
9 August 2012 (09.08.2012)

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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Published:

— without international search report and to be republished upon receipt of that report (Rule 48.2(g))

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WO 2013/024404 A2

(54) Title: A CONDUCTIVE LAYER OF A LARGE SURFACE FOR DISTRIBUTION OF POWER USING CAPACITIVE POWER TRANSFER

(57) Abstract: An apparatus (300) for supplying power to a load in a capacitive power transfer system comprises a power generator (350) operating at a first frequency; a transmitter comprising a plurality of first electrodes (310) connected to a first terminal of the power generator (350) and a plurality of second electrodes (320) connected to a second terminal of the power generator (350) of a transmitter portion of the apparatus (300); and a plurality of inductors (340), wherein each inductor of the plurality of inductors is connected between a pair of a first electrode and a second electrode of the plurality of first and second electrodes, wherein each inductor comprises, together with a parasitic capacitor (330) formed between each pair of the first electrode and the second electrode, a resonant circuit at the first frequency in order to compensate for current loss due to parasitic capacitances.

A CONDUCTIVE LAYER OF A LARGE SURFACE FOR DISTRIBUTION OF POWER USING CAPACITIVE POWER TRANSFER

5 This application claims the benefit of US provisional patent application No. 61/523,948 and US provisional application No. 61/523,964, both filed on August 16, 2011, and US provisional application No. 61/671,855, filed July 16, 2012.

10 The invention generally relates to capacitive power transfer and, more particularly, to parasitic capacitance when using large surfaces for power distribution using capacitive power transfer.

A wireless power transfer refers to supplying electrical power without any wires or contacts, whereby the powering of electronic devices is performed through a wireless medium. One popular application for contactless powering is for charging portable electronic devices, e.g., mobile phones, laptop computers, and the like.

15 One implementation of wireless power transfers is by an inductive powering system. In such a system, the electromagnetic inductance between a power source (transmitter) and the device (receiver) allows for contactless power transfers. Both the transmitter and receiver are fitted with electrical coils, and when brought into physical proximity, an electrical signal flows from the transmitter to the receiver by a generated magnetic field.

20 In inductive powering systems, the generated magnetic field is concentrated within the coils. As a result, the power transfer to the receiver pick-up field is very concentrated in space. This phenomenon creates hot-spots in the system which limits the efficiency of the system. To improve the efficiency of the power transfer, a high quality factor for each coil is needed. To this end, the coil should be characterized with an optimal ratio of an inductance to 25 resistance, be composed of materials with low resistance, and be fabricated using a Litze-wire process to reduce skin-effect. Moreover, the coils should be designed to meet complicated geometries to avoid Eddy-currents. Therefore, expensive coils are required for efficient inductive powering systems. A design for a contactless power transfer system for large areas would necessitate many expensive coils, and thus for such applications an inductive powering system 30 may not be feasible.

Capacitive coupling is another technique for transferring power wirelessly. This technique is predominantly utilized in data transfer and sensing applications. A car-radio antenna

glued on the window with a pick-up element inside the car is an example of a capacitive coupling. The capacitive coupling technique is also utilized for contactless charging of electronic devices. For such applications, the charging unit (implementing the capacitive coupling) operates at frequencies outside the inherent resonance frequency of the device. In the related art, a

5 capacitive power transfer circuit that enables LED lighting is also discussed. The circuit is based on an inductor in the power source (driver). As such, only a single receiver can be used and the transmitter frequency should be tuned to transfer the maximum power. In addition, such a circuit requires pixelated electrodes which ensure power transfer between the receiver and transmitter when they are not perfectly aligned. However, increasing the number of the pixelated electrodes

10 increases the number of connections to the electrodes, thereby increasing the power losses. Thus, when having only a single receiver and limited size electrodes, the capacitive power transfer circuits discussed in the related art cannot supply power over a large area, e.g., windows, walls, and so on. In addition, providing power over large surface areas poses several challenges. For example, a typical user would desire power from any arbitrary position over a large surface area.

15 Moreover, when large surface areas are used for capacitive power transfer there are various parasitic capacitances that impact the performance of the system.

Therefore, it would be advantageous to provide a low cost and feasible capacitive power transfer system for wireless power applications over large surface areas, while reducing the impact of parasitic capacitance appearing in such a capacitive power transfer system.

20 Certain embodiments disclosed herein include an apparatus for supplying power to a load of a capacitive power transfer system. The apparatus comprises a power generator operating at a first frequency; a transmitter comprising a plurality of first electrodes connected to a first terminal of the power generator and a plurality of second electrodes connected to a second terminal of the power generator of a transmitter portion of the apparatus; and a plurality of inductors, wherein each inductor of the plurality of inductors is connected between a pair of a first electrode and a second electrode of the plurality of first and second electrodes, wherein each inductor comprises together with a parasitic capacitor formed between each pair of the first electrode and the second electrode a resonant circuit at the first frequency in order to compensate for current loss due to parasitic capacitances.

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30 Certain embodiments disclosed herein also include a circuit for reducing common mode (CM) currents in a capacitive power transfer system. The circuit comprises a first terminal

connected to a first transmitter electrode of the capacitive power transfer system, wherein the first transmitter electrode forms a first parasitic capacitor to a protected earth connected to an earth ground; a second terminal connected to a second transmitter electrode of the capacitive power transfer system, wherein the second transmitter electrode forms a second parasitic

5 capacitor to the PE; and wherein the circuit generates a first periodic voltage signal between the first terminal and the earth ground, the circuit further generates a second periodic voltage signal between the second terminal and the earth ground, wherein at least an amplitude of each of the first periodic voltage signal and the second periodic voltage signal is controlled to essentially offset the common mode (CM) current flowing through the first parasitic capacitor and the

10 second parasitic capacitor.

The subject matter that is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other features and advantages of the invention will be apparent from the following detailed description taken in conjunction with the accompanying drawings.

15

Figure 1 shows a capacitive power transfer system according to an embodiment;

Figure 2 shows an electric diagram of the capacitive power transfer system implemented according to an embodiment;

20 Figure 3 shows a schematic diagram of a capacitive power transmission grid with parasitic capacity compensation, without a load;

Figure 4 shows a schematic diagram of a capacitive power transmission grid with parasitic capacity compensation, with a load;

Figure 5 is a schematic diagram of a capacitive power transfer system equipped with a current compensation circuit designed to eliminate common mode current paths according to one embodiment;

25 Figure 6 is an electric diagram of a capacitive power transfer system equipped with the current compensation circuit depicted in Fig. 5;

Figure 7 is a timing diagram for controlling the switches of the current compensation circuit depicted in Fig. 5 according to one embodiment;

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Figure 8 is a wall covering having a backside covered with vertical conductive stripes with a bottom segment detailing electrical connections thereto;

5 Figure 9 is a wall covering having a backside covered with horizontal conductive stripes and vertical connecting lines;

Figure 10 is a view of an electrical connection of a plurality of segments with integrated connections and connectors; and

Figure 11 is a schematic drawing of a rectifier used in the power transfer system of Fig. 5

10 Figures 12A, 12B, and 12C depict the operation of the current compensation circuit according to various embodiments.

It is important to note that the embodiments disclosed herein are only examples of the many advantageous uses of the innovative teachings herein. In general, statements made in 15 the specification of the present application do not necessarily limit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others. In general, unless otherwise indicated, singular elements may be in plural and vice versa with no loss of generality. In the drawings, like numerals refer to like parts through several views.

Fig. 1 shows an exemplary and non-limiting schematic diagram of a capacitive 20 power system 100 utilized to describe various embodiments disclosed herein. The system 100 enables power transmissions over large areas. The system 100 can be installed in places where open electrical contacts are not preferred or are not desirable, such as bathrooms, retail-shops where regular variations are needed to illuminate a product(s), furniture, and the like. The system 100 can transfer power over a large area, such that the system 100 can be utilized to power 25 devices mounted on walls, windows, mirrors, floors, seats, aisles, and so on.

The system 100 includes a driver 110 connected to a pair of transmitter electrodes 121 and 122 which are attached to an insulating layer 130. The system 100 also includes a pair of receiver electrodes 141 and 142 connected to a load 150 and an inductor 160. Optionally, the system 100 may include an inductor 112 coupled to the driver 110. The connection between the 30 transmitter electrodes 121,122 to the driver 110 is by means of a galvanic contact or a capacitive in-coupling.

A power signal is supplied to the load 150 by placing the receiver electrodes 141, 142 in proximity to the transmitter electrodes 121, 122 without having a direct contact between the two. Thus, neither a mechanical connector nor any electrical contact is required in order to power the load 150. The load 150 may be, but is not limited to, lighting elements (e.g., LED, 5 LED string, a lamp, etc.), organic light emitting diode (OLED) surfaces, displays, computers, power chargers, loudspeakers, and the like.

The driver 110 outputs an AC voltage signal having a frequency that substantially matches the series-resonance frequency of a circuit consisting of a series of the capacitors and inductors 112, 160. The capacitors – shown in dotted lines in Fig. 1 and labeled as C1 and C2 – 10 are the capacitive impedance of the transmitter electrodes 121, 122 and receiver electrodes 141, 142. The impedances of the capacitors C1, C2 and inductor 160, and optionally inductor 112, cancel each other at the resonance frequency, resulting in a low-ohmic circuit. Thus, the system 100 is capable of delivering power to the load 150 with very low power losses.

An electric diagram 200 of the system 100 is provided in Fig. 2. The maximum 15 power is obtained when the frequency of the power signal U_{gen} is close to the series-resonance of the circuit comprised of the load R_L , the resistor R_S (representing the inductor resistance) capacitors C₁ and C₂, and inductor L_S. The series-resonance is determined by the values of the capacitors C₁, C₂ and inductor L_S. The values of the capacitors C₁, C₂ and inductor L_S are 20 selected such that they cancel each other at the operating frequency of the signal U_{gen} . Therefore, only the series resistance of the inductor R_S and the connectivity of the electrodes limit the power transfer. It should be appreciated that this allows transferring AC signals characterized by high power with low frequency signals.

Referring back to Fig. 1, the driver 110 generates an AC signal of which 25 amplitude, frequency, and waveform can be controlled. The output signal typically has an amplitude of tens of volts and a frequency of up to a few Mega Hertz (MHz). Frequency tuning between the generated signal and the series-resonance is performed by changing the frequency, phase, or duty cycle of the signal output by the driver 110. Alternatively, the frequency tuning is achieved by changing the capacitance or inductive values of the circuit connected to the driver 110.

The insulating layer 130 is a thin layer substrate material that can be of any 30 insulating material, including for example, air, paper, wood, textile, glass, DI-water, and so on.

Preferably, a material with dielectric permittivity is selected. The thickness of the insulating layer 130 is typically between 10 microns (e.g., a paint layer) and a few millimeters (e.g., a glass layer).

The transmitter electrodes 121, 122 are comprised of two separate bodies of conductive material placed on one side of the insulating layer 130 that is not adjacent to the receiver electrodes 141, 142. For example, as illustrated in Fig. 1, the transmitter electrodes 121, 122 are at the bottom of the insulating layer 130. In another embodiment, the transmitter electrodes 121, 122 can be placed on opposite sides of the insulating layer 130. The transmitter electrodes 121, 122 can be any shape including, for example, a rectangle, a circle, a square, or combinations thereof. The conductive material of each transmitter electrode may be, for example, carbon, aluminum, indium tin oxide (ITO), organic material, such as Poly(3,4-ethylenedioxythiophene (PEDOT), copper, silver, conducting paint, or any conductive material.

The receiver electrodes 141, 142 can be of the same conductive material as the transmitter electrodes 121, 122 or made of different conductive material. The total capacitance of the system 100 is formed by the overlapping areas of respective transmitter and receiver electrodes 121, 141, and 122, 142, as well as the thickness and material properties of the insulating layer 130. The capacitance of the system 100 is illustrated as C1 and C2 in Fig. 1. In order to allow electrical resonance, the system 100 should also include an inductive element. This element may be in a form of one or more inductors that are part of the transmitter electrodes or the receiver electrodes, distributed over the driver 110 and the load (e.g., inductors 160 and 112 shown in Fig. 1), inductors incorporated within insulating layer 130, or any combination thereof. In an embodiment, an inductor utilized in the system 100 can be in a form of a lumped coil.

The load 150 allows for an AC bi-directional current flow. In an embodiment, the load 150 may include a diode or an AC/DC converter to locally generate a DC voltage. The load 150 may further include electronics for controlling or programming various functions of the load 150 based on a control signal generated by the driver 110. To this end, in an embodiment, the driver 110 generates a control signal that is modulated on the AC power signal. For example, if the load 150 is a LED lamp, a control signal output by the driver 110 may be utilized for dimming or color setting of the LED lamp.

The capacitive power system 100, as exemplary illustrated in Fig. 1, depicts a single load 150 that is powered by the driver 110. However, it should be noted that the driver 110 can also power multiple loads, each of which may be tuned to a different operational frequency. Alternatively, the multiple loads may be tuned to the same operational frequency.

5 Fig. 3 depicts an exemplary and non-limiting schematic diagram of a capacitive power transmission grid 300 with parasitic capacitance compensation without a load. The construction of such exemplary and non-limiting embodiments of capacitive power transmission grids is discussed with respect to Figs. 8 through 10 herein below. In Fig. 3 the transmitter portion is illustrated as comprising a power generator 350 and a plurality of transmitter electrodes 310, 320 that form the transmitter-side plates of the capacitors C_1 and C_2 , respectively, as shown in Fig. 2. However, when the transmitter electrodes 310 and 320 are large, then parasitic capacitance C_p 330 appears between the transmitter electrodes 310 and 320. The transmitter electrodes 310 and 320 are part of transmitter modules 301. This parasitic capacitance C_p 330 impacts the performance of the capacitive power transfer system. To compensate for the 10 parasitic capacitance C_p 330, an inductor L_c 340 is connected in parallel to the transmitter electrodes 310 and 320. The value for the inductor L_c 340 is selected such that it forms a parallel resonant circuit with the parasitic capacitance C_p 330, which is in resonance at the operating frequency of the power generator 350. As a result, the current through the inductor 340 cancels 15 out the capacitive current of the parasitic capacitance C_p 330, such that the current is negligible parasitic capacitance C_p 330, such that the current is negligible outside the transmitter module.

20

According to one embodiment, each transmitter module 301 comprises, for example, two electrodes 310 and 320 and a compensating inductor 340, whereby the compensated transmitter module 301 does not cause additional loading on the generator 350. A person of ordinary skill in the art readily appreciates that this embodiment reduces the idle 25 current that would otherwise be present in these kinds of capacitive power transfer systems. In a further embodiment the compensating inductor L_c 340 may be a variable inductor that can be adjusted to a necessary value to compensate for a specific and unpredictable parasitic capacitance C_p 330.

Fig. 4 shows an exemplary and non-limiting schematic diagram 400 of a 30 capacitive power transmission grid with parasitic capacitance compensation and a load. A receiver module 410 is capacitively coupled to the two electrodes (a transmitter module 301 of

Fig. 3) of the capacitive power transfer grid 300, as represented by the coupling capacitors C_1 and C_2 . Preferably, the receiver 410 comprises a matching inductor (L_{res}) 411 that forms a series resonant circuit together with the coupling capacitors C_1 and C_2 , which is in resonance at an operating frequency of the power generator 350 of the capacitive power transfer grid 300. As 5 noted above, in one embodiment the compensation inductors L_c 340 advantageously reduce idle currents of the power generator.

A capacitive power transfer system may also experience adverse effects resulting from common mode (CM) currents induced between the alternating current (AC) potential of the electrodes of the transmitter portion and ground, due to the parasitic capacitances of the 10 transmitter electrodes to ground (as opposed to the parasitic capacitance between transmitter electrodes discussed in detail hereinabove). While the below discussion details the parasitic capacitances of the transmitter electrodes to ground, the discussion is also applicable for parasitic capacitances of the receiver electrodes to ground.

Fig. 5 shows an exemplary and non-limiting diagram of a capacitive power 15 transfer system 500 equipped with a current compensation circuit 560 designed to eliminate CM current paths. Also illustrated in Fig. 5 are parasitic capacitances 542 and 544 of the transmitter electrodes to ground from a physical perspective.

A power supply 510 is connected to a current compensation circuit 560, that together provide an opposite alternating voltage signal to transmitter electrodes 572 and 574. A 20 pair of receiver electrodes 576 and 578 is connected to a load 579, which is powered by the transmitter electrodes 572, 574 by means of the capacitive coupling as discussed above. Thus, between the transmitter electrodes 572, 574 and receiver electrodes 576, 578 a pair of capacitors (not shown in Fig. 5) is formed.

Between each of the transmitter electrodes 572, 574 and earth ground 550 there 25 exists parasitic capacitors 542 and 544. Such parasitic capacitance may occur from iron material in a concrete wall or ceiling, or could be the result of a conducting floor, or the like, forming a parasitic capacitance between two effective conductive plates that have a dielectric material therebetween.

Typically, the distance and the nature of the dielectric to ground is unpredictable, 30 and hence so too is the specific capacitive value. Furthermore, the parasitic capacitances may be different for each of the transmitter electrodes, i.e., if one transmitter electrode is situated directly

above an enforcement iron rod in a wall and another transmitter electrode is not. In addition, the shape of the transmitter electrodes may be different, which also may lead to asymmetric parasitic capacitances.

If an alternating voltage against earth ground 550 is applied to the transmitter electrodes 572 and 574, currents flow through the parasitic capacitors 542 and 544 as indicated in Fig. 5 and denoted by I_{p1} and I_{p2} , respectively. These currents flow along the earth ground 550 and then back as common mode (CM) currents (I_{CM}) through, for example, a mains plug 511 of the power supply 510 back to the earth ground 550. As a non-limiting example, the mains plug 511 may be a plug to a wall outlet to power supply 510. However, the CM currents may be a cause of malfunction, especially if the current in the connection cable is unwanted, and therefore must be limited according to electromagnetic interference (EMI) standards. Usually, bulky and expensive CM filters with large inductors are applied to block the path for CM currents. However, it is difficult to match the filter components and a resulting filter is big in size, prone to losses, and expensive.

According to various embodiments disclosed herein, the CM currents are reduced and essentially offset by means of the current compensation circuit 560 as discussed herein below. The CM currents are offset to a minimal value, i.e., a value that an additional reduction of the CM currents cannot achieve, or is otherwise negligible. The current compensation circuit 560 includes two terminals (564 and 563) that are connected to the transmitter electrodes 572 and 574 respectively. To minimize the CM currents, the electrodes 572 and 574 are driven with a voltage asymmetrically to ground, such that the CM currents of the positive electrode (e.g., electrode 572) and the negative electrode (e.g., electrode 574) essentially cancel each other, i.e., until a common mode current flowing through the two electrodes is minimal, or otherwise negligible. With this aim, the AC voltage against the earth potential of one of the terminals (564) is reduced. This also reduces the related parasitic current I_{p1} . The opposite voltage at the terminal (563) is increased such that the parasitic current I_{p2} has the same amplitude as I_{p1} , whereby both currents compensate each other. The common mode current I_{CM} is the sum of both parasitic currents I_{p1} and I_{p2} . It should be noted the voltage difference between the two terminals 563, 564 remains the same for both operation modes, thus the power transferred to the receiver electrodes is not affected by the balancing of the common mode currents.

The operation for common mode current compensation is further illustrated in Fig. 12A. In the example shown in Fig. 12A, the power supply generates sinusoidal voltage signals. The signals shown in Fig. 12A are as follows:

5 U_{S1} represents the voltage signal between the first generator terminal 564 and the earth ground 550. The amplitude of this voltage signal (peak-to-peak) determines the amplitude of the first parasitic current I_{p1} . A DC offset is canceled by the parasitic capacitor.

U_{S2} represents the voltage signal between the second generator terminal 563 and earth ground 550. The amplitude of this voltage signal (peak-to-peak) determines the amplitude of the second parasitic current I_{p2} . A DC offset is canceled by the parasitic capacitor.

10 I_{p1} represents the parasitic current through the capacitor C_{p1} (542) formed by the first electrode (572) to the earth ground 550. Due to the capacitor C_{p1} (542), there is a phase shift to the voltage U_{S1} .

I_{p2} represents the parasitic current through the capacitor C_{p2} (544) formed by the second electrode 574 to earth ground 550.

15 I_{CM} represents the sum of both parasitic currents I_{p1} and I_{p2} , which is the resulting common mode current, and which is to be compensated.

U_{el} represents the voltage between the first terminal 564 and the second terminal 563. It is the difference of the voltages U_{S1} and U_{S2} . The amplitude of U_{el} determines the amount of power that can be transmitted in the capacitive power transmission system.

20 I_{el} represents the current through the transmitter electrodes (572, 574) and the receiver electrodes (576, 578). The I_{el} current depends on the voltage U_{el} and the load 579 resistance.

25 The solid lines represent operation of a circuit according to the state of the art (i.e., excluding the effect of the compensation circuit 560). As an example, the parasitic currents I_{p1} and I_{p2} are assumed to be different in this operation mode because of asymmetries of the electrodes. The dashed lines represent the operation according to the teachings disclosed herein. The AC voltage against earth potential of one of the terminals (U_{S1}) is reduced. This also reduces the related parasitic current I_{p1} . The opposite voltage U_{S2} is increased, such that the parasitic current I_{p2} has the same amplitude as I_{p1} , so that both currents compensate each other.

As the graph representing the signal U_{el} shows, the voltage difference between the two terminals (563, 564) remains the same for both operation modes. Therefore, the power transmission is not affected by the balancing of the common mode currents.

In one embodiment, the current compensation circuit 560 includes a rectifier 561, 5 the details of which are shown in Fig. 11, and a switching bridge 562 consisting of four switches. By means of the current compensation circuit 560 the transmitter electrodes 572, 574 are driven with a voltage symmetrically to ground.

The operation of the current compensation circuit 560 will be described with reference to Fig. 6, where the switching bridge 562 is shown in Fig. 6 as switches 532, 534, 536, 10 and 538. For ease of description the same numerical references are used in Figs. 5 and 6.

The power supply 510 is typically connected to a power grid, for example, but without limitation, a main power grid to supply the power to drive the power supply. The power supply 510 has a Phase lead, denoted P, and a neutral lead, denoted N. Usually, the N lead is also connected to protected earth (PE). Via the rectifier 561, the ground potential of the current 15 compensation circuit is connected to the N lead and then also to PE.

The rectifier 561, as further shown in Fig. 11, comprises diodes 1111, 1112, 1113 and 1114, as well as a capacitor 1115 connected at the output. The capacitor 1115 operates such that at low frequencies the leads P and N are free to alternate at the power signal frequency, while at high frequencies, the capacitor 1115 operates as a short-circuit. The high frequency is 20 typically the frequency of the power supply signal.

Referring back to Fig. 6, via the switching bridge, the ground potential of the transmitter electrodes (labeled as GND in Fig. 6) is connected to the N lead and also to the PE. Thus, the earth ground 550 is at the same electrical potential as the transmitter ground GND. As noted above, if an alternating voltage against GND is applied to the transmitter electrodes 572, 25 574, currents (I_{p1} and I_{p2}) flow through the parasitic capacitors (capacitors 542 and 544 in Fig. 5). These currents flow along earth ground and then back as common mode (CM) currents through, for example, the mains plug 511, shown in Fig. 5, back to GND of the transmitter circuit.

Using the current compensation circuit 560, the transmitter ground GND is directly connected (e.g., via the rectifier 561) to the N lead during a positive half-period of the 30 voltage signal. Then, the DC-Supply rectified voltage (V_{dc}) of the rectifier 561 is connected to the P lead of the power supply. During the negative half-period of the voltage signal, this is

reversed and the transmitter ground GND is connected to the P lead, and Vdc is connected to the N lead. The transmitter ground GND and Vdc are connected by the rectifier's capacitor (e.g., capacitor 1115 shown in Fig. 11). For high frequencies (e.g., the frequency of a power generator), this capacitor can effectively be considered a short, such that for high frequencies 5 Vdc and GND are connected together (whereas for low frequencies and DC they are not). Since either Vdc or GND are directly connected to the N lead by a diode, for high frequencies both are always connected to N (but only for high frequencies).

It should be noted that the rectifier 561 may also include a power factor correction circuit (not shown). One of ordinary skill in the art would readily realize that the rectifier 561 is 10 merely used in an exemplary embodiment, and other rectifiers may be used, DC and AC, without departing from the scope of the invention. All such rectifiers have in common, a common mode current that may find a path through the power supply back to a power generator. Therefore, the embodiments disclosed herein provide a solution for this common mode current problem.

In another embodiment, the current compensation circuit 560 may not include the 15 rectifier 561. Such an embodiment can be utilized when a DC voltage, for example, from a DC grid, can be supplied to the circuit 560. It should be noted that even when DC voltage is supplied, CM current can exist.

As noted above, the current compensation circuit provides a solution to reduce 20 CM currents where the electrodes are driven with a voltage symmetrically to ground. If the positive and negative electrodes are equal, their parasitic capacity to ground is also similar. Then, the induced CM currents flowing through the parasitic capacitors of the positive electrodes and the negative electrodes are equal in amplitude but opposite in phase. Thus, they compensate each other and the overall CM current is zero.

The symmetric driving is achieved with a switching bridge 562 formed of 25 switches 532, 534, 536 and 538 as shown in Fig. 6. In an embodiment, the switching bridge 562 may be configured as a full bridge including two pairs of switches. For example, a first pair of switches may include switches 532 and 538, while a second pair of switches may include switches 534 and 536. In one embodiment, each pair of switches may be controlled by the other pair of switches. The pairs of switches are driven such that their output voltage is in opposite 30 phase to each other as shown in exemplary and non-limiting Fig. 7, in which solid lines 710 and 720 correspond to U_{S1} and U_{S2} , as shown in Fig. 6.

The output of the first pair of switches comprising switches 532 and 538 is connected to the positive transmitter electrode, and the other output of the second pair of switches including switches 534 and 536 is connected to the negative transmitter electrode.

In most practical cases the parasitic capacitances in the vicinity of the positive and 5 negative transmitter electrodes (e.g., a wall to which the electrodes 572, 574 are mechanically connected) are slightly different. Thus, if the output voltage of the respective pairs of switches is exactly opposite, the currents through the parasitic capacitors 542 and 544 may not compensate each other as expected, and a remaining CM current may flow. To account for such an 10 asymmetry of the parasitic capacitances, the switching bridge of the current compensation circuit is operated asymmetrically rather than symmetrically.

In one embodiment, the asymmetrical operation of the pair of switches is achieved by causing the duty cycle of the two pairs of switches to be unequal. This is shown in the exemplary and non-limiting Fig. 7 as a dashed line output 730 that is slightly larger in duty cycle 15 than the duty cycle of 710 (that in symmetric operation is equal to the duty cycle of 720). The duty cycle of the output voltage affects the amplitude of the fundamental frequency contribution to the pair of switches voltage against ground. By varying the duty cycle, the fundamental frequency amplitude can be adjusted such that the currents through the parasitic capacitors are again equal and compensate each other.

In order to avoid a phase shift between the positive and negative parasitic current, 20 the pulses of the first pair of switches and of the second pair of switches appear symmetrically in time. The center of the positive pulse of the first pair of switches match exactly the center of the negative pulse of the second pair of switches (not shown). A common control method for the duty cycle of the full-bridge is a phase shift control between the two pairs of switches running at a 50% duty cycle, where a duty cycle control of each pair of switches is performed.

In another embodiment, the supply voltage for one of the two pairs of switches (or 25 for both) is varied such that the voltage amplitude of the pair of switches is adjusted by varying the supply voltage. This can be done by using a DC-to-DC converter. As a result, the duty cycles of both pairs of switches can remain exactly equal (but opposite) such that higher harmonic contributions of the CM currents may also be compensated.

30 Figs. 12B and 12C illustrate the operation of the current compensation circuit 560 that includes the switching bridge 562 consisting of four switches in a full-bridge configuration.

Fig. 12B depicts the states of the signals U_{S1} , U_{S2} , I_{P1} , I_{P2} , I_{CM} , U_{el} , I_{el} , each of which discussed above with respect to Fig. 12A. In addition, Fig. 12B shows the states of the switches S_{1a} (534) S_{1b} (532), S_{2a} (538), and S_{2b} (536), in which a high signal indicates a closed switch.

As noted, the voltage signals U_{S1} and U_{S2} at the terminals (564) and (563) have a pulse like shape. The parasitic currents I_{P1} and I_{P2} are represented by their fundamental frequency only, which is sinusoidal and constitutes the most energetic part of the common mode current I_{CM} .

The solid lines represent “normal” operation of a full-bridge without performing the CM current compensation. The dashed lines represent the common mode currents compensation according to the embodiments disclosed herein. The I_{CM} is reduced and minimized by changing the amplitude of the power supply, which relates to the amplitudes of the pulses in U_{S1} and U_{S2} . As a result, the amplitudes of the respective parasitic currents I_{P1} and I_{P2} are changed, such that their respective amplitudes compensate each other. As depicted by the graph I_{el} , the current I_{el} flowing through the load is not being affected by the changes in the amplitudes of the parasitic currents. It should be noted that the current I_{el} is also represented by its fundamental frequency, which is valid, as the receiver is a resonant circuit matched to the operating frequency of the power signal.

Fig. 12C depicts an embodiment current compensation circuit 560 that includes the switching bridge 562 consisting of four switches in a full-bridge configuration where the common mode currents are reduced by changing the pulse widths of the signals U_{S1} , U_{S2} . The description of signals depicted in Fig. 12C is similar to those illustrated in Fig. 12B.

The solid lines represent “normal” operation of a full-bridge without performing the current compensation. The dashed lines represent the common mode currents compensation according to the embodiments disclosed herein. The I_{CM} is reduced and minimized by modulating the width (thereby, the duty-cycle) of the power supply signal, which relates to the amplitudes of the pulses in U_{S1} and U_{S2} . As a result, the amplitudes of the respective parasitic currents I_{P1} and I_{P2} are changed, such that their respective amplitudes compensate each other. Specifically, a wider pulse increases the amplitude of the fundamental frequency of the related parasitic current. Therefore, changing the pulse width can be used to adjust the parasitic currents until these compensate the common mode currents.

Several exemplary and non-limiting embodiments of capacitive power transmission grids are discussed herein below. Fig. 8 shows an exemplary and non-limiting wall covering having a backside covered with vertical conductive stripes with a bottom segment having details of electrical connections thereto. As a non-limiting example a wall covering is 5 depicted as wallpaper 810 having a backside covered with vertical conductive stripes 820. The conductive stripes 820 are placed on the back side of the wallpaper material 810 that forms the insulating layer. When the wallpaper 810 is placed on a surface (not shown), for example, a wall, the conductive stripes 820 are between that surface and the wallpaper 810, while the wallpaper material 810 is in fact the insulator layer 130 discussed in greater detail with respect to Fig. 1 10 hereinabove, where conductive stripes 820 form the transmitter electrodes 122 and 124.

The conductive stripes 820 may be made of, for example, conducting ink, conducting paint, and the like. The stripes can be printed or added to the backside of regular wallpaper, or they may be under an outer surface of the wallpaper 810. The connections to the driver 110 (Fig. 1) are provided by interleaving the connections of the conductive stripes 820. 15 That is, a first conductive stripe 820 is connected in the manner of electrode 121 (Fig. 1) and, therefore, to the supply line 834 of the connection baseboard 830, while the immediately next conductive stripe 820 is connected in the manner of electrode 122 (Fig. 1) and, therefore, to the supply line 832 of the conductive connection 830, and so on and so forth, alternating between the connections. The connections 832 and 834 are part of a connection baseboard 830 designed to be 20 operative with, for example, the wallpaper 810 and accepting the output of driver 110 (Fig. 1).

Fig. 9 shows an exemplary and non-limiting transmission grid of the capacitive power system. The infrastructure is designed as a wall covering having a backside covered with horizontal conductive stripes and vertical connecting lines. As a non-limiting example a wall covering is depicted as wallpaper 900A and 900B in Fig. 9. Two sheets of such wallpaper 900A 25 and 900B are shown side-by-side. The electrodes 910 and 920 begin with vertical connection lines that are directed horizontally in opposite directions, so that they interleave with each other resulting in a desired pattern allowing a horizontal-based wallpaper solution for capacitive power transfer. The structures shown in Figs. 8 and 9 are designed to allow for wallpaper that may be cut-to-measure, be connected from the top or the bottom part of the wallpaper, and can 30 optionally share connections between neighboring conducting stripes of neighboring wallpaper

sheets. Moreover, the manufactured wallpaper may be rolled into wallpaper rolls in any desired length.

It should be noted that power may be provided to the conducting stripes directly by clamping the wallpaper or protruding pins through the paper layer. However, it is also possible to couple the power to the conducting stripes in a capacitive way. To this end, the transmitter electrodes are positioned on the wallpaper. The power transmission principle for injection of the power to the transmitter electrodes of the wallpaper may be, for example, the same principle as the way the power is transferred from the wallpaper electrodes to the power receiver. The advantage of this configuration is that the position of power injection to the wallpaper can be freely chosen, and no damage is done to the cover layer.

Fig. 10 shows an exemplary and non-limiting embodiment 1000 of an electric connection of a plurality of segments with integrated connections and connectors. A plurality of segments 1050A, 1050B, and 1050C have integrated connection lines 1020 and 1030 that crossover at point 1040 without having an electrical connection at the intersection point 1040.

The connection lines 1020 and 1030 provide the power supply connectivity to the segments. The wire 1020 is electrically connected to the segment 1050A. When two segments are mounted adjacent to each other, their corresponding segments are connected to different electrical connection lines.

For example, in Fig. 10, the center segment 1050B of 1010B is connected in fact to a different connection line (i.e., connection line 1030) than the segments 1050A and 1050C (i.e., connection line 1020). As a result, the segments alternate in polarity, thereby providing the different electrodes as discussed in more detail with respect of Fig. 1 hereinabove. It should, therefore, be understood that the segment 1050A operates, for example, as electrode 121 shown in Fig. 1, while segment 1050B operates as electrode 122 shown in Fig. 1.

While the present invention has been described at some length and with some particularity with respect to the several described embodiments, it is not intended that it should be limited to any such particulars or embodiments or any particular embodiment, but it is to be construed with references to the appended claims so as to provide the broadest possible interpretation of such claims in view of the prior art and, therefore, to effectively encompass the intended scope of the invention. Furthermore, the foregoing describes the invention in terms of embodiments foreseen by the inventor for which an enabling description was available,

notwithstanding that insubstantial modifications of the invention, not presently foreseen, may nonetheless represent equivalents thereto.

CLAIMS:

1. An apparatus (300) for supplying power to a load in a capacitive power transfer system, comprising:
 - a power generator (350) operating at a first frequency;
 - a transmitter comprising a plurality of first electrodes (310) connected to a first terminal of the power generator (350) and a plurality of second electrodes (320) connected to a second terminal of the power generator (350) of a transmitter portion of the apparatus (300); and
 - a plurality of inductors (340), wherein each inductor of the plurality of inductors is connected between a pair of a first electrode and a second electrode of the plurality of first and second electrodes, wherein each inductor comprises, together with a parasitic capacitor (330) formed between each pair of the first electrode and the second electrode, a resonant circuit at the first frequency in order to compensate for current loss due to parasitic capacitances.
2. The apparatus of claim 1, wherein each inductor of the plurality of inductors is a variable inductor and the apparatus is a capacitive power transfer system (300).
3. A method for reducing idle currents in a transmitter for supplying a power to a load connected in a capacitive power transfer system (300), comprising:
 - operating a power generator (350) at a first frequency having a first terminal and a second terminal;
 - connecting a first electrode (310) of a transmitter portion of the capacitive power transfer system (300) to the first terminal of the power generator (350);
 - connecting a second electrode (320) of the transmitter portion of the capacitive power transfer system (300) to the second terminal of the power generator (350); and
 - connecting an inductor (340) between the first electrode (310) and the second electrode (320), the inductor (340) having an inductance to create a resonant circuit with a parasitic capacitor (330) formed between the first electrode (310) and the second electrode (320), such that the resonant circuit resonates at the first frequency.

4. The method of claim 3, wherein the inductor is a variable inductor.
5. The method of claim 4, further comprising:
adjusting variable inductance of the variable inductor to cause the resonant circuit to resonate at the first frequency.
6. A circuit (560) for reducing common mode (CM) currents in a capacitive power transfer system, comprising:
 - a first terminal (564) connected to a first transmitter electrode (572) of the capacitive power transfer system, wherein the first transmitter electrode (572) forms a first parasitic capacitor (542) to a protected earth connected to an earth ground; and
 - a second terminal (563) connected to a second transmitter electrode (574) of the capacitive power transfer system, wherein the second transmitter electrode (574) forms a second parasitic capacitor (544) to the protected earth;

wherein the circuit generates a first periodic voltage signal between the first terminal (564) and the earth ground, the circuit further generates a second periodic voltage signal between the second terminal and the earth ground, wherein at least an amplitude of each of the first periodic voltage signal and the second periodic voltage signal is controlled to essentially offset the common mode (CM) current flowing through the first parasitic capacitor (542) and the second parasitic capacitor (544).
7. The circuit of claim 5, wherein the first periodic voltage signal consists of a first period of time and a second period of time, wherein during the first period of time a voltage level of the first periodic voltage signal is substantially positive, and during the second time period a voltage level of the first periodic voltage signal is substantially negative; wherein the second periodic voltage signal consists of a first period of time and a second period of time, wherein during the first period of time a voltage level of the second periodic voltage signal is substantially negative, and during the second time period the voltage level of the second periodic voltage signal is substantially positive.

8. The circuit of claim 7, wherein each of the first and second time periods of the first periodic voltage signal substantially matches each of the first and second time periods of the second periodic voltage signal respectively.

9. The circuit of claim 8, wherein parasitic capacitances in a vicinity of the first and second transmitter electrodes are different, wherein the vicinity of the first transmitter electrode and the second transmitter electrode includes at least a surface to which the first transmitter electrode and second transmitter electrode are mechanically connected.

10. The circuit of claim 6, wherein the circuit is further configured to change a width of each of the first periodic voltage signal and the second periodic voltage signal until the CM current flowing through the first parasitic capacitor (542) and the second parasitic capacitor (544) is essentially offset.

11. The circuit of claim 10, further comprising:

a switching bridge (562) including a first pair of switches (534, 536) and a second pair of switches (532, 538);

wherein the first pair of switches includes two switches (534, 536), a switch (534) is connected to the first transmitter electrode (572) and a first terminal of a power supply generator and a second switch (536) is connected to the second transmitter electrode (574) and a second terminal of the power supply generator (510);

wherein the second pair of switches includes two switches (532, 538), a switch (532) is connected to the first transmitter electrode (572) and the second terminal of the power supply generator and a switch (536) is connected to the second transmitter electrode (574) and to the second terminal of the power supply generator, the second terminal of the power supply generator is connected to the protected earth for connection to the earth ground; and

wherein switching of each of the first pair of switches (534, 536) and the second pair of switches (532, 538) is controlled to essentially offset the CM current flowing through the first parasitic capacitor (542) and the second parasitic capacitor (544).

12. The circuit of claim 11, wherein the CM current is a sum of the currents flowing through the first parasitic capacitor (542) and the second parasitic capacitor (544).

13. The circuit of claim 11, wherein the switching of each of the first pair of switches (534, 536) and the second pair of switches (532, 538) is controlled to change amplitudes of currents flowing through the first parasitic capacitor (542) and the second parasitic capacitor (544) until the amplitudes of the currents essentially cancel each other.

14. The circuit of claim 11, wherein the switching of the first pair of switches (534, 536) is controlled to change a width of a voltage pulse between the second transmitter electrode and the earth ground, wherein the switching of the second pair of switches (532, 538) is controlled to change a width of a voltage pulse between the first transmitter electrode and the earth ground.

15. The circuit of claim 11, wherein the first pair of switches (534, 536) and the second pair of switches (532, 538) are controlled in an asymmetric operation, wherein the asymmetric operation comprises a different duty cycle for control of the switches of the first pair of switches and control of the switches of the second pair of switches.

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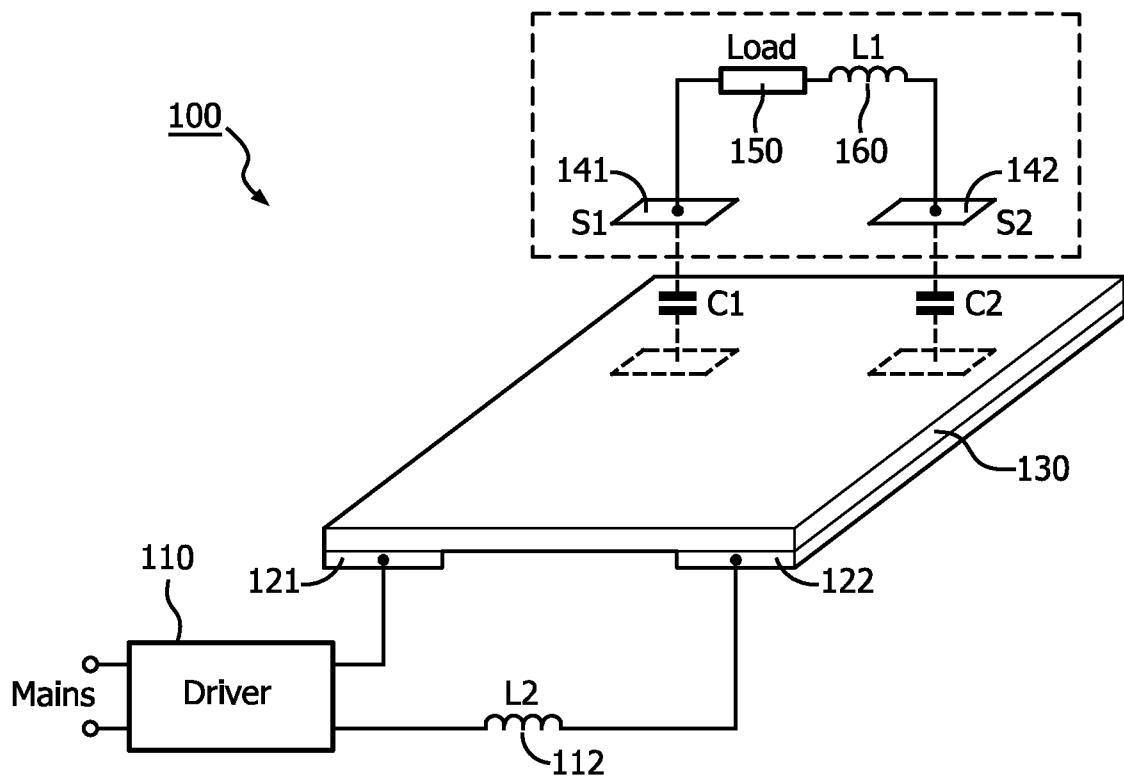


FIG. 1

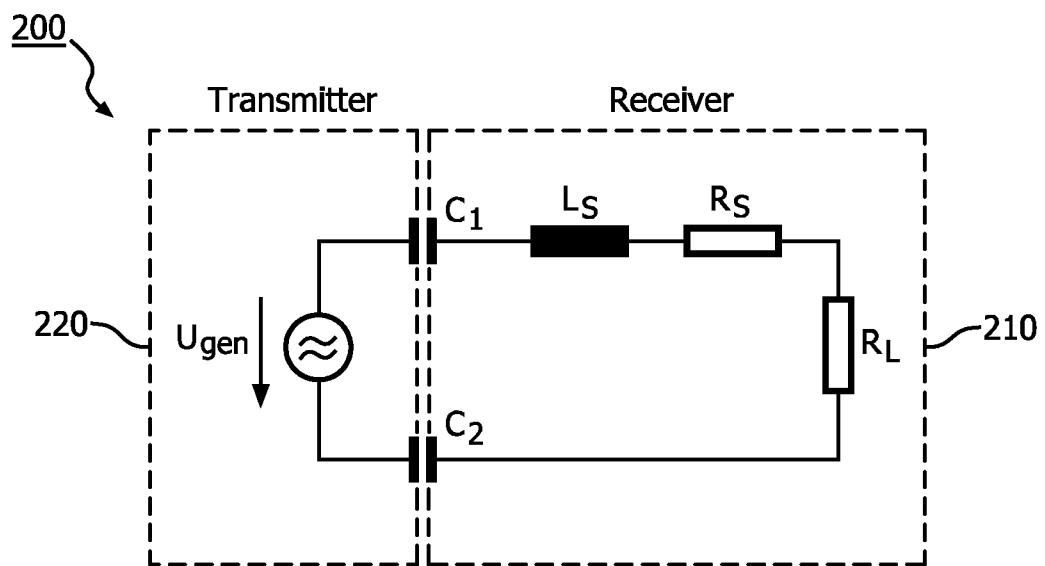


FIG. 2

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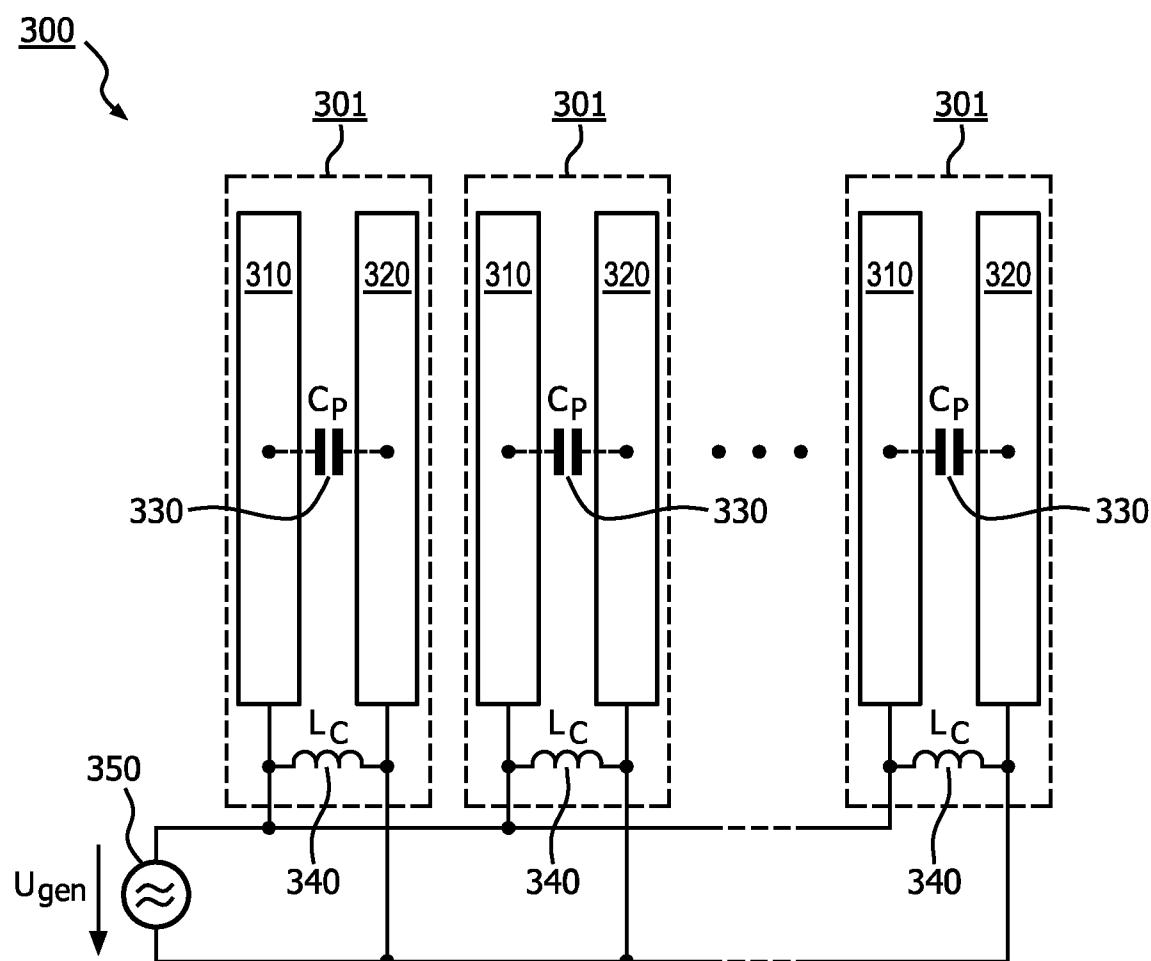


FIG. 3

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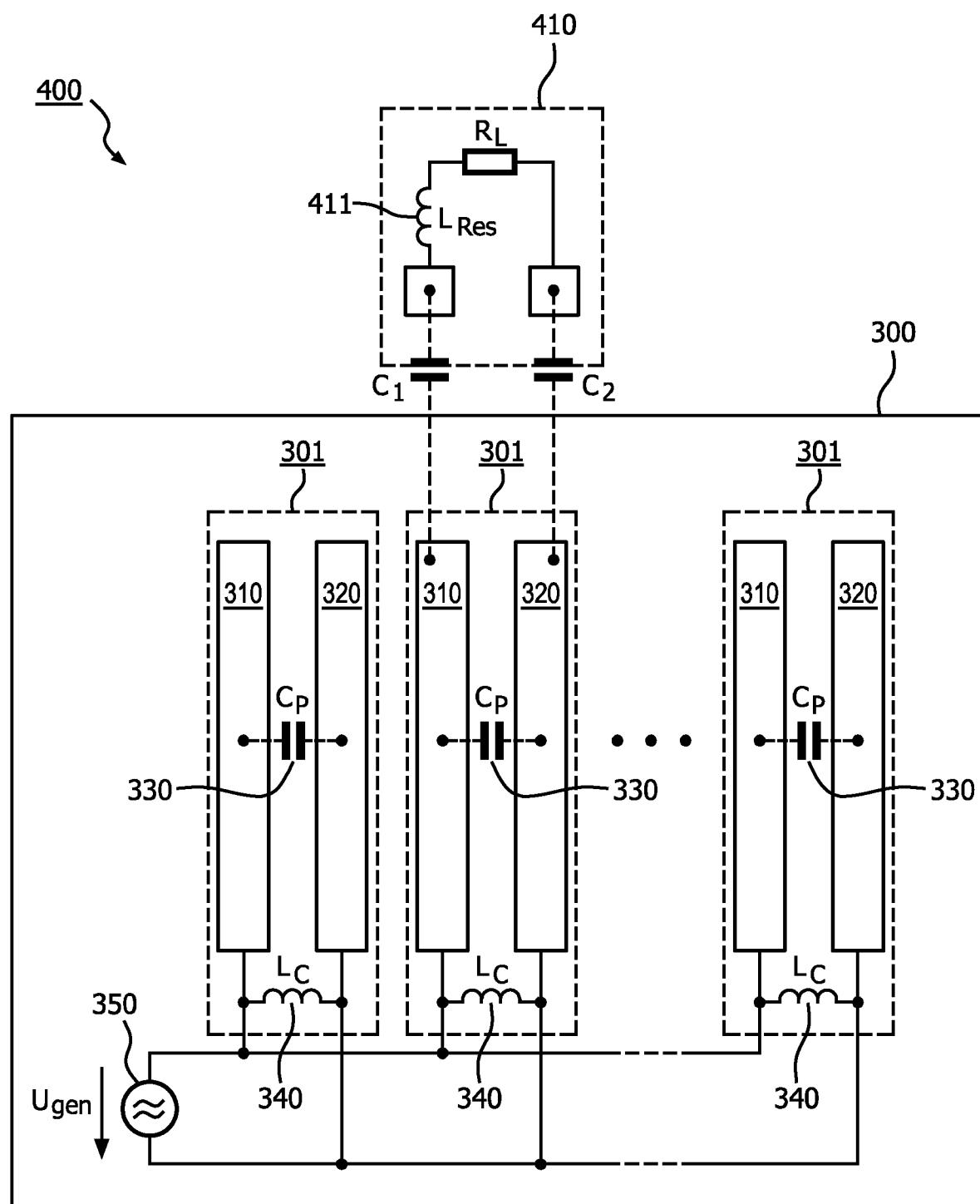


FIG. 4

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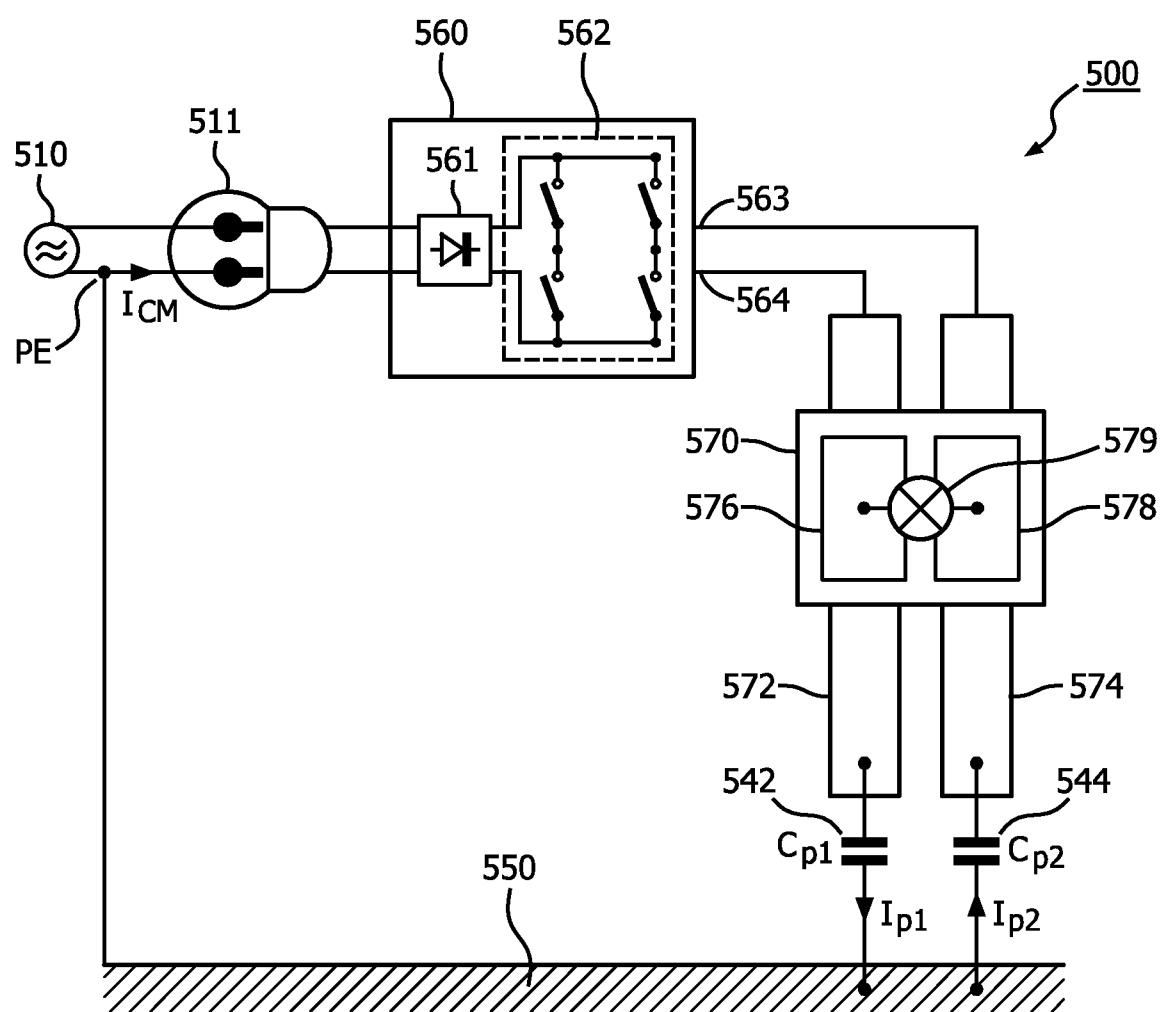
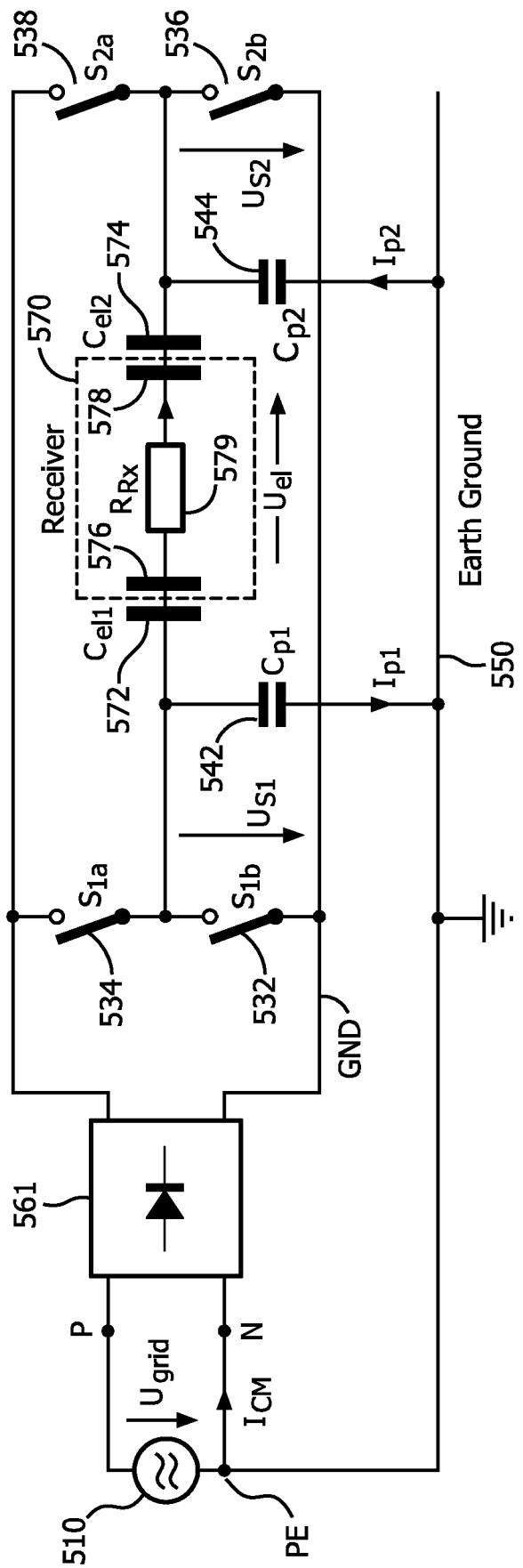


FIG. 5

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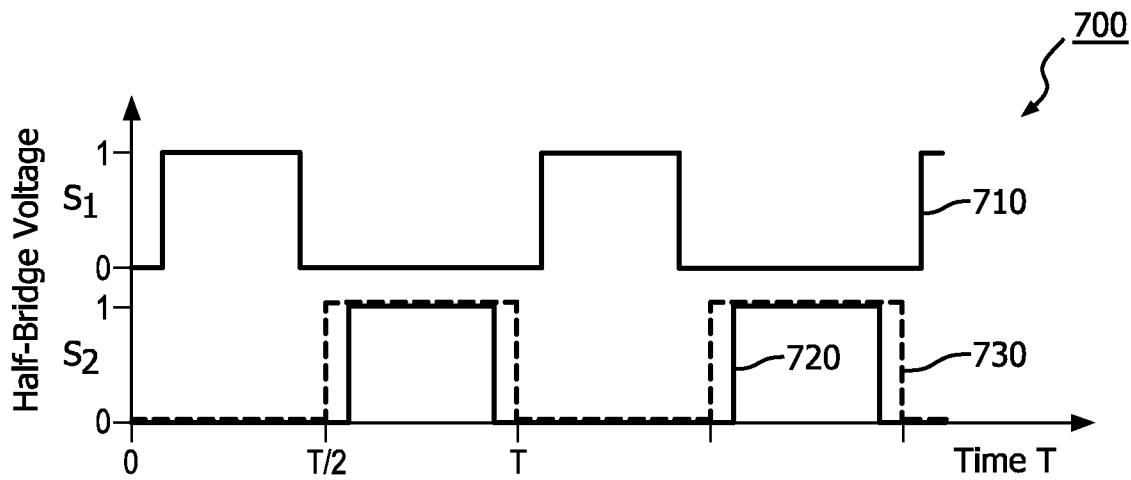


FIG. 7

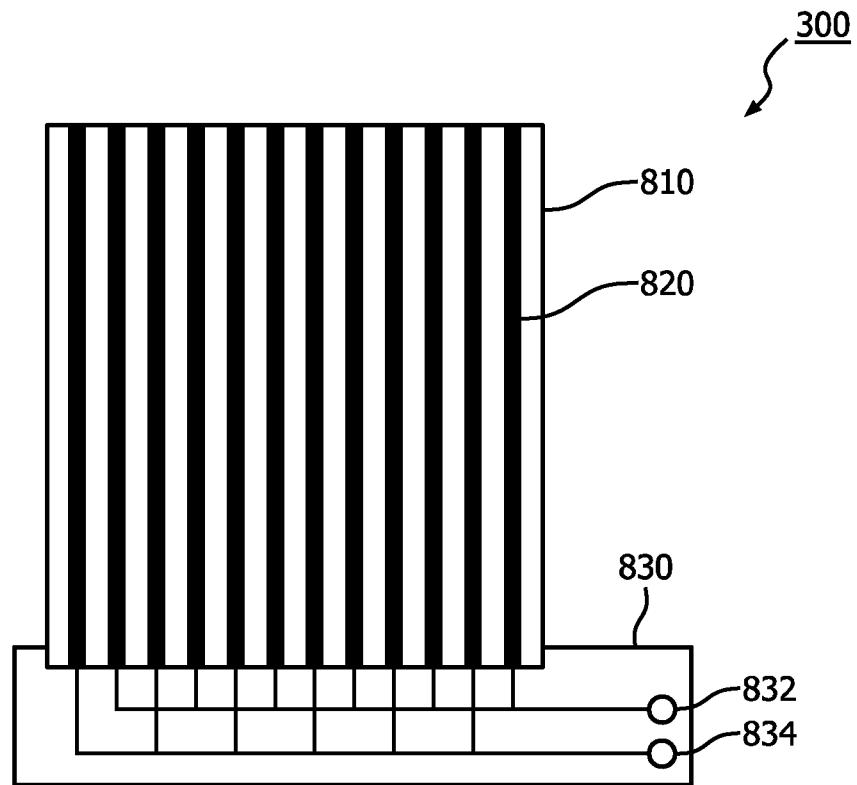


FIG. 8

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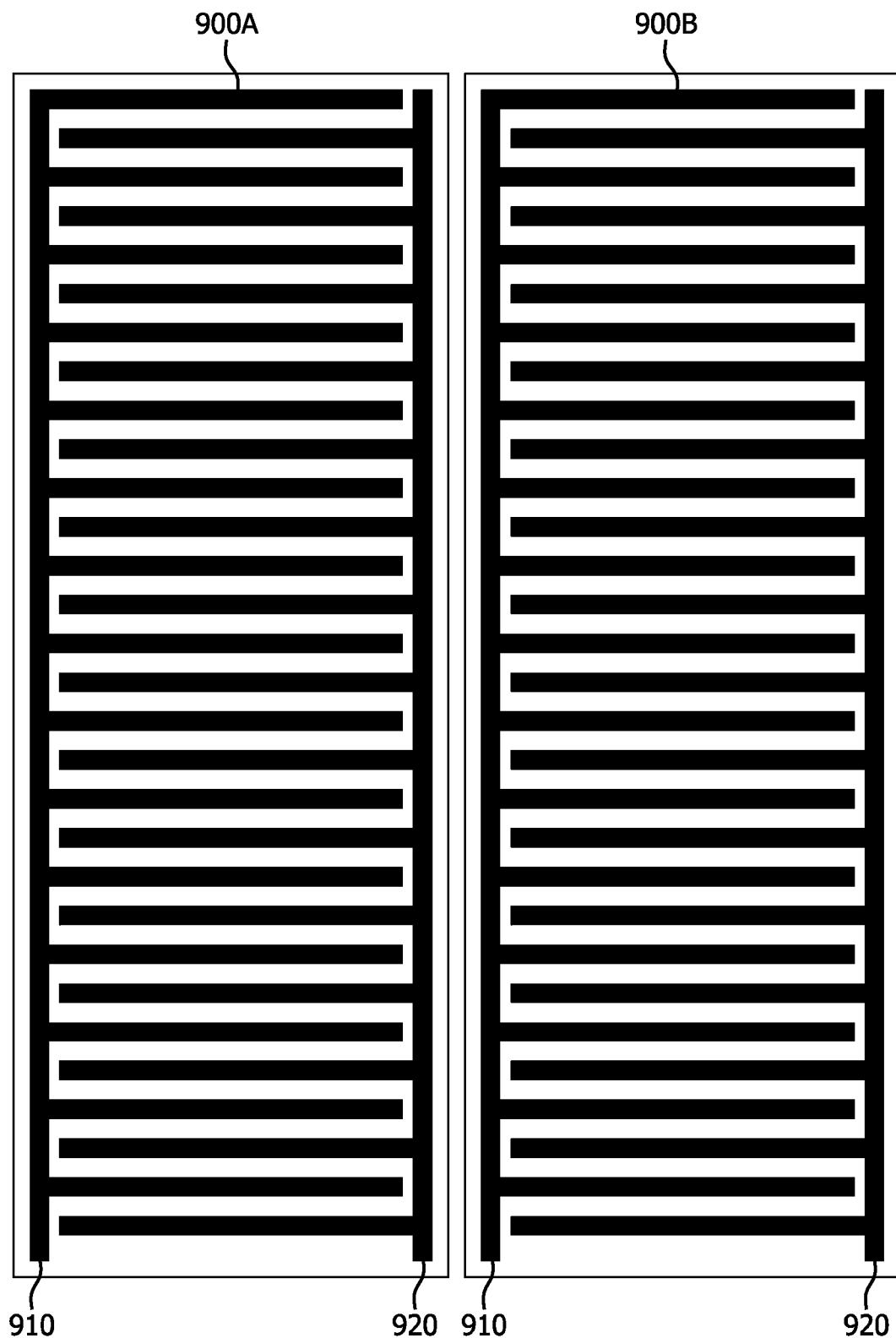


FIG. 9

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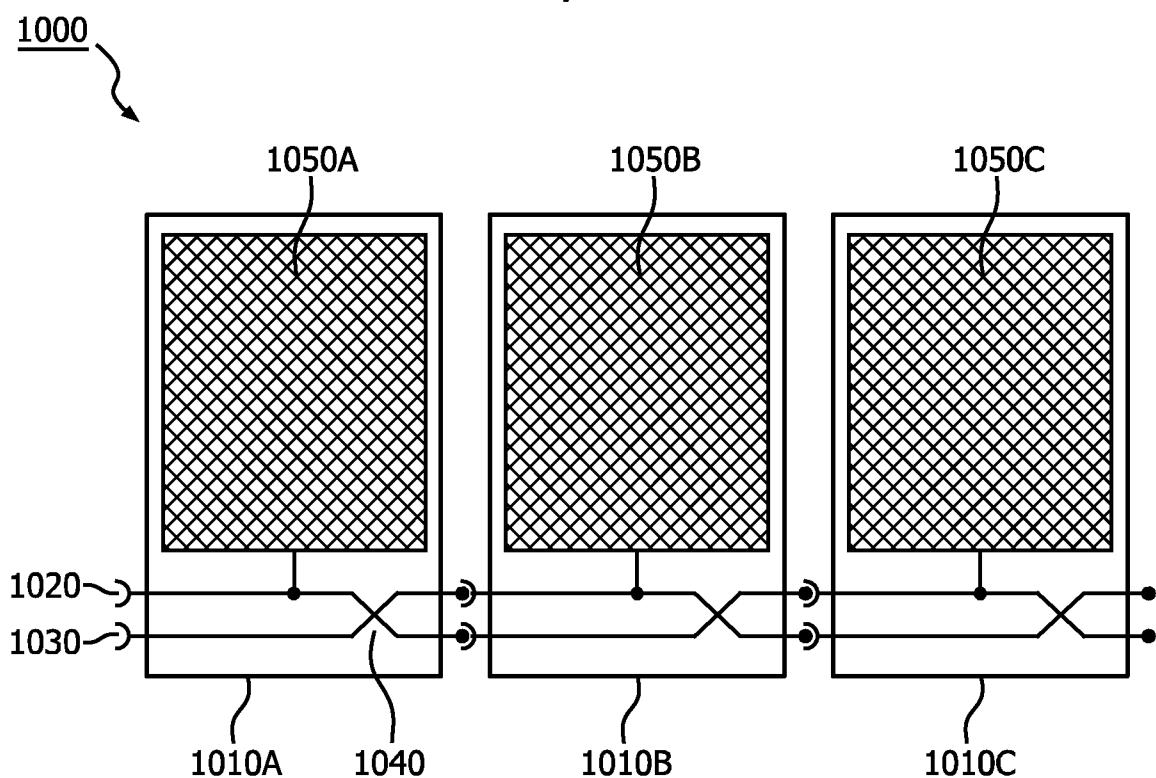


FIG. 10

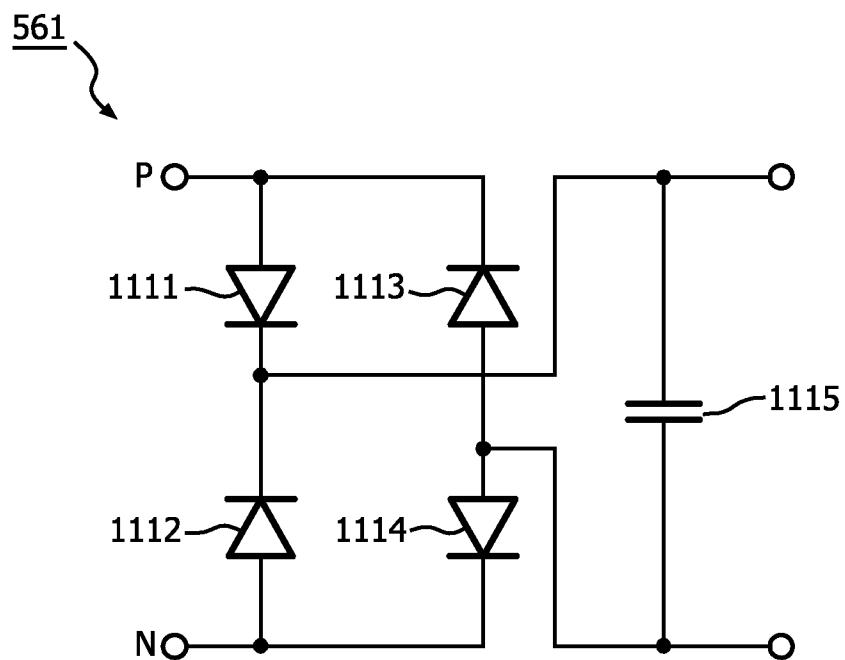


FIG. 11

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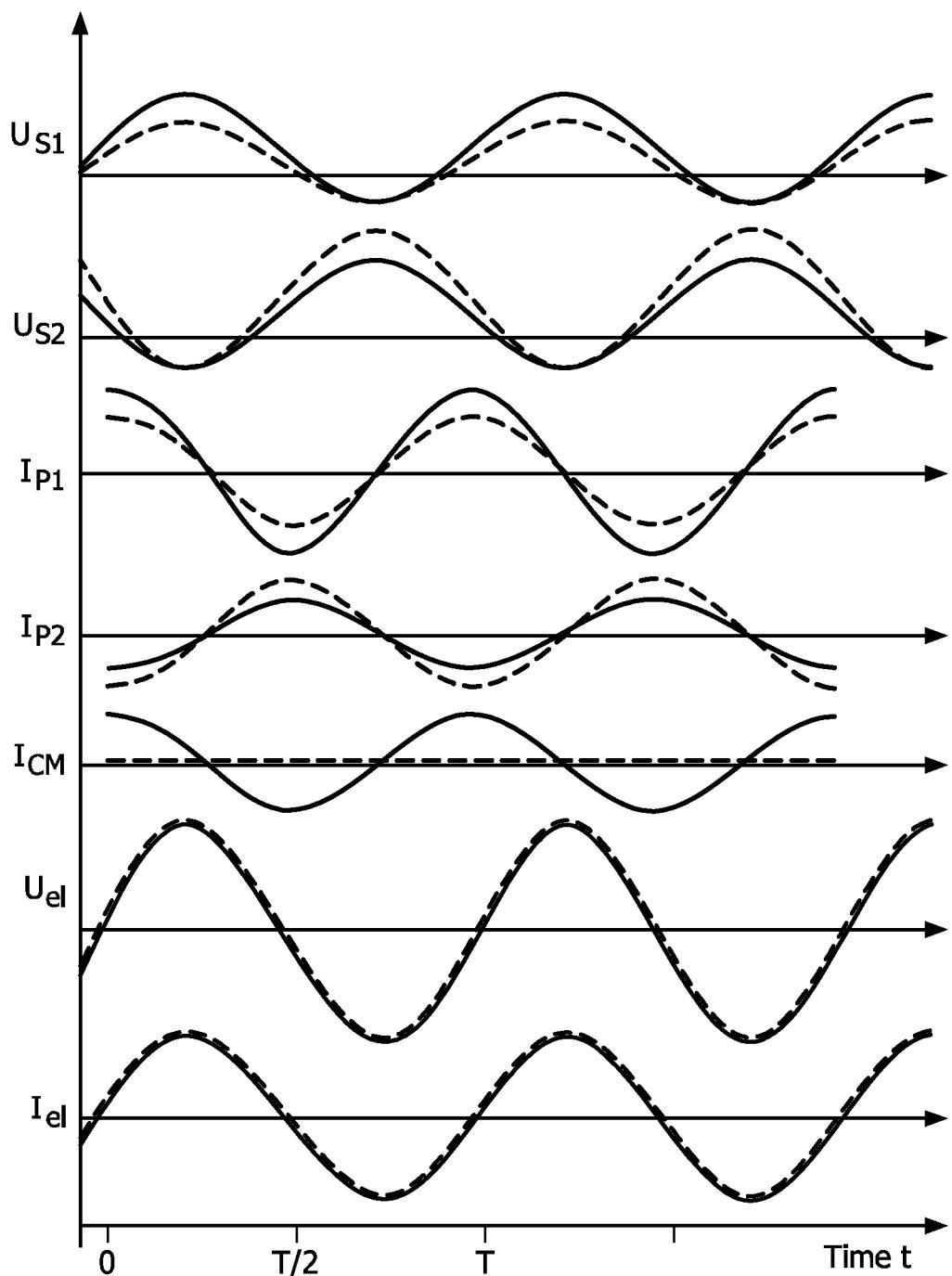


FIG. 12A

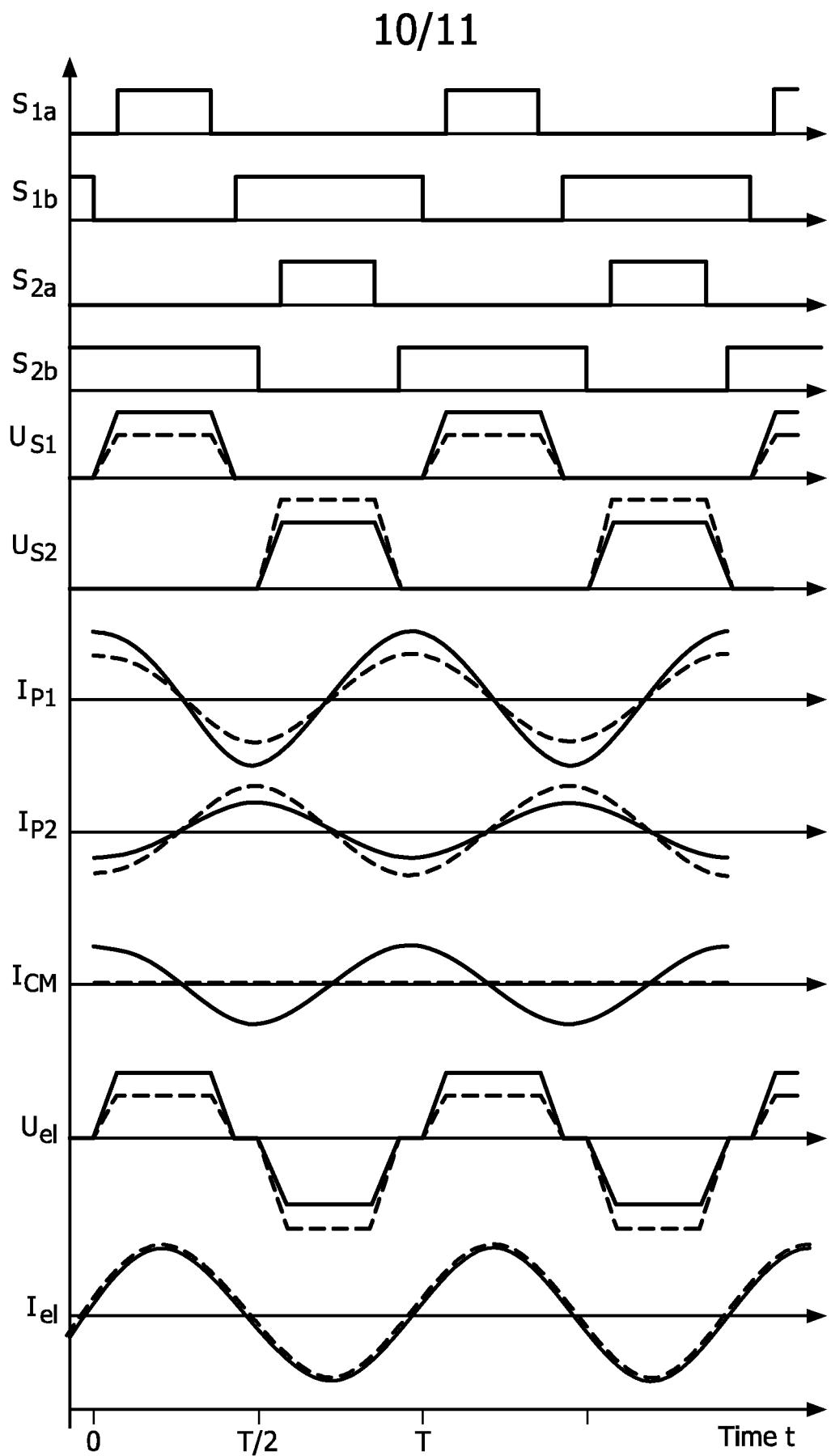


FIG. 12B

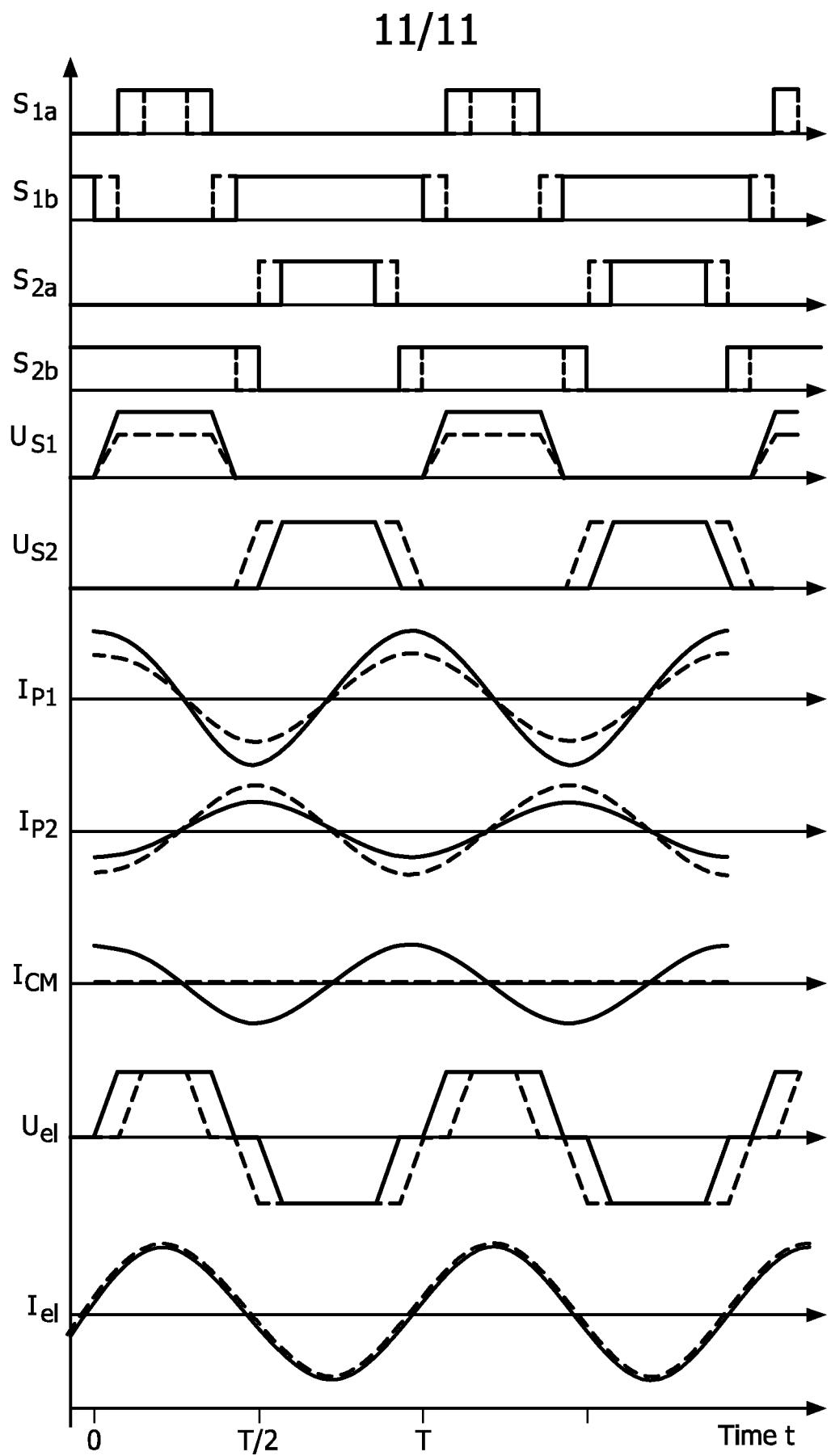


FIG. 12C