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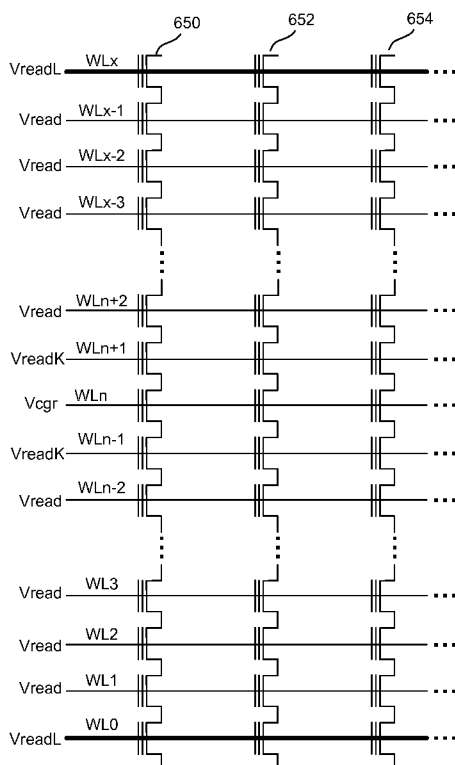
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[Continued on next page]

(54) **Title:** NON-VOLATILE STORAGE WITH READ PROCESS THAT REDUCES DISTURB



(57) **Abstract:** A apparatus and process for reading data from non-volatile storage includes applying a read compare signal to a selected data memory cell of a NAND string, applying a first set of one or more read pass voltages to unselected data memory cells at both ends of the NAND string and applying a second set of one or more read pass voltages to unselected data memory cells between both ends of the NAND string and on both sides of the selected data memory cell. The second set of one or more read pass voltages are all higher than the first set of one or more read pass voltages.



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NON-VOLATILE STORAGE WITH READ PROCESS THAT REDUCES DISTURB

[0001] This application claims the benefit of U.S. Provisional Application 61/610,387, filed on March 13, 2012, incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to technology for non-volatile storage.

Description of the Related Art

[0003] Semiconductor memory devices have become more popular for use in various electronic devices. For example, non-volatile semiconductor memory is used in cellular telephones, digital cameras, personal digital assistants, mobile computing devices, non-mobile computing devices and other devices. Electrical Erasable Programmable Read Only Memory (EEPROM) and flash memory are among the most popular non-volatile semiconductor memories.

[0004] Both EEPROM and flash memory utilize a floating gate that is positioned above and insulated from a channel region in a semiconductor substrate. The floating gate is positioned between source and drain regions. A control gate is provided over and insulated from the floating gate. The threshold voltage of the transistor is controlled by the amount of charge that is retained on the floating gate. That is, the minimum amount of voltage that must be applied to the control gate before the transistor is turned on to permit

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conduction between its source and drain is controlled by the level of charge on the floating gate.

[0005] When programming an EEPROM or flash memory device, typically a program voltage is applied to the control gate and the bit line is grounded. Electrons from the channel are injected into the floating gate. When electrons accumulate in the floating gate, the floating gate becomes negatively charged and the threshold voltage of the memory cell is raised so that the memory cell is in the programmed state. More information about programming can be found in U.S. Patent 6,859,397, titled "Source Side Self Boosting Technique For Non-Volatile Memory;" and U.S. Patent 6,917,542, titled "Detecting Over Programmed Memory," both patents are incorporated herein by reference in their entirety.

[0006] Some EEPROM and flash memory devices have a floating gate that is used to store two ranges of charges and, therefore, the memory cell can be programmed/erased between two states, an erased state and a programmed state that correspond to data "1" and data "0." Such a device is referred to as a binary or two-state device.

[0007] A multi-state flash memory cell is implemented by identifying multiple, distinct allowed threshold voltage ranges. Each distinct threshold voltage range corresponds to a predetermined value for the set of data bits. The specific relationship between the data programmed into the memory cell and the threshold voltage ranges of the memory cell depends upon the data encoding scheme adopted for the memory cells. For example, U.S. Patent No. 6,222,762 and U.S. Patent Application Publication No. 2004/0255090, both of which are incorporated herein by reference in their entirety, describe various data encoding schemes for multi-state flash memory cells.

[0008] Typically, the program voltage (V_{pgm}) is applied to the control gates of the memory cells as a series of pulses. The magnitude of the pulses is

increased with each successive pulse by a predetermined step size (e.g. 0.2v, 0.3v, 0.4v, or others). In the periods between the pulses, verify operations are carried out. That is, the programming level of each memory cell of a group of memory cells being programmed in parallel is sensed between each programming pulse to determine whether it is equal to or greater than a verify level to which it is being programmed. One means of verifying the programming is to test conduction at a specific compare point. The memory cells that are verified to be sufficiently programmed are locked out, for example, by raising the bit line voltage to stop the programming process for those memory cells. The above described techniques, and others described herein, can be used in combination with various boosting techniques to prevent program disturb and with various efficient verify techniques known in the art.

[0009] Memory cells can be read by separately applying one or more compare voltages to the control gate (or other terminal) of the memory cell and sensing whether the memory cell conduct sufficient current in response to the compare voltage. In these read operations, unselected word lines are raised to a read pass voltage (e.g. 7-10 volts) to make the associated transistors operate as pass gates. The selected word line is connected to a voltage, a level of which is specified for each read operation, in order to determine whether a threshold voltage of the concerned memory cell has reached such level. Because the unselected word lines receive the pass voltage, memory cells along unselected word lines during a read operation will receive a voltage on their control gate which over many read operations may cause electrons to be injected into their floating gate, thereby, raising the threshold voltage of those memory cells. This effect is called Read Disturb.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0011] Figure 1 is a top view of a NAND string.
- [0012] Figure 2 is an equivalent circuit diagram of the NAND string.
- [0013] Figure 3 is a block diagram of a non-volatile memory system.
- [0014] Figure 4 is a block diagram depicting one embodiment of a sense block.
- [0015] Figure 5 is a block diagram depicting one embodiment of a memory array.
- [0016] Figure 6 is a flow chart describing one embodiment of a process for programming.
- [0017] Figure 7 is a flow chart describing one embodiment of a process for programming data into a block of memory cells.
- [0018] Figure 8 depicts an example set of threshold voltage distributions and describes a process for programming non-volatile memory.
- [0019] Figure 9 depicts three programming pulses, and the verify pulses applied between the programming pulses.
- [0020] Figures 10A–E show various threshold voltage distributions and describe a process for programming non-volatile memory.
- [0021] Figure 11 is a flow chart describing one embodiment of a process for programming non-volatile memory.
- [0022] Figure 12 is a flow chart describing one embodiment of a process for reading from non-volatile storage.

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[0023] Figure 13 is a schematic diagram showing three NAND strings and an associated set of word lines being biased for reading.

[0024] Figure 14 is a timing diagram depicting a read process.

[0025] Figures 15-22 are schematic diagrams showing three NAND strings and an associated set of word lines being biased for reading.

[0026] Figure 23 shows one embodiment of a block of memory cells.

[0027] Figures 24-28 are schematic diagrams showing three NAND strings and an associated set of word lines being biased for reading.

DETAILED DESCRIPTION

[0028] A system is disclosed for reading data from non-volatile storage in a manner that reduces the chance of read disturb occurring. One set of embodiments includes applying a first set of one or more read pass voltages to unselected data memory cells at both ends of the NAND string and applying a second set of one or more read pass voltages to unselected data memory cells between both ends of the NAND string and on both sides of the selected data memory cell. The second set of one or more read pass voltages are all higher than the first set of one or more read pass voltages.

[0029] One example of a non-volatile storage system that can implement the technology described herein is a flash memory system that uses the NAND structure, which includes arranging multiple transistors in series, sandwiched between two select gates. The transistors in series and the select gates are referred to as a NAND string. Figure 1 is a top view showing one NAND string. Figure 2 is an equivalent circuit thereof. The NAND string depicted in

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Figures 1 and 2 includes four transistors 100, 102, 104 and 106 in series and sandwiched between (drain side) select gate 120 and (source side) select gate 122. Select gate 120 connects the NAND string to a bit line via bit line contact 126. Select gate 122 connects the NAND string to source line 128. Select gate 120 is controlled by applying the appropriate voltages to select line SGD. Select gate 122 is controlled by applying the appropriate voltages to select line SGS. Each of the transistors 100, 102, 104 and 106 has a control gate and a floating gate. For example, transistor 100 has control gate 100CG and floating gate 100FG. Transistor 102 includes control gate 102CG and a floating gate 102FG. Transistor 104 includes control gate 104CG and floating gate 104FG. Transistor 106 includes a control gate 106CG and a floating gate 106FG. Control gate 100CG is connected to word line WL3, control gate 102CG is connected to word line WL2, control gate 104CG is connected to word line WL1, and control gate 106CG is connected to word line WL0.

[0030] Note that although Figures 1 and 2 show four memory cells in the NAND string, the use of four memory cells is only provided as an example. A NAND string can have less than four memory cells or more than four memory cells. For example, some NAND strings will have 128 memory cells or more. The discussion herein is not limited to any particular number of memory cells in a NAND string. One embodiment uses NAND strings with 66 memory cells, where 64 memory cells are used to store data and two of the memory cells are referred to as dummy memory cells because they do not store data.

[0031] A typical architecture for a flash memory system using a NAND structure will include several NAND strings. Each NAND string is connected to the common source line by its source select gate controlled by select line SGS and connected to its associated bit line by its drain select gate controlled by select line SGD. Each bit line and the respective NAND string(s) that are connected to that bit line via a bit line contact comprise the columns of the array of memory cells. Bit lines are shared with multiple NAND strings.

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Typically, the bit line runs on top of the NAND strings in a direction perpendicular to the word lines and is connected to a sense amplifier.

[0032] Relevant examples of NAND type flash memories and their operation are provided in the following U.S. Patents/Patent Applications, all of which are incorporated herein by reference in their entirety: U.S. Pat. No. 5,570,315; U.S. Pat. No. 5,774,397; U.S. Pat. No. 6,046,935; U.S. Pat. No. 6,456,528; and U.S. Pat. Publication No. US2003/0002348.

[0033] Other types of non-volatile storage devices, in addition to NAND flash memory, can also be used to implement the new technology described herein. For example, a TANOS structure (consisting of a stacked layer of TaN-Al₂O₃-SiN-SiO₂ on a silicon substrate), which is basically a memory cell using trapping of charge in a nitride layer (instead of a floating gate), can also be used with the technology described herein. Another type of memory cell useful in flash EEPROM systems utilizes a non-conductive dielectric material in place of a conductive floating gate to store charge in a non-volatile manner. Such a cell is described in an article by Chan et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," IEEE Electron Device Letters, Vol. EDL-8, No. 3, March 1987, pp. 93-95. A triple layer dielectric formed of silicon oxide, silicon nitride and silicon oxide ("ONO") is sandwiched between a conductive control gate and a surface of a semi-conductive substrate above the memory cell channel. The cell is programmed by injecting electrons from the cell channel into the nitride, where they are trapped and stored in a limited region. This stored charge then changes the threshold voltage of a portion of the channel of the cell in a manner that is detectable. The cell is erased by injecting hot holes into the nitride. See also Nozaki et al., "A 1-Mb EEPROM with MONOS Memory Cell for Semiconductor Disk Application," IEEE Journal of Solid-State Circuits, Vol. 26, No. 4, April 1991, pp. 497-501, which describes a similar cell in a split-gate configuration where a doped polysilicon

gate extends over a portion of the memory cell channel to form a separate select transistor.

[0034] Another example is described by Eitan et al., “NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell,” IEEE Electron Device Letters, vol. 21, no. 11, November 2000, pp. 543-545. An ONO dielectric layer extends across the channel between source and drain diffusions. The charge for one data bit is localized in the dielectric layer adjacent to the drain, and the charge for the other data bit is localized in the dielectric layer adjacent to the source. United States patents Nos. 5,768,192 and 6,011,725 disclose a non-volatile memory cell having a trapping dielectric sandwiched between two silicon dioxide layers. Multi-state data storage is implemented by separately reading the binary states of the spatially separated charge storage regions within the dielectric. Other types of non-volatile memory technologies can also be used.

[0035] Figure 3 illustrates a memory device 210 having read/write circuits for reading and programming a page of memory cells (e.g., NAND multi-state flash memory) in parallel. Memory device 210 may include one or more memory die or chips 212. Memory die 212 includes an array (two-dimensional or three dimensional) of memory cells 200, control circuitry 220, and read/write circuits 230A and 230B. In one embodiment, access to the memory array 200 by the various peripheral circuits is implemented in a symmetric fashion, on opposite sides of the array, so that the densities of access lines and circuitry on each side are reduced by half. The read/write circuits 230A and 230B include multiple sense blocks 300 which allow a page of memory cells to be read or programmed in parallel. The memory array 200 is addressable by word lines via row decoders 240A and 240B and by bit lines via column decoders 242A and 242B. In a typical embodiment, a controller 244 is included in the same memory device 210 (e.g., a removable storage card or package) as the one or more memory die 212. Commands and data are

transferred between the host and controller 244 via lines 232 and between the controller and the one or more memory die 212 via lines 234. Some memory systems may include multiple dies 212 in communication with Controller 244.

[0036] Control circuitry 220 cooperates with the read/write circuits 230A and 230B to perform memory operations on the memory array 200. The control circuitry 220 includes a state machine 222, an on-chip address decoder 224 and a power control module 226. The state machine 222 provides chip-level control of memory operations. The on-chip address decoder 224 provides an address interface between that used by the host or a memory controller to the hardware address used by the decoders 240A, 240B, 242A, and 242B. The power control module 226 controls the power and voltages supplied to the word lines and bit lines during memory operations. In one embodiment, power control module 226 includes one or more charge pumps that can create voltages larger than the supply voltage. Control circuitry 220, power control 226, decoder 224, state machine 222, decoders 240 A/B & 242A/B, the read/write circuits 230A/B and the controller 244, collectively or separately, can be referred to as one or more managing circuits.

[0037] Figure 4 is a block diagram of an individual sense block 300 partitioned into a core portion, referred to as a sense module 480, and a common portion 490. In one embodiment, there will be a separate sense module 480 for each bit line and one common portion 490 for a set of multiple sense modules 480. In one example, a sense block will include one common portion 490 and eight sense modules 480. Each of the sense modules in a group will communicate with the associated common portion via a data bus 472. For further details, refer to U.S. Patent Application Publication 2006/0140007, which is incorporated herein by reference in its entirety.

[0038] Sense module 480 comprises sense circuitry 470 that determines whether a conduction current in a connected bit line is above or below a

predetermined level. In some embodiments, sense module 480 includes a circuit commonly referred to as a sense amplifier. Sense module 480 also includes a bit line latch 482 that is used to set a voltage condition on the connected bit line. For example, a predetermined state latched in bit line latch 482 will result in the connected bit line being pulled to a state designating program inhibit (e.g., Vdd).

[0039] Common portion 490 comprises a processor 492, a set of data latches 494 and an I/O Interface 496 coupled between the set of data latches 494 and data bus 420. Processor 492 performs computations. For example, one of its functions is to determine the data stored in the sensed memory cell and store the determined data in the set of data latches. The set of data latches 494 is used to store data bits determined by processor 492 during a read operation. It is also used to store data bits imported from the data bus 420 during a program operation. The imported data bits represent write data meant to be programmed into the memory. I/O interface 496 provides an interface between data latches 494 and the data bus 420.

[0040] During read or sensing, the operation of the system is under the control of state machine 222 that controls the supply of different control gate voltages to the addressed cell. As it steps through the various predefined control gate voltages (the read reference voltages or the verify reference voltages) corresponding to the various memory states supported by the memory, the sense module 480 may trip at one of these voltages and an output will be provided from sense module 480 to processor 492 via bus 472. At that point, processor 492 determines the resultant memory state by consideration of the tripping event(s) of the sense module and the information about the applied control gate voltage from the state machine via input lines 493. It then computes a binary encoding for the memory state and stores the resultant data bits into data latches 494. In another embodiment of the core portion, bit line

latch 482 serves double duty, both as a latch for latching the output of the sense module 480 and also as a bit line latch as described above.

[0041] It is anticipated that some implementations will include multiple processors 492. In one embodiment, each processor 492 will include an output line (not depicted in Fig. 4) such that each of the output lines is wired-OR'd together. In some embodiments, the output lines are inverted prior to being connected to the wired-OR line. This configuration enables a quick determination during the program verification process of when the programming process has completed because the state machine receiving the wired-OR line can determine when all bits being programmed have reached the desired level. For example, when each bit has reached its desired level, a logic zero for that bit will be sent to the wired-OR line (or a data one is inverted). When all bits output a data 0 (or a data one inverted), then the state machine knows to terminate the programming process. In embodiments where each processor communicates with eight sense modules, the state machine may (in some embodiments) need to read the wired-OR line eight times, or logic is added to processor 492 to accumulate the results of the associated bit lines such that the state machine need only read the wired-OR line one time. In some embodiments that have many sense modules, the wired-OR lines of the many sense modules can be grouped in sets of N sense modules, and the groups can then be grouped to form a binary tree.

[0042] During program or verify, the data to be programmed is stored in the set of data latches 494 from the data bus 420. The program operation, under the control of the state machine, comprises a series of programming voltage pulses (with increasing magnitudes) concurrently applied to the control gates of the addressed memory cells to that the memory cells are programmed at the same time. Each programming pulse is followed by a verify process to determine if the memory cell has been programmed to the desired state. Processor 492 monitors the verified memory state relative to the desired

memory state. When the two are in agreement, processor 492 sets the bit line latch 482 so as to cause the bit line to be pulled to a state designating program inhibit. This inhibits the memory cell coupled to the bit line from further programming even if it is subjected to programming pulses on its control gate. In other embodiments the processor initially loads the bit line latch 482 and the sense circuitry sets it to an inhibit value during the verify process.

[0043] Data latch stack 494 contains a stack of data latches corresponding to the sense module. In one embodiment, there are three (or four or another number) data latches per sense module 480. In some implementations (but not required), the data latches are implemented as a shift register so that the parallel data stored therein is converted to serial data for data bus 420, and vice versa. In one preferred embodiment, all the data latches corresponding to the read/write block of memory cells can be linked together to form a block shift register so that a block of data can be input or output by serial transfer. In particular, the bank of read/write modules is adapted so that each of its set of data latches will shift data into or out of the data bus in sequence as if they are part of a shift register for the entire read/write block.

[0044] Additional information about the structure and/or operations of various embodiments of non-volatile storage devices can be found in (1) United States Patent Application Pub. No. 2004/0057287, “Non-Volatile Memory And Method With Reduced Source Line Bias Errors,” published on March 25, 2004; (2) United States Patent Application Pub No. 2004/0109357, “Non-Volatile Memory And Method with Improved Sensing,” published on June 10, 2004; (3) U.S. Patent Application Pub. No. 20050169082; (4) U.S. Patent Application Pub. 2006/0221692, titled “Compensating for Coupling During Read Operations of Non-Volatile Memory,” Inventor Jian Chen, filed on April 5, 2005; and (5) U.S. Patent Application Pub. 2006/0158947, titled “Reference Sense Amplifier For Non-Volatile Memory, Inventors Siu Lung Chan and Raul-Adrian Cernea, filed on December 28, 2005. All five of the

immediately above-listed patent documents are incorporated herein by reference in their entirety.

[0045] Figure 5 depicts an exemplary structure of memory cell array 200. In one embodiment, the array of memory cells is divided into a large number of blocks of memory cells. As is common for flash EEPROM systems, the block is the unit of erase. That is, each block contains the minimum number of memory cells that are erased together. Other embodiments can use different units of erase.

[0046] As one example, the NAND flash EEPROM depicted in Fig. 5 is partitioned into 1,024 blocks. However, more or less than 1024 blocks can be used. In each block, in this example, there are 69,624 columns corresponding to bit lines BL0, BL1, ... BL69,623. In one embodiment, all of the bit lines of a block can be simultaneously selected during read and program operations. Memory cells along a common word line and connected to any bit line can be programmed (or read) at the same time (e.g., concurrently). In another embodiment, the bit lines are divided into even bit lines and odd bit lines. In an odd/even bit line architecture, memory cells along a common word line and connected to the odd bit lines are programmed at one time, while memory cells along a common word line and connected to even bit lines are programmed at another time.

[0047] Figure 5 shows four memory cells connected in series to form a NAND string. Although four cells are shown to be included in each NAND string, more or less than four can be used (e.g., 16, 32, 64, 128 or another number or memory cells can be on a NAND string). One terminal of the NAND string is connected to a corresponding bit line via a drain select gate (connected to select gate drain line SGD), and another terminal is connected to the source line via a source select gate (connected to select gate source line SGS).

[0048] Each block is typically divided into a number of pages. In one embodiment, a page is a unit of programming. One or more pages of data are typically stored in one row of memory cells. A page can store one or more sectors. A sector includes user data and overhead data. Overhead data typically includes an Error Correction Code (ECC) that has been calculated from the user data of the sector. The controller calculates the ECC when data is being programmed into the array, and also checks it when data is being read from the array. In some embodiments, the state machine, controller, or other component can calculate and check the ECC. In some alternatives, the ECCs and/or other overhead data are stored in different pages, or even different blocks, than the user data to which they pertain. A sector of user data is typically 512 bytes, corresponding to the size of a sector in magnetic disk drives. A large number of pages form a block, anywhere from 8 pages, for example, up to 32, 64, 128 or more pages. In one embodiment, each word line of a block is associated with one page. In another embodiment, each word line of a block is associated with 3 pages. In other embodiments, the word lines can be associated with other numbers of pages.

[0049] Some memory cells are slower to program or erase than others because of manufacturing variations among those memory cells, because those cells were previously erased to a lower threshold voltage than others, because of uneven wear among the cells within a page, or other reasons. And, of course, some memory cells cannot be programmed or erased whatsoever, because of a defect or other reason. Additionally, some memory cells program fast and can be over programmed, which may also cause an error. As mentioned above, error correction coding provides the capability of tolerating some number of failed cells, while still maintaining the memory as usable. In some applications, a page of data is programmed by repeatedly applying programming pulses until all memory cells on that page verify to the desired programmed state. In some implementation, programming and erasing time is

saved by terminating the sequence of programming or erasing pulses when the number of error memory cells that are not yet fully programmed or erased is fewer than the number of bits that are correctable.

[0050] Figure 6 is a flow chart describing one embodiment of a process for programming. In step 520, a request for programming is received from the Host, the Controller or other entity. In step 522, the Controller (or state machine or other entity) will determine which set of one or more blocks to store the data. In step 524, the data received for the request is programmed into one or more blocks of memory cells. In step 526, the data can be read. The dashed line between steps 524 and 526 indicates that there can be an unpredictable amount of time between programming and reading.

[0051] Figure 7 is a flow chart describing a process for programming a block of memory. The process of Figure 7 is performed one or more times during step 524 of Figure 6. In one example implementation, memory cells are pre-programmed in order to maintain even wear on the memory cells (step 550). In one embodiment, the memory cells are preprogrammed to the highest data state, a random pattern, or any other pattern. In some implementations, pre-programming need not be performed. Some embodiments do not implement pre-programming.

[0052] In step 552, memory cells are erased (in blocks or other units) prior to programming. Memory cells are erased in one embodiment by raising the p-well to an erase voltage (e.g., 20 volts) for a sufficient period of time and grounding the word lines of a selected block while the source and bit lines are floating. In blocks that are not selected to be erased, word lines are floated. Due to capacitive coupling, the unselected word lines, bit lines, select lines, and the common source line are also raised to a significant fraction of the erase voltage thereby impeding erase on blocks that are not selected to be erased. In blocks that are selected to be erased, a strong electric field is applied to the

tunnel oxide layers of selected memory cells and the selected memory cells are erased as electrons of the floating gates are emitted to the substrate side, typically by Fowler-Nordheim tunneling mechanism. As electrons are transferred from the floating gate to the p-well region, the threshold voltage of a selected cell is lowered. Erasing can be performed on the entire memory array, on individual blocks, or another unit of memory cells. In one embodiment, after erasing the memory cells, all of the erased memory cells in the block will be in state S0 (discussed below). One implementation of an erase process includes applying several erase pulses to the p-well and verifying between erase pulses whether the NAND strings are properly erased.

[0053] In step 554, soft programming is (optionally) performed to narrow the distribution of erased threshold voltages for the erased memory cells. Some memory cells may be in a deeper erased state than necessary as a result of the erase process. Soft programming can apply programming pulses to move the threshold voltage of the deeper erased memory cells to the erase threshold distribution. In step 556, the memory cells of the block are programmed. The programming can be performed in response to a request to program from the host, or in response to an internal process. After programming, the memory cells of the block can be read. Many different read processes known in the art can be used to read data. In some embodiments, the read process includes using ECC to correct errors. The data that is read is output to the hosts that requested the read operation. The ECC process can be performed by the state machine, the controller or another device. The erase-program cycle can happen many times without or independent of reading, the read process can occur many times without or independent of programming and the read process can happen any time after programming. The process of Figure 7 can be performed at the direction of the state machine using the various circuits described above. In other embodiments, the process of Figure

7 can be performed at the direction of the Controller using the various circuits described above.

[0054] At the end of a successful programming process (with verification), the threshold voltages of the memory cells should be within one or more distributions of threshold voltages for programmed memory cells or within a distribution of threshold voltages for erased memory cells, as appropriate. Figure 8 illustrates example threshold voltage distributions for the memory cell array when each memory cell stores three bits of data. Other embodiments, however, may use more or less than three bits of data per memory cell (e.g., such as three bits of data per memory cell).

[0055] In the example of Figure 8, each memory cell stores three bits of data; therefore, there are eight valid threshold voltage distributions, also called data states: S0, S1, S2, S3, S4, S5, S6 and S7. In one embodiment, data state S0 is below 0 volts and data states S1-S7 are above 0 volts. In other embodiments, all eight data states are above 0 volts, or other arrangements can be implemented. In one embodiment, the threshold voltage distribution for S0 is wider than for S1-S7. In one embodiment, S0 is for erased memory cells. Data is programmed from S0 to S1-S7.

[0056] Each data state corresponds to a unique value for the three data bits stored in the memory cell. In one embodiment, S0=111, S1=110, S2=101, S3=100, S4=011, S5=010, S6=001 and S7=000. Other mapping of data to states S0-S7 can also be used. The specific relationship between the data programmed into the memory cell and the threshold voltage levels of the cell depends upon the data encoding scheme adopted for the cells. For example, U.S. Patent No. 6,222,762 and U.S. Patent Application Publication No. 2004/0255090, "Tracking Cells For A Memory System," filed on June 13, 2003, both of which are incorporated herein by reference in their entirety, describe various data encoding schemes for multi-state flash memory cells. In

one embodiment, data values are assigned to the threshold voltage ranges using a Gray code assignment so that if the threshold voltage of a floating gate erroneously shifts to its neighboring threshold voltage distribution, only one bit will be affected. However, in other embodiments, Gray code is not used.

[0057] In one embodiment, all of the bits of data stored in a memory cell are stored in the same logical page. In other embodiments, each bit of data stored in a memory cell corresponds to different logical pages. Thus, a memory cell storing three bits of data would include data in a first page, data in a second page and data in a third page. In some embodiments, all of the memory cells connected to the same word line would store data in the same three pages of data. In some embodiments, the memory cells connected to a word line can be grouped into different sets of pages (e.g., by odd and even bit lines, or by other arrangements).

[0058] In some devices, the memory cells will be erased to state S0. From state S0, the memory cells can be programmed to any of states S1-S7. In one embodiment, known as full sequence programming, memory cells can be programmed from the erased state S0 directly to any of the programmed states S1-S7. For example, a population of memory cells to be programmed may first be erased so that all memory cells in the population are in erased state S0. While some memory cells are being programmed from state S0 to state S1, other memory cells are being programmed from state S0 to state S2, state S0 to state S3, state S0 to state S4, state S0 to state S5, state S0 to state S6, and state S0 to state S7. Full sequence programming is graphically depicted by the seven curved arrows of Fig. 8.

[0059] Figure 8 shows a set of verify target levels Vv1, Vv2, Vv3, Vv4, Vv5, Vv6, and Vv7. These verify levels are used as comparison levels (also known as target levels) during the programming process. For example, when programming memory cells to state S1, the system will check to see if the

threshold voltages of the memory cells have reached V_{v1} . If the threshold voltage of a memory cell has not reached V_{v1} , then programming will continue for that memory cell until its threshold voltage is greater than or equal to V_{v1} . If the threshold voltage of a memory cell has reached V_{v1} , then programming will stop for that memory cell. Verify target level V_{v2} is used for memory cells being programmed to state S2. Verify target level V_{v3} is used for memory cells being programmed to state S3. Verify target level V_{v4} is used for memory cells being programmed to state S4. Verify target level V_{v5} is used for memory cells being programmed to state S5. Verify target level V_{v6} is used for memory cells being programmed to state S6. Verify target level V_{v7} is used for memory cells being programmed to state S7.

[0060] Figure 8 also shows a set of read compare levels V_{r1} , V_{r2} , V_{r3} , V_{r4} , V_{r5} , V_{r6} , and V_{r7} . These read compare levels are used as comparison levels during the read process. By testing whether the memory cells turn on or remain off in response to the read compare levels V_{r1} , V_{r2} , V_{r3} , V_{r4} , V_{r5} , V_{r6} , and V_{r7} being separately applied to the control gates of the memory cells, the system can determine which states that memory cells are storing data for.

[0061] In general, during verify operations and read operations, the selected word line is connected to a voltage, a level of which is specified for each read operation (e.g., see read compare levels V_{r1} , V_{r2} , V_{r3} , V_{r4} , V_{r5} , V_{r6} , and V_{r7} of Fig. 8) or verify operation (e.g. see verify target levels V_{v1} , V_{v2} , V_{v3} , V_{v4} , V_{v5} , V_{v6} , and V_{v7} of Fig. 8) in order to determine whether a threshold voltage of the concerned memory cell has reached such level. After applying the word line voltage, the conduction current of the memory cell is measured to determine whether the memory cell turned on in response to the voltage applied to the word line. If the conduction current is measured to be greater than a certain value, then it is assumed that the memory cell turned on and the voltage applied to the word line is greater than the threshold voltage of the memory cell. If the conduction current is not measured to be greater than

the certain value, then it is assumed that the memory cell did not turn on and the voltage applied to the word line is not greater than the threshold voltage of the memory cell. During a read or verify process, the unselected memory cells are provided with one or more read pass voltages at their control gates so that these memory cells will operate as pass gates (e.g., conducting current regardless of whether they are programmed or erased).

[0062] There are many ways to measure the conduction current of a memory cell during a read or verify operation. In one example, the conduction current of a memory cell is measured by the rate it discharges or charges a dedicated capacitor in the sense amplifier that is in communication with the bit line. In another example, the conduction current of the selected memory cell allows (or fails to allow) the NAND string that includes the memory cell to discharge a corresponding bit line. The voltage on the bit line is measured after a period of time to see whether it has been discharged or not. Note that the technology described herein can be used with different methods known in the art for verifying/reading. More information about verifying/reading can be found in the following patent documents that are incorporated herein by reference in their entirety: (1) United States Patent Application Pub. No. 2004/0057287; (2) United States Patent Application Pub No. 2004/0109357; (3) U.S. Patent Application Pub. No. 2005/0169082; and (4) U.S. Patent Application Pub. No. 2006/0221692. The read and verify operations described above are performed according to techniques known in the art. Thus, many of the details explained can be varied by one skilled in the art. Other read and verify techniques known in the art can also be used.

[0063] In some embodiments, the program voltage applied to the control gate includes a series of pulses that are increased in magnitude with each successive pulse by a predetermined step size (e.g. 0.2v, 0.3v, 0.4v, or others). Between pulses, some memory systems will verify whether the individual memory cells have reached their respective target threshold voltage ranges.

For example, Figure 9 shows a portion of a signal applied to the control gates of a plurality of memory cells connected to a common word line. Figure 9 shows programming pulses 564, 565 and 566, with a set of verify pulses between the programming pulses. When performing full sequence programming in one embodiment, the verification process between programming pulses will test for each of the threshold voltage distribution (data states) S1-S7. Therefore, Figure 9 shows seven verify pulses that have magnitudes corresponding to verify target levels Vv1, Vv2, Vv3, Vv4, Vv5, Vv6, and Vv7. In some embodiments, one or more of the verify operations can be skipped (and, therefore one or more of the verify pulses can be skipped) because the verify operation is not necessary or superfluous. For example, if none of the memory cells being programmed according to Figure 8 have reached Vv2, there is no reason to verify at Vv7. More information about intelligent verification schemes that skip verification for one or more states can be found in the following patent documents which are incorporated herein by reference in their entirety: U.S. Patent 7,073,103; U.S. Patent 7,224,614; U.S. Patent 7,310,255; U.S. Patent 7,301,817; U.S. Patent App. 2004/0109362; and U.S. Patent App. 2009/0147573.

[0064] Figure 8 shows a programming process that includes one phase where all memory cells connected to the same word line are programmed concurrently during that one phase. Figures 10A-E illustrates a multi-phase programming approach. In this embodiment, the programming process includes three phases. Prior to programming, the memory cells are erased so that all memory cells connected to a common word line are in an erased threshold voltage distribution E, as depicted in Figure 10A. During the first phase of programming, those memory cells whose targets (due to the data to be stored in those memory cells) are data states S4, S5, S6 or S7 are programmed to an intermediate state IM. Those memory cells are targeted for data states S0, S1, S2 or S3 and remain in the erased threshold voltage distribution E. The

first phase is graphically depicted by Figure 10B. Memory cells being programmed to intermediate state IM are programmed to a target threshold voltage of V_{vIM} .

[0065] During the second phase of the programming process of Figures 10A-E, those memory cells that are in the erased threshold voltage distribution E are programmed to their target data states. For example, those memory cells to be programmed to data state S3 are programmed from erased threshold voltage distribution E to data state S3, those memory cells to be programmed to data state S2 are programmed from erased threshold voltage distribution E to data state S2, those memory cells to be programmed to data state S1 are programmed from erase threshold voltage distribution E to data state S1, and those memory cells to be in data state S0 are not programmed during the second phase of the programming process. Thus, erased threshold voltage distribution E becomes data state S0. Also, during the second phase, memory cells are programmed from the intermediate state IM to various data states S4-S7. For example, those memory cells to be programmed to data state S7 are programmed from the intermediate state IM to data state S7, those memory cells targeted to be in data state S6 are programmed from intermediate state IM to data state S6, both memory cells to be programmed to data state S5 are programmed from intermediate state IM to data state S5, and those memory cells to be programmed to data state S4 are programmed from intermediate state IM to data state S4. This second phase of programming is illustrated in Figure 10C.

[0066] As can be seen in Figure 10C, at the end of the second phase of programming data states S1-S7 overlap with neighboring data states. For example, data state S1 overlaps with data state S2, data state S2 overlaps with data states S1 and S3, data state S3 overlaps with data states S2 and S4, data state S4 overlaps with data states S3 and S5, data state S5 overlaps with data

states S4 and S6, and data state S6 overlaps with data states S5 and S7. In some embodiments, all or some of the data states do not overlap.

[0067] In the third phase of programming, each of data states S1-S7 are tightened so that they no longer overlap with neighboring states. This is depicted graphically by Figure 10D. The final result of the three phase programming process is depicted in step 10E, which shows data states S0-S7. In some embodiments, data state S0 is wider than data states S1-S7.

[0068] In some embodiments, those memory cells to be programmed to data state S4 are not programmed during the second phase and, therefore, remain in intermediate state IM. During the third programming phase, the memory cells are programmed from IM to S4. In other embodiments, memory cells destined for other states can also remain in IM or E during the second phase.

[0069] Figure 11 is a flow chart describing one embodiment of a process for performing programming on memory cells connected to a common word line to one or more targets (e.g., data states or threshold voltage ranges). The process of Figure 11 can be performed one or multiple times during step 556 of Figure 7. For example, the process of Figure 11 can be used to program memory cells (e.g., full sequence programming) from state S0 directly to any of states S1-S7. Alternatively, the process of Figure 11 can be used to perform one or each of the phases of the process of Fig. 10A-E. For example, when performing the process of Fig. 10A, the process of Fig. 11 is used to implement the first phase that includes programming some of the memory cells from state E to state IM. The process of Fig. 11 can then be used again to implement the second phase that includes programming some of the memory cells from state E to states S1-S3 and from state IM to states S4-S7. The process of Fig. 11 can be used again to adjust states S1-S7 in the third phase

(see Fig. 10D). The process of Fig. 11 can also be used with other multi-phase programming processes.

[0070] Typically, the program voltage applied to the control gate during a program operation is applied as a series of program pulses. Between programming pulses are a set of verify pulses to perform verification. In many implementations, the magnitude of the program pulses is increased with each successive pulse by a predetermined step size. In step 570 of Figure 11, the programming voltage (V_{pgm}) is initialized to the starting magnitude (e.g., ~12-16V or another suitable level) and a program counter PC maintained by state machine 222 is initialized at 1. In step 572, a program pulse of the program signal V_{pgm} is applied to the selected word line (the word line selected for programming). In one embodiment, the group of memory cells being programmed concurrently are all connected to the same word line (the selected word line). The unselected word lines receive one or more boosting voltages (e.g., ~7-11 volts) to perform boosting schemes known in the art. If a memory cell should be programmed, then the corresponding bit line is grounded. On the other hand, if the memory cell should remain at its current threshold voltage, then the corresponding bit line is connected to V_{dd} to inhibit programming. In step 572, the program pulse is concurrently applied to all memory cells connected to the selected word line so that all of the memory cells connected to the selected word line are programmed concurrently. That is, they are programmed at the same time (or during overlapping times). In this manner all of the memory cells connected to the selected word line will concurrently have their threshold voltage change, unless they have been locked out from programming.

[0071] In step 574, the appropriate memory cells are verified using the appropriate set of target levels to perform one or more verify operations. In one embodiment, the verification process is performed by applying the testing whether the threshold voltages of the memory cells selected for programming

have reached the appropriate verify compare voltage (V_{v1} , V_{v2} , V_{v3} , V_{v4} , V_{v5} , V_{v6} , and V_{v7}).

[0072] In step 576, it is determined whether all the memory cells have reached their target threshold voltages (pass). If so, the programming process is complete and successful because all selected memory cells were programmed and verified to their target states. A status of "PASS" is reported in step 578. If, in 576, it is determined that not all of the memory cells have reached their target threshold voltages (fail), then the programming process continues to step 580.

[0073] In step 580, the system counts the number of memory cells that have not yet reached their respective target threshold voltage distribution. That is, the system counts the number of cells that have failed the verify process. This counting can be done by the state machine, the controller, or other logic. In one implementation, each of the sense block 300 (see Fig. 3) will store the status (pass/fail) of their respective cells. These values can be counted using a digital counter. As described above, many of the sense blocks have an output signal that is wire-Or'd together. Thus, checking one line can indicate that no cells of a large group of cells have failed verify. By appropriately organizing the lines being wired-Or together (e.g., a binary tree-like structure), a binary search method can be used to determine the number of cells that have failed. In such a manner, if a small number of cells failed, the counting is completed rapidly. If a large number of cells failed, the counting takes a longer time. More information can be found in United States Patent Publication 2008/0126676, incorporated herein by reference in its entirety. In another alternative, each of the sense amplifiers can output an analog voltage or current if its corresponding memory cell has failed and an analog voltage or current summing circuit can be used to count the number of memory cells that have failed.

[0074] In one embodiment, there is one total count, which reflects the total number of memory cells currently being programmed that have failed the last verify step. In another embodiment, separate counts are kept for each data state.

[0075] In step 582, it is determined whether the count from step 580 is less than or equal to a predetermined limit. In one embodiment, the predetermined limit is the number of bits that can be corrected by ECC during a read process for the page of memory cells. If the number of failed cells is less than or equal to the predetermined limit, then the programming process can stop and a status of "PASS" is reported in step 578. In this situation, enough memory cells programmed correctly such that the few remaining memory cells that have not been completely programmed can be corrected using ECC during the read process. In some embodiments, step 580 will count the number of failed cells for each sector, each target data state or other unit, and those counts will individually or collectively be compared to a threshold in step 582.

[0076] In another embodiment, the predetermined limit can be less than the number of bits that can be corrected by ECC during a read process to allow for future errors. When programming less than all of the memory cells for a page, or comparing a count for only one data state (or less than all states), then the predetermined limit can be a portion (pro-rata or not pro-rata) of the number of bits that can be corrected by ECC during a read process for the page of memory cells. In some embodiments, the limit is not predetermined. Instead, it changes based on the number of errors already counted for the page, the number of program-erase cycles performed, temperature or other criteria.

[0077] If number of failed memory cells is not less than the predetermined limit, then the programming process continues at step 584 and the program counter PC is checked against the program limit value (PL). Examples of

program limit values include 20 and 30 ; however, other values can be used. If the program counter PC is not less than the program limit value PL, then the program process is considered to have failed and a status of FAIL is reported in step 588. If the program counter PC is less than the program limit value PL, then the process continues at step 586 during which time the Program Counter PC is incremented by 1 and the program voltage Vpgm is stepped up to the next magnitude. For example, the next pulse will have a magnitude greater than the previous pulse by a step size (e.g., a step size of 0.1-0.4 volts). After step 586, the process loops back to step 572 and another program pulse is applied to the selected word line.

[0078] Figure 12 is a flow chart describing one embodiment of a process for reading data. The depicted method reduces the effects of read disturb (described above).

[0079] In many memory systems, the end word lines (e.g. word lines at or close to the select gates of a NAND string) are wider than the middle word lines (word lines that are between the end word lines) in a memory array due to process limitations. In other embodiments, other critical dimensions can also vary for the end word lines as compared to the middle word lines. As memory cells scale down to smaller sizes, the difference in width between the end and middle word lines will become even more of a disparity. In NAND flash memory, the wider word lines at the end will provide a stronger coupling between the control gate and floating gate, which results in faster programming and a higher chance of Read Disturb occurring. Although error correction (ECC) can be used to fix errors in the data, if there are too many errors, even ECC will not work.

[0080] Previous systems have used dynamic read compare levels to reduce failures. For example, Vr1, Vr2, Vr3, ... are periodically recomputed.

However, this may not be sufficient if the Read Disturb is severe enough on the end word lines.

[0081] A memory system could also lower the pass voltage (e.g. V_{read} – see below) applied to unselected word lines to reduce the overall Read Disturb. However, this would cause a higher NAND string resistance to the downscaling of the pass voltage, thereby reducing the accuracy of the read process.

[0082] To reduce the effects of Read Disturb due to the end word lines being wider, the process of Figure 12 proposes to use a lower pass voltage at the end of the NAND strings as compared to the middle of the NAND strings. Step 600 of Figure 12 includes applying voltage signals to the source line, source select line SGS and drain select line SGD (see Figures 2 and 5). In step 602, a lower read pass voltage, V_{readL} , is applied to memory cells at the ends of the NAND string. In step 604, the standard read pass voltage, V_{read} , is applied to the middle memory cells, which are those memory cells between the ends of the NAND string that are not selected for reading. In step 606, a higher read pass voltage, V_{readK} , is applied to those memory cells of the NAND string that are neighbors to the selected memory cell. In step 608, the read compare voltage, V_{cgr} , is applied to the selected memory cell. In step 610, the system will sense the current through the selected memory cell in response to the voltages applied in steps 600-608.

[0083] In many embodiments, the system will read multiple memory cells at the same time. Therefore, the process of 600-610 will be performed concurrently on multiple NAND strings of the same block such that multiple memory cells will be read concurrently.

[0084] Figure 13 shows three NAND strings 650, 652 and 654 of a block of memory cells implementing the process of Figure 12. In the example embodiment of Figure 13, a NAND string will include $x+1$ memory cells.

Therefore, the block of NAND strings will include $x+1$ word lines (WL0-WL x). In the depicted example, word line WL n is selected for reading; therefore, all the memory cells connected to WL n will be read. As per step 608 of Figure 12, Figure 13 shows WL n receiving V cgr , the read compare voltage. As per step 606 of Figure 12, Figure 13 shows neighboring word lines WL $n-1$ and WL $n+1$ receiving the higher read pass voltage, V $readK$. As per step 604 Figure 12, Figure 13 shows the word lines (WL1, WL2...WL $n-2$, WL $n+2$,...WL $x-3$, WL $x-2$, WL $x-1$) that are not connected to end memory cells receiving the standard read pass voltage, V $read$. As per step 602 of Figure 12, Figure 13 shows the end word lines (in the example, the word lines at the extreme end of the NAND string), WL0 and WL x , receiving the lower read pass voltage V $readL$. In this embodiment, the various voltages V $read$, V $readL$ and V $readK$ are provided to the control gates of the respective memory cells by applying the voltages to the word lines, which are connected to the control gates of memory cells. As seen from Figure 13, each word line is connected to the control gate of multiple memory cells so that the read and programming operations are performed in parallel.

[0085] Figure 14 is a timing diagram depicting the behavior of various signals during one iteration of a read or verify operation (e.g., the process of Figure 12). For example, if the memory cells are binary memory cells, the process of Fig. 14 may be performed in parallel for each memory cell during a read or verify process. If the memory cells are multi-state memory cells, the process of Fig. 14 may be performed multiple times for each memory cell in parallel during a read or verify process. For example, when reading data from a memory cell with eight states, the read process may be performed once with V cgr =V $r1$, once with V cgr =V $r2$, once with V cgr =V $r3$, once with V cgr =V $r4$, once with V cgr =V $r5$, once with V cgr =V $r6$, and once with V cgr =V $r7$. Other sets of read values can also be used and some embodiments will perform less

than all of the read operations based on a need to read only a subset of pages of data or other reasons.

[0086] Figure 14 shows signals SGD, WL_unsel, WL_unsel_neighbor, WL_unsel_end, WLn, SGS, Selected BL, and Source starting at Vss (approximately 0 volts). SGD represents the signal on the drain select line connected to the gate of the drain select gate. SGS represents the signal on the source select line connected to the gate of the source select gate. WLn is the word line selected for reading/verification. WL_unsel_neighbor represents the unselected word lines that are adjacent to the selected word line. WL_unsel_end represents the unselected word lines that are connected to memory cells at the end of the NAND strings. WL_unsel represents the unselected word lines that are not WL_unsel_neighbor and WL_unsel_end. Selected_BL is the bit line selected for reading/verification. Source is the source line for the memory cells.

[0087] Figure 14 describes the behavior of a system that measures the conduction current of a memory cell by determining whether the bit line has appropriately discharged. At time t1 of Fig. 14, SGD is raised to Vdd (e.g., approximately 3.5 volts) or another voltage, typically in the 3-5V range, the unselected word lines (WL_unsel) are raised to Vread (e.g., approximately 7.4 volts), the unselected word lines that are next to the selected word line (WL_unsel_neighbor) are raised to VreadK (e.g., $\sim Vread + 0.6$ volts), the unselected word lines at the end of the NAND string (WL_unsel_end) are raised to VreadL (e.g., $\sim Vread - 0.1v$), the selected word line WLn is raised to Vcgr, and the selected bit line Selected BL is precharged to approximately 0.7 volts. The voltages Vread, VreadK and VreadL act as pass voltages because they cause the unselected memory cells to turn on and act as pass gates. At time t2, the source select gate is turned on by raising SGS to Vdd. This provides a path to reduce the charge on the bit line. If the threshold voltage of the memory cell selected for reading is greater than Vcgr, then the selected

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memory cell will not turn on (or at least will not turn on sufficiently) and the bit line will not discharge (or at least will not discharge sufficiently), as depicted by signal line 690. If the threshold voltage in the memory cell selected for reading is below V_{cgr} , then the memory cell selected for reading will turn on (conduct) and the bit line voltage will decrease, as depicted by curve 692. At some point after time t_2 and prior to time t_3 (as determined by the particular implementation), the appropriate sense amplifier will determine whether the bit line voltage has decreased by a sufficient amount. At time t_3 , the depicted signals will be lowered to V_{ss} (or another value for standby or recovery). Note that in other embodiments, the timing of some of the signals can be changed.

[0088] Figure 15 is a schematic of the same three NAND strings 650, 652 and 654 implementing the same embodiment as Figure 14; however, in the situation depicted in Figure 15, WL1 is selected for programming. Since it is selected for programming, word line WL1 receives the read compare voltage V_{cgr} . In the situation of Figure 15, the end word line WL0 is the neighbor word line to the selected word line so word line WL0 will receive the higher read pass voltage V_{readK} . The other neighbor word line, WL2, will also receive the higher read pass voltage V_{readK} . Word lines WL3-WL x -1 will receive V_{read} . The other end word line, WL x , will receive V_{readL} .

[0089] If WL0 is selected for programming, then WL0 will receive V_{cgr} , WL1 will receive V_{readK} , WL2-WL x -1 will receive V_{read} , and WL x will receive V_{readL} . Similarly, if WL x is selected for reading, then WL x will receive V_{cgr} , WL x -1 will receive V_{readK} , WL x -2-WL1 will receive V_{read} , and WL0 will receive V_{readL} .

[0090] Figure 16-22 and 24-28 depict other embodiments for implementing the read process. For example, in the embodiment of Figures 16-19, the end memory cells for a NAND string include a set of three memory

cells at each side of the NAND string (as compared to the embodiment of Figure 13 where the end memory cells include only one memory cell each end). In one embodiment, all the memory cells that are end memory cells will receive VreadL. In another embodiment, as depicted in Figure 16, the memory cells at the end of NAND string will receive a set of lower read pass voltages applied as a gradient. For example, Figure 16 shows word line WL0 (the extreme end of the NAND string) receiving Vread-3 Δ , WL1 receiving Vread-2 Δ and WL2 receiving Vread- Δ . Similarly, WLx receives Vread-3 Δ , WLx-1 receives Vread-2 Δ and WLx-2 receives Vread- Δ . There are many suitable values can be used for Δ . In one embodiment, Δ is equal to 0.1 volts and Vread is equal to 7.4; therefore, WL0 receives 7.1 volts [7.4-3(.1)], WL1 receives 7.2 volts [7.4-2(.1)], WL2 receives 7.3[7.4-(.1)], and WL3 receives 7.4 volts. in other embodiments, Δ can be equal to other values (e.g., 0.2, 0.3, 0.4, etc.).

[0091] Figure 17 shows the same embodiment as Figure 16, in the situation where WL2 is the selected word line and memory cells connected to WL2 will be read. In this example, WL2 will receive Vcgr and its two neighbors (WL1 and WL3) will receive VreadK. WL0 and WLx will receive Vread-3 Δ . WLx-1 will receive Vread-2 Δ and WLx-2 will receive Vread- Δ . WL4 (note depicted) through WLx-3 receive Vread.

[0092] Figure 18 depicts the same embodiment as Figures 16 and 17, but in the situation where WL1 is selected for reading. Therefore, WL1 will receive Vcgr and its two neighbors (WL0 and WL2) will receive VreadK. WLx will receive Vread-3 Δ , WLx-1 will receive Vread-2 Δ , and WLx-2 will receive Vread- Δ . WL3 through WLx-3 receive Vread.

[0093] Figure 19 shows the same embodiments as Figure 16-18, but in a situation where WL0 is selected for reading. Therefore, WL0 will receive Vcgr and its one neighbor (WL1) will receive VreadK. WLx will receive

Vread-3 Δ , WLx-1 will receive Vread-2 Δ and WLx-2 will receive Vread- Δ . The other word lines (WL2-WLx-3) will receive Vread.

[0094] Figure 20 shows another embodiment in which the set of end memory cells includes two memory cells at each end of the NAND string. In this embodiment, word lines at the extreme ends WL0 and WLx will receive Vread-2 Δ as their read pass voltage. WL1 and WLx-1 will receive Vread- Δ . In this embodiment, the set of lower read pass voltages includes Vread-2 Δ and Vread- Δ . Other than the selected memory cell and its neighbors, the remaining word lines will receive the standard read pass voltage Vread. The selected word line, WLn will receive Vcgr. The neighboring word line to the selected word line, WLn+1 and WLn-1, will receive VreadK.

[0095] Figure 21 depicts the same embodiment as Figure 20, but in a situation where WL2 is selected for reading. In this case, WL1 and WL3 are neighbors to WL2 so they will receive VreadK. WL0 will receive Vread-2 Δ because it is in the set of end word lines. The end word line WLx will receive Vread-2 Δ and WLx-1 will receive Vread- Δ .

[0096] Figure 22 shows the same embodiment as Figures 20 and 21, but in the situation where WL1 is selected for programming. Therefore, WL1 will receive Vcgr and its two neighbors (WL0 and WL2) will receive VreadK. Even though WL0 is in the set of end word lines, since it is a neighboring word line it will receive VreadK rather than a lower read pass voltage. The other side of the NAND string will remain unchanged from the earlier examples. Therefore, WLx will receive Vread-2 Δ and WLx-1 will receive Vread- Δ . The remaining word lines will receive Vread. Note that in Figures 15-22, word lines WL0 and WLx are drawn thicker than the other word lines in order to represent that they are wider than the other word lines.

[0097] Figure 23 shows another embodiment of a block of memory cells. This block includes dummy memory cells and dummy word lines. In one

embodiment, as depicted in Figure 23, there are one or more dummy word lines at one end of a NAND string and one or more dummy word lines at another end of a NAND string. For example, WLd0 and WLd1 of Figure 23 are both dummy word lines connected to dummy memory cells. These dummy memory cells do not store user data. The remaining memory cells on a NAND string (other than the dummy memory cells) can be referred to as data memory cells because they store user data or system data. The embodiments described above with respect to Figures 12-22 can be used with memory systems that include dummy memory cells (as depicted in Figure 23 or another arrangement). In one example set of embodiments, the dummy word lines (e.g. WLd0 and WLd1) will receive a voltage Vsg (4.6 volts – 5.6 volts) during the read process. Therefore, the process of Figure 12 would include an additional step of applying Vsg to the dummy word lines. For example, Figure 24 shows the embodiment of Figures 12-14 with the inclusion of dummy word lines receiving Vsg. The embodiments of Figures 15 -22 can also include dummy word lines receiving Vsg.

[0098] In another set of embodiments, it is proposed to apply VreadK to the dummy word lines when performing a read process to read data from memory cells connected to an end word line and using Vsg on the dummy word lines when reading from memory cells connect to word lines in the middle of a NAND string. When performing a read process (read or verify) on memory cells connected to the end word lines (WL0 or WLx), using a higher voltage on the dummy word line (such as VreadK) will shift down the erase state (e.g. S0 of Figure 8) for memory cells connected to the edge word lines to gain more margin to combat Read Disturb for memory cells connected to the end word lines WL0 and WLx. To further enhance this effect, it may be preferred to use a higher voltage than VreadK on the dummy word lines. For example, the dummy word lines could receive VreadK+ Δ (the word $\Delta + 0.1$ volts or another value suitable to a particular implementation).

[0099] Figure 25 shows one example of an embodiment which applies a higher voltage to the dummy word lines when reading an end word line. For example, Figure 25 shows end word line WL0 selected for reading. Therefore, WL0 will receive Vcgr and its neighbor, WL1, will receive VreadK. The remaining word lines (other than dummy word lines) will receive Vread (the standard read pass voltage). In this embodiment, the dummy word line next to WL0 (WL_d0) will receive the higher voltage VreadK+ Δ . The dummy word line on the other side of the NAND string, WL_d1, can receive Vsg or VreadK+ Δ . It may be preferable to use Vsg as it is a lower voltage and will generally require less power. If WLx is selected for reading, then WL_d1 would receive VreadK+ Δ , WLx would receive Vcgr, WLx-1 will receive VreadK, WL_d0 will receive Vsg or VreadK+ Δ , and the remaining word lines would receive Vread.

[00100] If a middle word line is selected for reading, then the dummy word lines (WLd0 and WLd1) will receive Vsg, as depicted by Figure 26. In the situation depicted in Figure 26, WLn is selected for reading. Therefore, WLn receives Vcgr, WLn+1 receives VreadK, WLn-1 receives VreadK and the remaining word lines will receive Vread.

[00101] Figure 27 shows the situation where WLx is selected for reading and, therefore, receives Vcgr. Its neighbor, WLx-1 will receive VreadK. WLx-2 through WL0 will receive Vread. The dummy word line next to the selected word line, WL_d1, will receive VreadK+ Δ . The opposite side dummy word line can receive Vsg or VreadK+ Δ .

[00102] The technique of driving a higher voltage on a dummy word lines when the end word lines are being programmed can be used separate from the technique for using one or more lower read pass voltages for the end word lines or can be used in combination with the technique for using one or more lower read pass voltages for the end word lines. For example, Figure 28 shows

one example embodiment that uses both techniques. In this example, an end word line, WL0 is selected for reading. Therefore, WL0 receives V_{cgr} . Its adjacent dummy word line, WL_d0 will receive $V_{readK} + \Delta$. Its neighboring data word line, WL1 will receive V_{readK} . Word lines WL2-WL_x-1 will receive the standard read pass voltage V_{read} . The end word line on the opposite side of the NAND string, WL_x, will receive the lower read pass voltage V_{readL} . The opposite side dummy word line, WL_d1, can receive V_{sg} or $V_{readK} + \Delta$. In other embodiments, the technique for driving a higher voltage on the dummy word lines can be used with any of the other embodiments discussed above including those depicted in Figures 16-22 and 24-27.

[00103] The above described embodiments show that although end memory cells (or end word lines) receive a lower read pass voltage, a majority of the memory cells (and word lines) for a NAND string receive the standard read pass voltage. In most cases, memory cells (and word lines) on both sides of the memory cell selected for programming receive the standard read pass voltage.

[00104] For purposes of clarity, the portion of the NAND string that is at the end of the NAND string can be referred to as an end zone. There will be a first end zone at a first end of a NAND string and a second end zone at a second side of a NAND string. As described above, each end zone can include one, two or three memory cells. In some embodiments, an end zone can include more than three memory cells.

[00105] The processes described above can be used as part of a read process or as part of a verify process during programming.

[00106] One embodiment includes a method of reading non-volatile storage, comprising: applying a read compare voltage to a selected data memory cell of a NAND string; applying a first set of one or more read pass

voltages to one or more unselected data memory cells at a first end of the NAND string and on a first side of the selected data memory cell; and applying a second set of one or more read pass voltages to multiple unselected data memory cells on the NAND string that are on the first side of the selected data memory cell, the second set of one or more read pass voltages are all higher voltages than the first set of one or more read pass voltages.

[00107] One embodiment includes a non-volatile storage system, comprising: a plurality of non-volatile storage elements; a plurality of word lines connected to the non-volatile storage elements; and one or more managing circuits in communication with the non-volatile storage elements via the word lines to program and read the non-volatile storage elements. The one or more managing circuits apply a read compare voltage to a selected word line connected to selected data memory cells of a plurality of NAND strings. The one or more managing circuits apply a first set of one or more read pass voltages to one or more unselected word lines connected to unselected data memory cells at a first end of the NAND strings and on a first side of the selected data memory cells. The one or more managing circuits apply a second set of one or more read pass voltages to multiple unselected word lines connected to unselected data memory cells on the NAND strings that are between the selected data memory cells and the unselected data memory cells at the first end of the NAND strings. The second set of one or more read pass voltages are all higher than the first set of one or more read pass voltages.

[00108] One embodiment includes a method of reading non-volatile storage, comprising: applying a read compare voltage to a selected data memory cell of a NAND string; applying a first set of one or more read pass voltages to unselected data memory cells at both ends of the NAND string; and applying a second set of one or more read pass voltages to unselected data memory cells between both ends of the NAND string and on both sides of the

selected data memory cell, the second set of one or more read pass voltages are all higher than the first set of one or more read pass voltages.

[00109] One embodiment includes a method of reading non-volatile storage, comprising: applying a read compare voltage to a selected word line that is connected to selected data memory cells of a plurality of NAND strings, the NAND string is connected to word lines of a block, the block includes dummy word lines; applying a set of one or more read pass voltages to unselected word lines connected to unselected data memory cells of the NAND strings; and applying a higher read pass voltage to dummy word lines when reading data memory cells at extreme ends of the NAND strings, the dummy word lines are connected to dummy cells that are not intended to store user data.

[00110] The foregoing detailed description has been presented for purposes of illustration and description. It is not intended to be exhaustive or limiting to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. The described embodiments were chosen in order to best explain the principles of the disclosed technology and its practical application, to thereby enable others skilled in the art to best utilize the technology in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope be defined by the claims appended hereto.

CLAIMS

We claim:

1. A method of reading non-volatile storage, comprising:
applying a read compare voltage to a selected data memory cell of a NAND string;
applying a first set of one or more read pass voltages to one or more unselected data memory cells at a first end of the NAND string and on a first side of the selected data memory cell; and
applying a second set of one or more read pass voltages to multiple unselected data memory cells on the NAND string that are on the first side of the selected data memory cell, the second set of one or more read pass voltages are all higher voltages than the first set of one or more read pass voltages.
2. The method of claim 1, further comprising:
applying one or more read pass voltages, that are all higher than the first set of one or more read pass voltages, to multiple unselected data memory cells on the NAND string that are on a second side of the selected data memory cell.
3. The method of claims 1 or 2, wherein:
a majority of the data memory cells on the NAND string that are on the first side of the selected data memory cell receive the second set of one or more read pass voltages.
4. The method of any of claims 1-3, wherein:
the NAND string includes a first end zone of one or more data memory cells on the first side of the selected data memory cell and a second end zone of one or more data memory cells on a second side of the selected data memory cell; and
all unselected data memory cells of the NAND string that are between

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the first end zone and second end zone receive the second set of one or more read pass voltages during a read operation.

5. The method of any of claims 1-4, wherein:
the first set of one or more read pass voltages includes one read pass voltage; and
the second set of one or more read pass voltages includes one read pass voltage.

6. The method of any of claims 1-3, wherein:
the NAND string includes a first end zone of one or more data memory cells on the first side of the selected data memory cell and a second end zone of one or more data memory cells on a second side of the selected data memory cell;
the first end zone and the second end zone each include three memory cells receiving the first set of one or more read pass voltages;
a first data memory cell of the first end zone and a first memory cell of the second end zone receive a first read pass voltage of the first set of one or more read pass voltages;
a second data memory cell of the first end zone and a second memory cell of the second end zone receive a second read pass voltage of the first set of one or more read pass voltages ;and
a third data memory cell of the first end zone and a third memory cell of the second end zone receive a third read pass voltage of the first set of one or more read pass voltages.

7. The method of claim 6, wherein:
the first read pass voltage > the second read pass voltage > the third read pass voltage;
the second data memory cell of each end zone is outside the first data

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memory cell and inside the third data memory cell; and

the third data memory cell of each end zone is at the extreme end of the NAND string;

8. The method of any of claims 1-3, wherein:
- the NAND string includes two end zones;
 - the two end zones each include two memory cells receiving the first set of one or more read pass voltages;
 - a first memory cell of each end zone receives a first read pass voltage of the first set of one or more read pass voltages; and
 - a second memory cell of each end zone receives a second read pass voltage of the first set of one or more read pass voltages.

9. The method of any of claims 1-8, wherein:
- the NAND string is connected to word lines of a block;
 - the block includes dummy word lines; and
 - the method includes applying a higher read pass voltage to dummy word lines when reading a data memory cell at an extreme end of the NAND string.

10. A non-volatile storage system, comprising:
- a plurality of non-volatile storage elements;
 - a plurality of word lines connected to the non-volatile storage elements;
- and

one or more managing circuits in communication with the non-volatile storage elements via the word lines to program and read the non-volatile storage elements, the one or more managing circuits apply a read compare voltage to a selected word line connected to selected data memory cells of a plurality of NAND strings, the one or more managing circuits apply a first set of one or more read pass voltages to one or more unselected word lines connected to unselected data memory cells at a first end of the NAND strings and on a first

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side of the selected data memory cells, the one or more managing circuits apply a second set of one or more read pass voltages to multiple unselected word lines connected to unselected data memory cells on the NAND strings that are between the selected data memory cells and the unselected data memory cells at the first end of the NAND strings, the second set of one or more read pass voltages are all higher than the first set of one or more read pass voltages.

11. The non-volatile storage system of claim 10, wherein:
 - a majority of the word lines that are on the first side of the selected word line receive the second set of one or more read pass voltages.
12. The non-volatile storage system of claims 10 or 11, wherein:
 - the NAND strings each include a first end zone of one or more data memory cells on the first side of the selected data memory cell and a second end zone of one or more data memory cells on a second side of the selected data memory cell;
 - the first end zone and the second end zone of each NAND string each include three memory cells receiving the first set of one or more read pass voltages;
 - a first data memory cell of the first end zone and a first memory cell of the second end zone receive a first read pass voltage of the first set of one or more read pass voltages;
 - a second data memory cell of the first end zone and a second memory cell of the second end zone receive a second read pass voltage of the first set of one or more read pass voltages;
 - a third data memory cell of the first end zone and a third memory cell of the second end zone receive a third read pass voltage of the first set of one or more read pass voltages;
 - the first read pass voltage > the second read pass voltage > the third read pass voltage;
 - the second data memory cell of each end zone is outside the first data

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memory cell and inside the third data memory cell; and

the third data memory cell of each end zone is at the extreme end of the NAND string.

13. The non-volatile storage system of claims 10 or 11, wherein:

the NAND strings each include a first end zone of one or more data memory cells on the first side of the selected data memory cell and a second end zone of one or more data memory cells on a second side of the selected data memory cell; and

all unselected data memory cells of the NAND string that are between the first end zone and second end zone receive the second set of one or more read pass voltages during a read operation.

14. The non-volatile storage system of claims 10 or 11, wherein:

the NAND strings each include two end zones;

the two end zones each include two memory cells receiving the first set of one or more read pass voltages;

a first memory cell of each end zone receives a first read pass voltage of the first set of one or more read pass voltages; and

a second memory cell of each end zone receives a second read pass voltage of the first set of one or more read pass voltages.

15. The non-volatile storage system of any of claims 10-14, further comprising:

dummy word lines connected to transistors that are not used to store data, the one or more managing circuits apply a higher read pass voltage to dummy word lines when reading a data memory cell at an extreme end of the NAND string.

Fig. 1

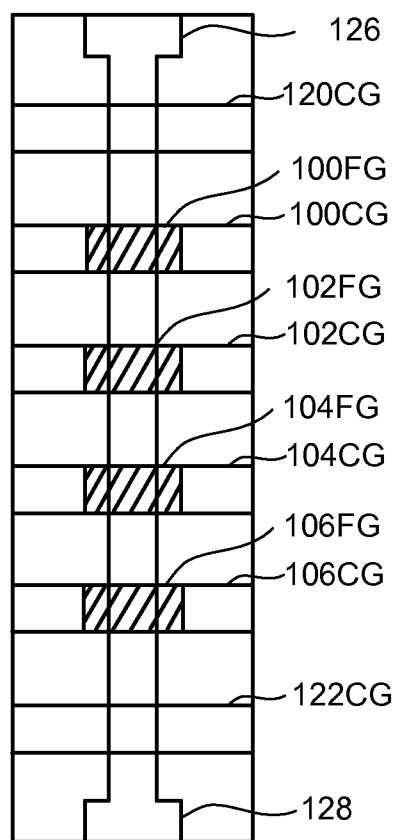
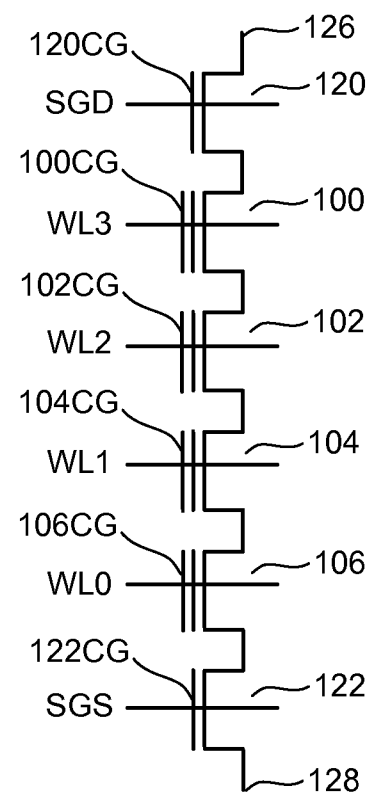


Fig. 2



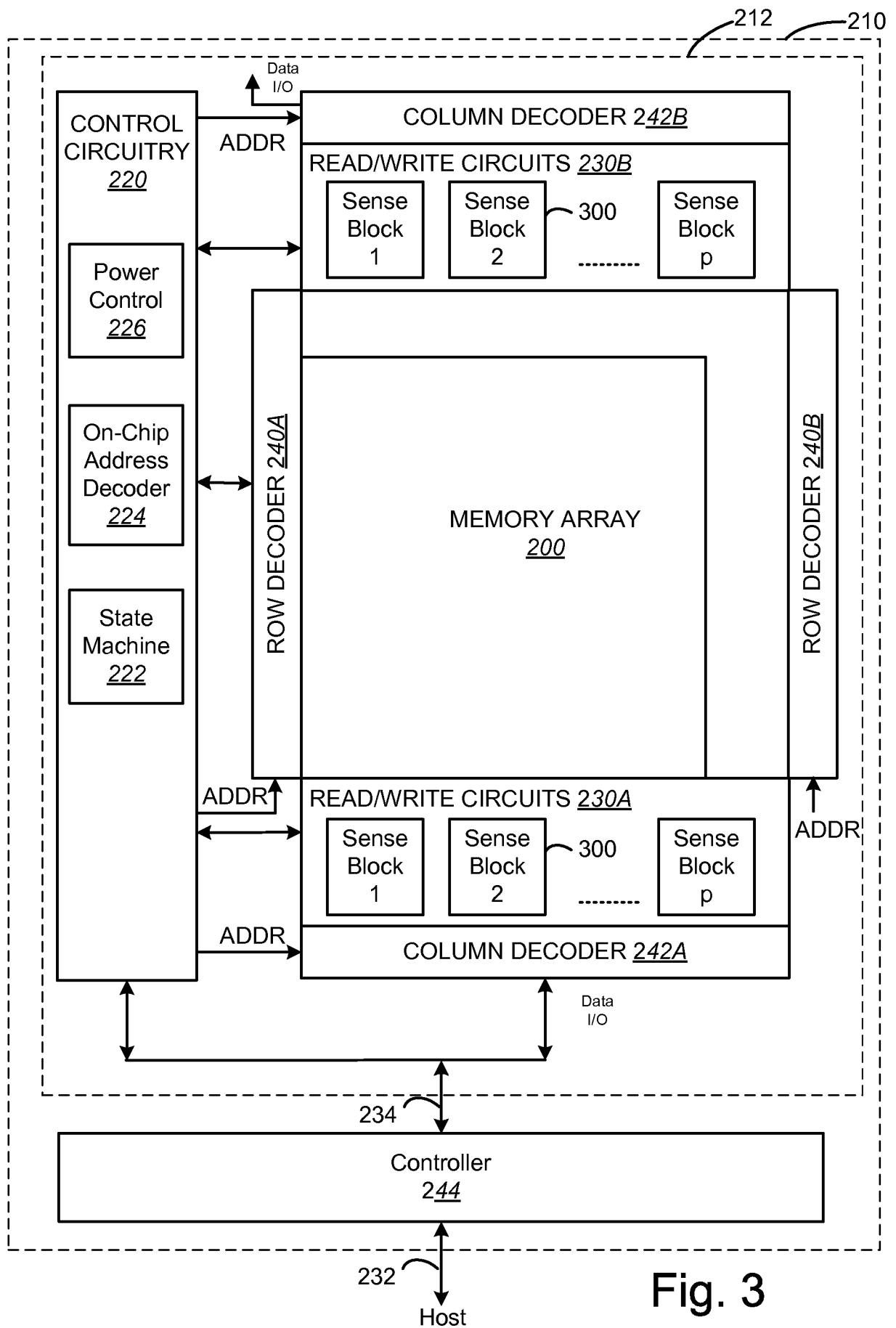
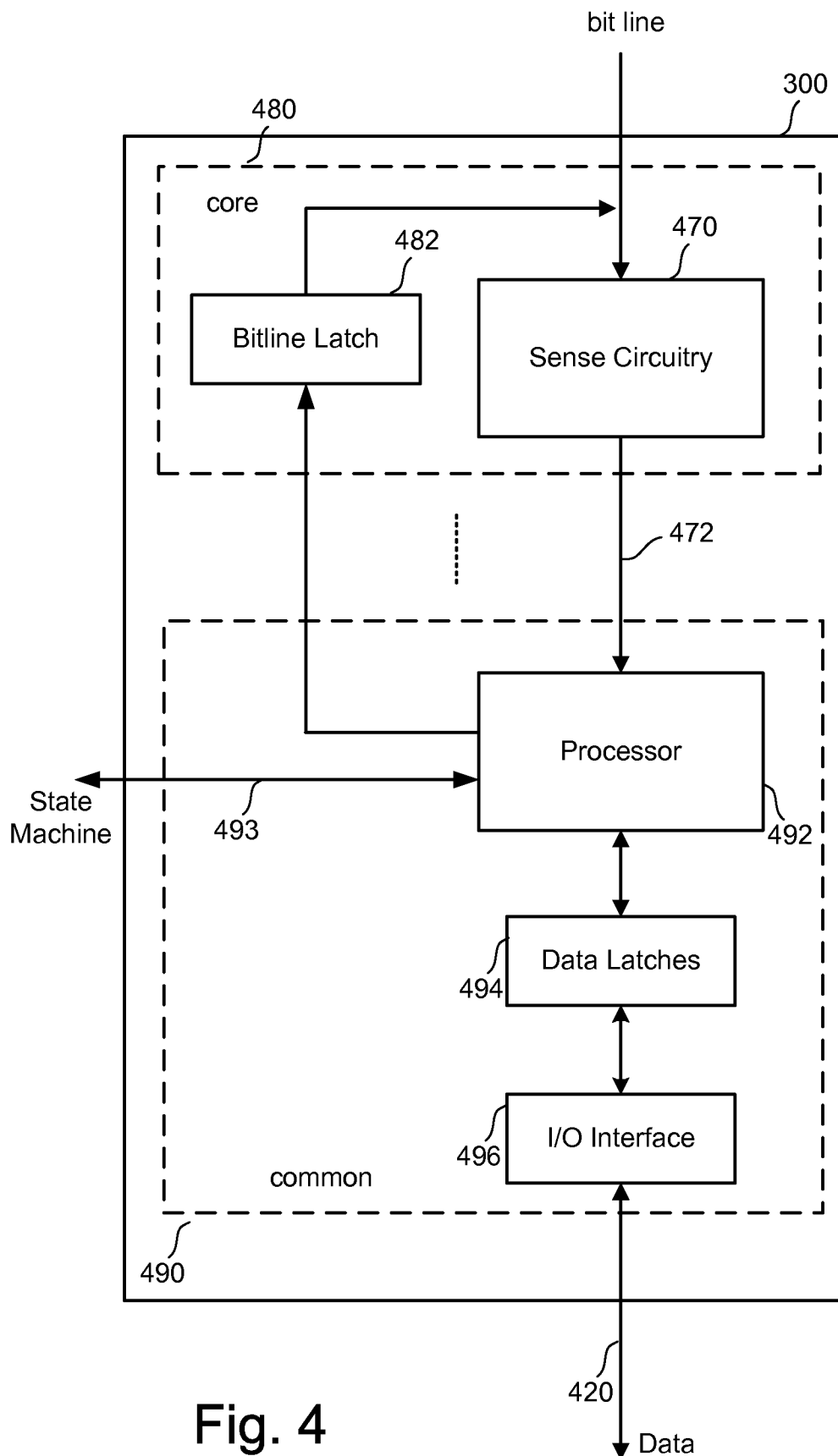


Fig. 3

**Fig. 4**

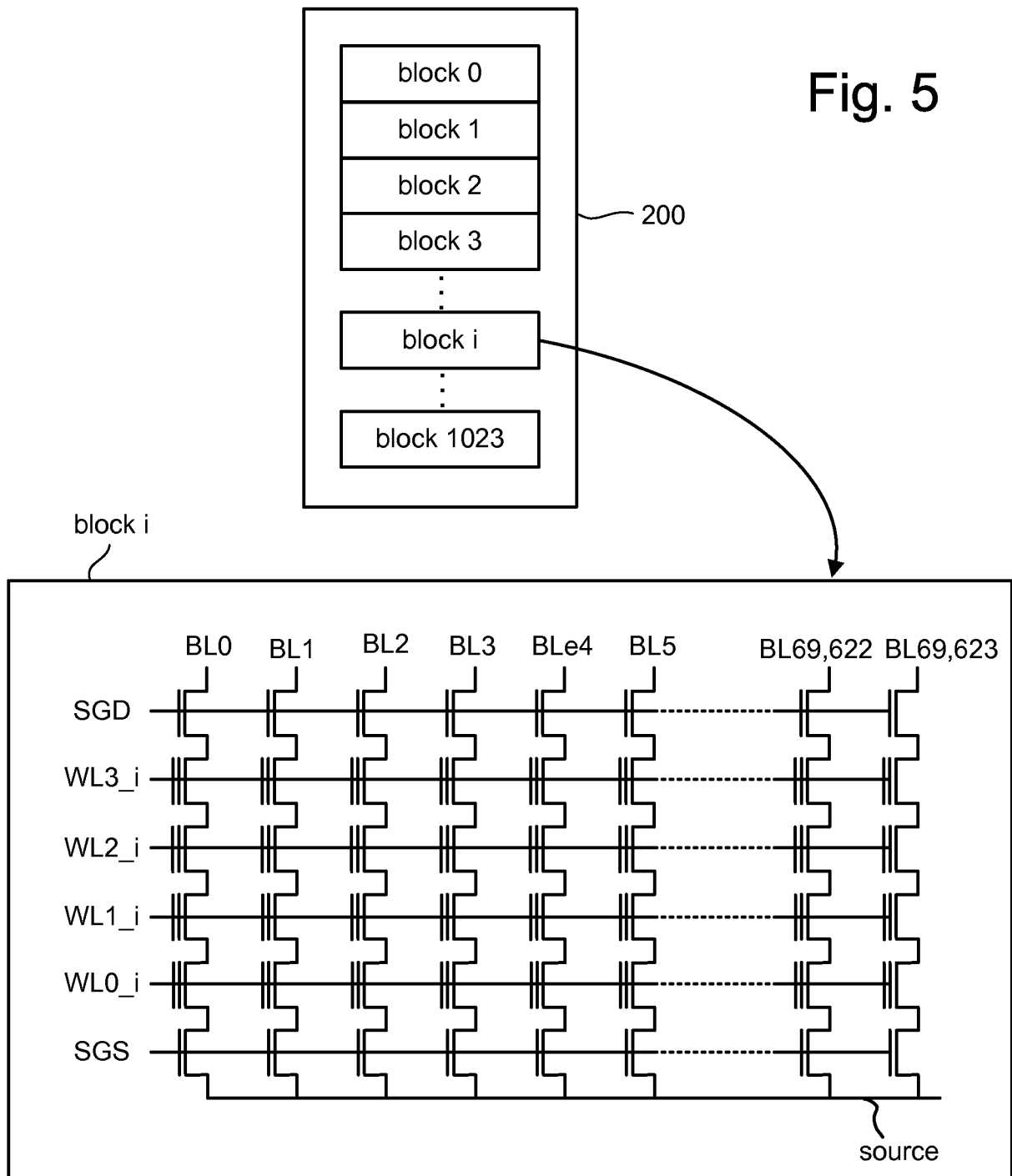


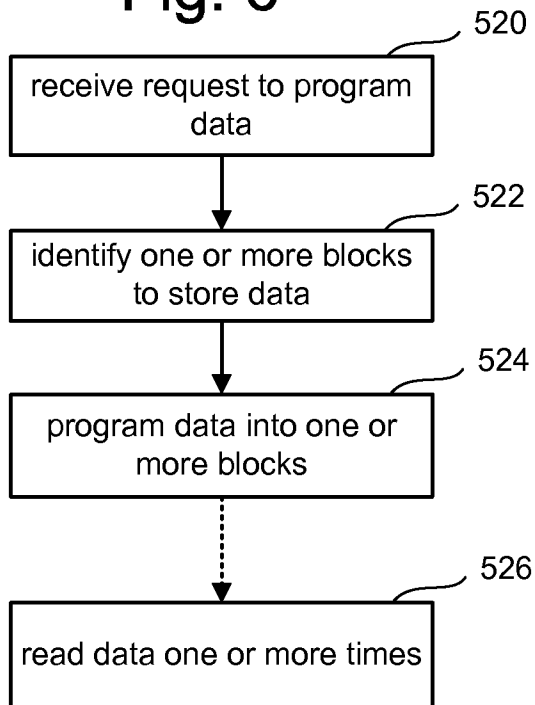
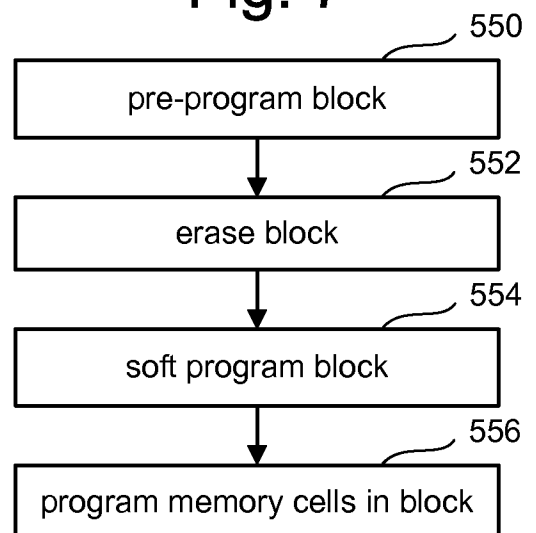
Fig. 6**Fig. 7**

Fig 8

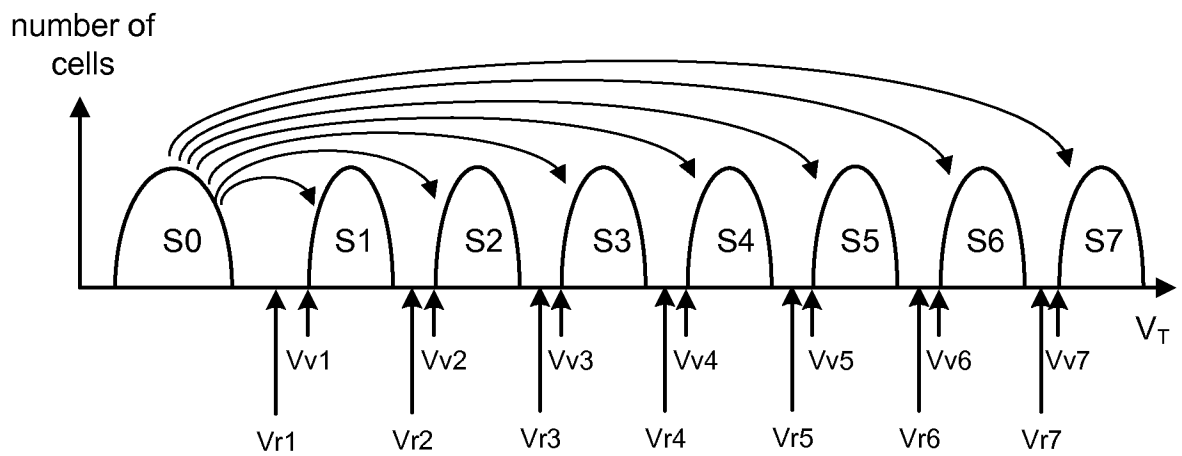
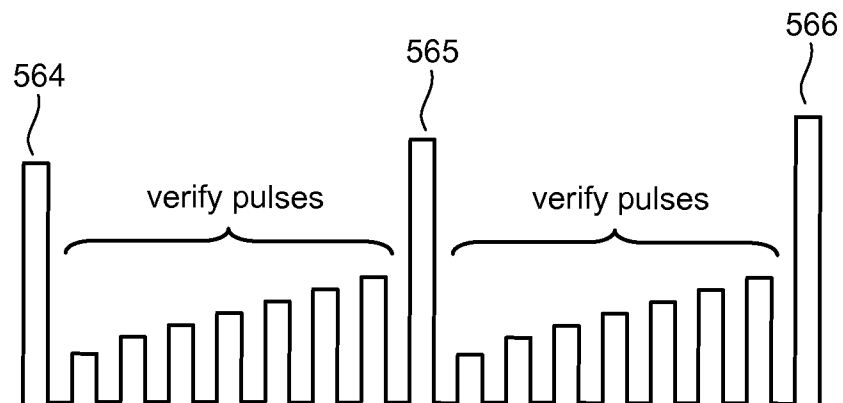


Fig. 9



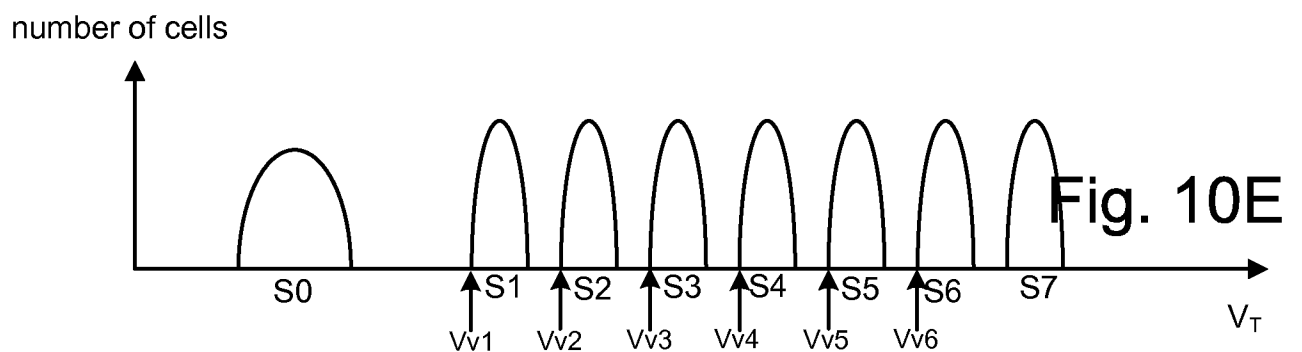
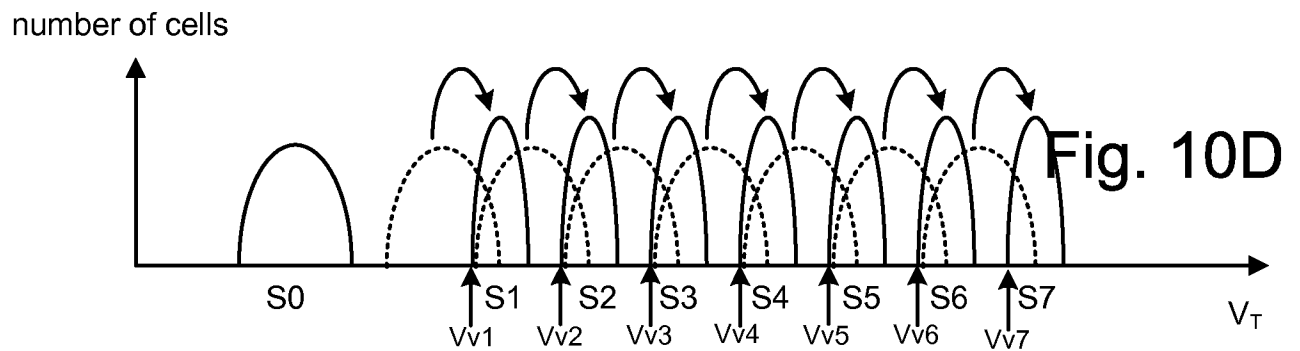
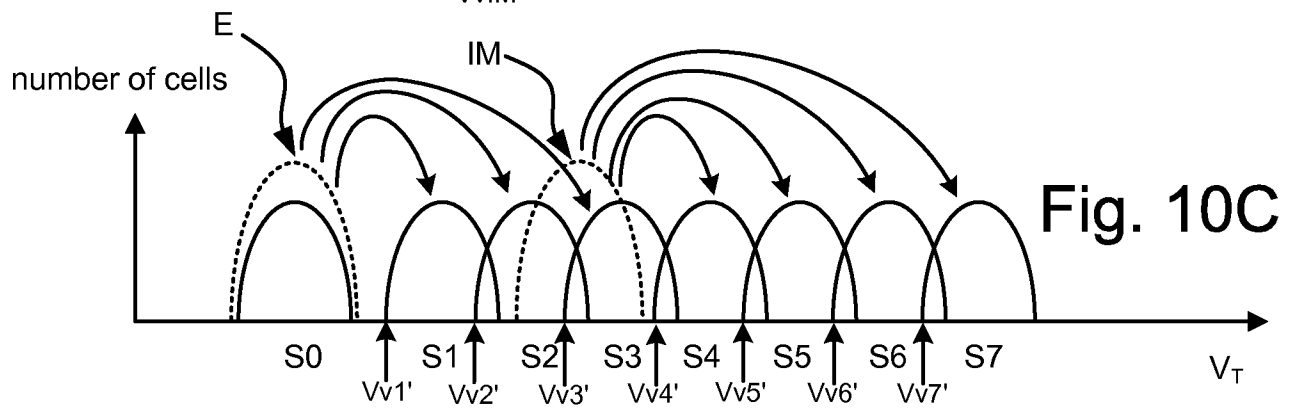
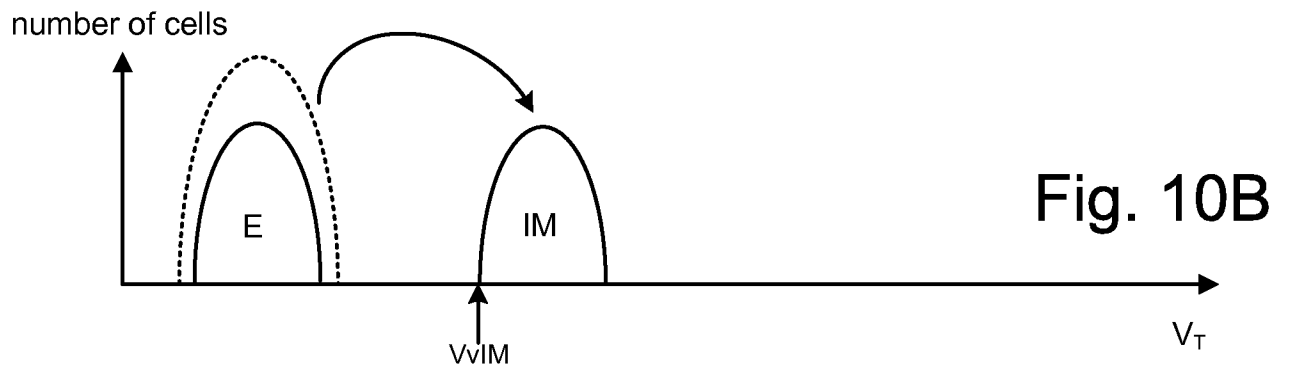
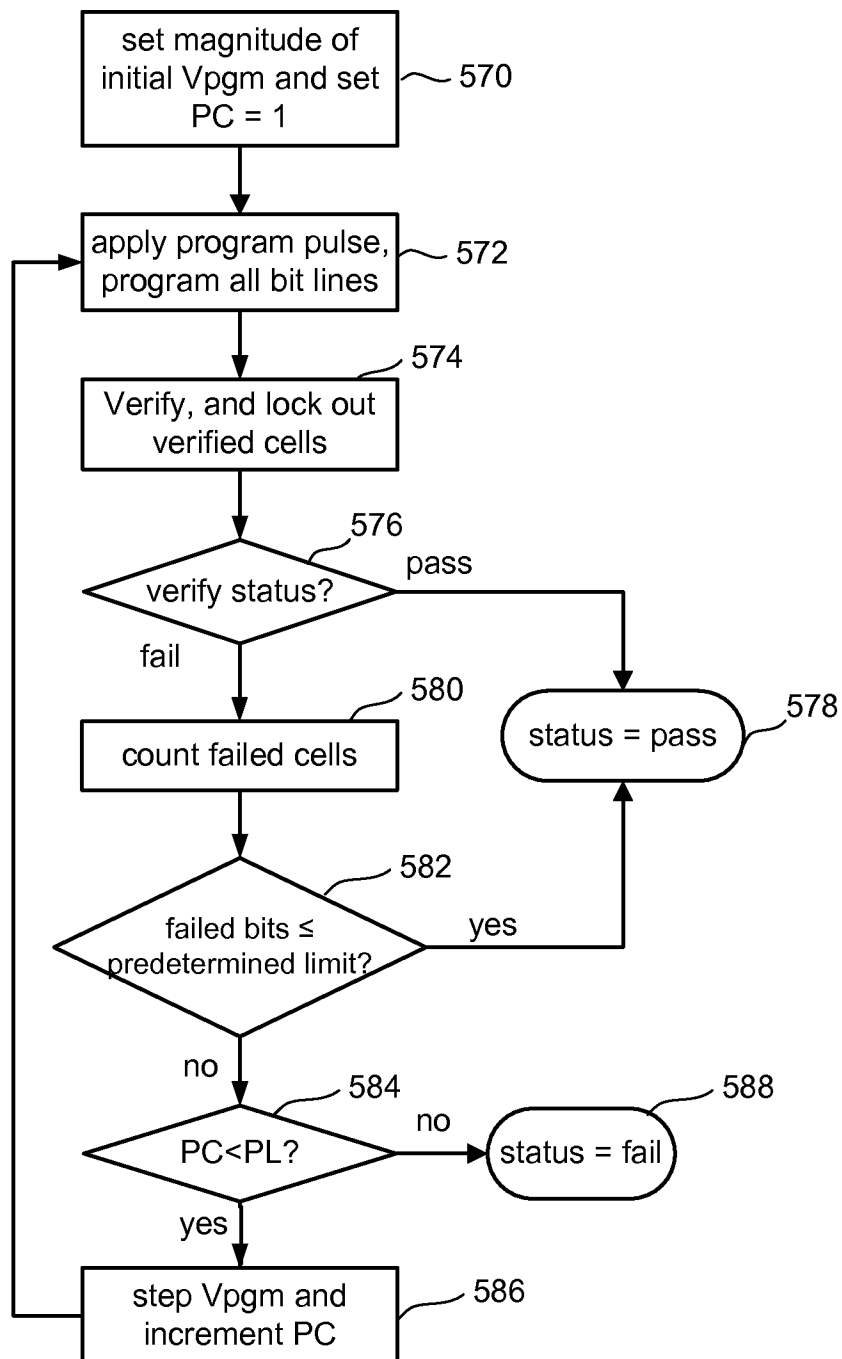


Fig. 11



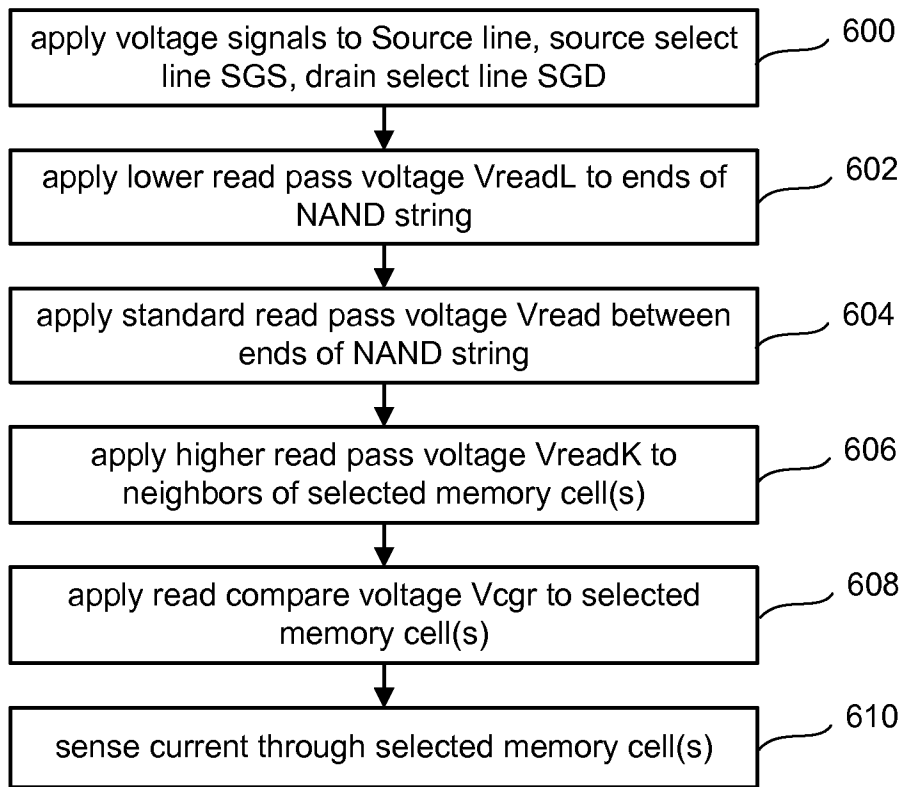


Fig. 12

Fig. 14

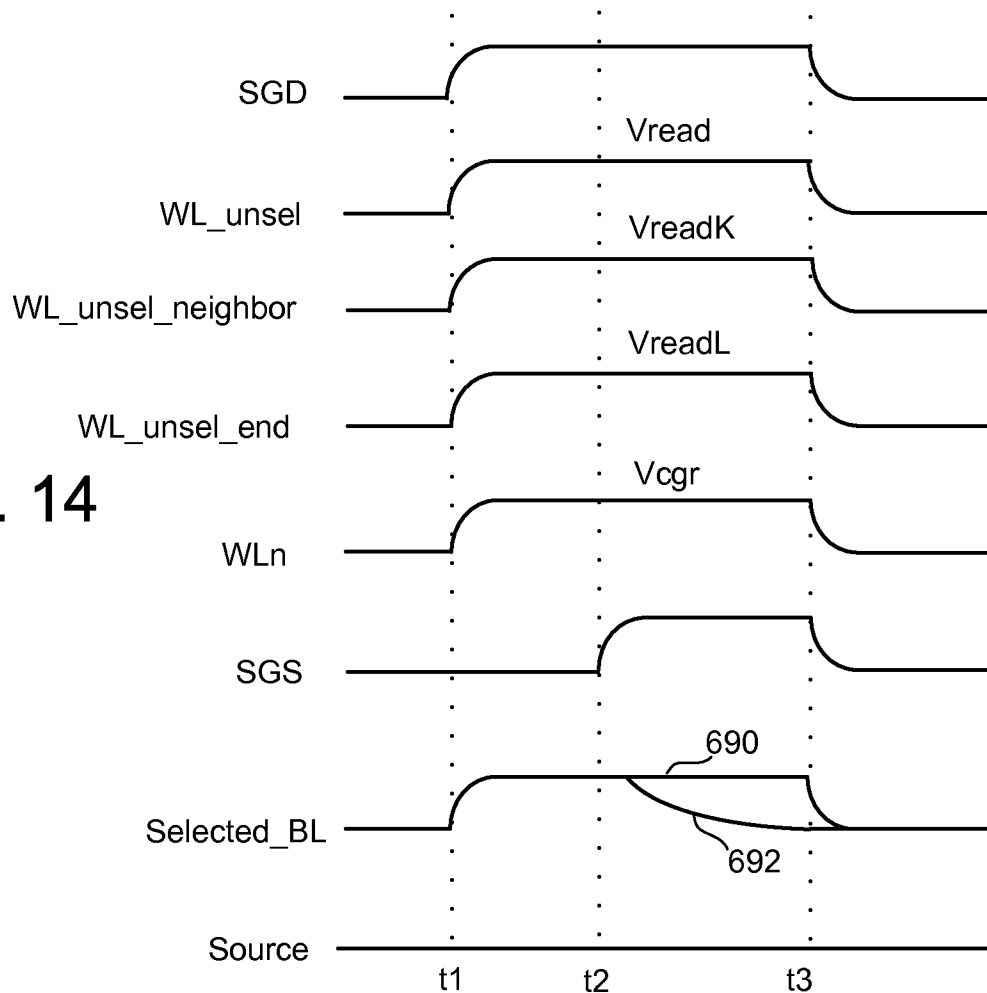


Fig. 13

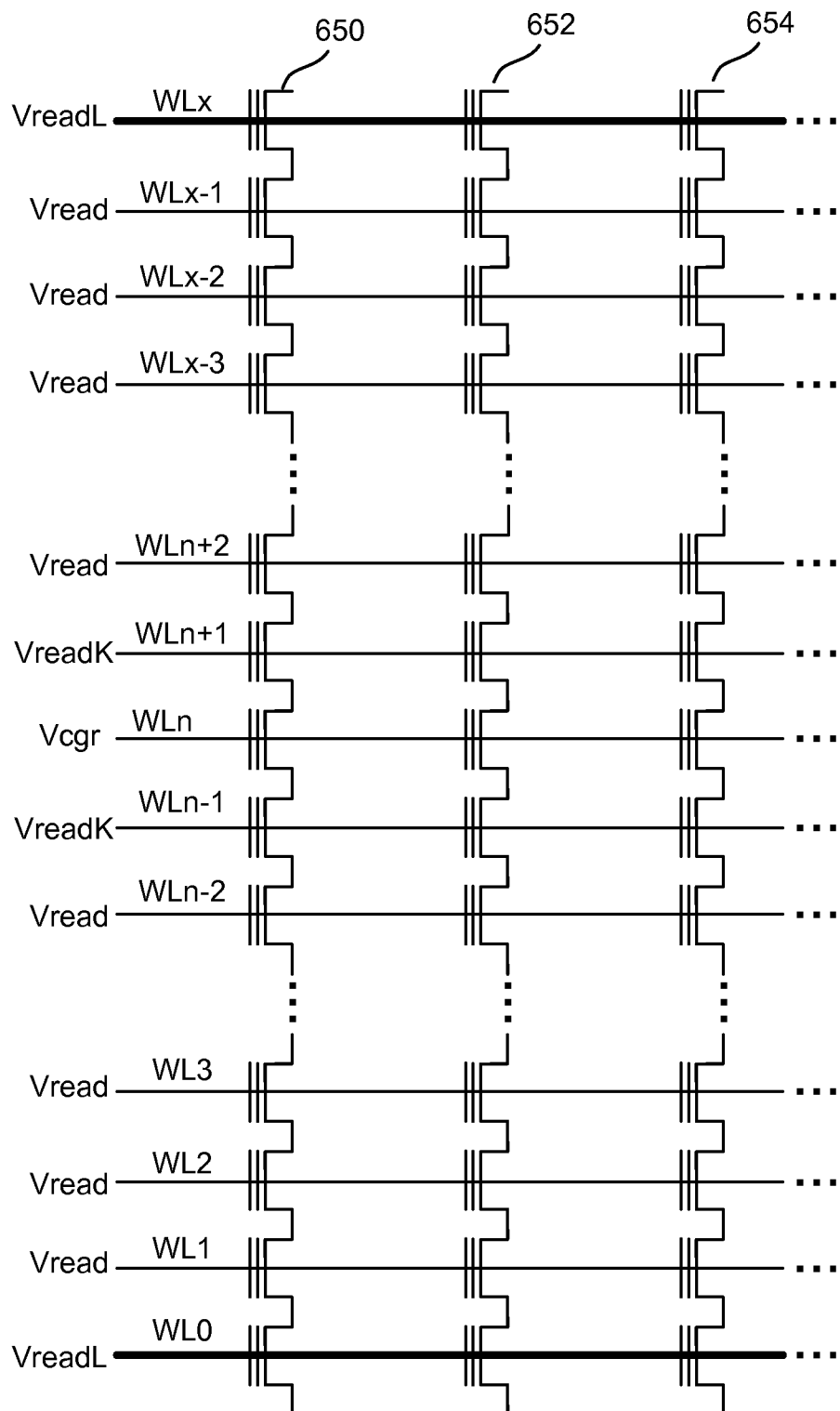


Fig. 15

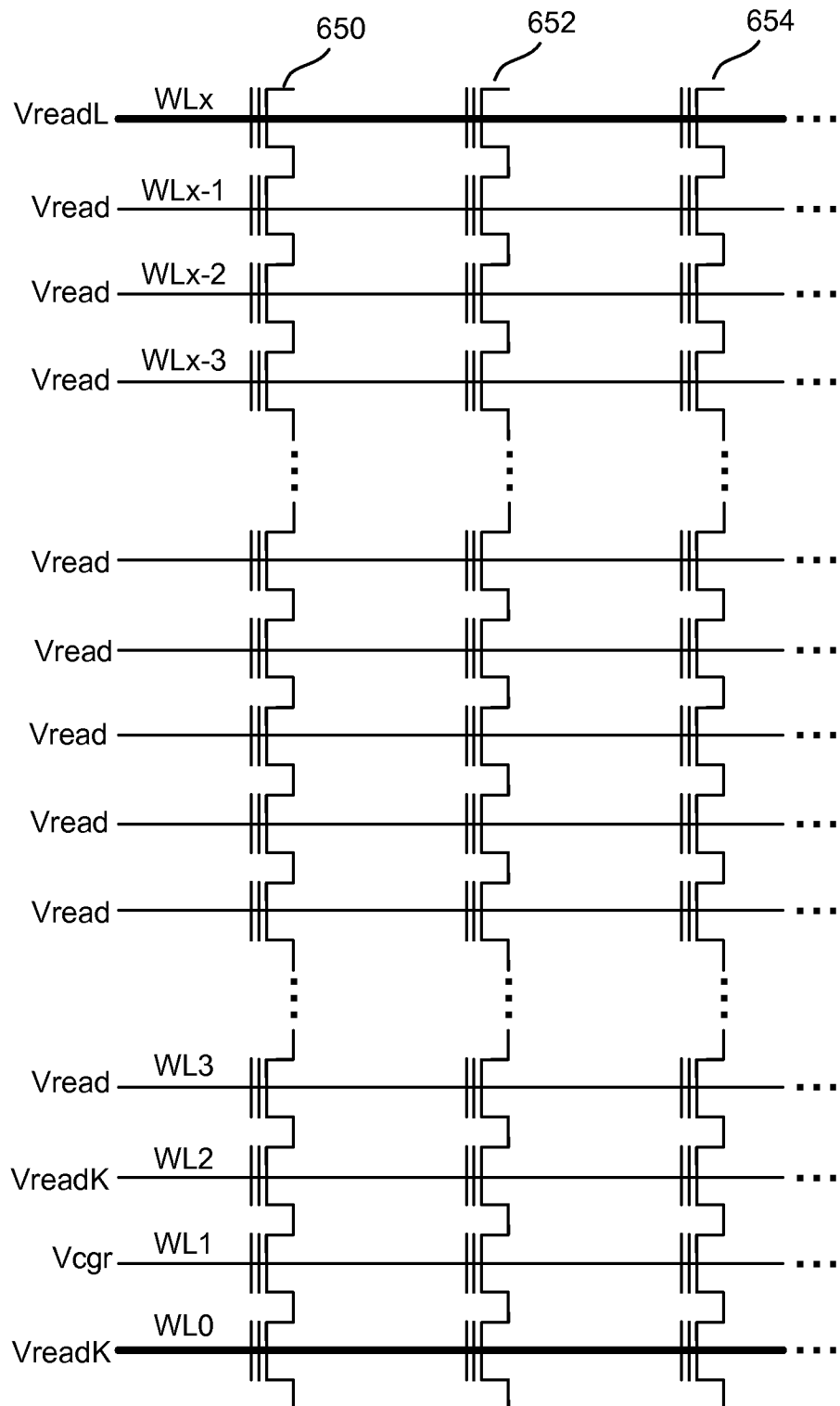


Fig. 16

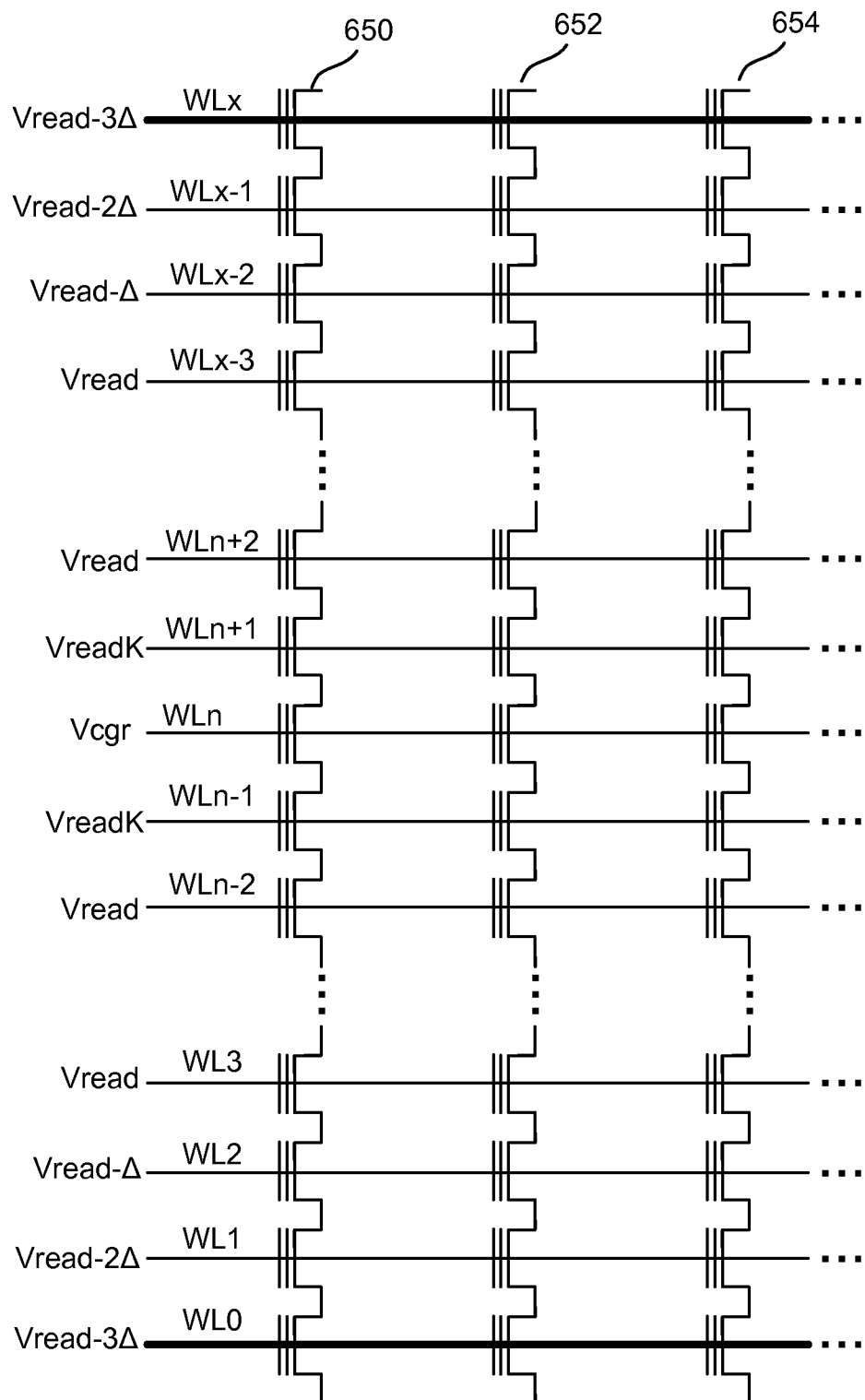


Fig. 17

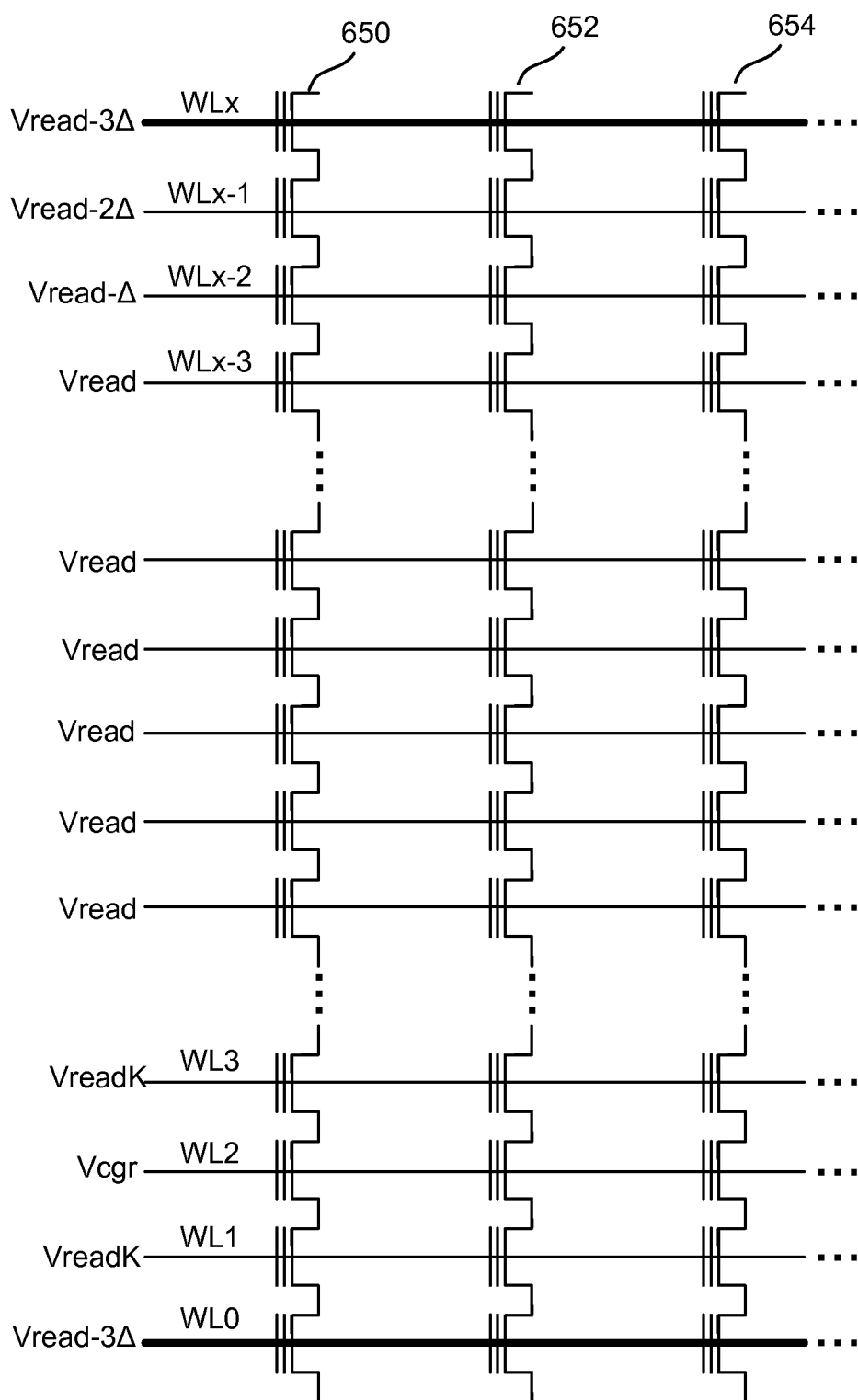


Fig. 18

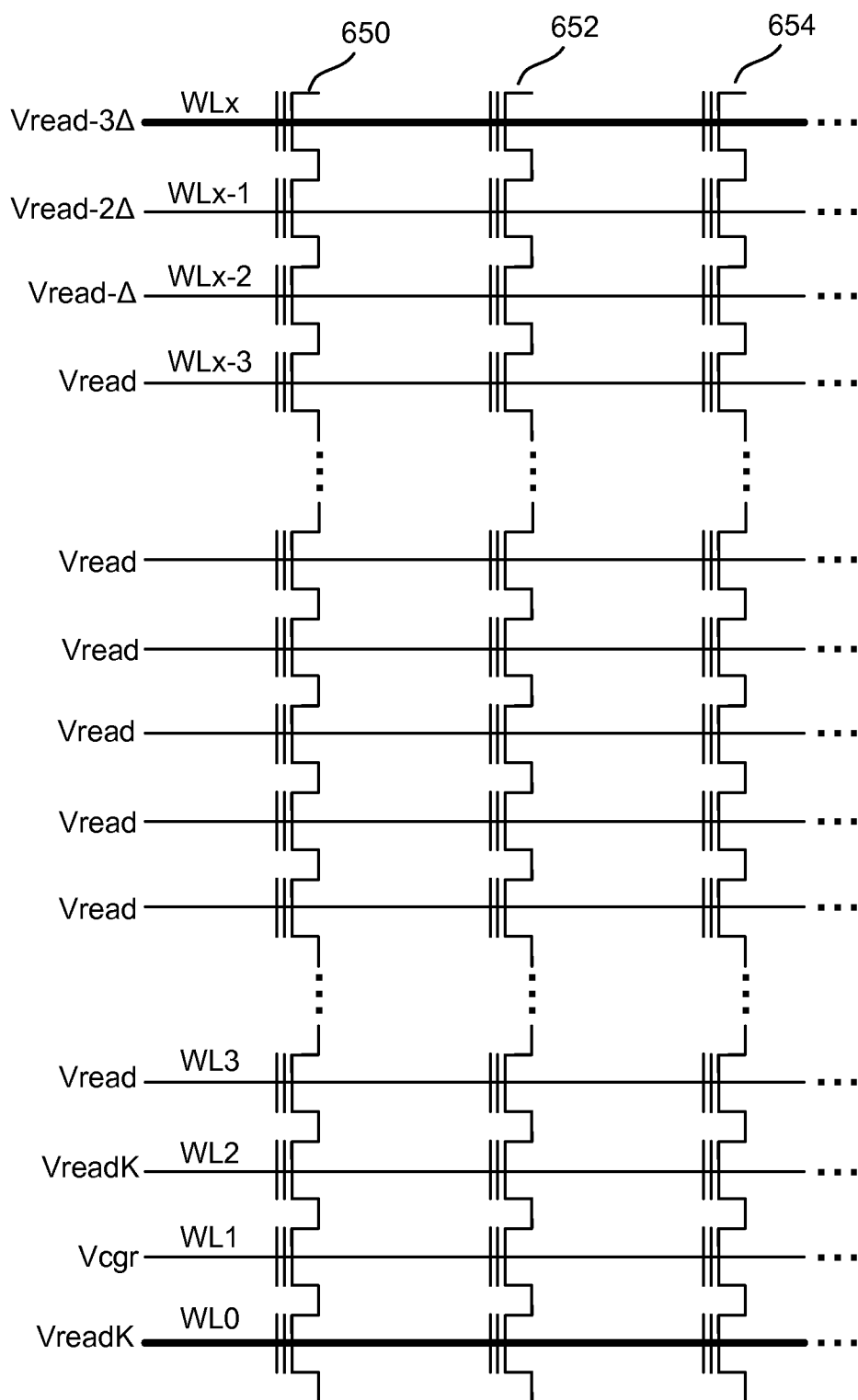


Fig. 19

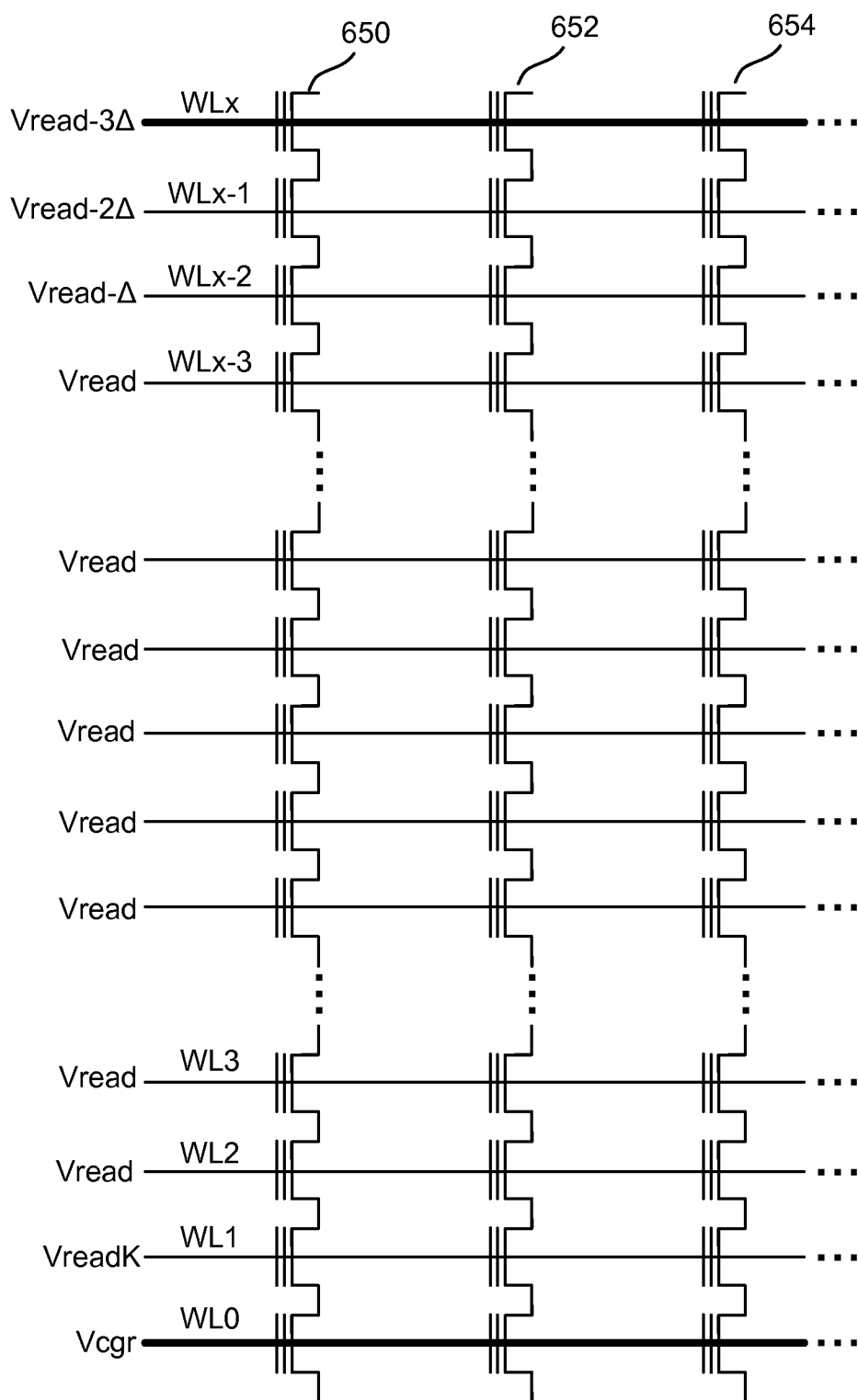


Fig. 20

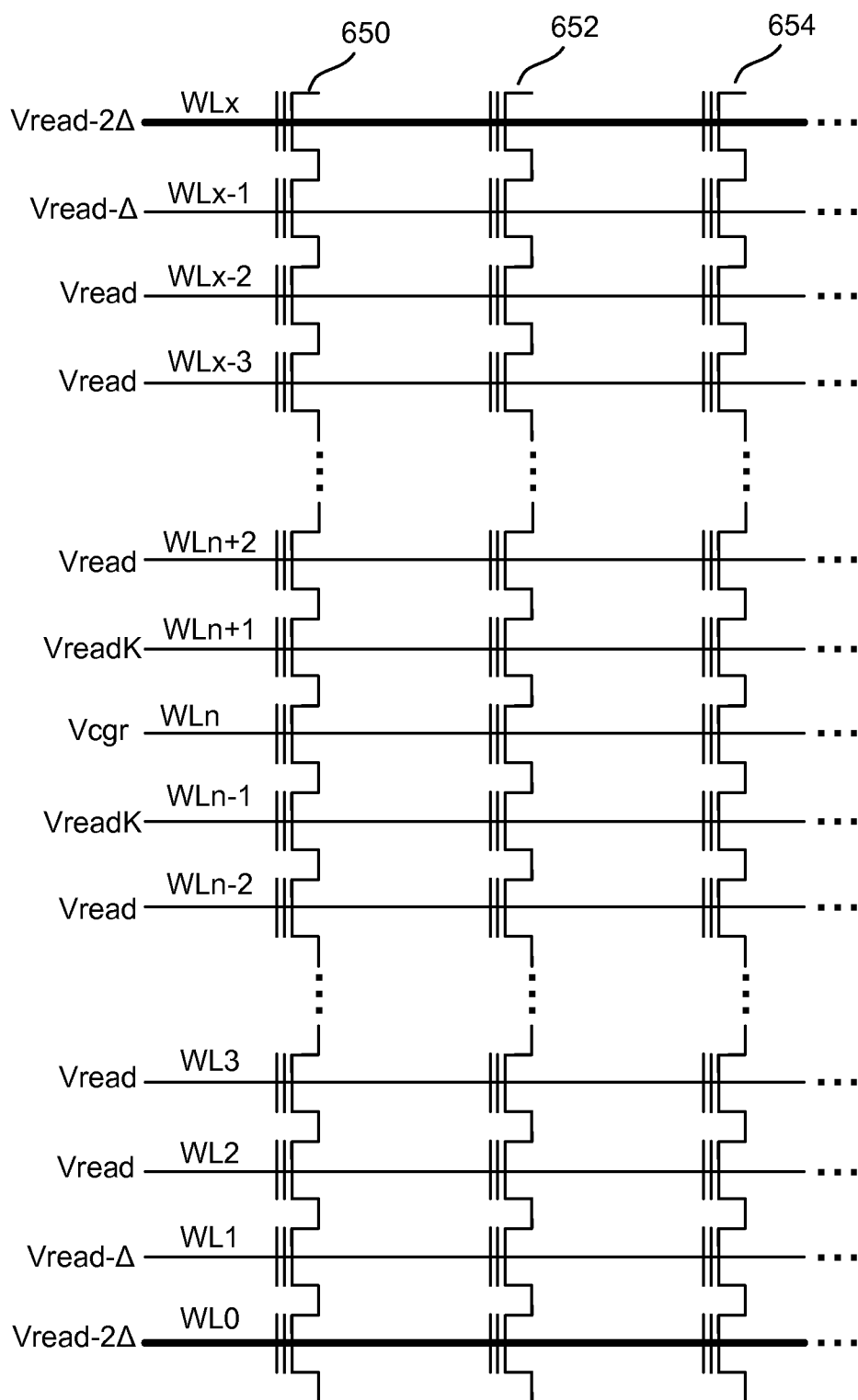


Fig. 21

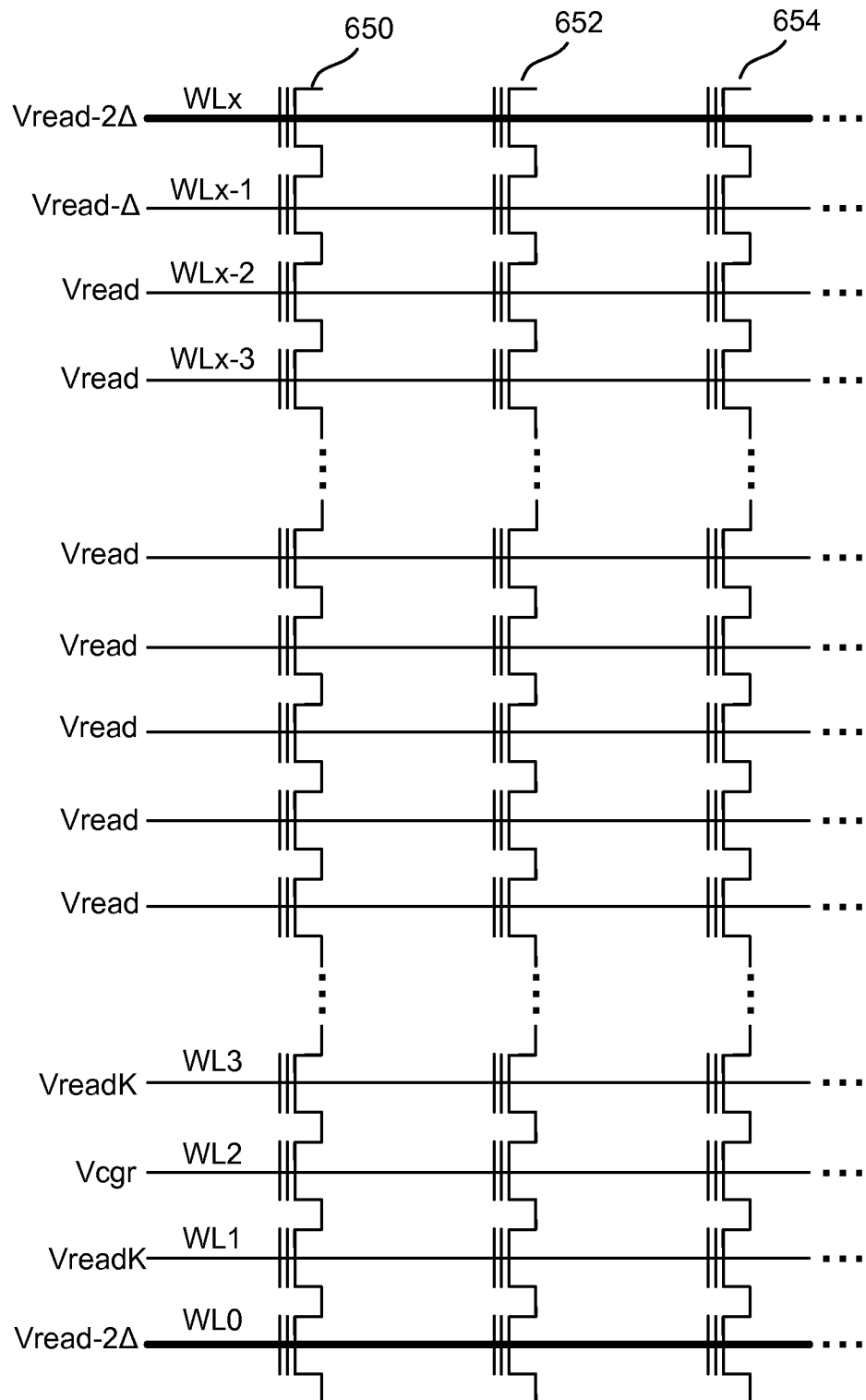


Fig. 22

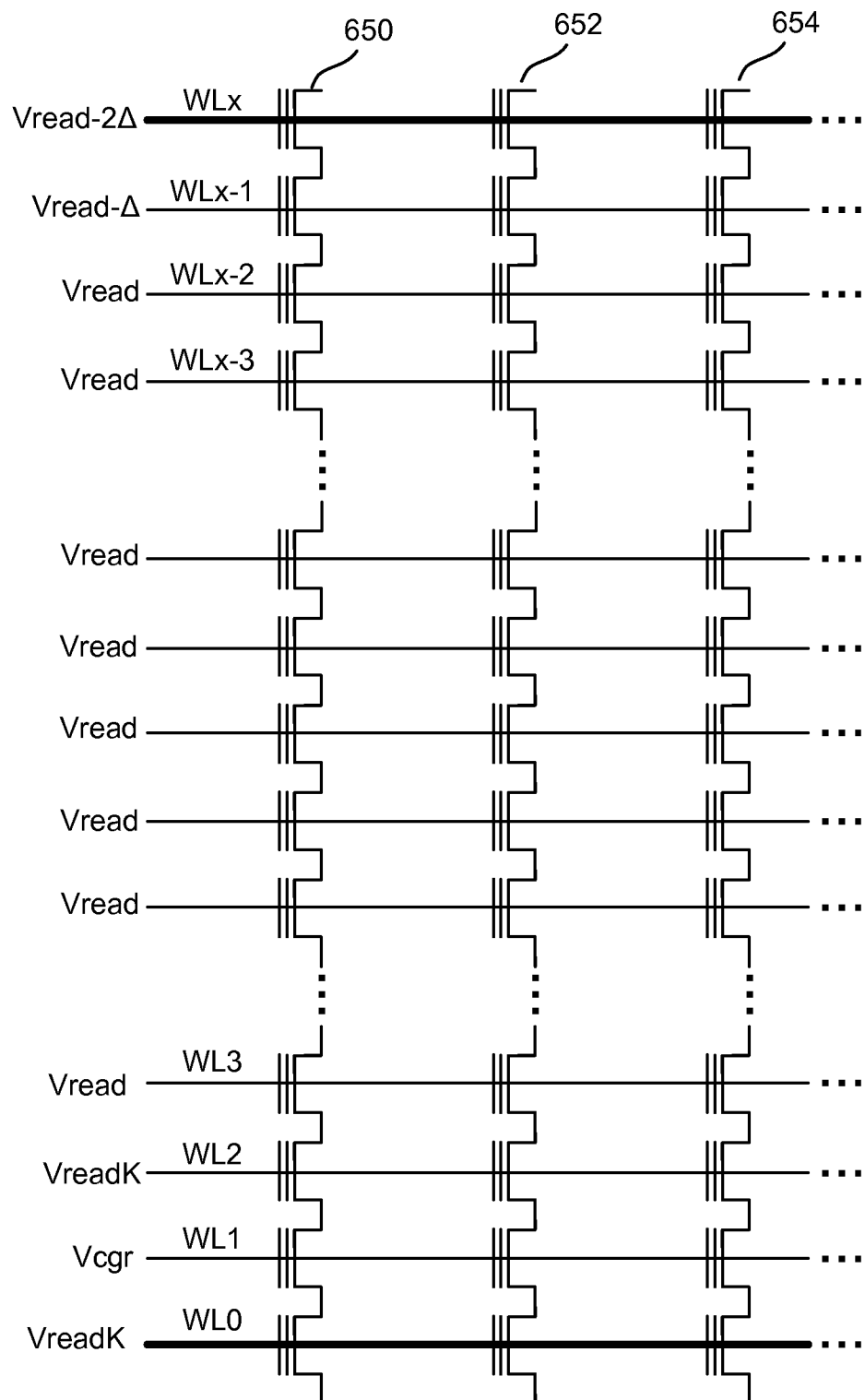


Fig. 23

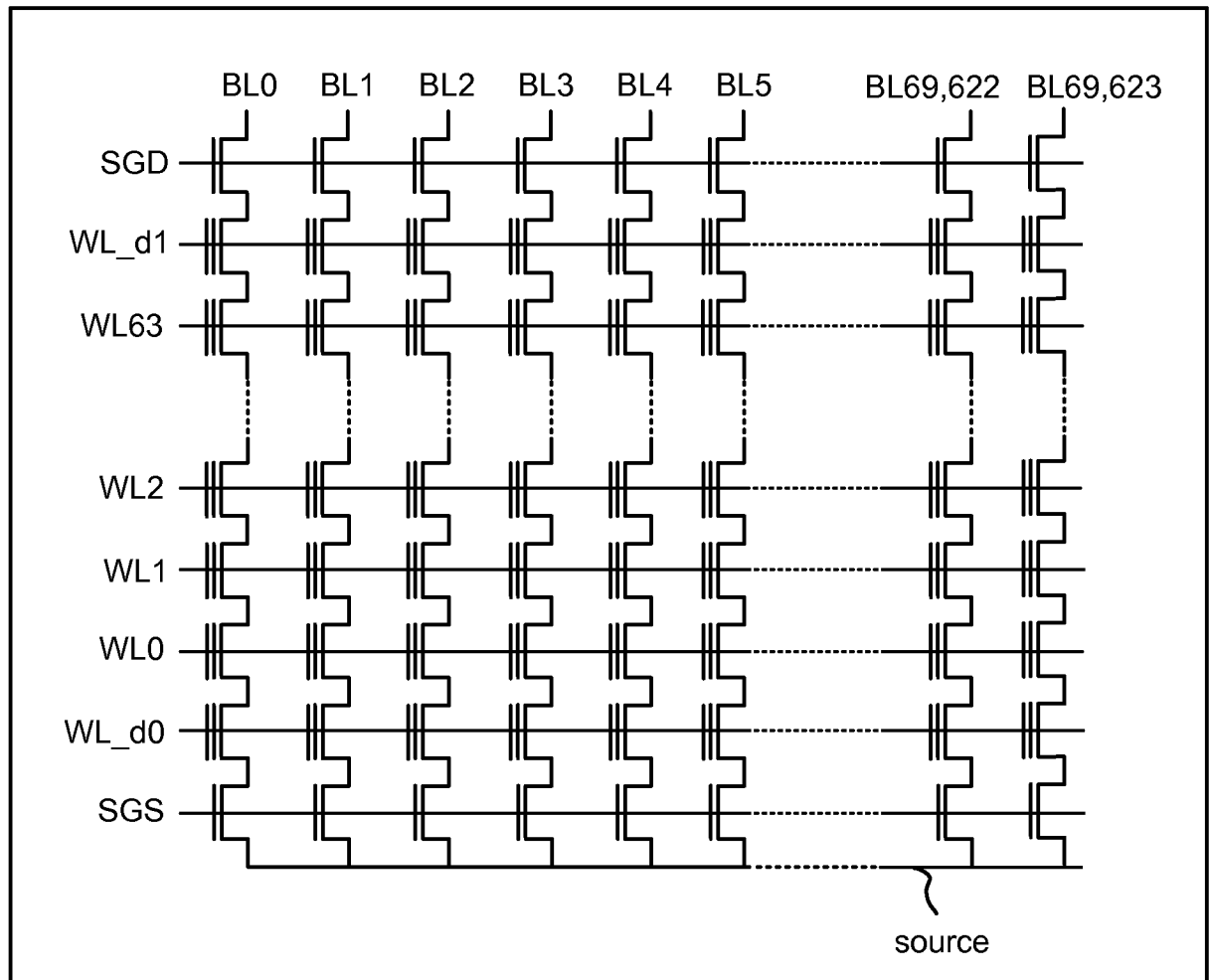


Fig. 24

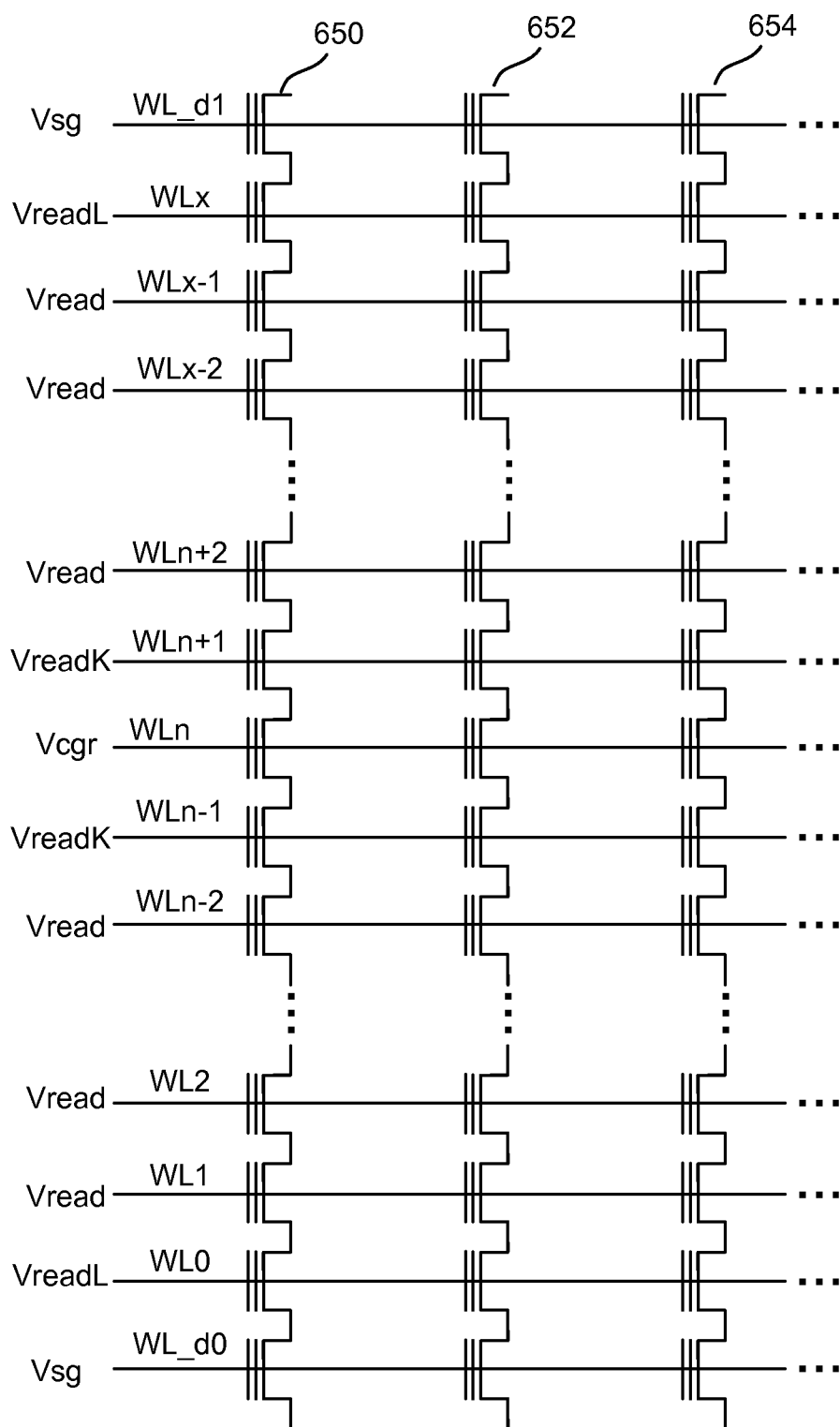


Fig. 25

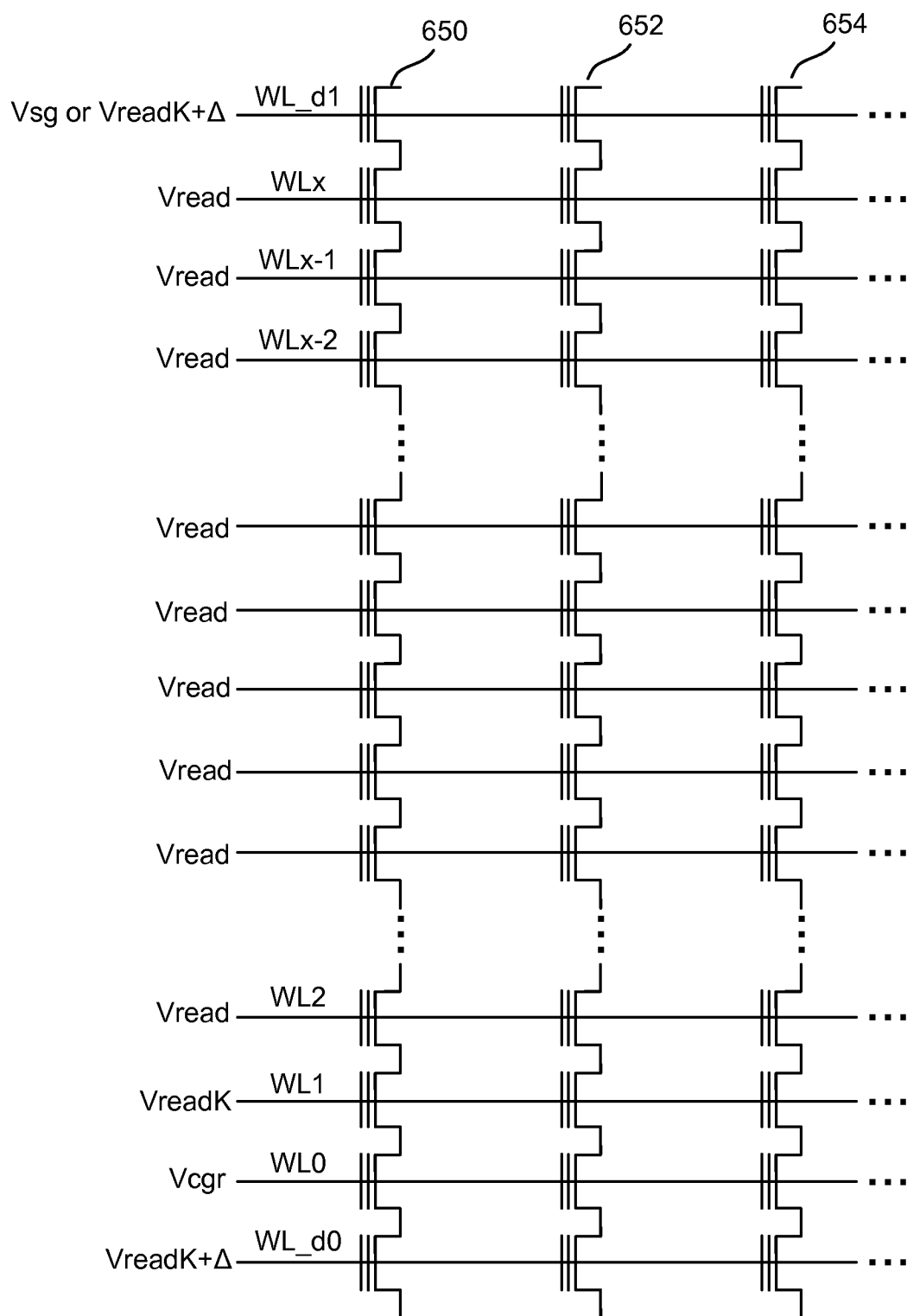
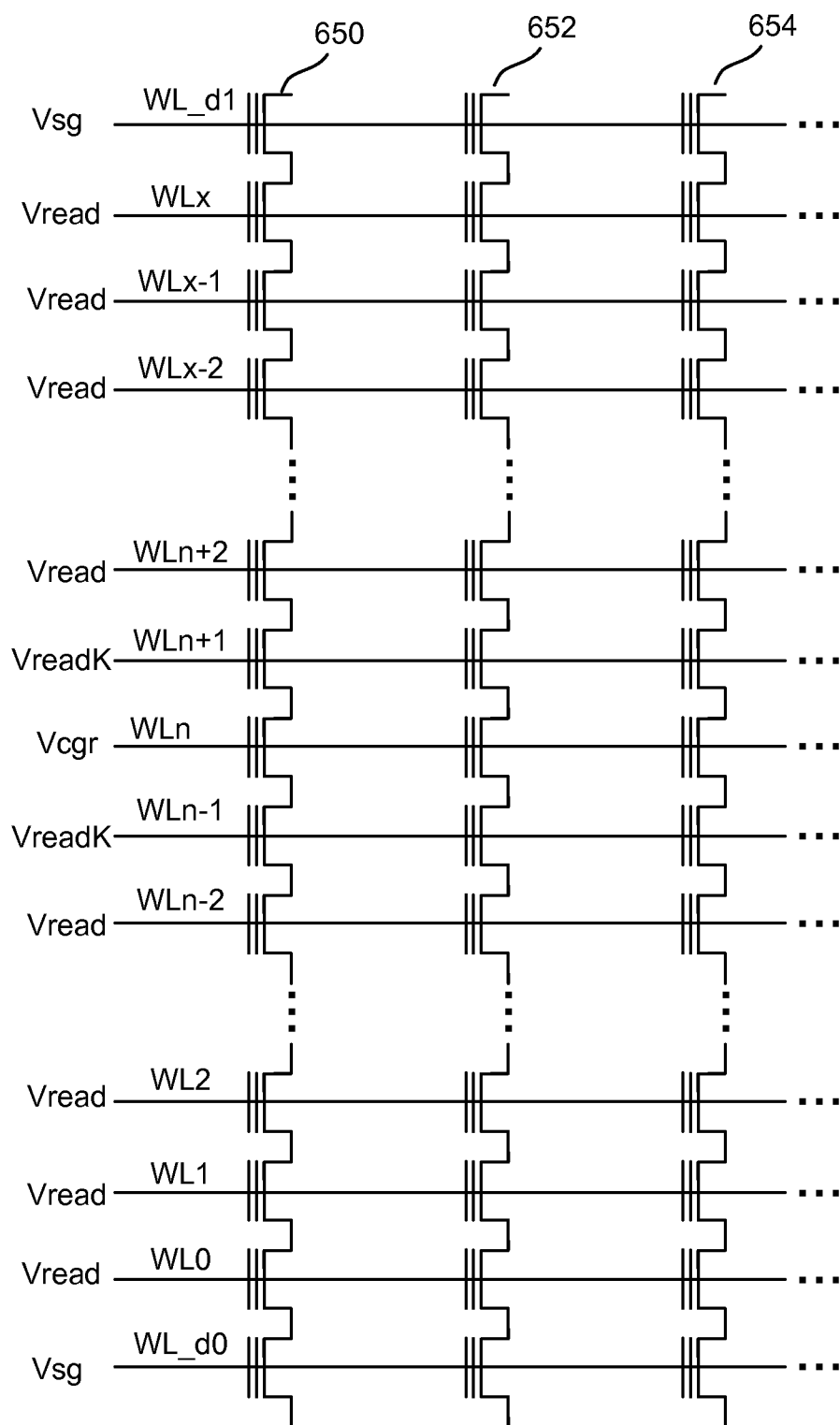


Fig. 26

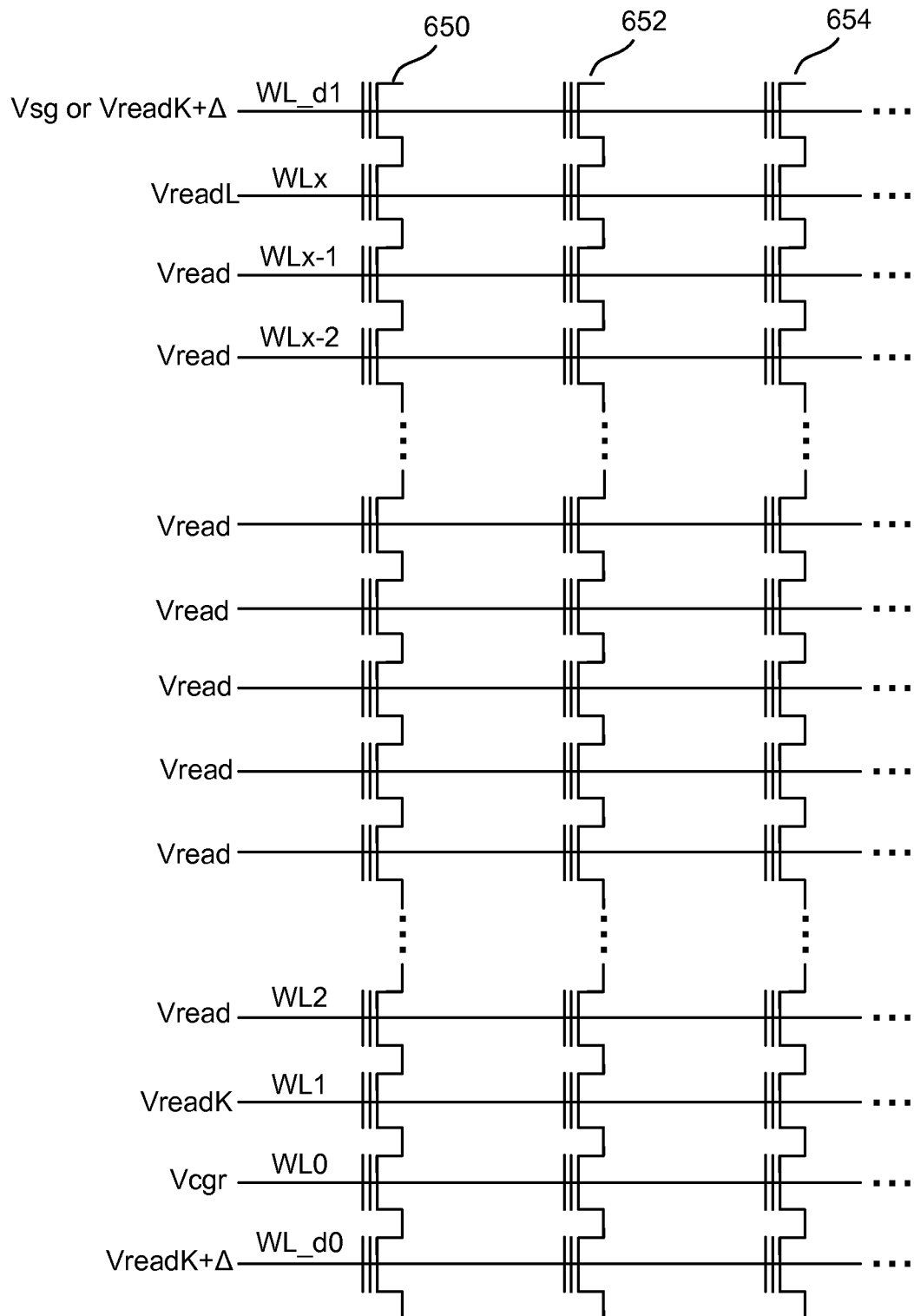


The diagram illustrates the timing of various signals in a memory array across three time points: 650, 652, and 654. The signals include:

- Wordlines (WL):** WL_{d1}, WL_x, WL_{x-1}, WL_{x-2}, ..., WL₂, WL₁, WL₀, and WL_{d0}.
- Bitlines:** V_{readK+Δ}, V_{cgr}, V_{readK}, V_{read}, and V_{sg or V_{readK+Δ}}.

The signals show a sequence of pulses and levels, with V_{readK+Δ} and V_{sg or V_{readK+Δ}} being high during the read operation. The wordlines WL_x, WL_{x-1}, and WL_{x-2} are active during the read operation. The diagram is labeled with 650, 652, and 654 at the top, indicating time points or clock cycles.

Fig. 28



INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/029991

A. CLASSIFICATION OF SUBJECT MATTER
 INV. G11C16/26 G11C16/34 G11C11/56
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/317489 A1 (KIM KIHYUN [KR] ET AL) 29 December 2011 (2011-12-29)	1-8, 10-14
Y	paragraphs [0144] - [0147], [0168] - [0169]; figures 14, 15, 24, 25 -----	9,15
X	US 2008/049508 A1 (IWAI MAKOTO [JP] ET AL) 28 February 2008 (2008-02-28)	1-6,8, 10,11,13
Y	paragraphs [0046] - [0068], [0077]; figures 5, 8 -----	9,15
Y	US 2010/067299 A1 (FUTATSUYAMA TAKUYA [JP]) 18 March 2010 (2010-03-18) paragraphs [0103] - [0108]; figure 15 -----	9,15



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

27 June 2013

Date of mailing of the international search report

04/07/2013

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Authorized officer

Vidal Verdú, Jorge

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2013/029991

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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