(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 January 2008 (03.01.2008)

PCT

(10) International Publication Number
WO 2008/000907 A1

(51) International Patent Classification:
H03G 1/00 (2006.01) *H03G 3/20* (2006.01)
H03G 3/00 (2006.01) *H03G 3/30* (2006.01)
H02M 3/18 (2006.01) *H03F 3/00* (2006.01)
H02M 5/32 (2006.01) *H03F 3/45* (2006.01)

(21) International Application Number:
PCT/FI2007/050390

(22) International Filing Date: 26 June 2007 (26.06.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
20065464 30 June 2006 (30.06.2006) FI
20065861 28 December 2006 (28.12.2006) FI

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL,

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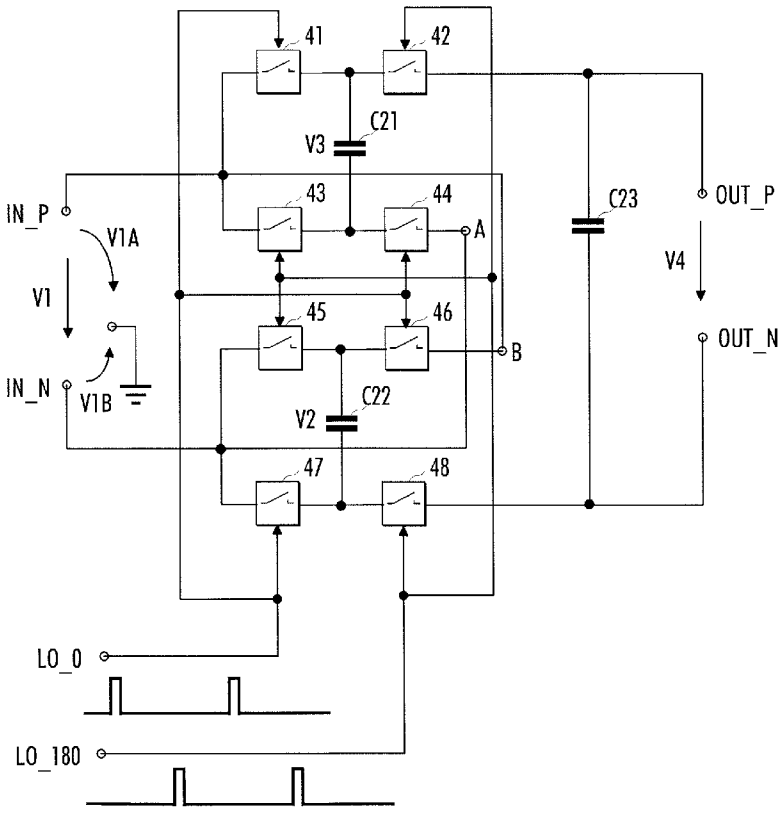
(54) Title: PASSIVE AMPLIFICATION OF SIGNALS



(57) Abstract: A passive amplifier structure capable of multiplying the voltage of an input signal is provided. In a first stage, a first (C21) and a second (C22) capacitor are connected between a first (IN_P) and a second (IN_N) terminal of a balanced input port in response to a first oscillator signal (LO_0). In a second stage, in response to a second oscillator signal (LO_180) having a phase different from that of the first oscillator signal, the first capacitor (C21) is connected between the first input terminal (IN_P) and a third capacitor (C23) and the second capacitor (C22) is connected between the second input terminal (IN_N) and the third capacitor (C23). An output voltage over the third capacitor (C23) is obtained from terminals of the third capacitor (OUT_P, OUT_N). Presented embodiments also describe an automatic gain control feature.

WO 2008/000907 A1

PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Passive Amplification of Signals

Field

[0001] The invention relates to passive amplification of received signals in a radio receiver.

Background

[0002] In radio transceivers, and particularly in direct-conversion receivers, amplifiers having low noise figures and capable of handling high-level signals are needed in front-ends of an in-phase (I) and a quadrature (Q) signal paths. Figure 1 illustrates a receiver structure converting a received radio signal directly to the baseband. The receiver comprises a first amplifier 2 before mixers 4 and 5. The first amplifier 2 is typically a low-noise amplifier. Bandpass filters 1 and 3 have been provided before and after the amplifier 2 to remove undesired frequency components. Mixers 4 and 5 mix in-phase (I) and quadrature (Q) components of the received radio signal to the baseband with local oscillator signals LO_0, LO_90, LO_180, and LO_270. The number refers to the phase shift of the respective local oscillator signal. After the downmixing, baseband amplifiers 6 and 7 amplify the downmixed I and Q components, respectively, and low-pass filters 8 and 9 remove harmonic signal components resulting in the downmixing. Amplifiers 10 and 11 further amplify the low-pass filtered signals before analog-to-digital (A/D) conversion in an A/D-converter 12.

[0003] In case the baseband amplifiers 6 and 7 are active amplifiers, noise figures of the baseband amplifiers 6 and 7 are typically relatively poor due to flicker noise (known also as 1/f noise), among others. Nowadays, supply voltages applied to the active amplifiers 6 and 7 are quite low, which degrades their ability to handle input signals having large amplitudes. As a consequence, the amplifiers 6 and 7 may distort input signals severely causing difficulties in further processing of the input signals. Low-pass filters may be arranged to have low impedance levels in order to minimize noise levels. This may result in high capacitance values in the low-pass filter components and, as a

consequence, increase the size of an actual implementation in an integrated circuit.

Brief description of the invention

[0004] An object of the invention is to provide an improved solution for amplifying a received radio signal.

[0005] According to an aspect of the invention, there is provided a method, comprising: receiving an input signal voltage into a first and a second input port of a balanced input port, connecting, in a first stage in response to a first oscillator signal, a first and a second capacitance between the first and the second input port of the balanced input port, connecting, in a second stage in response to a second oscillator signal, the first capacitance between the first input port and a third capacitance and the second capacitance between the second input port and the third capacitance, and obtaining the voltage over the third capacitance as an output voltage.

[0006] According to another aspect of the invention, there is provided a method, comprising: producing a first and a second oscillator signal having the same frequency, charging a first capacitance and a second capacitance with an input signal sample received into a first and a second input port of a balanced input port during the first half cycle of the oscillator signals, and charging a third capacitance operationally coupled with the first and the second capacitance, with the charges in the first and the second capacitances together with an input signal sample received into the first and the second input port of the balanced input port during the second half cycle of the oscillator signal.

[0007] According to another aspect of the invention, there is provided an apparatus, comprising an input interface comprising a balanced input port to receive a balanced input signal and a oscillator signal input port to receive a first and a second oscillator signal, a first, a second, and a third capacitance, a first set of switches responsive to the first oscillator signal and arranged to connect, in response to the first oscillator signal, the first and the second

capacitance between a first and a second input port of the balanced input port, a second set of switches responsive to the second oscillator signal and arranged to connect, in response to the second oscillator signal, the first capacitance between the first input port and the third capacitance and the second capacitance between the second input port and the third capacitance, and an output port connected to terminals of the third capacitance.

[0008] According to another aspect of the invention, there is provided an apparatus, comprising input means comprising a balanced input port to receive a balanced input signal and an oscillator signal input port to receive a first and a second oscillator signal, first, second, and third capacitance means, first switching means responsive to the first oscillator signal and arranged to connect, in response to the first oscillator signal, the first and the second capacitance means between a first and a second input port of the balanced input port, second switching means responsive to the second oscillator signal and arranged to connect, in response to the second oscillator signal, the first capacitance means between the first input port and the third capacitance means and the second capacitance means between the second input port and the third capacitance means, and output means connected to terminals of the third capacitance means.

[0009] According to another aspect of the invention, there is provided an automatic gain control amplifier comprising the above-described apparatus.

[0010] According to another aspect of the invention, there is provided a radio transmitter comprising the above-described apparatus.

List of drawings

[0011] In the following, the invention will be described in greater detail with reference to the embodiments and the accompanying drawings, in which

Figure 1 illustrates an example of components of a radio receiver;

Figure 2 illustrates a passive amplifier structure according to an embodiment of the invention;

Figure 3A illustrates an equivalent circuit in a first stage of the operation of the passive amplifier illustrated in Figure 2;

Figure 3B illustrates an equivalent circuit in a second stage of the operation of the passive amplifier illustrated in Figure 2;

Figure 4 illustrates signals input to the passive amplifier illustrated in Figure 2 and voltage levels in components of the passive amplifier;

Figure 5A illustrates an exemplary switched capacitor filter structure;

Figure 5B illustrates an equivalent circuit diagram of the switched capacitor filter structure illustrated in Figure 5A;

Figure 6 illustrates a basic structure for a passive amplifier according to an embodiment of the invention;

Figure 7 illustrates an automatic gain control (AGC) passive amplifier structure according to an embodiment of the invention;

Figure 8A illustrates an equivalent circuit diagram in a first stage of operation of the AGC passive amplifier having a voltage multiplication factor of two;

Figure 8B illustrates an equivalent circuit diagram in a first stage of operation of the AGC passive amplifier having a voltage multiplication factor of one;

Figure 9 illustrates the structure of a passive amplifier according to an embodiment of the invention and having an adjustable voltage multiplication factor;

Figure 10 illustrates an adjustment circuit configured to adjust the voltage multiplication factor of the embodiment illustrated in Figure 9;

Figure 11 illustrates the structure of a passive amplifier according to another embodiment of the invention and having an adjustable voltage multiplication factor;

Figure 12 illustrates an automatic gain control (AGC) passive amplifier structure according to another embodiment of the invention, and

Figure 13 illustrates an implementation of the passive amplifier illustrated in Figure 2.

Description of embodiments

[0012] Figure 2 illustrates the structure of an apparatus according to an embodiment of the invention. The apparatus may be a baseband passive

amplifier or a voltage multiplier implemented in a radio receiver. The amplifier may be located after a mixer converting a received radio frequency signal into the baseband.

[0013] The amplifier comprises an input interface including a balanced input port to receive a balanced input signal to be amplified. The balanced input port comprises a first and a second input port IN_P and IN_N to receive a balanced input signal. As known in the art, the balanced input signal comprises two components having opposite phases. Referring to Figure 2, a signal input to the second input port IN_N is accordingly an inverted version of a signal input to the first input port IN_P.

[0014] The input interface further comprises an oscillator signal input port to receive a first and a second oscillator signal LO_0 and LO_180. A local oscillator may provide a local oscillator signal which may be modified into the first and the second oscillator signals LO_0 and LO_180 input to the oscillator signal input port of the amplifier. The oscillator signals LO_0 and LO_180 may be modified to have substantially the same frequency.

[0015] The amplifier according to the embodiment of the invention includes a first capacitance C21, a second capacitance C22, and a third capacitance C23. Additionally, the amplifier comprises a first set of switches responsive to the first oscillator signal LO_0 and a second set of switches responsive to the second oscillator signal LO_180. In the embodiment illustrated in Figure 2, the first set of switches comprises a first switch 41, a second switch 44, a third switch 46, and a fourth switch 47. The first switch 41 may be disposed between the first input port IN_P of the balanced input port and a first terminal of the first capacitance C21.The second switch 44 may be disposed between a second terminal of the first capacitance and a first connection port A which is connected to the second input port IN_N of the balanced input port in this embodiment. The third switch 46 may be disposed between a first terminal of the second capacitance and a second connection port B which is connected to the first input port of the balanced input port in this embodiment. The fourth

switch 47 may be disposed between the second input port of the balanced input port and a second terminal of the second capacitance.

[0016] The second set of switches may include a fifth switch 42, a sixth switch 43, a seventh switch 45, and an eighth switch 48. The fifth switch 42 may be disposed between the first terminal of the first capacitance and a first end of the third capacitance C23. The sixth switch 43 may be disposed between the first input port of the balanced input port and the second terminal of the first capacitance C21. The seventh switch 45 may be disposed between the second input port of the balanced input port and the first terminal of the second capacitance C22. The eighth switch 48 may be disposed between the second terminal of the second capacitance C22 and the second terminal of the third capacitance C23.

[0017] As described above, the first oscillator signal LO_0 may be applied to each switch of the first set of switches and the second oscillator signal LO_180 may be applied to each switch of the second set of switches.

[0018] Let us now consider the operation of the amplifier according to this embodiment of the invention during a clock cycle of the local oscillator signals LO_0 and LO_180. The clock cycle may be divided into two stages. In the first stage, the value of the first oscillator signal LO_0 is high and the value of the second oscillator signal LO_180 remains low. Accordingly, the first set of switches, i.e. the switches 41, 44, 46, and 47, is closed in the first stage. Thereby, the closed first set of switches forms a circuit illustrated in Figure 3A. That is, the first and the second capacitance C21 and C22 are connected in parallel between the first and the second input port of the balanced input port. The first switch 41 connects the first terminal of the first capacitance C21 to the first input port and the second switch 44 connects the second terminal of the first capacitance C21 to the second input port. Correspondingly, the third switch 46 connects the first terminal of the second capacitance C22 to the first input port and the fourth switch 47 connects the second terminal of the second capacitance C22 to the second input port.

[0019] When connected in parallel between the first and the second input port, the first and the second capacitance are charged with a voltage corresponding to the voltage between the first and the second input port IN_P and IN_N. The voltages over the first and the second input port IN_P and IN_N are illustrated in Figure 4. With reference to Figures 2 and 4, voltage V1A represents the voltage between the first input port and the ground level, and voltage V1B represents the voltage between the second input port and the ground level. Voltage V1 represents the voltage between the first and the second input port IN_P and IN_N, voltage V2 represents the voltage over the second capacitance C22, and voltage V3 represents the voltage over the first capacitance C21. Signals input into the input ports IN_P and IN_N are also illustrated in Figure 4. Accordingly, the first and the second capacitance C21 and C22 are charged with voltage V1 in the first stage.

[0020] In the second stage, the value of the first oscillator signal LO_0 is low and the value of the second oscillator signal LO_180 is high. Accordingly, the first set of switches, i.e. the switches 41, 44, 46, and 47, is open in the second stage, and the second set of switches, i.e. the switches 42, 43, 45, and 48, is closed. Thereby, the closed second set of switches forms a circuit illustrated in Figure 3B. That is, the first capacitance C21 is connected in series with the second capacitance C22 and the third capacitance C23 between the first and the second input port. In more detail, the sixth switch 43 connects the second terminal of the first capacitance C21 to the first input port IN_P, and the fifth switch 42 connects the first terminal of the first capacitance C21 to the first terminal of the third capacitance C23. The rest of the circuit illustrated in Figure 3B is formed by the seventh switch 45 connecting the first terminal of the second capacitance C22 to the second input port IN_N and the eighth switch 48 connecting the second terminal of the second capacitance C22 to the second terminal of the third capacitance C23.

[0021] Accordingly, the first and the second capacitance C21 and C22 release their charges into the third capacitance C23. In addition to the voltages in the first and the second capacitance C21 and C22, the third capacitance

C23 is charged with the input voltage which sums up together with the voltages in the first and the second capacitance C21 and C22 in the second stage. Referring to Figure 4, voltage V2 represents the voltage charged into the second capacitance C22 just before closing the second set of switches, and voltage V3 represents the voltage charged into the first capacitance C21 just before closing the second set of switches. In practice, voltages V2 and V3 roughly equal the voltage V1, if the level of the input signal has not changed significantly between the first and the second stage. Accordingly, the sum of voltages V2 and V2 is charged into the third capacitance C23 together with the current voltage V1' between the input ports of the balanced input port, i.e. the voltage V4 over the third capacitance C23 becomes V4=V1'+V2+V3. A first and a second output port OUT_P and OUT_N of a balanced output port may be connected to the first and the second terminal of the third capacitance C23, respectively. If the oscillator signal frequency is higher than the highest frequency component of the input signals IN1 and IN2 input to the input ports IN_P and IN_N, i.e. the voltages of the input signals IN1 and IN2 do not vary significantly over one period of the local oscillator signals LO_0 and LO_180, the input voltage V1 is roughly tripled. In other words, the amplification of the passive amplifier according to this embodiment of the invention is 9 dB, which is affected by the actual implementation and the properties of the components used in the amplifier. The amplification of 9 dB is obtained with a passive amplifier structure without an additional power supply (except the oscillator signals, of course).

[0022] The principles of the amplifier according to the embodiment of the invention are based on charging the first and the second capacitance C21 in the first stage and C22 and releasing the charges in the first and the second capacitance C21 and C22 in series with the input signal to the third capacitance C23 in the second stage. This operation of sequentially charging and discharging the first capacitance C21 makes the first capacitance C21 and the switches 41, 42, 43, and 44 (the first, second, fifth and sixth switch) to

function as a resistor implemented with a switched capacitor filter (SC filter) technique.

[0023] Figures 5A and 5B illustrate a schematic diagrams of a low-pass filter implemented with the SC filter technique (Figure 5A) and its equivalent circuit (Figure 5B). Switches 25 and 26 operated according to respective oscillator signals CLK_0 and CLK_180 and a first capacitor between the switches 25, 26 function as a resistor having a resistance R2=T/C1, where T is the period of the oscillator signals CLK_0 and CLK_180 and C1 is the capacitance of the first capacitor. V_in denotes an input port and V_out an output port of the filter. The equivalent circuit is illustrated in Figure 5B in which the switches 25 and 26 and the first capacitor have been replaced with a resistor having resistance R2. Additionally, the SC filter includes a second capacitor connected in parallel to the second switch 26. The corner frequency of the SC filter is defined as:

$$f_c = \frac{1}{2\pi T} \cdot \frac{C1}{C2}, \quad (1)$$

where C2 is the capacitance of the second capacitor. It can be seen that if the frequency of the oscillator signals is constant, the corner frequency depends on the ratio of the capacitances C1 and C2. In CMOS implementations, the absolute capacitance values may have a high diversity, but the ratio of the capacitance values remains very stable and accurate. That is, the ratio C1/C2 remains quite constant regardless of variations in the absolute values of C1 and C2. Accordingly, the corner frequency may be defined accurately and it has only marginal variations.

[0024] Consequently, the amplifier according to an embodiment of the invention may be used as a low-pass filter by designing the components, i.e. the first, the second, and the third capacitance C21, C22, and C23, the switches 41 to 48 and the oscillator signals LO_0 and LO_180 properly. Now, the first, second, fifth, and sixth switch 41, 42, 43, and 44 and the first capacitance C21 function as a first resistor, and the third, fourth, seventh, and eighth switch 45, 46, 47, and 48 and the second capacitance C22 function as a second resistor. The corner frequency is defined by the ratio of the

capacitance values of the first and the third capacitance C21 and C23 and the ratio of the capacitance values of the second and the third capacitance C22 and C23. If the capacitance value of the second capacitance C22 equals to that of the first capacitance C21, the corner frequency simplifies into

$$f_c = \frac{1}{4\pi T} \cdot \frac{C21}{C23} .$$

[0025] Accordingly, the amplifier according to an embodiment of the invention is configured to function also as a low-pass filter having a corner frequency defined by capacitance values of the first, second, and third capacitance C21, C22, and C23. Therefore, no additional components are required for implementation of the low-pass filter. This reduces the size of a receiver structure employing the passive amplifier according to the embodiment of the invention.

[0026] Figure 6 illustrates an amplifier configuration similar to that illustrated in Figure 2. Referring to Figure 2 and the embodiment described above, the connection ports A and B were connected to the second and the first input port IN_N and IN_P, respectively. In Figure 6, the connection ports A and B are now open. It is possible to control the amplification or voltage multiplication factor of the amplifier by connecting the connection ports A and B appropriately. Figure 6 is a starting point for an automatic gain control (AGC) amplifier according to embodiments of the invention.

[0027] In an embodiment illustrated in Figure 7, the amplifier illustrated in Figure 6 is now denoted by reference numeral 70. The first connection port A is connected to a first switching mechanism 72 which is configured to connect the first connection port A to one of output ports C, D, or E of the first switching mechanism 72. The second connection port B is connected to a second switching mechanism 74 which is configured to connect the second connection port B to one of output ports F, G, or H of the second switching mechanism 74. Output port C of the first switching mechanism 72 and output port H of the second switching mechanism 74 may be connected to the first input port IN_P

of the balanced input port of the amplifier 70. Output port D of the first switching mechanism 72 may be connected to the output port G of the second switching mechanism 74. Output port E of the first switching mechanism 72 and output port F of the second switching mechanism 74 may be connected to the second input port IN_N of the balanced input port of the amplifier 70.

[0028] The first and the second switching mechanism may be controlled by a controller 76 according to the desired voltage multiplication factor. The controller 76 may determine the desired voltage multiplication factor according to a method known in the art related to AGC amplifiers. When the desired voltage multiplication factor is three (amplification is 9dB), the controller 76 may control the first switching mechanism 72 to connect the first connection port A to output port E, i.e. to the second input port IN_N, and the second switching mechanism 74 to connect the second connection port B to output port H, i.e. to the first input port IN_P. This configuration corresponds to the embodiment described above with reference to Figure 2. Accordingly, the first and the second capacitance C21 and C22 are connected in parallel between the input ports IN_P and IN_N of the balanced input port in the first stage (as illustrated in Figure 3A) and in series with the third capacitance C23 between the input ports in the second stage (as illustrated in Figure 3B).

[0029] When the desired voltage multiplication factor is two (amplification is 6 dB), the controller 76 may control the first switching mechanism 72 to connect the first connection port A to output port D and the second switching mechanism 74 to connect the second connection port B to output port G. In other words, the first connection port A is connected to the second connection port B. Accordingly, the first and the second capacitance C21 and C22 are connected in series between the input ports IN_P and IN_N of the balanced input port in the first stage, as illustrated in Figure 8A. Now, the voltage between the input ports IN_P and IN_N is divided between the first and the second capacitance in the first stage and, therefore, the voltage charged into the first and the second capacitance, and the voltage multiplication factor of the amplifier is lower than in the case where the capacitances were connected

in parallel. If the capacitance values of the first and the second capacitance C21 and C22 are equal, the input voltage is divided equally between the first and the second capacitance. The second stage is again similar to that illustrated in Figure 3B, i.e. the first, second, and third capacitance C21, C22, and C23 are connected in series between the input ports IN_P and IN_N.

[0030] When the desired voltage multiplication factor is one, the controller 76 may control the first switching mechanism 72 to connect the first connection port A to output port C, i.e. to the first input port IN_P, and the second switching mechanism 74 to connect the second connection port B to output port F, i.e. to the second input port IN_N. This configuration is illustrated in Figure 8B. In this case, the first and the second capacitance are not charged in the first stage and, as a result, no voltage multiplication is obtained (amplification is 0 dB). The second stage is again similar to that illustrated in Figure 3B, i.e. the first, second, and third capacitance C21, C22, and C23 are connected in series between the input ports IN_P and IN_N.

[0031] In some cases, the desired voltage multiplication factor may, however, be other than 1 (0 dB), 2 (6 dB), or 3 (9 dB). Figure 9 illustrates an embodiment of the invention, which is similar to the configuration illustrated in Figure 6 except that a fourth capacitance C5 is provided between the first and the second connection port A and B. In this embodiment, the first set of switches connects the first, second, and fourth capacitance C21, C22, and C5 in series between the input ports IN_P and IN_N in the first stage. Accordingly, a portion of the total input voltage is charged into the fourth capacitance C5, and the rest of the input total voltage is charged into the first and the second capacitance C21 and C22. The degree of voltage charged into the fourth capacitance C5 depends on the capacitance value of the fourth capacitance with respect to the capacitance values of the first and the second capacitance C21 and C22. In the second stage, the second set of switches connects the first and the second capacitance in series with the third capacitance C23 between the input ports IN_P and IN_N. Now, the voltage charged into the first and the second capacitance C21 and C22 is released into the third

capacitance C23 in series with the input voltage. The fourth capacitance C5 may be isolated from the circuit in the second stage.

[0032] In this embodiment, the amplification depends on the amount of input voltage charged into the fourth capacitance C5, i.e. on the capacitance value of the fourth capacitance C5, according to the following equation:

$$A = \frac{4 \cdot C5 + C21}{2 \cdot C23 + 2 \cdot C5 + C21} \quad (2)$$

where *C*21, *C*23, and *C*5 represent the capacitance values of the first, third, and fourth capacitance C21, C23, and C5, respectively. Here, it is assumed that the capacitance value of the second capacitance C22 equals that of the first capacitance C21.The higher the capacitance value of the fourth capacitance C5 is, the lower is the voltage over the fourth capacitance C5 in the first stage, i.e. the higher is the voltage multiplication factor of the amplifier. The voltage multiplication factor of the amplifier may be adjusted on-the-fly by adjusting the capacitance value of the fourth capacitance C5. For that purpose, an adjustment circuit may be arranged into the amplifier. Figure 10 illustrates the basic amplifier structure 70 in which the fourth capacitance C5 is provided between the connection ports A and B. In addition to the fourth capacitance, the adjustment circuit is arranged between the connection ports A and B and in parallel with the fourth capacitance C5. The adjustment circuit may comprise capacitances C31, C32, C33, and C34 and switches 42 and 43. The effective capacitance value of the fourth capacitance value, i.e. the additional capacitance contributed to the amplifier circuit 70 by the fourth capacitance, is adjusted by selecting capacitances of the adjustment circuit appropriately in parallel with the fourth capacitance. The capacitances C31, C32, C33, and C34 may be selected by closing and/or opening the switches 42 and 43 appropriately. The operation of the switches 42 and 43 may be controlled by a control signal generator 100. The more capacitances that are connected in parallel with the fourth capacitance C5, the higher is their combined capacitance value, i.e. the higher is the effective capacitance induced by the fourth capacitance C5. The adjustment circuit may comprise more stages than illustrated in Figure 10, or it may be implemented according to any other method known in the art.

[0033] In the embodiment described above with reference to Figure 9, a maximum voltage multiplication factor of the amplifier is two (6 dB), since the configuration is based on connecting the connection port A to the connection port B (see Figure 7 for connection D, G in the respective switches 72 and 74).

[0034] In other words, the amplification may be adjustable up to 6 dB. Figure 11 illustrates another embodiment in which the maximum voltage multiplication factor of the amplifier is three (9 dB) and the amplification is adjustable up to 9 dB. This embodiment is based on the embodiment illustrated in Figure 2 in which the first connection port A was connected to the second input port IN_N and the second connection port B was connected to the first input port IN_P. In the embodiment illustrated in Figure 11, a fifth capacitance C26 is arranged between the first connection port A and the second input port IN_N. Correspondingly, a sixth capacitance C25 is arranged between the second connection port B and the first input port IN_P. Wording "fifth" and "sixth" capacitance is used in order not to cause confusion with the fourth capacitance comprised in the embodiment described above.

[0035] In the first stage, the first set of switches connects the first capacitance C21 in series with the fifth capacitance C26 and in parallel with the second and the sixth capacitance C22 and C25 between the input ports IN_P and IN_N. Consequently, the voltage between the input ports IN_P and IN_N is divided between the first and the fifth capacitance C21 and C26 and between the second and the sixth capacitance C22 and C26. Therefore, the voltage over the first capacitance C21 depends on the capacitance value of the fifth capacitance C26 and the voltage over the second capacitance C22 depends on the capacitance value of the sixth capacitance C25. The higher is the capacitance values of the fifth and the sixth capacitance C26 and C25, the higher is the voltage over the first and the second capacitance C21 and C22, respectively. The second stage is similar to the embodiments described above, i.e. the second set of switches connects the first and the second capacitance C21 and C22 in series with the third capacitance C23 between the input ports

IN_P and IN_N. Accordingly, the fifth and the sixth capacitance C26 and C25 are isolated from the circuit in the second stage.

[0036] The capacitance values of the fifth and the sixth capacitance C26 and C25 may be adjusted according to the desired voltage multiplication factor. For example, an adjustment circuit similar to that illustrated in Figure 11 may be arranged in parallel with each of the fifth and the sixth capacitance C26 and C25. The amplification of the amplifier may be calculated from the capacitance values according to the following equation:

$$A = \frac{3 \cdot C26 + C21}{C26 + C21 + 2 \cdot C23}, \quad (3)$$

where C21, C23, and C26 represent the capacitance values of the first, third and fifth capacitance, respectively. In this case, it is assumed that the second capacitance C22 and the sixth capacitance C25 have the same capacitance values as the first and the fifth capacitance C21 and C26, respectively. It should be noted that equation (3) is simplified in the sense that it does not take into account on-resistances of the switches 41 to 48 and input and output impedances of the amplifier. The same simplification has been applied to equation (3), too.

[0037] Embodiment illustrated in Figure 7 comprising the switches 72 and 74 controlled according to the desired voltage multiplication factor may still be improved by providing a fourth optional connection for the connection ports. In the embodiment illustrated in Figure 7, the possible voltage multiplication factors were one, two, and three, that is amplification of 0, 6, and 9 dB. Figure 12 illustrates an embodiment of the invention in which a fourth voltage multiplication factor may be selected with by connecting the connection ports A and B appropriately. The fourth voltage multiplication factor may be 1.4 (amplification is 3 dB), for example. The embodiment illustrated in Figure 12 comprises switching mechanisms 80 and 82, both having one input port and four output ports. Output ports C, D, and E of switching mechanism 80 are connected as those of the first switching mechanism 72 described above with

reference to Figure 7. Correspondingly, output ports F, G, and H of switching mechanism 82 are connected as those of the second switching mechanism 74.

[0038] Both switching mechanisms 80 and 82 comprise an additional output port which are connected to each other through an additional capacitance C7 (seventh capacitance). Accordingly, output port I of switching mechanism 80 is connected to output port J of switching mechanism 82 through the seventh capacitance C7. The capacitance value of the seventh capacitance C7 may be selected to provide a desired amplification factor (3 dB, for example) for the amplifier.

[0039] Switching mechanisms 80 and 82 may be controlled by a controller 84. The controller 84 may have a functionality similar to the controller 76 described above with reference to Figure 7. The only difference is that the switching mechanisms 80 and 82 now have four output ports, and the controller selects the desired voltage multiplication factor from a set of four possible factors.

[0040] With the embodiments having adjustable voltage multiplication factor as described above, the passive amplifier may be implemented with automatic gain control functionality. This feature is very practical in radio transceivers, since the level of a received radio signal may have high variations.

[0041] In general, the embodiments of the invention are advantageous in multi-mode radio receivers (or transceivers) operating at multiple frequency bands and requiring high linearity and noise figures from the receiver components. In such transceivers, it is generally difficult to arrange a low-noise amplifier (amplifier 2 in Figure 1) followed by filters changeable according to the current frequency band. If the filters following the low-noise amplifier are omitted, the amplification of the low-noise amplifier should typically be lowered and, as a result, noise figures of amplifiers following a downmixer (4 and 5 in Figure 1) have to be reduced. The embodiments of the invention comprise a passive amplifier having low noise figures and functioning also as a low-pass

switched capacitor filter without an increase in components or increase in the size of an actual implementation (integrated circuit, for example).

[0042] In practice, the passive amplifier according to embodiments of the invention may be implemented by arranging the first set of switches to respond to the first oscillator signal and the second set of switches to respond to the second oscillator signal, as described above. In that case, the first and the second oscillator signals may be different oscillator signals and the individual switches may have the same functionality, i.e. a switch may be closed when the level of an oscillator signal controlling the switch is high and open when the level of the oscillator signal is low. Alternatively, the first and the second set of switches may be arranged to respond to the same oscillator signal which may be the first or the second oscillator signal. In this case, the first set of switches may be arranged to be closed when the level of the oscillator signal is high (and open otherwise), and the second set of switches may be arranged to be closed when the level of the oscillator signal is low (and open otherwise). This functionality may be achieved by implementing the first set of switches by NMOS transistors and the second set of switches by PMOS transistors, for example. Accordingly, the operation of the first and the second set of switches may be complementary in the sense that both sets of switches are not closed at the same time.

[0043] In the description above, it is mentioned that the first and the second oscillator signals may have the same frequency. Accordingly, the oscillator signals may have different pulse ratios and/or pulse shapes, for example, as long as the first and the second set of switches are not closed at the same time. The first and the second oscillator signals may also have opposite phases.

[0044] Figure 13 illustrates an example of a practical implementation of the amplifier illustrated in Figure 2. Each of the switches 41 to 48 may be implemented by a single MOS transistor Q89 to Q96. The oscillator signals

CLK_0 and CLK_180 may be applied to the gates of the corresponding switches through a small capacitor C110 and C112 to C118.

[0045] The third capacitance C23 may be implemented by three capacitors C111, C108 and C130. Capacitor C130 may be connected in parallel with capacitors C111 and C108, and capacitors C111 and C108 may be connected in series, as shown in Figure 12. Capacitance values of capacitors C111 and C108 may be very small compared with the capacitance value of capacitor C130, and the main purpose of capacitors C111 and C108 may be to attenuate common mode oscillator signals.

[0046] While the embodiments are described above in conjunction with balanced input and output ports, an embodiment employing dual balanced structure may be formed by arranging two balanced passive amplifier structures in parallel and providing input signals into corresponding balanced input ports of the parallel structures in opposite phases and also obtaining output signals from corresponding balanced output ports of the parallel structures in opposite phases. In this structure, the oscillator signal may be input into corresponding input ports of the parallel structures in the same phase. Alternatively, oscillator signals may be provided into corresponding oscillator signal input ports of the parallel structures in opposite phases and signals in the corresponding input or output ports of the parallel structures are arranged to be in opposite phases. In a further alternative solution, the input signals, oscillator signals, or the output signals may be provided into (or obtained from) the corresponding ports of the parallel structures in opposite phases and switches of one structure may be implemented with NMOS transistors and switches of the other structure may be implemented with PMOS transistors. Other solutions for arranging a dual balanced structure are also possible. Advantages obtained with a dual balanced structure depend on the actual implementation but, generally, leakage of the oscillator signals into the input ports is lower with a dual-balanced structure. Additionally, loads experienced by the oscillator signals equalize better with respect to the

balanced structure, and this property facilitates maintaining the correct phasing of the oscillator signals.

[0047] It is obvious to one skilled in the art that the embodiments of the invention may be carried out in numerous ways in terms of practical implementation. For example, the switches 41 to 48 or Q89 to Q96 may be realized with GaAs field effect transistors, SOI-CMOS transistors, diodes, etc. Additional components may also be included in the embodiments described above, depending on the practical implementation. The embodiments may be realized on an integrated circuit, a printed circuit board, or any other material. Applications of the embodiments include radio transceivers or radio transmitters or receivers according to the following exemplary technologies: mobile telephones, Global Positioning System (GPS), Galileo, Wireless Local Area Network (WLAN), Bluetooth®, FM radio, television receivers, digital video broadcasting for handheld devices (DVB-H), AM receivers, audio amplifiers, measuring instruments, etc.

[0048] Even though the invention has been described above with reference to an example according to the accompanying drawings, it is clear that the invention is not restricted thereto but it can be modified in several ways within the scope of the appended claims.

Claims

1. A method, comprising:

receiving an input signal voltage into a first input port and a second input port of a balanced input port;

connecting, in a first stage, in response to a first oscillator signal, a first capacitance and a second capacitance between the first input port and the second input port of the balanced input port;

connecting, in a second stage, in response to a second oscillator signal, the first capacitance between the first input port and a third capacitance, and the second capacitance between the second input port and the third capacitance; and

obtaining a voltage over the third capacitance as an output voltage.

2. The method of claim 1, further comprising:

connecting a first terminal of the first capacitance, connected to the second input port in the first stage, to the first input port at the second stage;

connecting a second terminal of the first capacitance to a first terminal of the third capacitance in the second stage;

connecting a first terminal of the second capacitance, connected to the first input port in the first stage, to the second input port in the second stage; and

connecting a second terminal of the second capacitance to a second terminal of the third capacitance in the second stage.

3. The method of claim 1 or 2, further comprising:

charging, in the first stage, the first capacitance and the second capacitance with a voltage corresponding to the voltage over the first input port and the second input port; and

releasing, in the second stage, the charge in the first capacitance and the second capacitance into the third capacitance in series with the current voltage over the first input port and the second input port, to produce a voltage over the third capacitance, which is the sum of the voltage over the first capacitance in the first stage, the voltage over the second capacitance in the first stage, and the current voltage over the first input port and the second input port.

4. The method according to any of claims 1 to 3, further comprising:

producing the first oscillator signal and the second oscillator signal from a local oscillator signal used for downmixing a received radio signal.

5. The method according to any of claims 1 to 3, further comprising:

connecting, in the first stage, the first capacitance and the second capacitance between the first input port and the second input port either in series or in parallel depending on a desired voltage multiplication factor of the output signal.

6. The method of claim 5, further comprising:

connecting, in the first stage, the first capacitance and the second capacitance between the first input port and the second input port in series when the desired voltage multiplication factor is two and in parallel when the desired voltage multiplication factor is three.

7. The method of claim 5 or 6, further comprising:

connecting the first terminal and the second terminal of the first capacitance to the first input port in the first stage; and

connecting the first terminal and the second terminal of the second capacitance to the second input port in the first stage when the desired voltage multiplication factor is one.

8. The method according to any of claims 5 to 7, further comprising:

connecting, in the first stage, the first capacitance and the second capacitance in series between the first input port and the second input port; and

providing, in series with the first and the second capacitance, an additional capacitance having a capacitance value determined according to the desired voltage multiplication factor.

9. The method according to any of claims 1 to 8, further comprising:

configuring the frequencies of the first oscillator signal and the second oscillator signal to be higher than the highest frequency component of input signals at the input ports.

10. The method according to any of claims 1 to 9, further comprising:

defining a corner frequency of a low-pass filter with the capacitance values of the first capacitance, the second capacitance, and the third capacitance; and

low-pass filtering an input signal input to the first and the second input port.

11. The method according to any of claims 1 to 10, further comprising:

connecting, in the first stage, the first capacitance and the second capacitance between the first input port and the second input port in series; and

providing a fourth capacitance in series between the first capacitance and the second capacitance in the first stage,

wherein the capacitance value of the fourth capacitance is adjustable to enable adjustable voltage multiplication.

12. The method according to any of claims 1 to 10, further comprising:

connecting, in the first stage, the first capacitance and the second capacitance between the first input port and the second input port in series;

providing a fourth capacitance in series with the first capacitance in the first stage; and

providing a fifth capacitance in series with the second capacitance in the first stage,

wherein the capacitance values of the fourth capacitance and the fifth capacitance are adjustable to enable adjustable voltage multiplication.

13. The method according to any of claims 1 to 12, further comprising:

configuring the first stage to be the first half cycle of the oscillator signals; and

configuring the second stage to be the second half cycle of the oscillator signals.

14. The method according to any of claims 1 to 13, further comprising:

configuring the first oscillator signal and the second oscillator signal to be a same oscillator signal.

15. The method according to any of claims 1 to 13, further comprising:

configuring the first oscillator signal and the second oscillator signal to have a same frequency and different phases.

16. The method of claim 1, which method is carried out in an apparatus having a dual balanced structure.

17. A method, comprising:

producing a first oscillator signal and a second oscillator signal having the same frequency;

charging a first capacitance and a second capacitance with an input signal sample received into a first input port and a second input port of a balanced input port during a first half cycle of the first oscillator signal and the second oscillator signal; and

charging a third capacitance operationally coupled with the first capacitance and the second capacitance, with the charges in the first capacitance and the second capacitance together with an input signal sample received into the first input port and the second input port of the balanced input port during a second half cycle of the first oscillator signal and the second oscillator signal.

18. An apparatus, comprising:

an input interface comprising a balanced input port configured to receive a balanced input signal and an oscillator signal input port configured to receive a first oscillator signal and a second oscillator signal;

a first capacitance;

a second capacitance;

a third capacitance;

a first set of switches responsive to the first oscillator signal and configured to connect, in response to the first oscillator signal, the first and the

second capacitance between a first input port and a second input port of the balanced input port;

a second set of switches responsive to the second oscillator signal and configured to connect, in response to the second oscillator signal, the first capacitance between the first input port and the third capacitance, and the second capacitance between the second input port and the third capacitance; and

an output port connected to terminals of the third capacitance.

19. The apparatus of claim 18, wherein a first set of switches is configured to connect, when closed, a first terminal of the first and the second capacitance to the first input port and a second terminal of the first and the second capacitance to the second input port, and the second set of switches is configured to connect, when closed, the first terminal of the first capacitance to a first terminal of the third capacitance, the second terminal of the first capacitance to the first input port, the first terminal of the second capacitance to the second input port, and the second terminal of the second capacitance to a second terminal of the third capacitance.

20. The apparatus of claim 18 or 19, wherein the first oscillator signal and the second oscillator signal are a same oscillator signal.

21. The apparatus of claim 18 or 19, wherein the first oscillator signal and the second oscillator signal have a same frequency and different phases.

22. The apparatus according to any of claims 18 to 21, further comprising:

a local oscillator signal generator configured to apply the first oscillator signal and the second oscillator signal to the oscillator input port.

23. The apparatus of claim 22, wherein the local oscillator signal generator is configured to produce the first oscillator signal and the second oscillator signal from a local oscillator signal used for downmixing a received radio signal.

24. The apparatus of claim 22 or 23, wherein the local oscillator signal generator is configured to produce the first oscillator signal and the second oscillator signal to have a frequency higher than the highest expected frequency component of input signals at the input ports.

25. The apparatus according to any of claims 18 to 24, further comprising:

a controllable switching mechanism configured to connect, when the first set of switches is closed, the first capacitance and the second capacitance between the first input port and the second input port either in series or in parallel depending on a desired voltage multiplication factor effected by the apparatus on an input signal input to the balanced input port.

26. The apparatus of claim 25, wherein the switching mechanism is configured to connect the first capacitance and the second capacitance between the first input port and the second input port in series when the desired voltage multiplication factor is two and in parallel when the desired voltage multiplication factor is three.

27. The apparatus of claim 25 or 26, wherein the switching mechanism is further configured to connect, when the first set of switches is closed, two terminals of the first capacitance to the first input port and two terminals of the second capacitance to the second input port when the desired voltage multiplication factor is one.

28. The apparatus according to any of claims 25 to 27, further comprising:

an additional capacitance having a capacitance value determined according to the desired voltage multiplication factor,

wherein the switching mechanism is configured to connect the first capacitance and the second capacitance in series with the additional capacitance between the first input port and the second input port.

29. The apparatus according to any of claims 18 to 28, wherein the apparatus is configured to function as a low-pass filter having a corner

frequency defined by a ratio of the capacitance values of the first capacitance, the second capacitance, and the third capacitance.

30. The apparatus according to any of claims 18 to 29, wherein

the first set of switches comprises a first switch connected between the first input port and a first terminal of the first capacitance, a second switch connected between the second input port and a second terminal of the first capacitance, a third switch connected between the first input port and a first terminal of the second capacitance, and a fourth switch connected between the second input port and a second terminal of the second capacitance, and

the second set of switches comprises a fifth switch connected between the first terminal of the first capacitance and a first terminal of the third capacitance, a sixth switch connected between the first input port and the second terminal of the first capacitance, a seventh switch connected between the second input port and the first terminal of the second capacitance, and an eighth switch connected between the second terminal of the second capacitance and a second terminal of the third capacitance.

31. The apparatus according to any of claims 18 to 30, further comprising:

a fourth capacitance,

wherein the first set of switches is configured to connect, when closed, the fourth capacitance together with the first capacitance and the second capacitance in series between the first input port and the second input port of the balanced input port.

32. The apparatus of claim 31, further comprising:

an adjustment circuit configured to adjust the capacitance value of the fourth capacitance and to control a voltage multiplication factor of the apparatus.

33. The apparatus according to any of claims 18 to 30, further comprising:

a fifth capacitance; and

a sixth capacitance,

wherein the first set of switches is configured to connect, when closed, the fifth capacitance in series with the first capacitance, the sixth capacitance in series with the second capacitance, and the first capacitance and the fifth capacitance in parallel with the second capacitance and the sixth capacitance between the first input port and the second input port of the balanced input port.

34. The apparatus of claim 33, further comprising:

an adjustment circuit configured to adjust the capacitance value of the fifth capacitance and the sixth capacitance and to control a voltage multiplication factor of the apparatus.

35. The apparatus according to any of claims 18 to 34, having a dual balanced structure.

36. An automatic gain control amplifier, comprising:

an input interface comprising a balanced input port configured to receive a balanced input signal and an oscillator signal input port configured to receive a first oscillator signal and a second oscillator signal;

a first capacitance;

a second capacitance;

a third capacitance;

a first set of switches responsive to the first oscillator signal and configured to connect, in response to the first oscillator signal, the first and the second capacitance between a first input port and a second input port of the balanced input port;

a second set of switches responsive to the second oscillator signal and configured to connect, in response to the second oscillator signal, the first capacitance between the first input port and the third capacitance, and the second capacitance between the second input port and the third capacitance; and

an output port connected to terminals of the third capacitance.

37. A radio transmitter comprising an amplifier, comprising:

an input interface comprising a balanced input port configured to receive a balanced input signal and an oscillator signal input port configured to receive a first oscillator signal and a second oscillator signal;

a first capacitance;

a second capacitance;

a third capacitance;

a first set of switches responsive to the first oscillator signal and configured to connect, in response to the first oscillator signal, the first and the second capacitance between a first input port and a second input port of the balanced input port;

a second set of switches responsive to the second oscillator signal and configured to connect, in response to the second oscillator signal, the first capacitance between the first input port and the third capacitance, and the second capacitance between the second input port and the third capacitance; and

an output port connected to terminals of the third capacitance.

38. An apparatus, comprising:

input means comprising a balanced input port for receiving a balanced input signal and an oscillator signal input port for receiving a first and a second oscillator signal;

first capacitance means for holding charge;

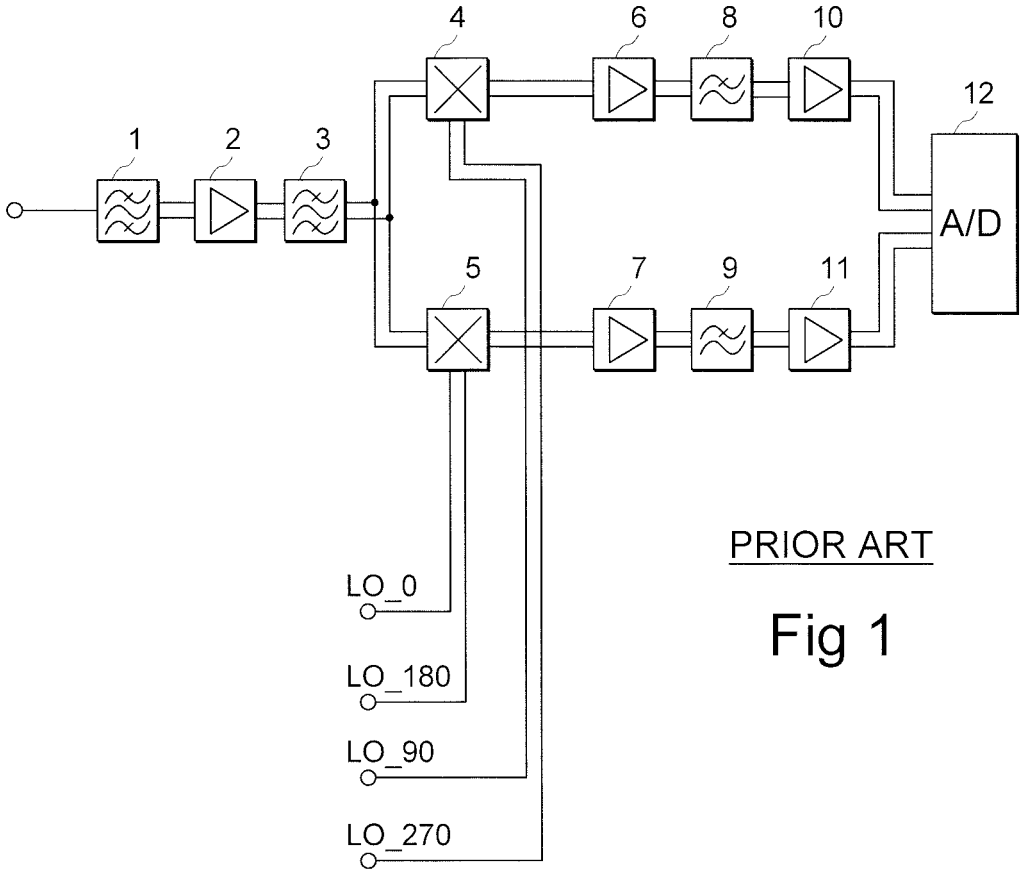
second capacitance means for holding charge;

third capacitance means for holding charge;

first switching means responsive to the first oscillator signal for connecting, in response to the first oscillator signal, the first capacitance means and the second capacitance means between a first input port and a second input port of the balanced input port;

second switching means responsive to the second oscillator signal for connecting, in response to the second oscillator signal, the first capacitance means between the first input port and the third capacitance means and the second capacitance means between the second input port and the third capacitance means; and

output means connected to terminals of the third capacitance means.



PRIOR ART

Fig 1

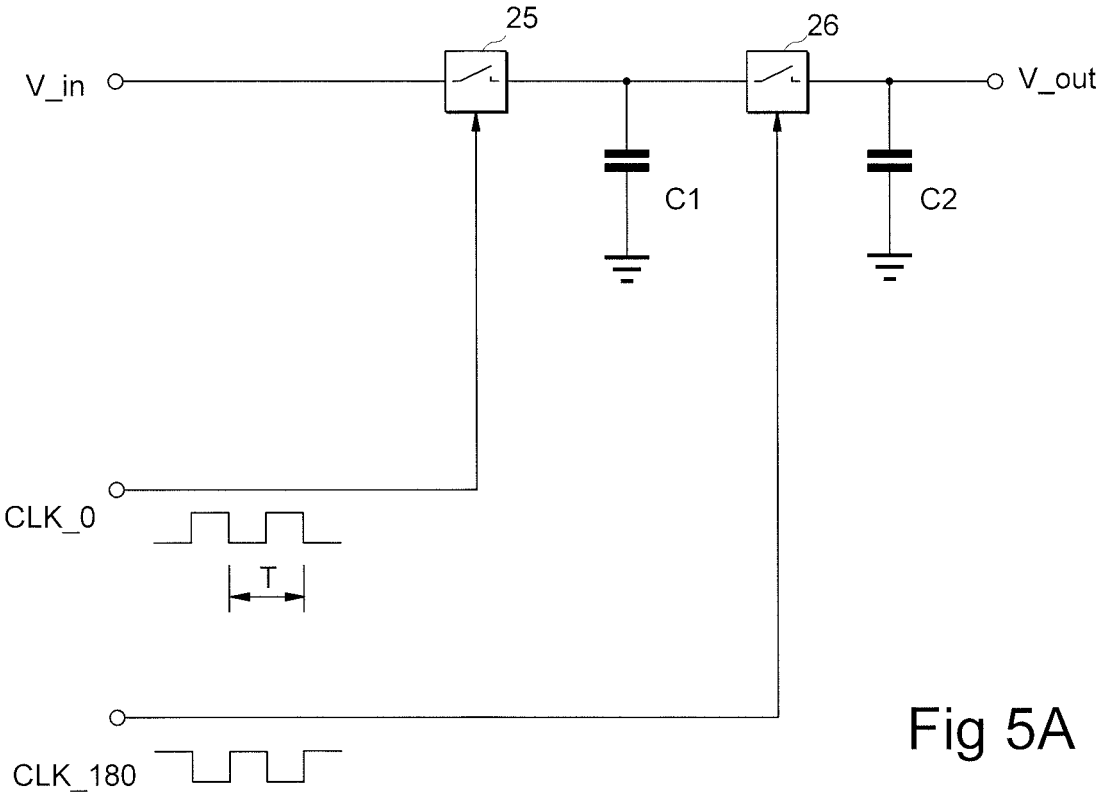


Fig 5A

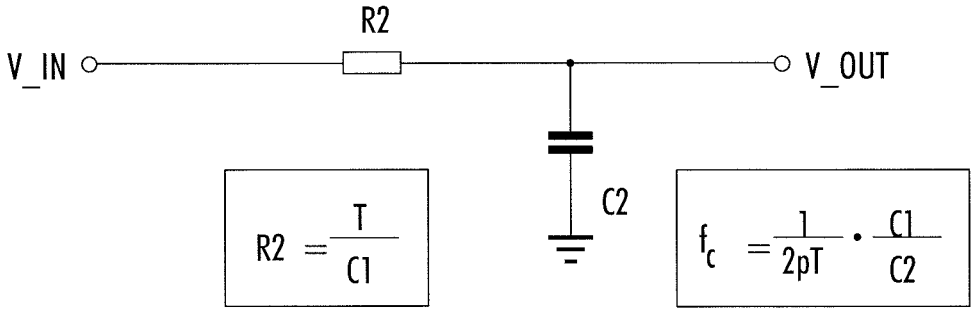

R2
V_IN
V_OUT
C2
$R2 = \frac{T}{C1}$
$f_c = \frac{1}{2pT} \cdot \frac{C1}{C2}$

Fig 5B

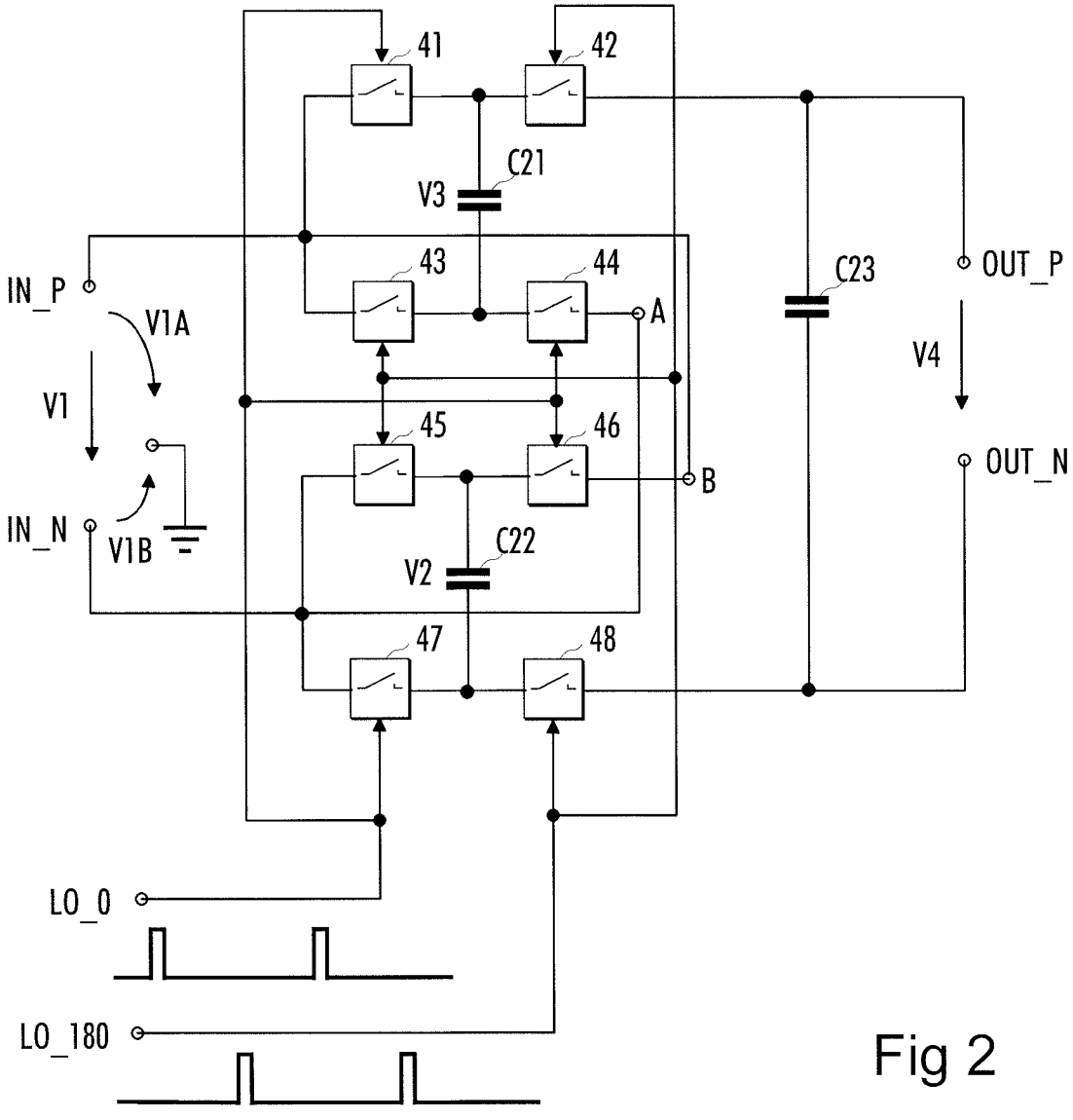

41
42
C21
V3
43
44
A
IN_P
V1A
V1
45
46
B
IN_N
V1B
C22
V2
47
48
C23
OUT_P
V4
OUT_N
LO_0
LO_180

Fig 2

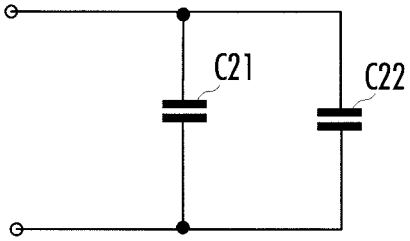


Fig 3A

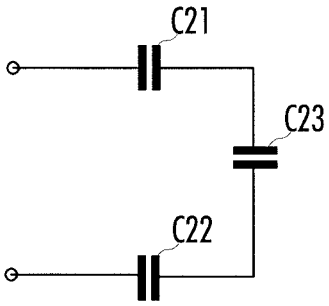


Fig 3B

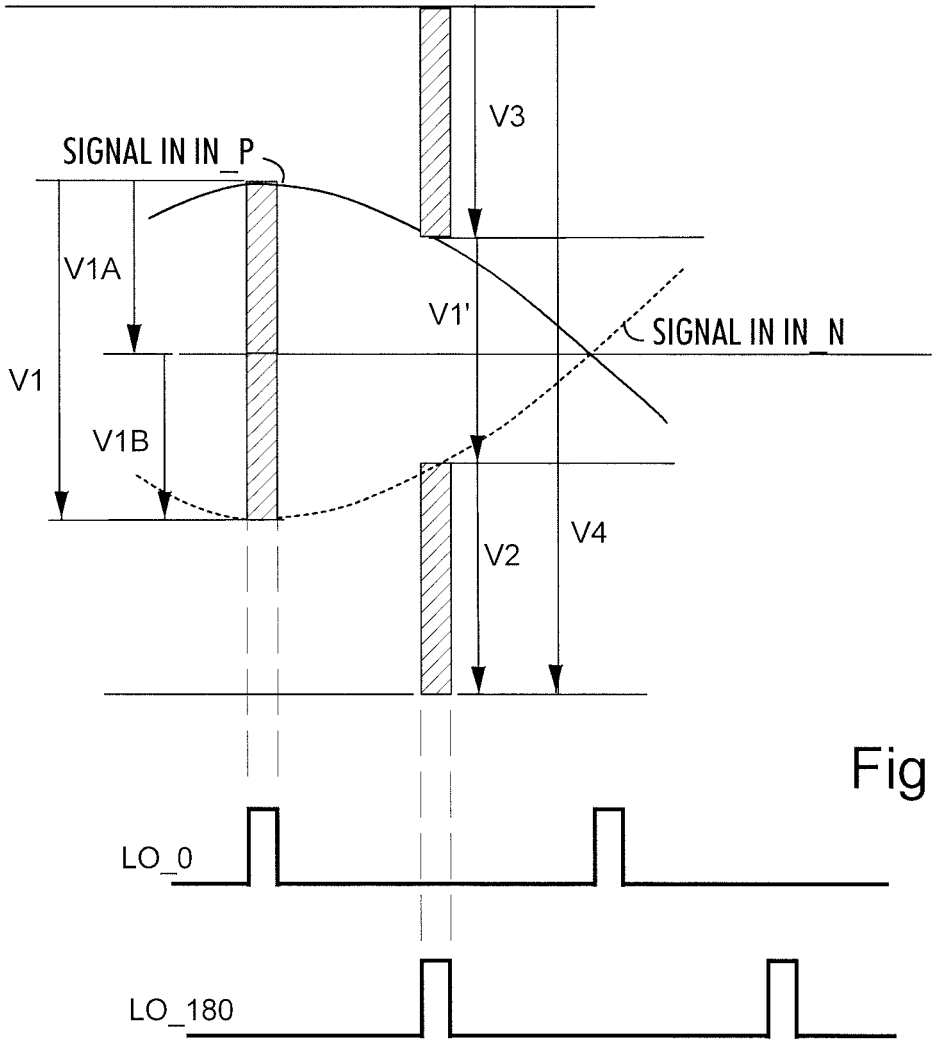


Fig 4

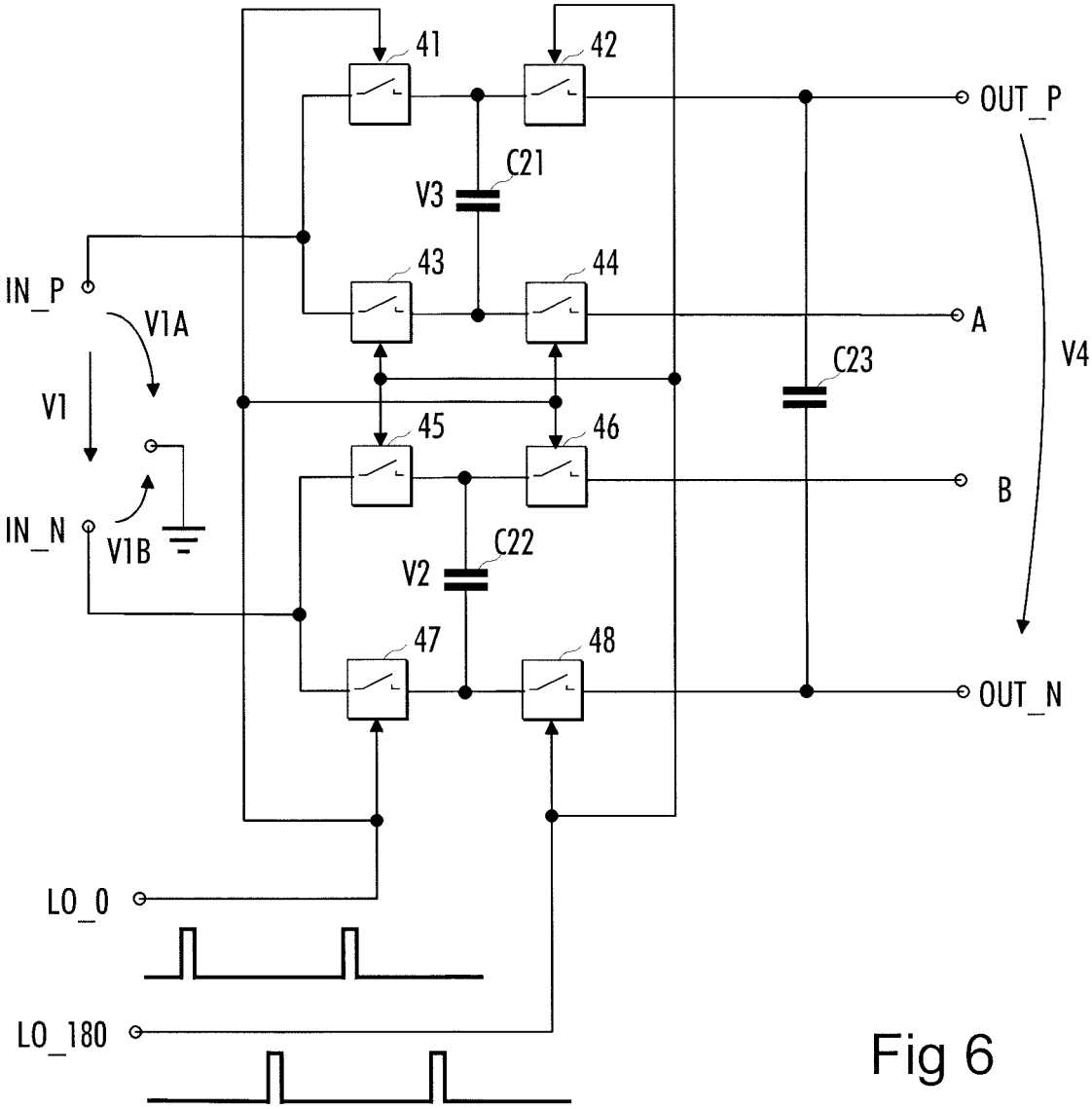

41
42
OUT_P
C21
V3
43
44
IN_P
V1A
A
V4
C23
V1
45
46
B
IN_N
V1B
C22
V2
47
48
OUT_N
LO_0
LO_180

Fig 6

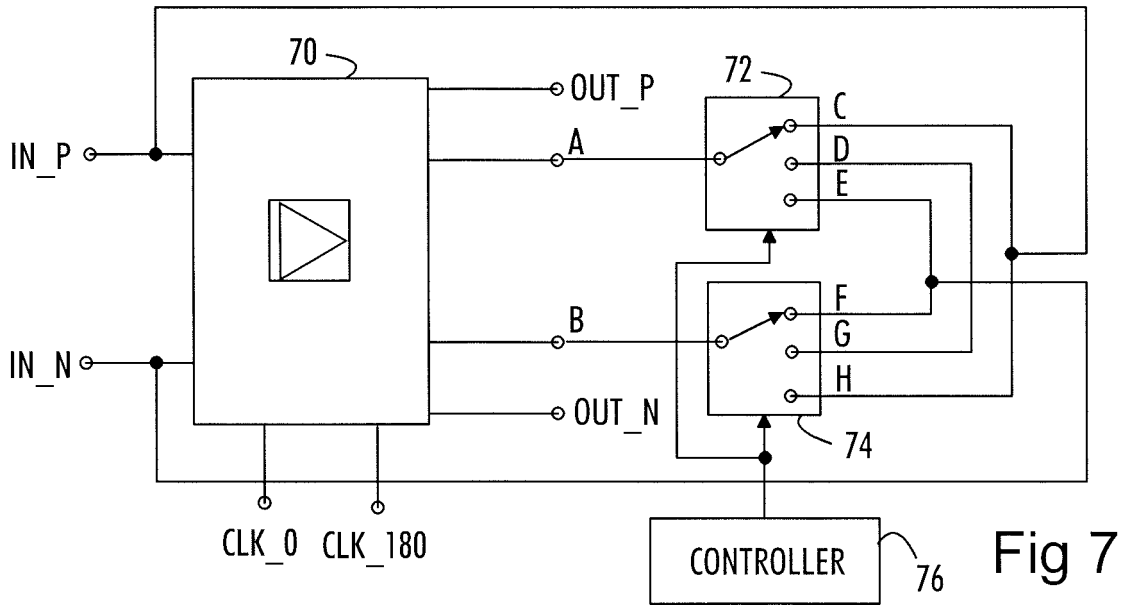
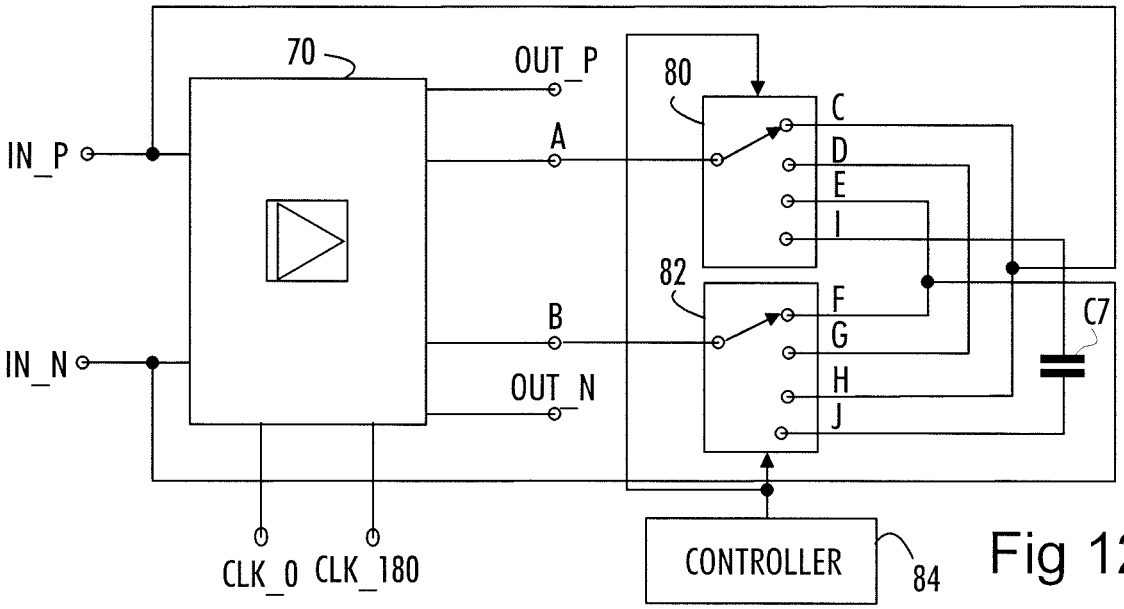

70
OUT_P
72
C
IN_P
A
D
E
F
B
G
IN_N
H
OUT_N
74
CLK_0
CLK_180
CONTROLLER
76

Fig 7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OUT_P
80
C
D
E
I
IN_P
A
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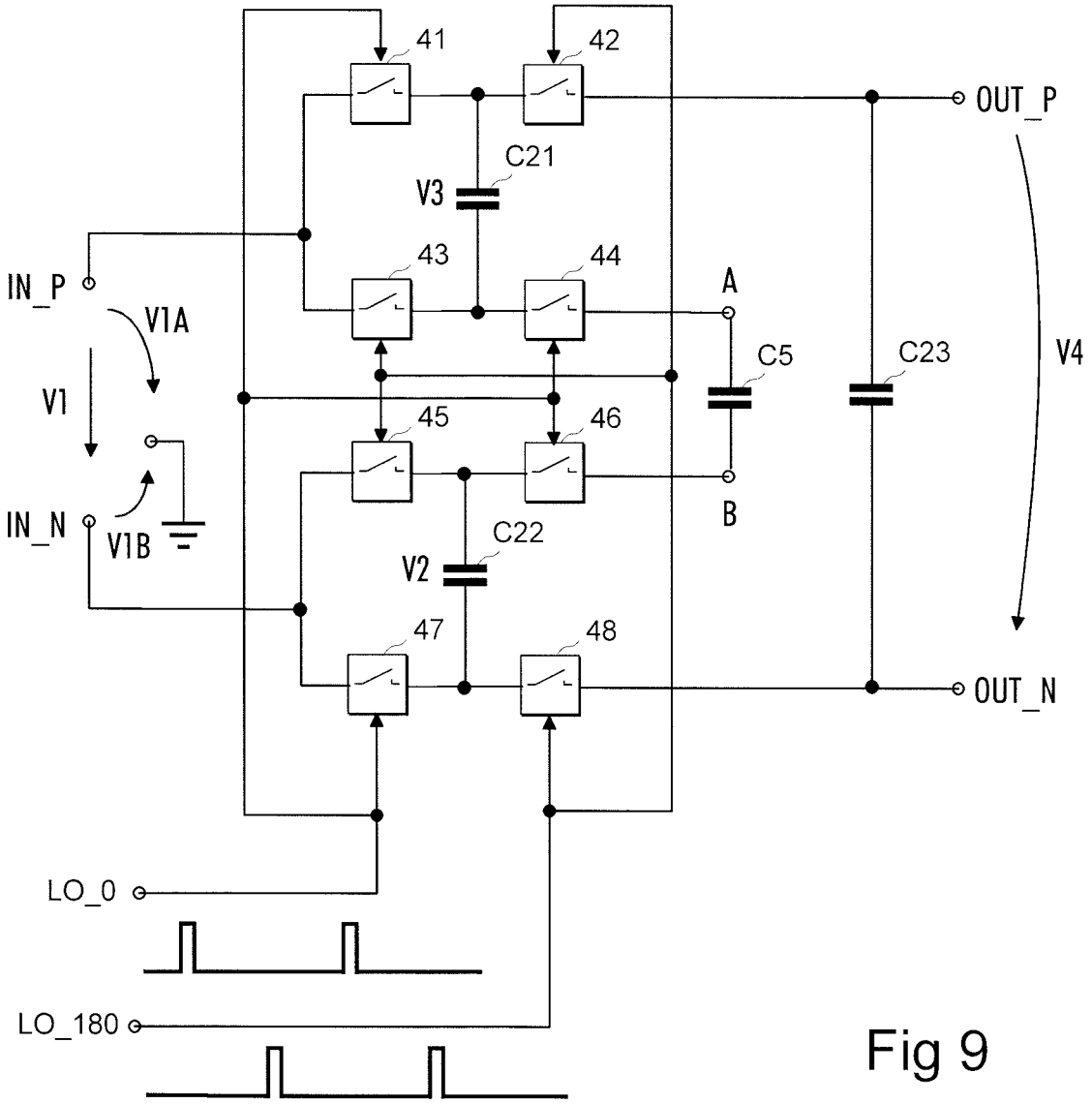
F
G
H
J
C7
B
IN_N
OUT_N
CLK_0
CLK_180
CONTROLLER
84

Fig 12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C21
V3
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A
IN_P
V1A
C5
C23
V4
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IN_N
V1B
B
C22
V2
47
48
OUT_N
LO_0
LO_180

Fig 9

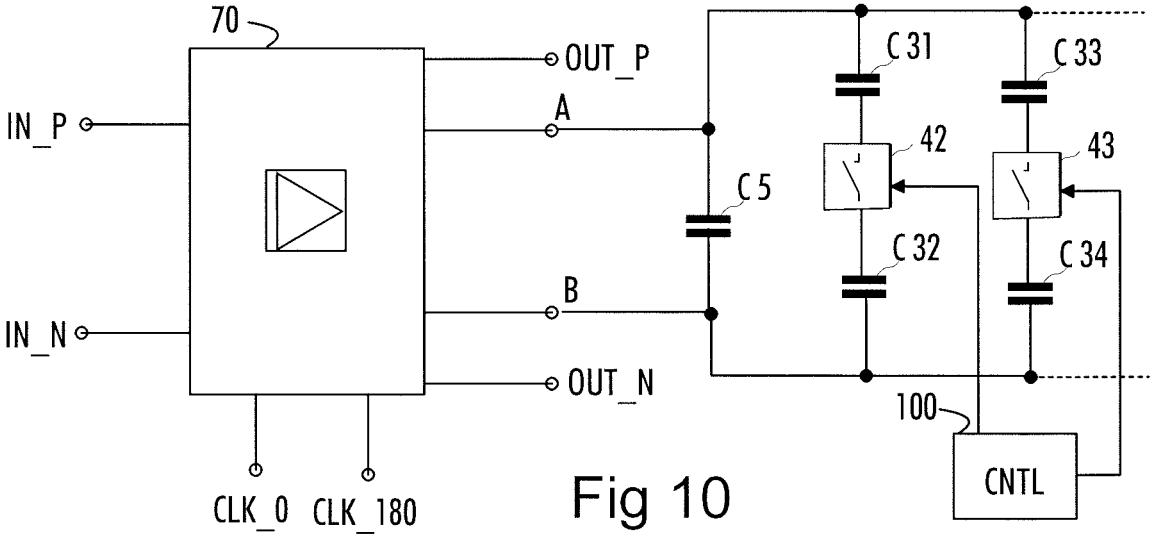
70
IN_P
IN_N
OUT_P
A
B
OUT_N
CLK_0
CLK_180
C 31
C 33
42
43
C 5
C 32
C 34
100
CNTL

Fig 10

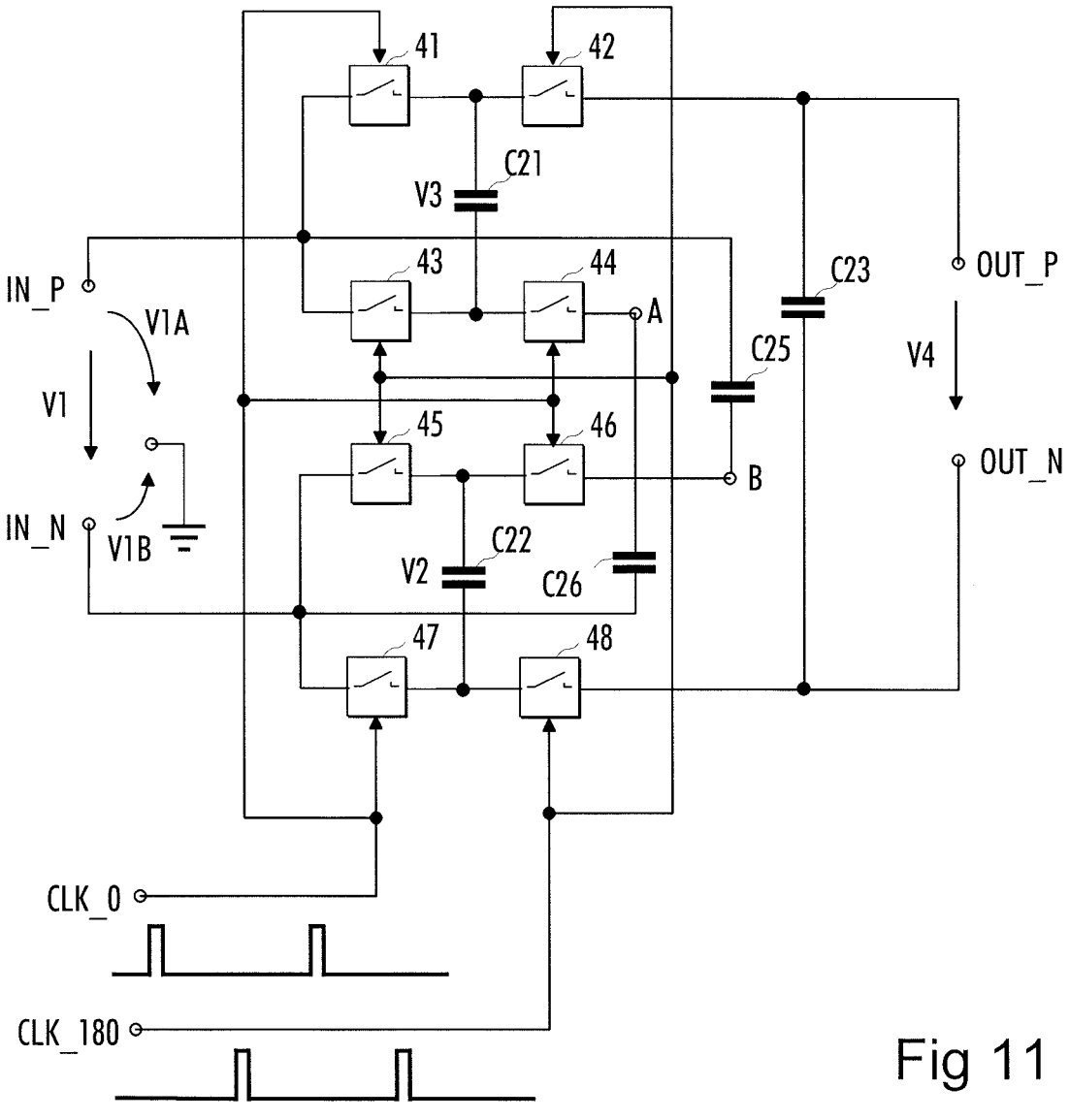
41
42
C21
V3
43
44
IN_P
V1A
V1
A
C23
OUT_P
C25
V4
45
46
IN_N
V1B
B
OUT_N
V2
C22
C26
47
48
CLK_0
CLK_180

Fig 11

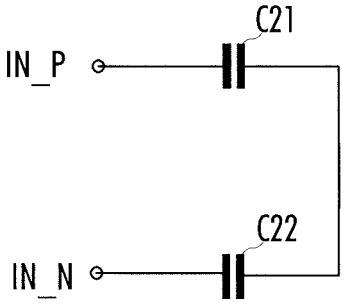

Fig 8A

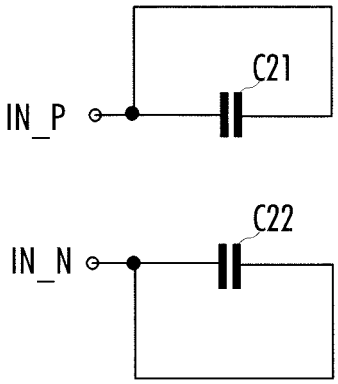

Fig 8B

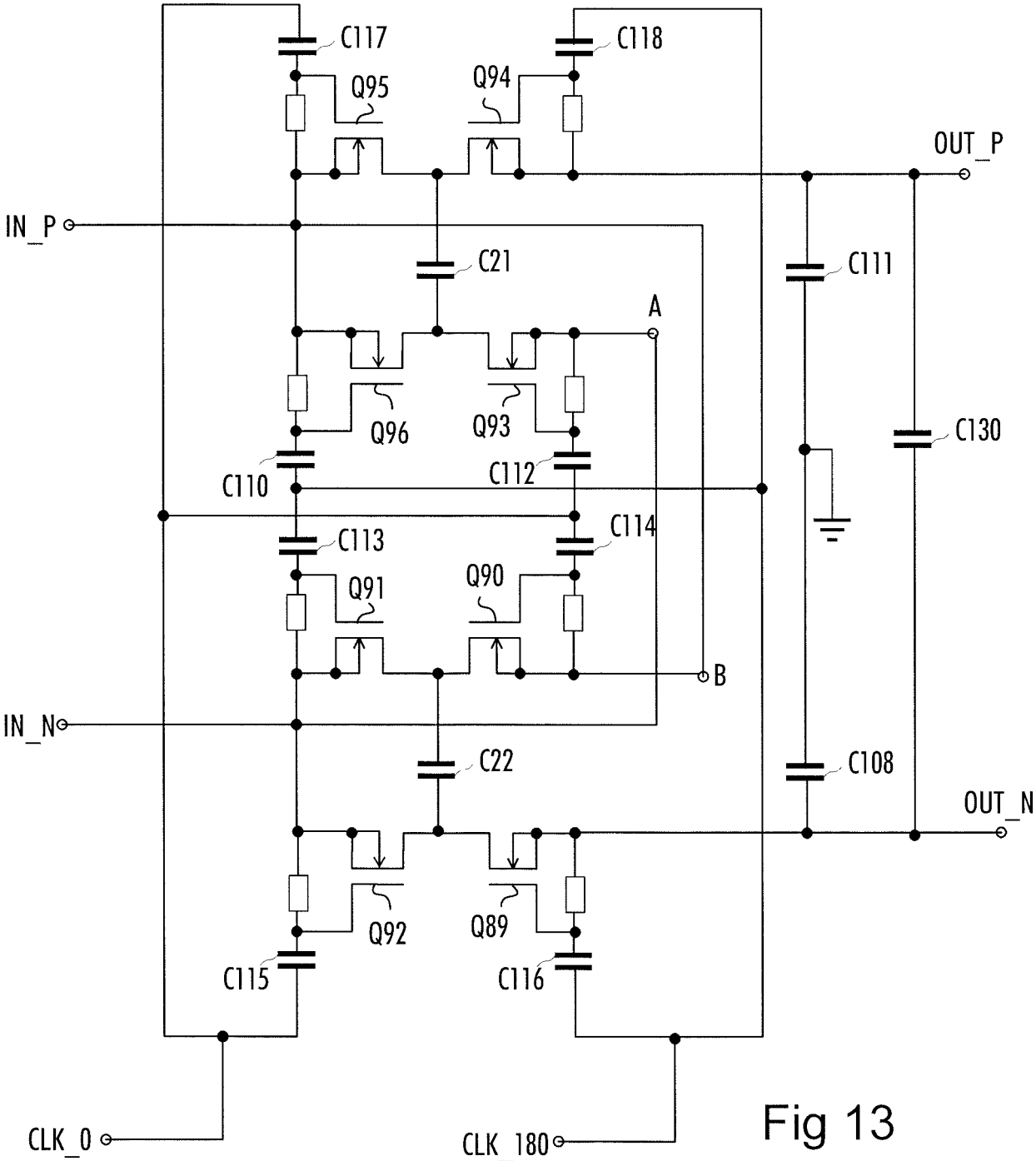

Fig 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI2007/050390

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC8: H03G, H02M, H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

DK, FI, NO, SE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-internal, WPI, INSPEC, XPIEE, XPI3E, Google

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5262934 A (PRICE, C. C.) 16 November 1993 (16.11.1993), abstract; column 3, row 65-column 6, row 36; figures 1 and 4	1-6, 9, 10, 13-26, 29, 35-38
X	US 5237209 A (BREWER, R. J.) 17 August 1993 (17.08.1993), abstract; column 2, row 66-column 4, row 62; figures 1, 3, and 5	1-6, 9, 10, 13-26, 29, 35-38
X	US 5581454 A (COLLINS, H.) 03 December 1996 (03.12.1996), abstract; column 8, row 65-column 13, row 40; figures 2, 3, and 8-12	1, 4, 5, 8-10, 13-16, 18, 20-25, 28, 29, 31, 33, 35-38
X	US 5828560 A (ALDERMAN, R. J.) 27 October 1998 (27.10.1998), abstract; column 5, row 40-column 6, row 62; figures 3-6	1, 4, 9, 10, 13-24, 29, 35-38
A	SE 470298 B (VATTENFALL) 10 January 1994 (10.01.1994), abstract; page 2, row 28-page 4, row 12; figures 1, 2, and 5	1-38
A	US 6198645 B1 (KOTOWSKI, J. et al.) 06 March 2001 (06.03.2001), whole document; specially abstract and figures 1-3, 5, 7-9, and 19	1-38

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
21 September 2007 (21.09.2007)	24 October 2007 (24.10.2007)

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI2007/050390

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4186436 A (ISHIWATARI, M.) 29 January 1980 (29.01.1980), abstract; column 1, row 55-column 2, row 64; figures 1-4	1-38
A	US 2005/0176396 A1 (MIYAGI, H.) 11 August 2005 (11.08.2005), abstract; paragraphs [0083]-[0093]; figures 1-4	1-38
A	US 6675003 B1 (DUBASH, N. B. et al.) 06 January 2004 (06.01.2004), abstract; column 3, row 19-column 4, row 10; figure 1	1-38
P, A	US 7212588 B1 (WONG, H. et al.) 01 May 2007 (01.05.2007), abstract; column 8, row 52-column 9, row 16; figures 5 and 6	1-38

INTERNATIONAL SEARCH REPORT
Information on patent family members

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PCT/FI2007/050390

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US 7212588 B1	01/05/2007	None	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI2007/050390

CLASSIFICATION OF SUBJECT MATTER

Int.Cl.
H03G 1/00 (2006.01)
H03G 3/00 (2006.01)
H02M 3/18 (2006.01)
H02M 5/32 (2006.01)
H03G 3/20 (2006.01)
H03G 3/30 (2006.01)
H03F 3/00 (2006.01)
H03F 3/45 (2006.01)